Intel ADL-N Ref: NISSA/NIVVIKS

TABLE OF CONTENTS

SHEET NO.	SHEET NAME
P01	TABLE OF CONTENTS
P02	System Block Diagram
P03	POWER TREE
P04	POWER SEQUENCING
P05	I2C MAP
P06	ADL-N: MEMORY
P07	ADL-N: DISPLAY, TYPE-C
P08	ADL-N: ESPI, SPI0, EMMC
P09	ADL-N: UART, I2C, AUDIO
P10	ADL-N: PCIE, USB, CLOCK
P11	ADL-N: MIPI CSI, CNV, MISC
P12	AD-N: POWER SEQUENCING
P13	ADL-N: STRAPS
P14	ADL-N: POWER (CPU & PCH)
P15	ADL-N: POWER DECOUPLING
P16	ADL-N: GND, RSVD
P17	ADL-N: DEBUG
P18	LPDDR5: CH-A1
P19	LPDDR5: CH-A2
P20	C2D2, CBI EEPROM,SPI FLASH
P21	GSC
P22	EC
P23	STORAGE: SD
P24	STORAGE: SSD
P25	AUDIO
P26	SENSORS, WCAM
P27	KBD, BTNS, LEDS, TRACKPAD, PEN GARAGE
P28	LID PANEL: DISP, UCAM

SHEET NO.	SHEET NAME
P29	WIFI,BT
P30	USB A0
P31	USB C0: DATA
P32	USB C0: BATTERY CHARGER
P33	POWER: SOC RAILS 1 (IMVP9.1)
P34	POWER: SOC RAILS 2
P35	POWER: SOC RAILS 3
P36	POWER: SOC RAILS 4
P37	POWER: LPDDR5 RAILS
P38	POWER: SYS RAILS 1
P39	POWER: SYS RAILS 2
P40	POWER: SYS RAILS 3
P41	DEBUG: PWR MEASUREMENTS
P42	SUB-BOARD CONNECTORS

Document Number LCFC

Size C | Title TABLE OF CONTENTS | Rev 0.3

Date: Thursday, January 05, 2023 | Sheet 1 of 44

R1059

270_0402_1%
PWR6W@

R1053

80.6K_0402_1%
PWR6W@

R1061

47.5K_0402_1%
PWR6W@

R1088

30K_0402_1%
PWR6W@

R1056

1/16W_196K_1%_0402
PWR6W@

R1067

1/16W_4.3K_1%_0402
PWR6W@

R3301

25.5K_0402_1%
PWR6W@

R1062

11.5K_0402_1%
PWR6W@

R1094

160_0402_1%
PWR6W@

R1077

1/16W_6.2K_1%_0402
PWR6W@

R1063

150_0402_1%
PWR6W@

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Thursday, January 05, 2023	Sheet 1 of 1	

PCB(DAZ)

ZZZ

PCB KC4LA NM-E931 NS-E933/NS-E934

CPU

15W	Pentium	Celeron
U1	U1	U1
15W CPU	Pentium CPU	Celeron CPU
CPU_15W@	CPU_PEN@	CPU_CEL@

X76 Gyro

BMI323	LSM6DS3TR-C
ZZZ	ZZZ
BMI323_X76	LSM6DS3TR-C_X76
Gero_BMI@	Gero_LSM@

X76 DDR

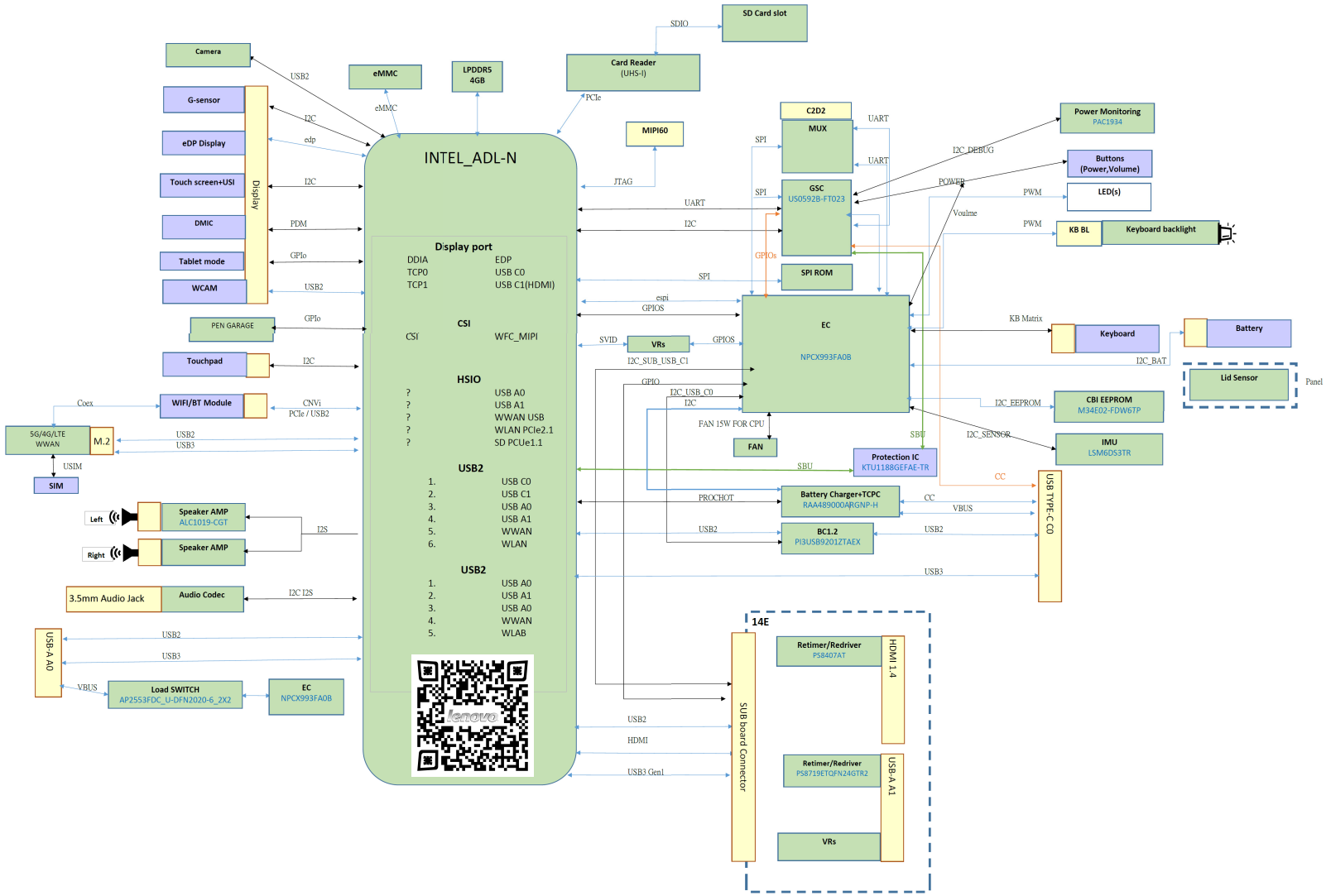
Micron 4G	SK Hynix 4G	Samsung 8G	Micron 8G	SK Hynix 8G
ZZZ	ZZZ	ZZZ	ZZZ	ZZZ
14E_500E_Micron 4G	14E_500E_Hynix 4G	14E_500E_Samsung 8G	14E_500E_Micron 8G	14E_500E_Hynix 8G
E_MIC_4G@	E_HYNIX_4G@	E_SAM_8G@	E_MIC_8G@	E_HYNIX_8G@

X76 EMMC

WD 32G	KIOXIA 32G	RAMAXEL 32G	WD 64G	KIOXIA 64G	RAMAXEL 64G
ZZZ	ZZZ	ZZZ	ZZZ	ZZZ	ZZZ
WD 32G	KIOXIA 32G	RAMAXEL 32G	WD 64G	KIOXIA 64G	RAMAXEL 64G
EM_WD_32G@	EM_KIO_32G@	EM_RAM_32G@	EM_WD_64G@	EM_KIO_64G@	EM_RAM_64G@

WD 128G	KIOXIA 128G	RAMAXEL 128G	WD 256G
ZZZ	ZZZ	ZZZ	ZZZ
WD 128G	KIOXIA 128G	RAMAXEL 128G	WD 256G
EM_WD_128G@	EM_KIO_128G@	EM_RAM_128G@	EM_WD_256G@

Title: <Title>		
Size: B	Document Number: <Doc>	Rev: <RevCode>
Date: Thursday, January 05, 2023	Sheet 1 of 1	

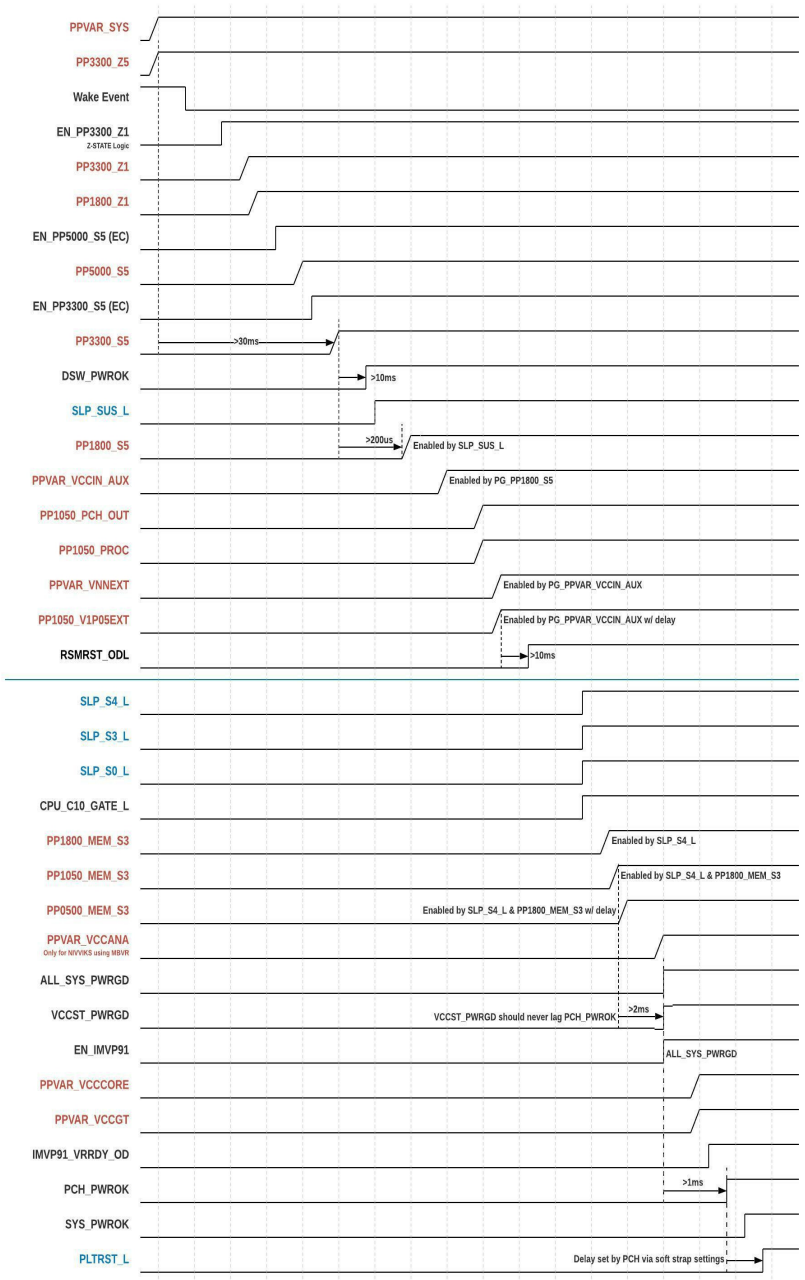

INTEL_ADL-N
Display port
DDIA
TCP0
TCP1
EDP
USB C0
USB C1(HDMI)
CSI
CSI
WFC_MIPI
HSIO
?
?
?
?
?
USB A0
USB A1
WWAN USB
WLAN PCIe2.1
SD PCUe1.1
USB2
1.
2.
3.
4.
5.
6.
USB C0
USB C1
USB A0
USB A1
WWAN
WLAN
USB2
1.
2.
3.
4.
5.
USB A0
USB A1
USB A0
WWAN
WLAB
Camera
G-sensor
eDP Display
Touch screen+USI
DMIC
Tablet mode
WCAM
Display
PEN GARAGE
Touchpad
WIFI/BT Module
5G/4G/LTE WWAN
M.2
SIM
Coex
USIM
Left
Right
Speaker AMP
ALC1019-CGT
Speaker AMP
I2S
3.5mm Audio Jack
Audio Codec
I2C I2S
USB-A A0
VBUS
Load SWITCH
AP2553FDC_U-DFN2020-6_2X2
EC
NPCX993FA0B
eMMC
LPDDR5 4GB
Card Reader (UHS-I)
SDIO
SD Card slot
PCIe
MIPI60
JTAG
C2D2
MUX
GSC
US0592B-FT023
SPI ROM
EC
NPCX993FA0B
VRs
SVID
GPIOS
FAN
FAN 15W FOR CPU
Protection IC
KTU1188GEFAE-TR
Battery Charger+TCPC
RAA489000ARGNP-H
BC1.2
PI3USB9201ZTAEX
USB TYPE-C C0
Power Monitoring
PAC1934
Buttons (Power,Volume)
LED(s)
KB BL
Keyboard backlight
Keyboard
Battery
Lid Sensor
Panel
CBI EEPROM
M34E02-FDW6TP
IMU
LSM6DS3TR
14E
Retimer/Redriver
PS8407AT
HDMI 1.4
Retimer/Redriver
PS8719ETQFN24GTR2
USB-A A1
VRs
SUB board Connector
USB2
HDMI
USB3 Gen1
USB3
UART
SPI
I2C
GPIOs
PWM
Voulme
KB Matrix
I2C_BAT
I2C_EEPROM
I2C_SENSOR
I2C_DEBUG
POWER
PROCHOT
CC
VBUS
SBU
I2C_SUB_USB_C1
I2C_USB_C0
eSPI
GPIO
PCIe / USB2
CNVi

Title	<Title>
Size: A	Document Number: <Doc>
Rev: 0.3	
Date: Thursday, January 05, 2023	Sheet 3 of 44

Power Rails
Platform Signals
SOC Signals

NISSA Power Sequence

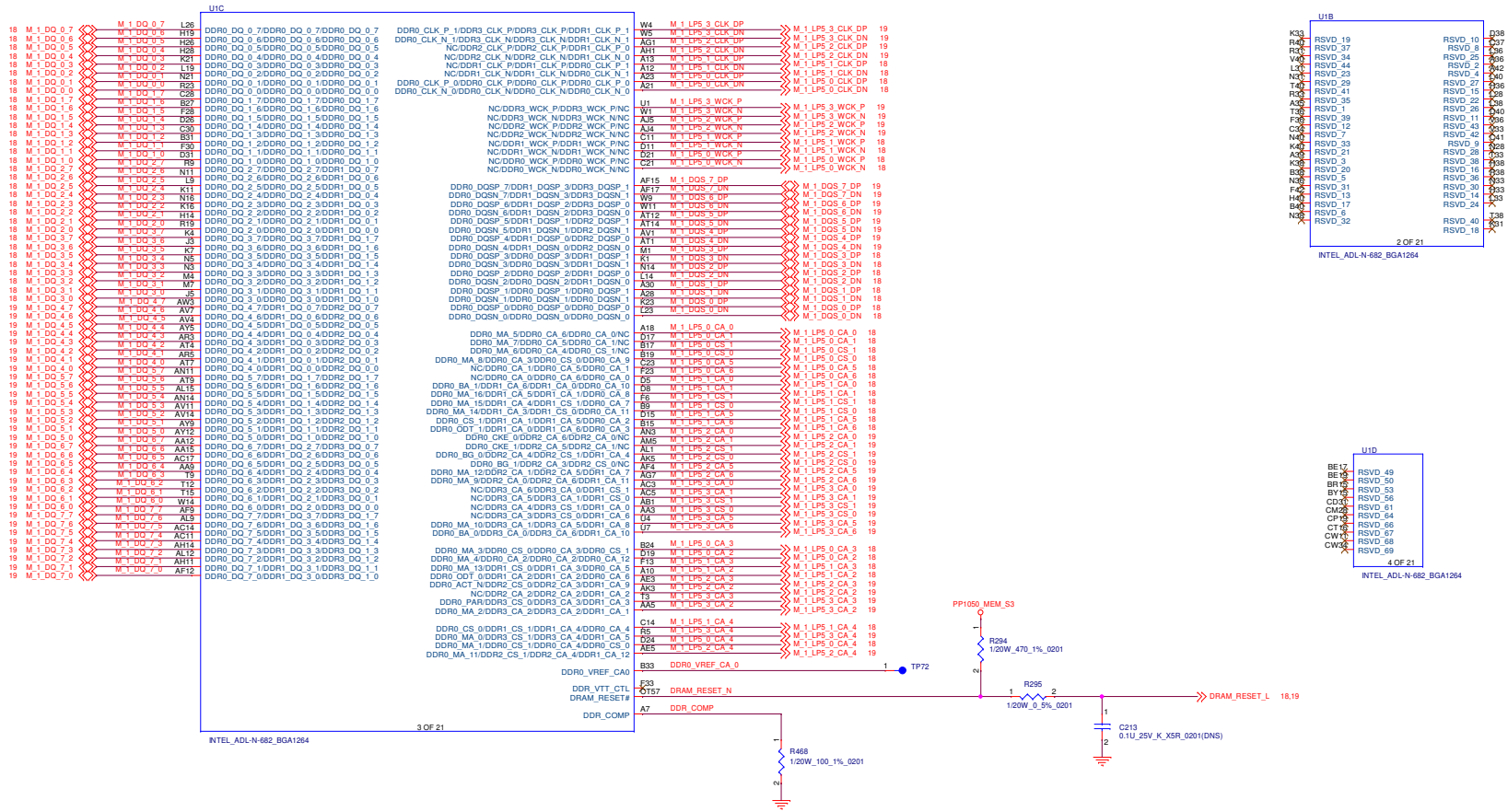
V1.0 2022-02-02



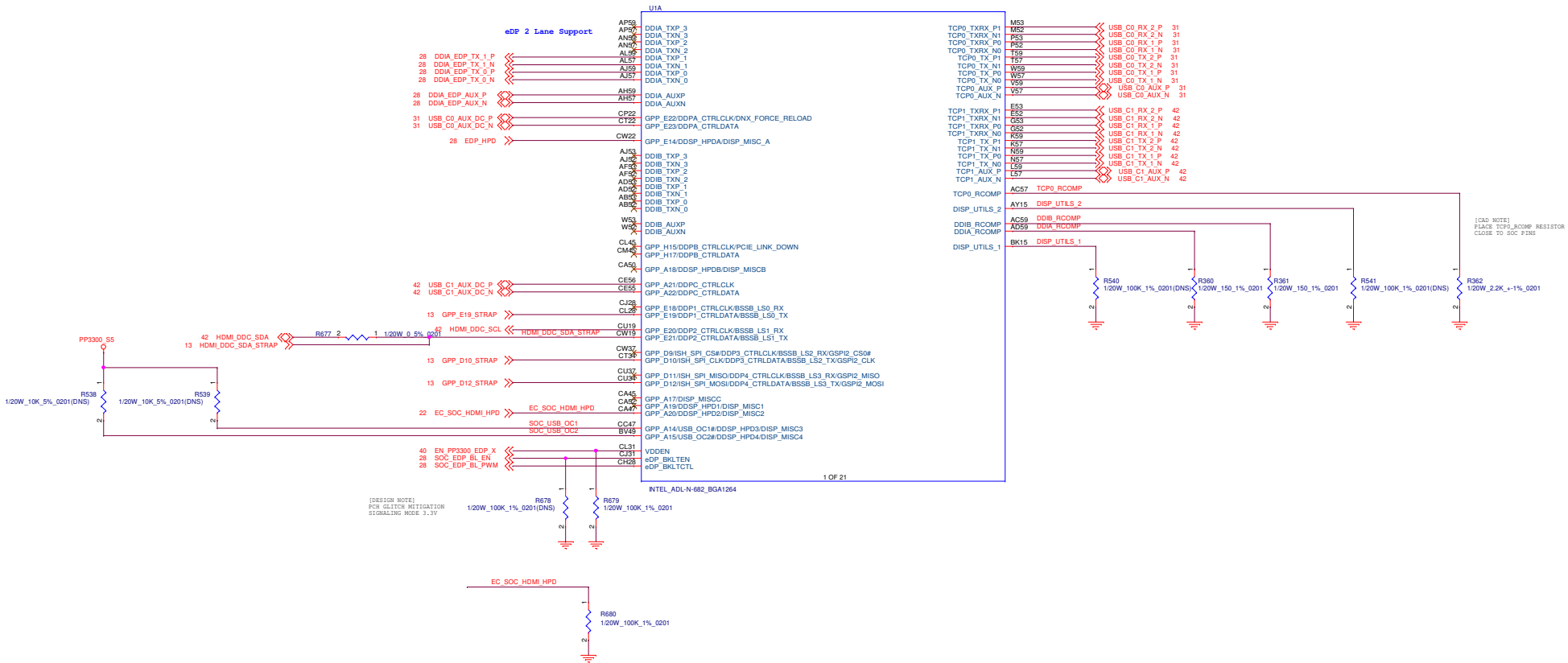
Document Number		LCFC
Size: A2	Title: POWER SEQUENCING	Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 4 of 44	

Controller	Port	Voltage Domain	Bus Net Names	Bus Speed	Device	7-bit Address	Device Description
SOC (ADL-N)	0	PP3300_S5	SOC_I2C_GSC_SCL SOC_I2C_GSC_SDA	400kHz	H1D3C	-	Google Security Chip
	1	PP3300_TCHSCR_X	SOC_I2C_TCHSCR_SCL SOC_I2C_TCHSCR_SDA	400kHz	Touch Screen	Project-Specific	Touch Screen Sensor (USI option)
	2	PP1800_S5	SOC_I2C_SUB_SCL SOC_I2C_SUB_SDA	400kHz	SX9324	0X28	SAR Sensor
	3	PP1800_S5	SOC_I2C_AUDIO_SCL SOC_I2C_AUDIO_SDA	400kHz	ALC5682I-VS	0X1A	Headphone Codec
	5	PP3300_S5	SOC_I2C_TCHPAD_SCL SOC_I2C_TCHPAD_SDA	400kHz	Touch Pad	Project-Specific	Touch pad

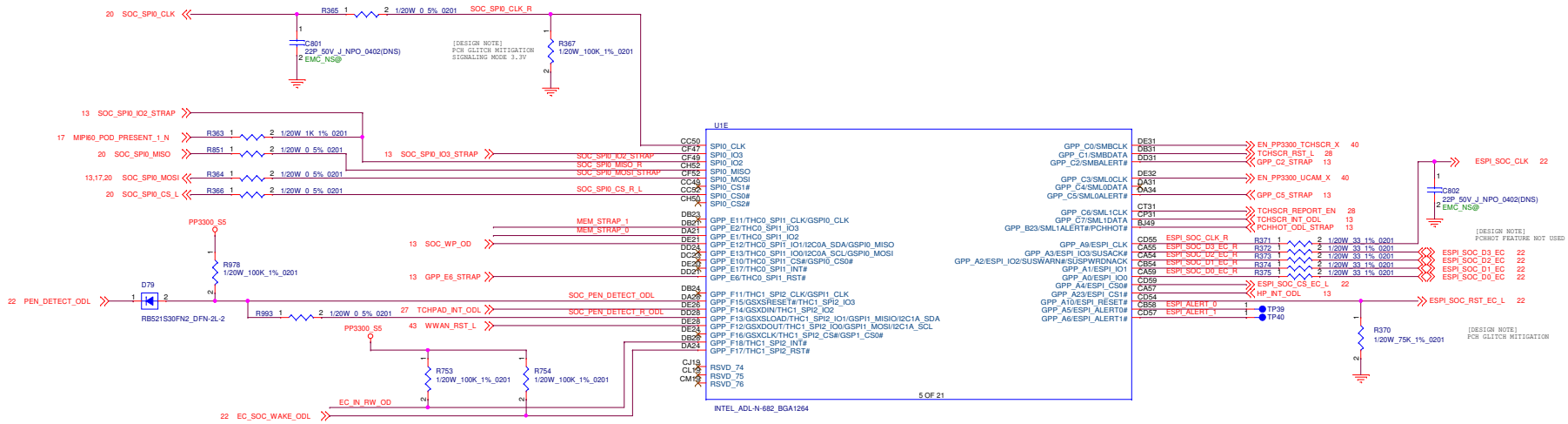
Controller	Port	Voltage Domain	Bus Net Names	Bus Speed	Device	7-bit Address	Device Description
EC (NPCX993)	0	PP3300_Z1	EC_I2C_EEPROM_SCL EC_I2C_EEPROM_SDA	400kHz	M34E02-FDW6TP	0X50, 0X30	CBI EEPROM 0X50 - Norm, 0X30 -WP
	1	PP1800_S5	EC_I2C_SENSOR_SCL EC_I2C_SENSOR_SDA	400kHz	BMI323 LSM6DS3TR-C(2nd)	0x69	IMU
					BMA422 LIS2DWLTR(2nd)	0x19	Accelerometer (LID)
	3	PP3300_Z1	EC_I2C_USB_C0_SCL EC_I2C_USB_C0_SDA	1MHz	RAA489000	0X09	Battery Charger
					RAA489000	0X22	TCPC
					PI3USB9201	0X5F	BC1.2 Detector
	7	PP3300_Z1	EC_I2C_BATTERY_SCL EC_I2C_BATTERY_SDA	100kHz	Smart Battery	Pack-Specific	



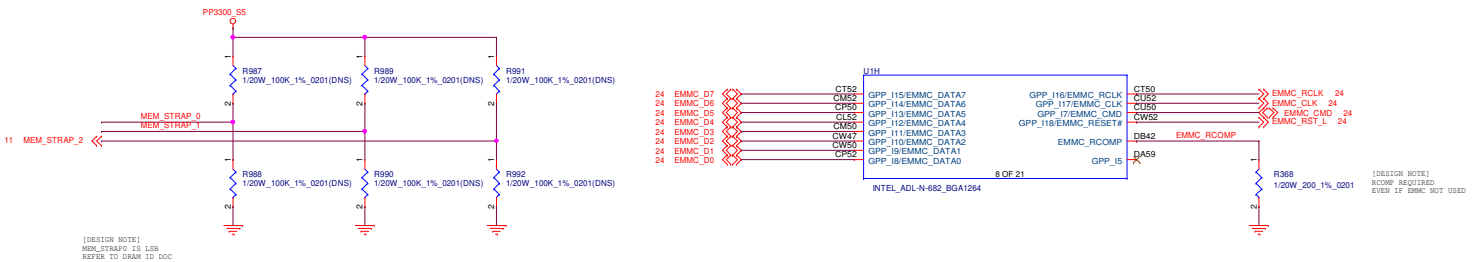
Document Number			LCFC
Size A2	Title ADL-N: MEMORY		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 6 of 44		



Document Number		LCFC
Size A2	Title ADL-N: DISPLAY, TYPE-C	Rev 0.3
Date: Thursday, January 05, 2023	Sheet 7 of 44	



MEMORY STRAP CONFIG



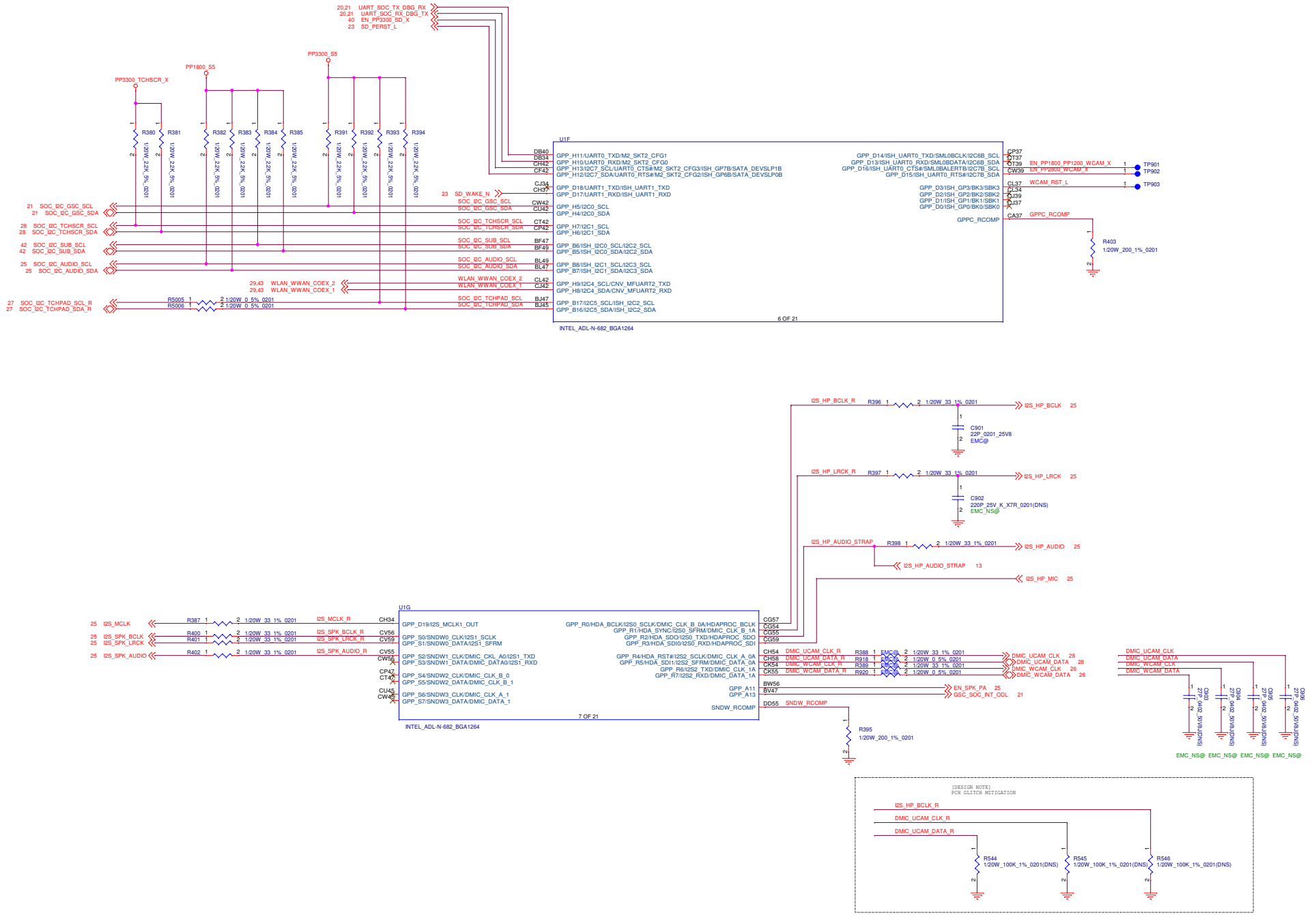
	Supplier	MPN	strap			
2GB	Micron	MT62F512M32D2DR-031 WT:B	001	R992	R990	R987
	SK Hynix	H9JCNNNBK3MLYR-N6E	001	R992	R990	R987
4GB	Samsung	K3LKBKB0BM-MGCP	000	R992	R990	R988
	Micron	MT62F1G32D4DR-031 WT:B	011	R992	R989	R987
	SK Hynix	H58G56AK6BX069	000	R992	R990	R988

Document Number

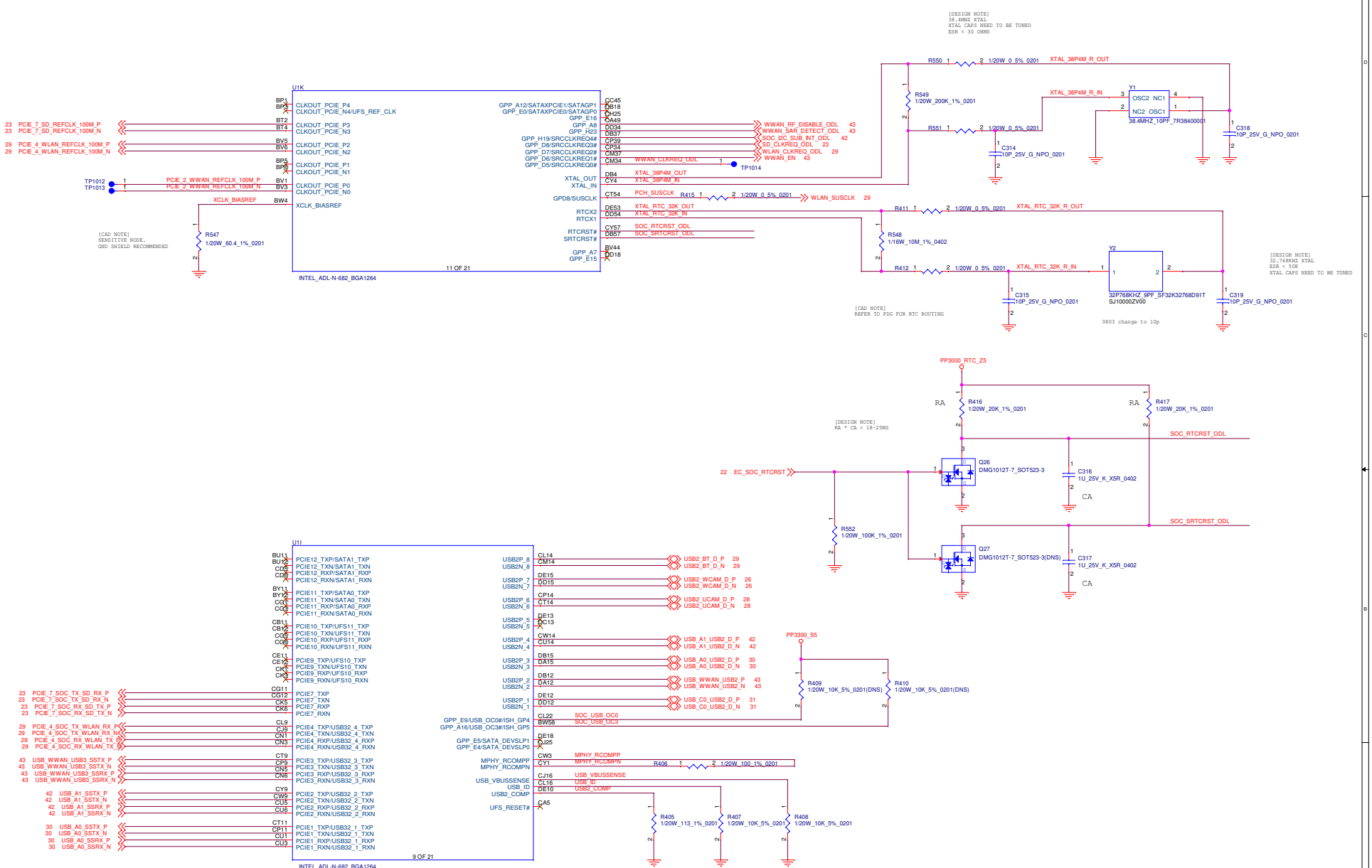
LCFC

Size A2 | Title ADL-N: ESPI, SPI0, EMMC | Rev 0.3

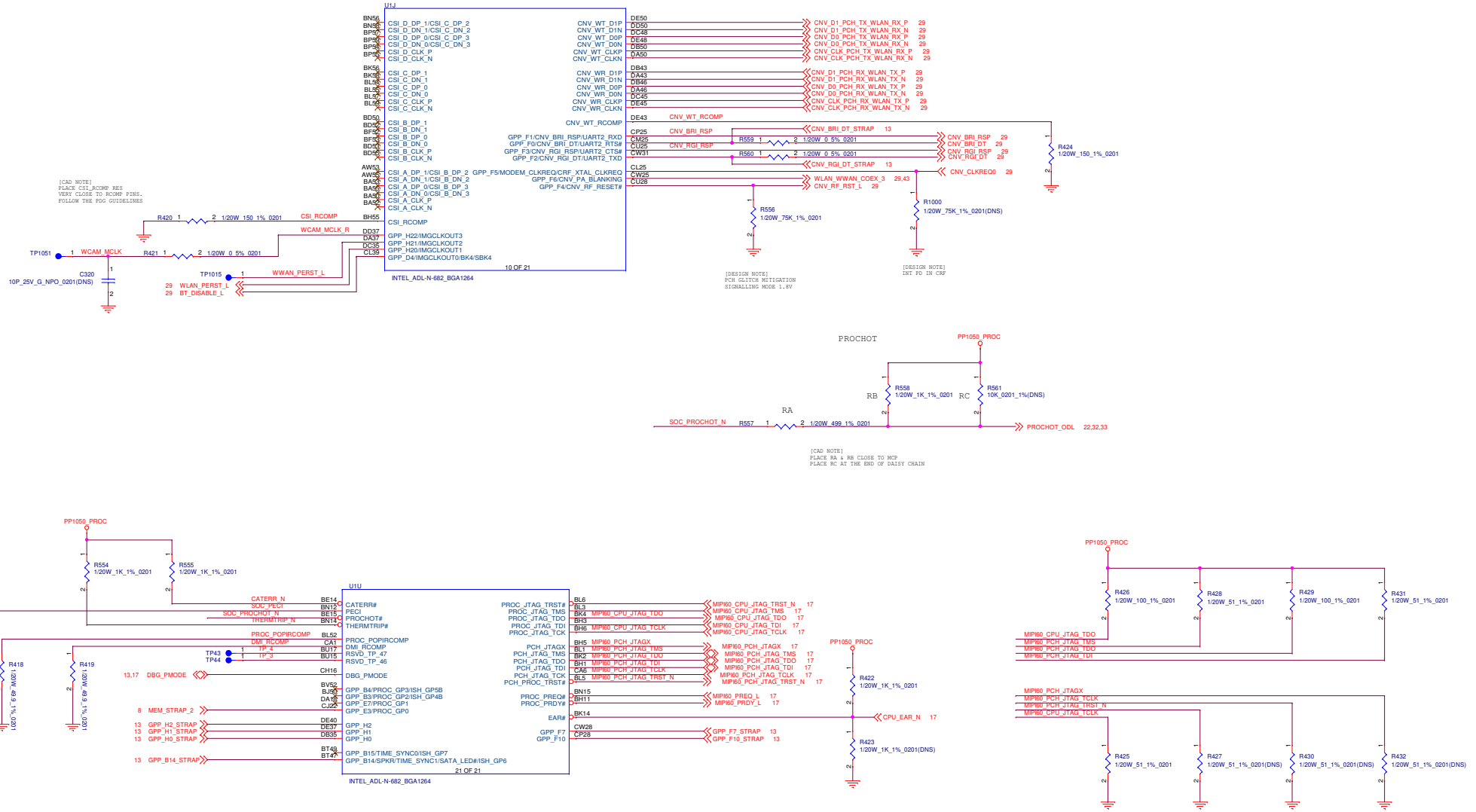
Date: Thursday, January 05, 2023 | Sheet 8 of 44

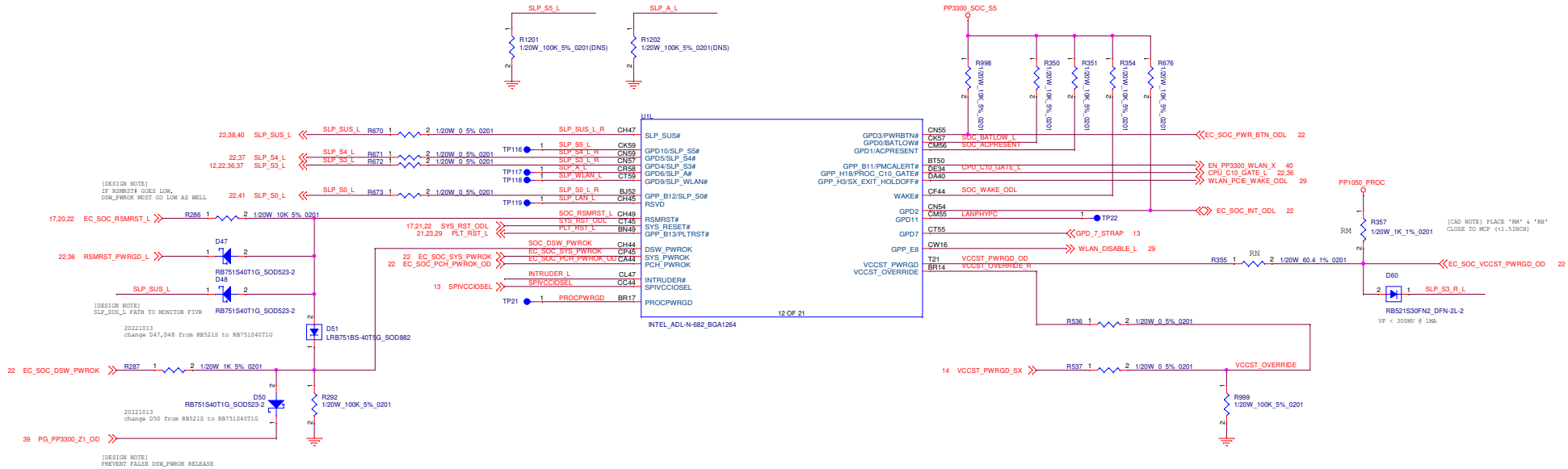


Document Number			LCFC
Size A2	Title ADL-N: UART, I2C, AUDIO		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 9 of 44		

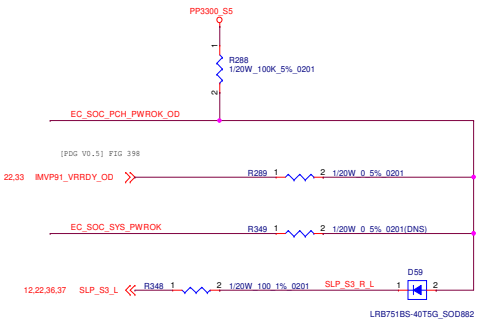


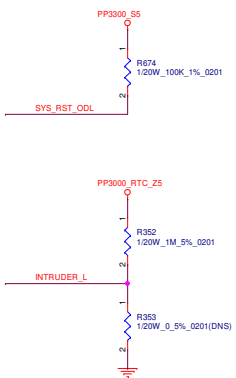
Document Number			LCFC
Size A2	Title ADL-N: PCIE, USB, CLOCK		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 10 of 44		


U1J
INTEL_ADL-N-682_BGA1264
10 OF 21
CSI_A_DP_1/CSI_B_DP_2
CSI_A_DN_1/CSI_B_DN_2
CSI_A_DP_0/CSI_B_DP_3
CSI_A_DN_0/CSI_B_DN_3
CSI_A_CLK_P
CSI_A_CLK_N
CSI_B_DP_1
CSI_B_DN_1
CSI_B_DP_0
CSI_B_DN_0
CSI_B_CLK_P
CSI_B_CLK_N
CSI_C_DP_1
CSI_C_DN_1
CSI_C_DP_0
CSI_C_DN_0
CSI_C_CLK_P
CSI_C_CLK_N
CSI_D_DP_1/CSI_C_DP_2
CSI_D_DN_1/CSI_C_DN_2
CSI_D_DP_0/CSI_C_DP_3
CSI_D_DN_0/CSI_C_DN_3
CSI_D_CLK_P
CSI_D_CLK_N
CSI_RCOMP
GPP_H22/IMGCLKOUT3
GPP_H21/IMGCLKOUT2
GPP_H20/IMGCLKOUT1
GPP_D4/IMGCLKOUT0/BK4/SBK4
GPP_F5/MODEM_CLKREQ/CRF_XTAL_CLKREQ
GPP_F6/CNV_PA_BLANKING
GPP_F4/CNV_RF_RESET#
GPP_F1/CNV_BRI_RSP/UART2_RXD
GPP_F0/CNV_BRI_DT/UART2_RTS#
GPP_F3/CNV_RGI_RSP/UART2_CTS#
GPP_F2/CNV_RGI_DT/UART2_TXD
CNV_WT_D1P
CNV_WT_D1N
CNV_WT_D0P
CNV_WT_D0N
CNV_WT_CLKP
CNV_WT_CLKN
CNV_WR_D1P
CNV_WR_D1N
CNV_WR_D0P
CNV_WR_D0N
CNV_WR_CLKP
CNV_WR_CLKN
CNV_WT_RCOMP
[CAD NOTE]
PLACE CSI_RCOMP RES
VERY CLOSE TO RCOMP PINS.
FOLLOW THE PDG GUIDELINES
R420 1 2 1/20W 150 1% 0201
CSI_RCOMP
WCAM_MCLK_R
TP1051 WCAM_MCLK
R421 1 2 1/20W 0 5% 0201
C320
10P_25V_G_NPO_0201(DNS)
TP1015 WWAN_PERST_L
29 WLAN_PERST_L
29 BT_DISABLE_L
CNV_D1_PCH_TX_WLAN_RX_P 29
CNV_D1_PCH_TX_WLAN_RX_N 29
CNV_D0_PCH_TX_WLAN_RX_P 29
CNV_D0_PCH_TX_WLAN_RX_N 29
CNV_CLK_PCH_TX_WLAN_RX_P 29
CNV_CLK_PCH_TX_WLAN_RX_N 29
CNV_D1_PCH_RX_WLAN_TX_P 29
CNV_D1_PCH_RX_WLAN_TX_N 29
CNV_D0_PCH_RX_WLAN_TX_P 29
CNV_D0_PCH_RX_WLAN_TX_N 29
CNV_CLK_PCH_RX_WLAN_TX_P 29
CNV_CLK_PCH_RX_WLAN_TX_N 29
CNV_WT_RCOMP
CNV_BRI_RSP
CNV_RGI_RSP
CNV_BRI_DT_STRAP 13
R559 1 2 1/20W 0 5% 0201
CNV_BRI_RSP 29
CNV_BRI_DT 29
CNV_RGI_RSP 29
CNV_RGI_DT 29
R560 1 2 1/20W 0 5% 0201
CNV_RGI_DT_STRAP 13
CNV_CLKREQ0 29
WLAN_WWAN_COEX_3 29,43
CNV_RF_RST_L 29
R424
1/20W_150_1%_0201
R556
1/20W_75K_1%_0201
R1000
1/20W_75K_1%_0201(DNS)
[DESIGN NOTE]
PCH GLITCH MITIGATION
SIGNALLING MODE 1.8V
[DESIGN NOTE]
INT PD IN CRF
PROCHOT
PP1050_PROC
RB
RC
RA
R558
1/20W_1K_1%_0201
R561
10K_0201_1%(DNS)
SOC_PROCHOT_N
R557 1 2 1/20W 499 1% 0201
PROCHOT_ODL 22,32,33
[CAD NOTE]
PLACE RA & RB CLOSE TO MCP
PLACE RC AT THE END OF DAISY CHAIN
PP1050_PROC
R554
1/20W_1K_1%_0201
R555
1/20W_1K_1%_0201
U1U
INTEL_ADL-N-682_BGA1264
21 OF 21
CATERR_N
SOC_PECI
SOC_PROCHOT_N
THERMTRIP_N
PROC_POPIRCOMP
DMI_RCOMP
RSVD_TP_47
RSVD_TP_46
TP43
TP44
TP_3
DBG_PMODE
13,17 DBG_PMODE
GPP_B4/PROC_GP3/ISH_GP5B
GPP_B3/PROC_GP2/ISH_GP4B
GPP_E7/PROC_GP1
GPP_E3/PROC_GP0
8 MEM_STRAP_2
13 GPP_H2_STRAP
13 GPP_H1_STRAP
13 GPP_H0_STRAP
13 GPP_B14_STRAP
GPP_B15/TIME_SYNC0/ISH_GP7
GPP_B14/SPKR/TIME_SYNC1/SATA_LED#/ISH_GP6
R553
200W_200_1%_0201
R418
1/20W_49.9_1%_0201
R419
1/20W_49.9_1%_0201
PROC_JTAG_TRST#
PROC_JTAG_TMS
PROC_JTAG_TDO
PROC_JTAG_TDI
PROC_JTAG_TCK
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK
PCH_PROC_TRST#
PROC_PREQ#
PROC_PRDY#
EAR#
GPP_F7
GPP_F10
MIPI60_CPU_JTAG_TRST_N 17
MIPI60_CPU_JTAG_TMS 17
MIPI60_CPU_JTAG_TDO 17
MIPI60_CPU_JTAG_TDI 17
MIPI60_CPU_JTAG_TCLK 17
MIPI60_PCH_JTAGX 17
MIPI60_PCH_JTAG_TMS 17
MIPI60_PCH_JTAG_TDO 17
MIPI60_PCH_JTAG_TDI 17
MIPI60_PCH_JTAG_TCLK 17
MIPI60_PCH_JTAG_TRST_N 17
MIPI60_PREQ_L 17
MIPI60_PRDY_L 17
CPU_EAR_N 17
GPP_F7_STRAP 13
GPP_F10_STRAP 13
PP1050_PROC
R422
1/20W_1K_1%_0201
R423
1/20W_1K_1%_0201(DNS)
PP1050_PROC
R426
1/20W_100_1%_0201
R428
1/20W_51_1%_0201
R429
1/20W_100_1%_0201
R431
1/20W_51_1%_0201
MIPI60_CPU_JTAG_TDO
MIPI60_CPU_JTAG_TMS
MIPI60_CPU_JTAG_TDO
MIPI60_CPU_JTAG_TDI
MIPI60_PCH_JTAGX
MIPI60_PCH_JTAG_TCLK
MIPI60_PCH_JTAG_TRST_N
MIPI60_CPU_JTAG_TCLK
R425
1/20W_51_1%_0201
R427
1/20W_51_1%_0201(DNS)
R430
1/20W_51_1%_0201(DNS)
R432
1/20W_51_1%_0201(DNS)
Document Number
LCFC
Size A2
Title ADL-N: MIPI CSI, CNV, MISC
Rev 0.3
Date: Thursday, January 05, 2023
Sheet 11 of 44

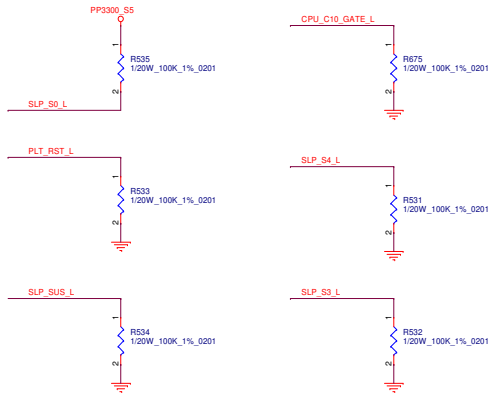


PCH_PWROK



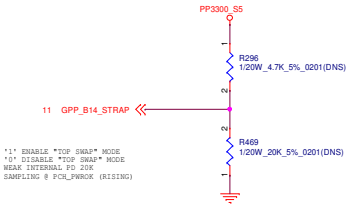


PCH GLITCH MITIGATION



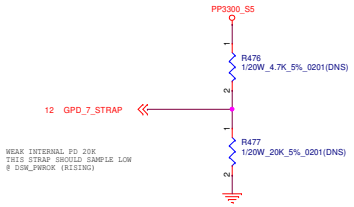
Document Number			LCFC
Size A2	Title ADL-N: POWER SEQUENCING		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 12 of 44		

[TOP SWAP OVERRIDE]

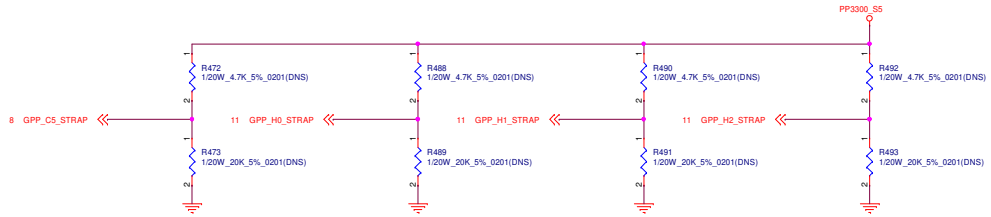


'1' ENABLE "TOP SWAP" MODE
'0' DISABLE "TOP SWAP" MODE
WEAK INTERNAL PD 20K
SAMPLING @ PCH_PWROK (RISING)

[RESERVED]



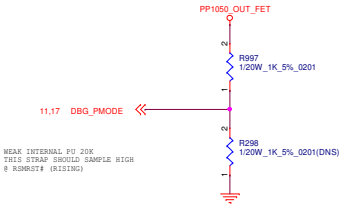
WEAK INTERNAL PD 20K
THIS STRAP SHOULD SAMPLE LOW
@ DSW_PWROK (RISING)



[4BIT BOOT CONFIGURATION]

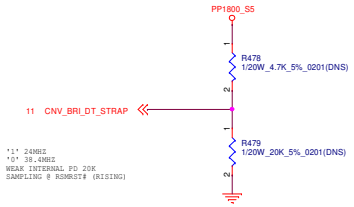
BIT3 - GPP_H2_STRAP
BIT2 - GPP_H1_STRAP
BIT1 - GPP_H0_STRAP
BIT0 - GPP_C5_STRAP
B'0000 - BIOS/CSE ON SPI. ESPI ENABLED
B'0010 - BIOS/CSE ON SPI, ESPI DISABLED
B'0100 - BIOS ON ESPI PERIPHERAL CHANNEL
CSE ON MASTER ATTACHED SPI
B'1000 - BIOS/CSE ON ESPI ATTACHED DEVICE
B'1100 - BIOS ON ESPI PERIPHERAL CHANNEL
CSE ON SLAVE ATTACHED SPI.
OTHERS: RESERVED.
WEAK INTERNAL PD 20K ON ALL STRAPS
SAMPLE @ RSMRST# (RISING)

[RESERVED]



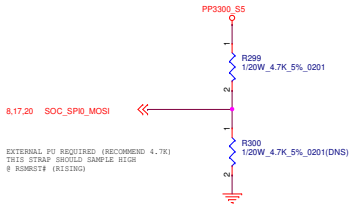
WEAK INTERNAL PU 20K
THIS STRAP SHOULD SAMPLE HIGH
@ RSMRST# (RISING)

[XTAL FREQUENCY SEL]



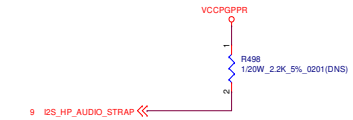
'1' 24MHZ
'0' 38.4MHZ
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

[RESERVED]



EXTERNAL PU REQUIRED (RECOMMEND 4.7K)
THIS STRAP SHOULD SAMPLE HIGH
@ RSMRST# (RISING)

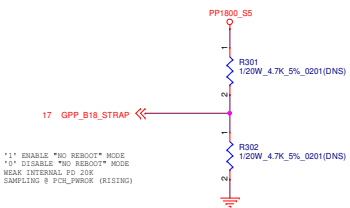
[FLASH DESCRIPTOR SECURITY OVERRIDE]



[CAD NOTE]
PLACE CLOSE TO
RDA SIGNAL TO AVOID STUB

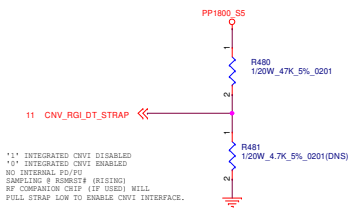
'1' DISABLE FLASH DESCRIPTOR SECURITY. ONLY TO BE PULLED HIGH W/ EXT PU, DURING MFG/DEBUG
'0' ENABLE SECURITY MEASURES DEFINED IN THE FLASH DESCRIPTOR
WEAK INTERNAL PD 20K
SAMPLING @ PCH_PWROK (RISING)

[NO REBOOT]



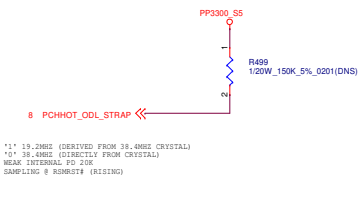
'1' ENABLE "NO REBOOT" MODE
'0' DISABLE "NO REBOOT" MODE
WEAK INTERNAL PD 20K
SAMPLING @ PCH_PWROK (RISING)

[M.2 CNVI MODE SELECT]



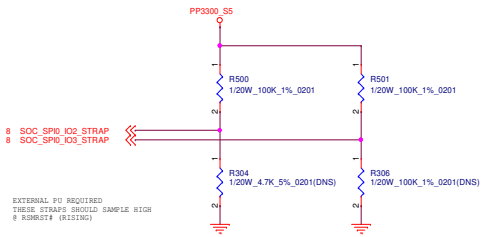
'1' INTEGRATED CNVI DISABLED
'0' INTEGRATED CNVI ENABLED
NO INTERNAL PD/PU
SAMPLING @ RSMRST# (RISING)
RF COMPANION CHIP (IF USED) WILL
PULL STRAP LOW TO ENABLE CNVI INTERFACE.

[CPUNSSC CLOCK FREQUENCY]



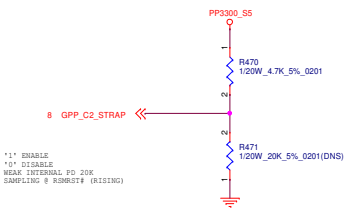
'1' 19.2MHZ (DERIVED FROM 38.4MHZ CRYSTAL)
'0' 38.4MHZ (DIRECTLY FROM CRYSTAL)
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

[RESERVED]



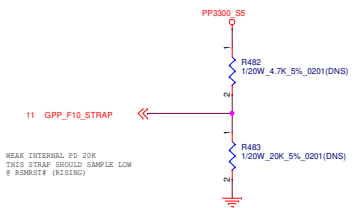
EXTERNAL PU REQUIRED
THESE STRAPS SHOULD SAMPLE HIGH
@ RSMRST# (RISING)

[TLS CONFIDENTIALITY]



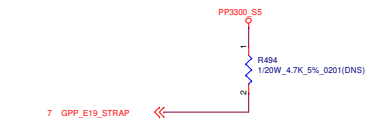
'1' ENABLE
'0' DISABLE
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

[RESERVED]



WEAK INTERNAL PD 20K
THIS STRAP SHOULD SAMPLE LOW
@ RSMRST# (RISING)

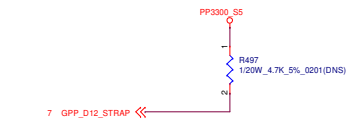
[DDP1 I2C/BSSB_LS0 VCC CONF]



'1' DDP1 I2C/BSSB_LS0 PINS AT 3.3V
'0' DDP1 I2C/BSSB_LS0 PINS AT 1.8V
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

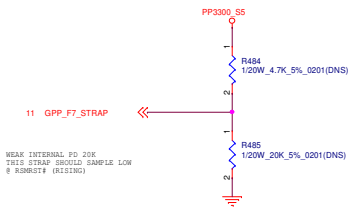
[STRAPS BASED ON EDS 0.5]

[DDP4 I2C/BSSB_LS3 VCC CONF]



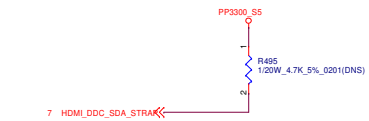
'1' DDP4 I2C/BSSB_LS3 PINS AT 3.3V
'0' DDP4 I2C/BSSB_LS3 PINS AT 1.8V
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

[RESERVED]



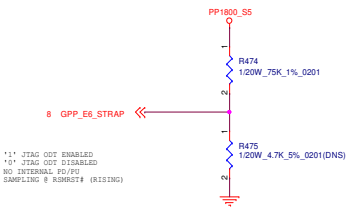
WEAK INTERNAL PD 20K
THIS STRAP SHOULD SAMPLE LOW
@ RSMRST# (RISING)

[DDP2 I2C/BSSB_LS1 VCC CONF]



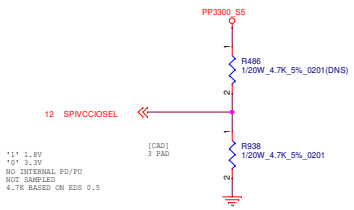
'1' DDP2 I2C/BSSB_LS1 PINS AT 3.3V
'0' DDP2 I2C/BSSB_LS1 PINS AT 1.8V
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

[JTAG ODT DISABLE]



'1' JTAG ODT ENABLED
'0' JTAG ODT DISABLED
NO INTERNAL PD/PU
SAMPLING @ RSMRST# (RISING)

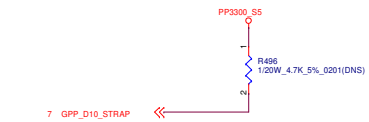
[SPI VOLTAGE SELECT]



'1' 1.8V
'0' 3.3V
NO INTERNAL PD/PU
NOT SAMPLED
4.7K BASED ON EDS 0.5

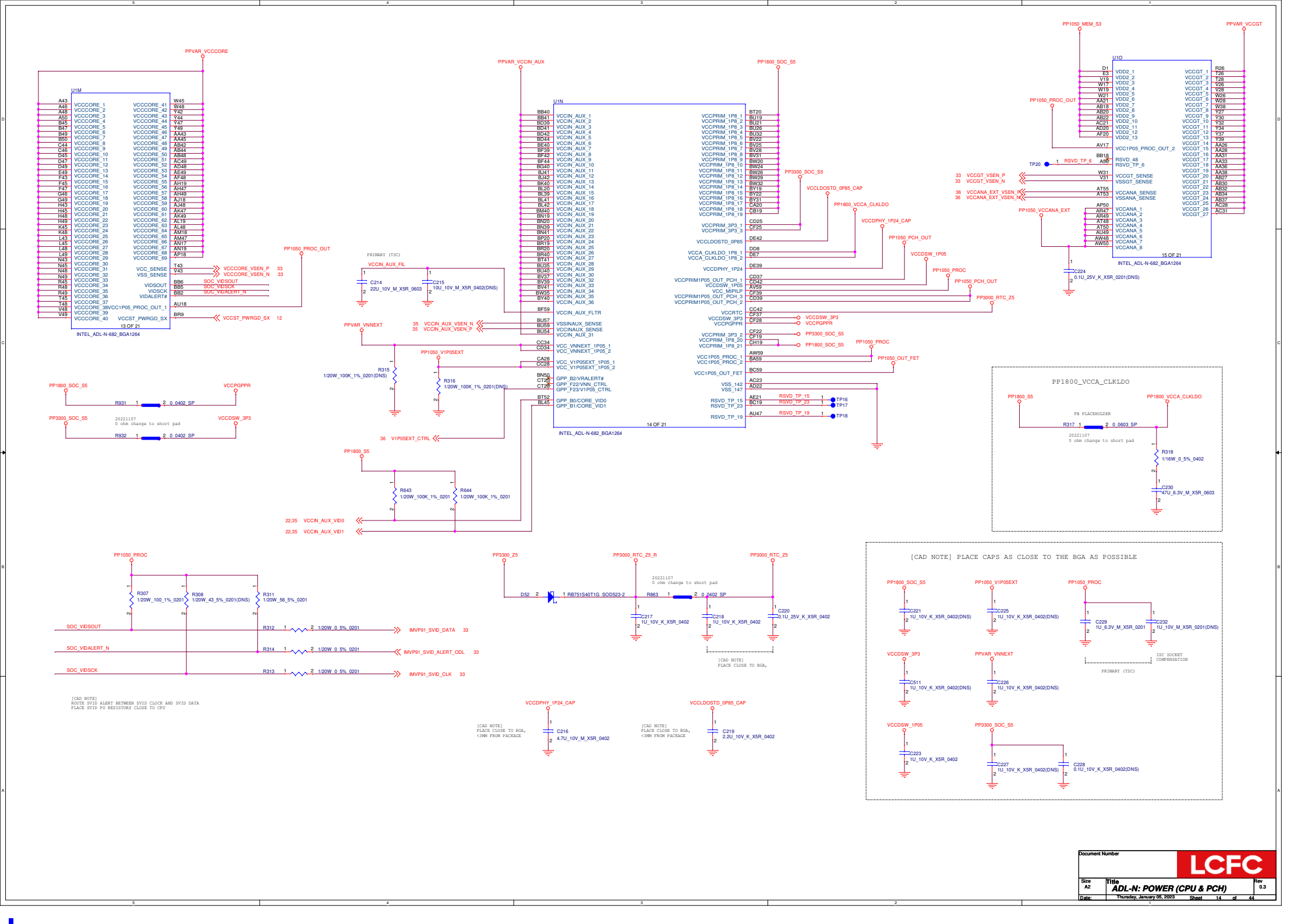
[CAD]
3 PAD

[DDP3 I2C/BSSB_LS2 VCC CONF]



'1' DDP3 I2C/BSSB_LS2 PINS AT 3.3V
'0' DDP3 I2C/BSSB_LS2 PINS AT 1.8V
WEAK INTERNAL PD 20K
SAMPLING @ RSMRST# (RISING)

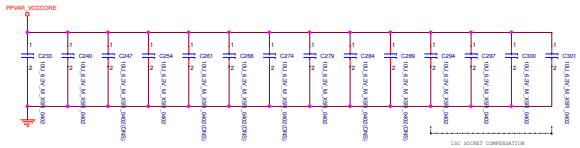
Document Number		LCFC
Size A2	Title ADL-N: STRAPS	Rev 0.3
Date: Thursday, January 05, 2023	Sheet 13 of 44	


PPVAR_VCCCORE
U1M
INTEL_ADL-N-682_BGA1264
13 OF 21
PP1050_PROC_OUT
PRIMARY (TSC)
VCCIN_AUX_FIL
C214
22U_10V_M_X5R_0603
C215
10U_10V_M_X5R_0402(DNS)
PPVAR_VCCIN_AUX
U1N
14 OF 21
PP1800_SOC_S5
PP3300_SOC_S5
VCCLDOSTD_0P85_CAP
PP1800_VCCA_CLKLDO
VCCDPHY_1P24_CAP
PP1050_PCH_OUT
VCCDSW_1P05
PP1050_PROC
PP3000_RTC_Z5
PPVAR_VNNEXT
PP1050_V1P05EXT
R315
1/20W_100K_1%_0201(DNS)
R316
1/20W_100K_1%_0201(DNS)
PP1800_S5
R643
1/20W_100K_1%_0201
R644
1/20W_100K_1%_0201
PP1800_SOC_S5
R931
0_0402_SP
VCCPGPPR
PP3300_SOC_S5
20221107
0 ohm change to short pad
R932
0_0402_SP
VCCDSW_3P3
PP1050_VCCANA_EXT
C224
0.1U_25V_K_X5R_0201(DNS)
PP1050_MEM_S3
PPVAR_VCCGT
U1O
15 OF 21
PP1050_PROC_OUT
TP20
RSVD_TP_6
VCCGT_VSEN_P
VCCGT_VSEN_N
VCCANA_EXT_VSEN_P
VCCANA_EXT_VSEN_N
PP1800_VCCA_CLKLDO
PP1800_S5
PP1800_VCCA_CLKLDO
FB PLACEHOLDER
R317
0_0603_SP
20221107
0 ohm change to short pad
R318
1/16W_0_5%_0402
C230
47U_6.3V_M_X5R_0603
[CAD NOTE] PLACE CAPS AS CLOSE TO THE BGA AS POSSIBLE
PP1800_SOC_S5
C221
1U_10V_K_X5R_0402(DNS)
PP1050_V1P05EXT
C225
1U_10V_K_X5R_0402(DNS)
PP1050_PROC
C229
1U_6.3V_M_X5R_0201
C232
1U_10V_M_X5R_0201(DNS)
ISC SOCKET COMPENSATION
PRIMARY (TSC)
VCCDSW_3P3
C511
1U_10V_K_X5R_0402(DNS)
PPVAR_VNNEXT
C226
1U_10V_K_X5R_0402(DNS)
VCCDSW_1P05
C223
1U_10V_K_X5R_0402
PP3300_SOC_S5
C227
1U_10V_K_X5R_0402(DNS)
C228
0.1U_10V_K_X5R_0402(DNS)
PP1050_PROC
R307
1/20W_100_1%_0201
R308
1/20W_43_5%_0201(DNS)
R311
1/20W_56_5%_0201
SOC_VIDSOUT
SOC_VIDALERT_N
SOC_VIDSCK
R312
R314
R313
1/20W_0_5%_0201
IMVP91_SVID_DATA
IMVP91_SVID_ALERT_ODL
IMVP91_SVID_CLK
[CAD NOTE]
ROUTE SVID ALERT BETWEEN SVID CLOCK AND SVID DATA
PLACE SVID PU RESISTORS CLOSE TO CPU
PP3300_Z5
D52
RB751S40T1G_SOD523-2
PP3000_RTC_Z5_R
20221107
0 ohm change to short pad
R863
0_0402_SP
PP3000_RTC_Z5
C217
1U_10V_K_X5R_0402
C218
1U_10V_K_X5R_0402
C220
0.1U_25V_K_X5R_0402
[CAD NOTE]
PLACE CLOSE TO BGA,
VCCDPHY_1P24_CAP
C216
4.7U_10V_M_X5R_0402
[CAD NOTE]
PLACE CLOSE TO BGA,
<3MM FROM PACKAGE
VCCLDOSTD_0P85_CAP
C219
2.2U_10V_K_X5R_0402
[CAD NOTE]
PLACE CLOSE TO BGA,
<3MM FROM PACKAGE
Document Number
LCFC
Size
A2
Title
ADL-N: POWER (CPU & PCH)
Rev
0.3
Date:
Thursday, January 05, 2023
Sheet
14
of
44

HW/EE Portion

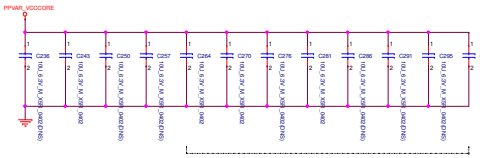
PPVAR_VCCCORE – PRIMARY (TSC)

14X 10UF (4X PLACEHOLDER)



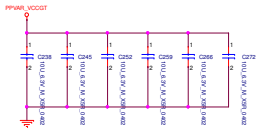
PPVAR_VCCCORE – SECONDARY (BSC)

12X 10UF (8X PLACEHOLDER)



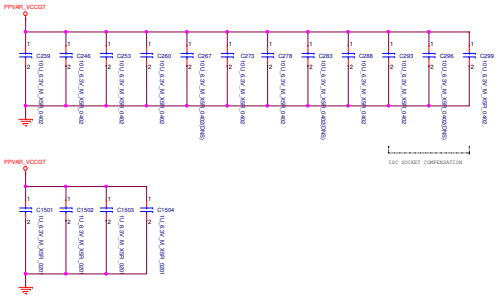
PPVAR_VCCGT – PRIMARY (TSC)

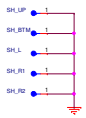
6X 10UF



PPVAR_VCCGT – SECONDARY (BSC)

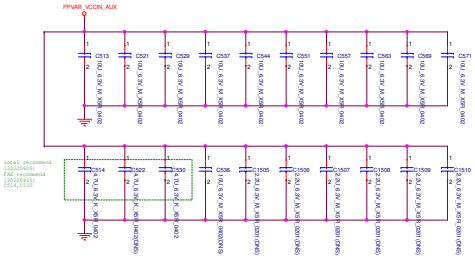
12X 10UF (3X PLACEHOLDER)
4X 1UF





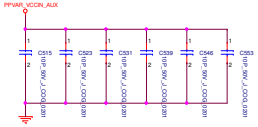
PPVAR_VCCIN_AUX – SECONDARY (BSC)

9X 10UF (1X PLACEHOLDER)
5X 4.7UF (3X PLACEHOLDER)
6X 2.2UF (6X PLACEHOLDER)

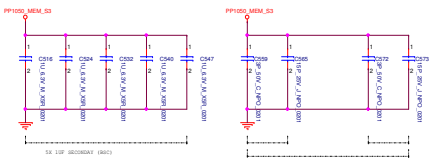


PPVAR_VCCIN_AUX – EMC (BSC)

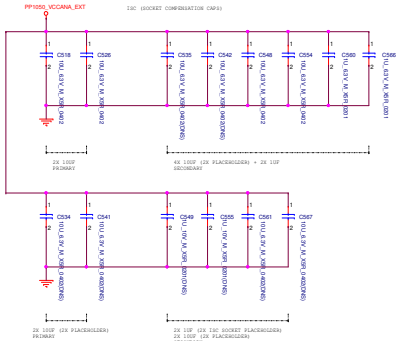
6X 10PF



PP1050_MEM_S3



PP1050_VCCANA_EXT

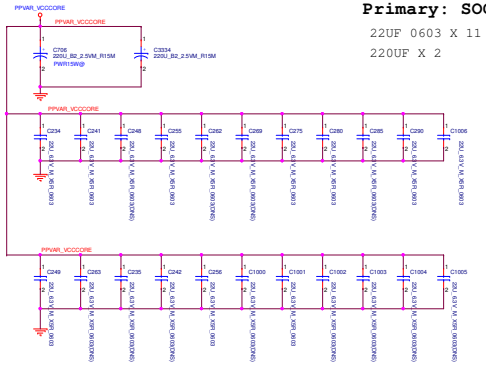


HW/PWR Portion

PPVAR_VCCCORE DECAP

Primary: SOC side
22UF 0603 X 11
220UF X 2

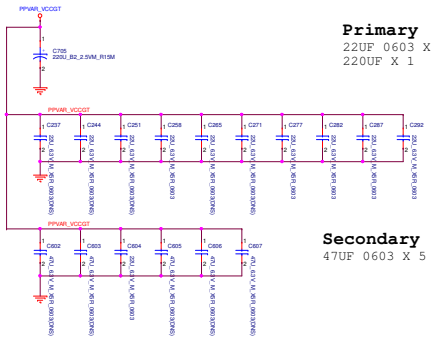
Secondary
22UF 0603 X 11



PPVAR_VCCGT DECAP

Primary
22UF 0603 X 13
220UF X 1

Secondary
47UF 0603 X 5

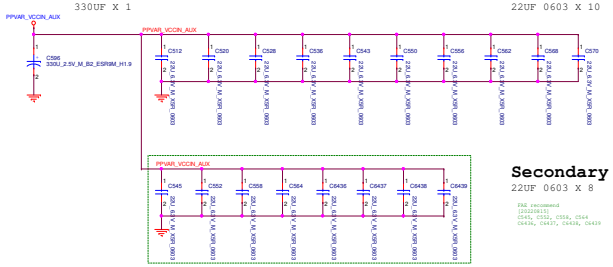


VCCIN_AUX DECAP

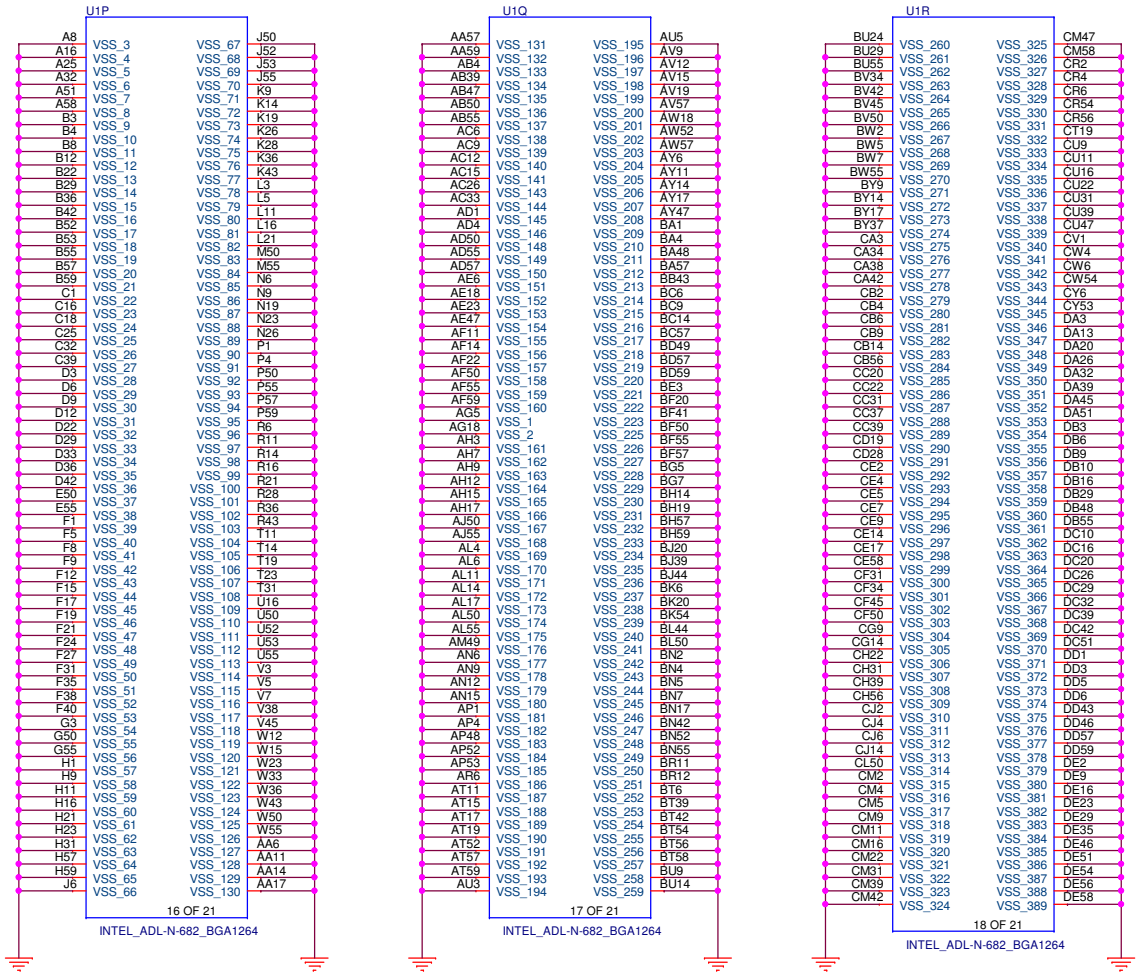
330UF X 1

Primary
22UF 0603 X 10

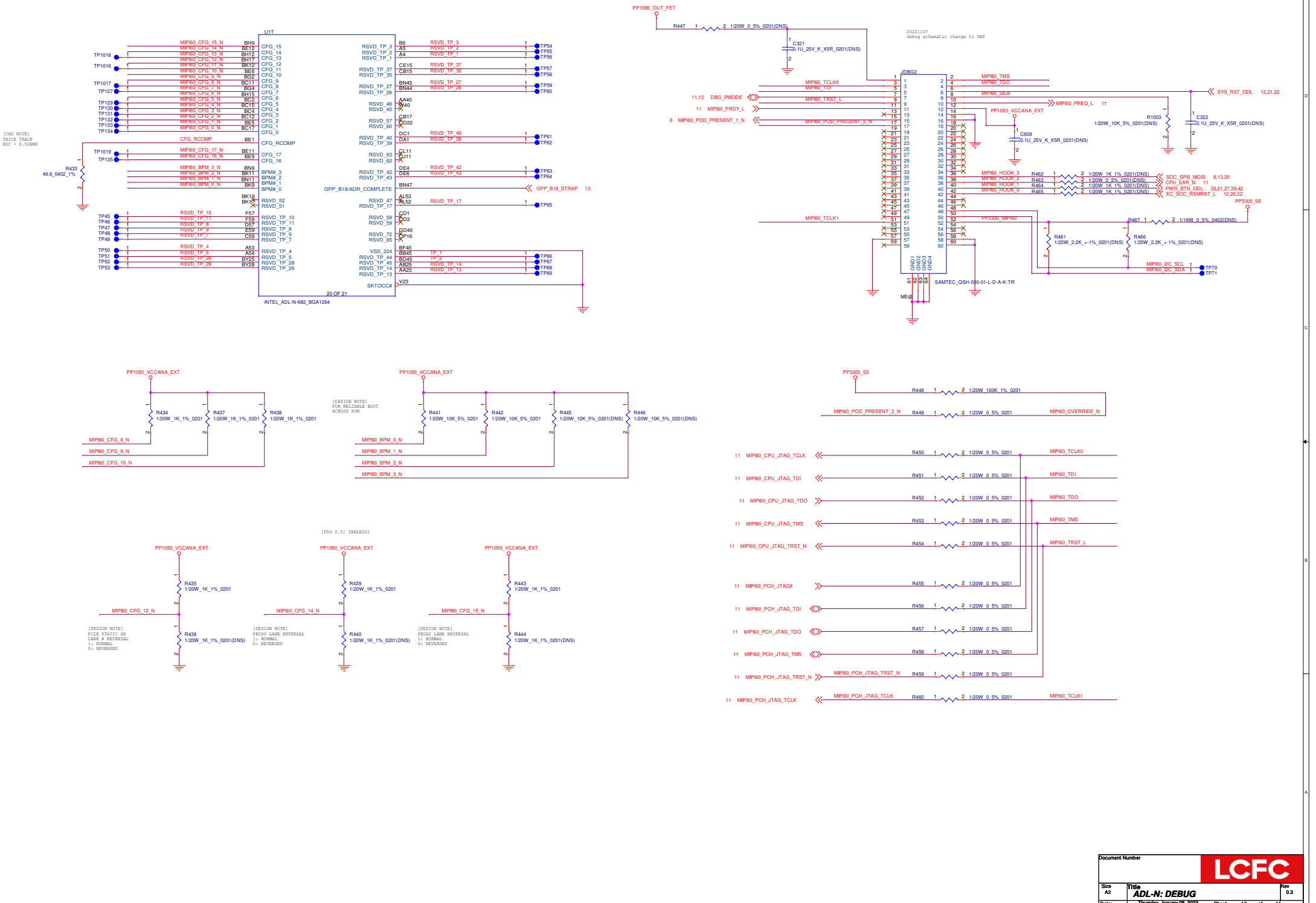
Secondary
22UF 0603 X 8

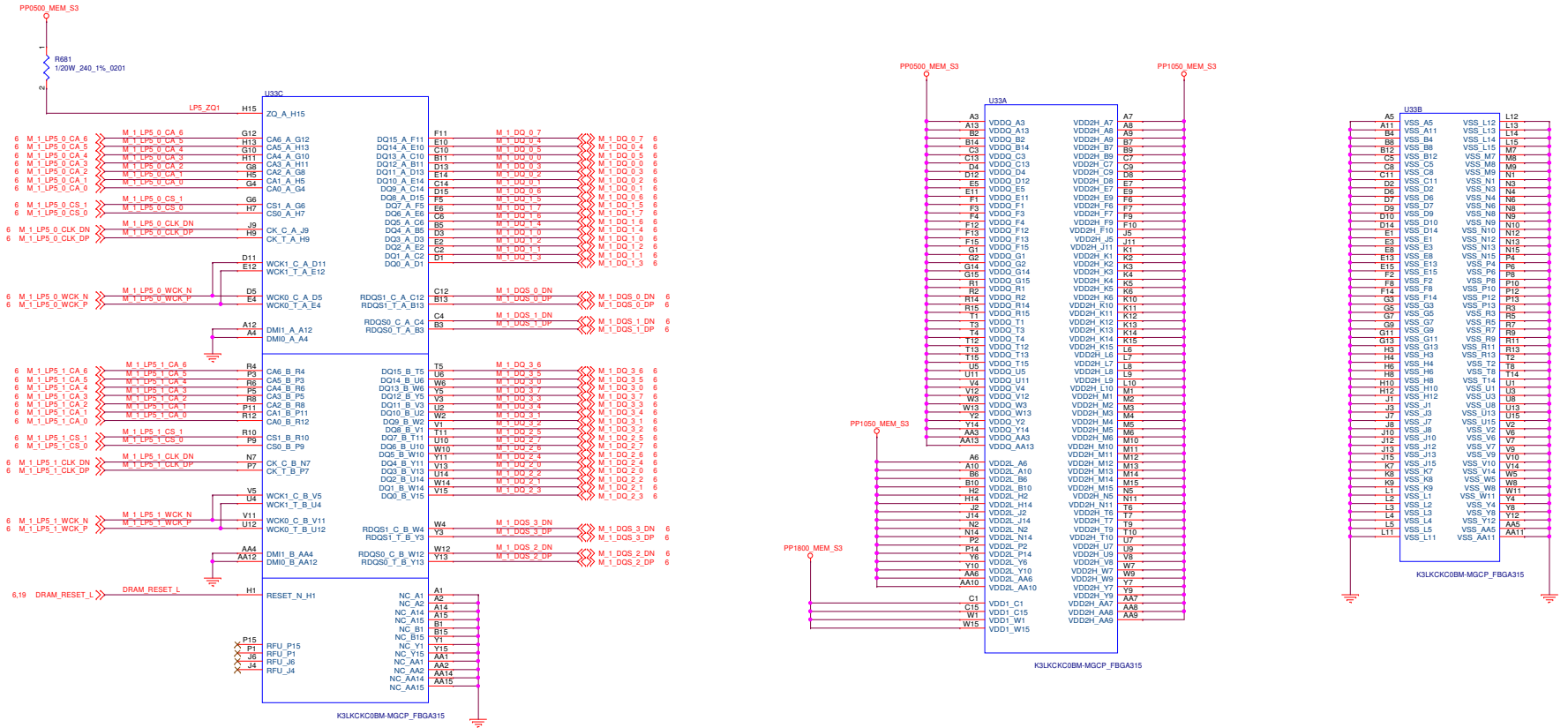


Document Number			LCFC
Size: A1	Title: ADL-N: POWER DECOUPLING		Rev: 0.3
Date: Thursday, January 09, 2020	Sheet 15 of 44		

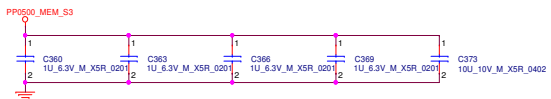


Document Number		LCFC
Size A3	Title ADL-N: GND, RSVD	Rev 0.3
Date: Thursday, January 05, 2023	Sheet 16 of 44	

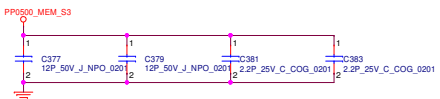

U1T
INTEL_ADL-N-682_BGA1264
20 OF 21
[CAD NOTE]
THICK TRACE
RDC < 0.5OHMS
CFG_RCOMP
R433
49.9_0402_1%
GPP_B18/ADR_COMPLETE
GPP_B18_STRAP
SKTOCC#
PP1050_OUT_FET
R447
C321
0.1U_25V_K_X5R_0201(DNS)
20221107
debug schematic change to DNS
JDBG2
SAMTEC_QSH-030-01-L-D-A-K-TR
ME@
C608
C322
R1003
1/20W_10K_5%_0201(DNS)
PP3300_S5
R467
1/16W_0_5%_0402(DNS)
R461
1/20W_2.2K_+-1%_0201(DNS)
R466
1/20W_2.2K_+-1%_0201(DNS)
PP1050_VCCANA_EXT
R434
1/20W_1K_1%_0201
R437
1/20W_1K_1%_0201
R438
1/20W_1K_1%_0201
[DESIGN NOTE]
FOR RELIABLE BOOT
ACROSS RVM
R441
1/20W_10K_5%_0201
R442
1/20W_10K_5%_0201
R445
1/20W_10K_5%_0201(DNS)
R446
1/20W_10K_5%_0201(DNS)
[PDG 0.5] TABLE201
R435
1/20W_1K_1%_0201
R436
1/20W_1K_1%_0201(DNS)
R439
1/20W_1K_1%_0201
R440
1/20W_1K_1%_0201(DNS)
R443
1/20W_1K_1%_0201
R444
1/20W_1K_1%_0201(DNS)
[DESIGN NOTE]
PCIE STATIC X8
LANE # REVERSAL
1: NORMAL
0: REVERSED
[DESIGN NOTE]
PEG60 LANE REVERSAL
1: NORMAL
0: REVERSED
[DESIGN NOTE]
PEG62 LANE REVERSAL
1: NORMAL
0: REVERSED
R448
1/20W_100K_1%_0201
R449
1/20W_0_5%_0201
R450
R451
R452
R453
R454
R455
R456
R457
R458
R459
R460
1/20W_0_5%_0201
Document Number
LCFC
Size
A2
Title
ADL-N: DEBUG
Rev
0.3
Date:
Thursday, January 05, 2023
Sheet
17
of
44



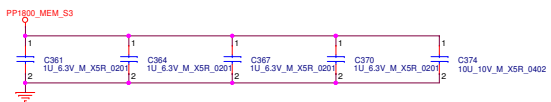
CAD NOTE: PP0500_MEM_S3
4X 1UF PER DRAM, 2 PER SHORT EDGE CLOSE TO VDDQ
1X 10UF PER DRAM



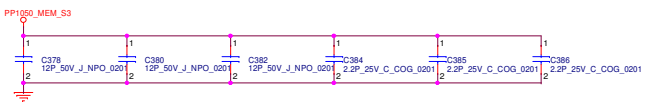
CAD NOTE: PP0500_MEM_S3 EMC CAPS
2X 12PF, 2X 2.2PF



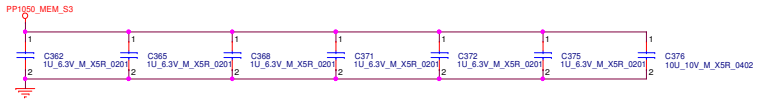
CAD NOTE: PP1800_MEM_S3
4X 1UF PER DRAM, 2 PER LONG EDGE CLOSE TO VDD1
1X 10UF PER DRAM



CAD NOTE: PP1050_MEM_S3 EMC CAPS
3X 12PF, 3X 2.2PF



CAD NOTE: PP1050_MEM_S3
6X 1UF PER DRAM, 2 PER SHORT EDGE, 1 PER LONG EDGE, CLOSE TO VDD2H/VDD2L
1X 10UF PER DRAM

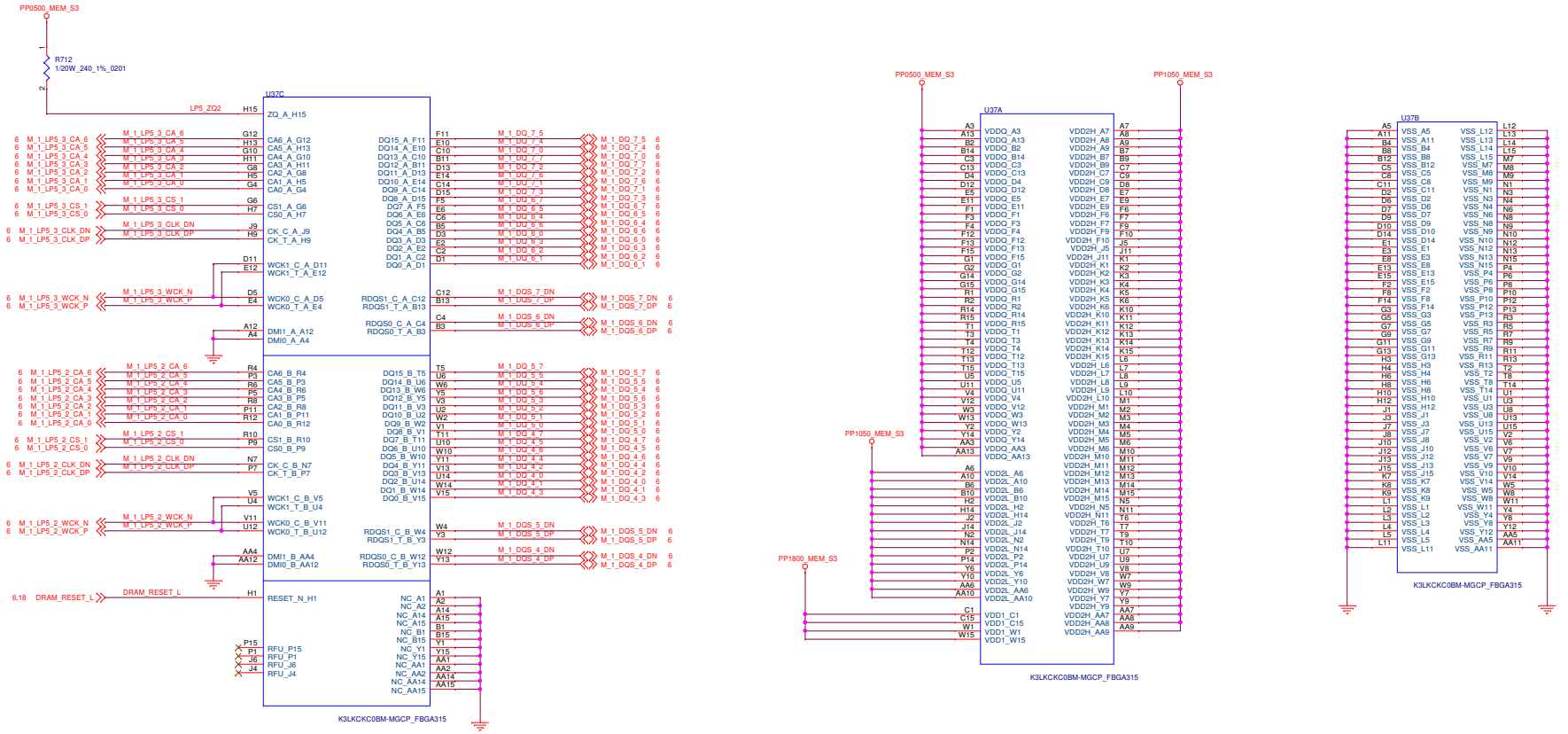


Document Number

LCFC

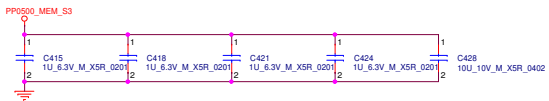
Size	Title	Rev
A2	LPDDR5: CH-A1	0.3

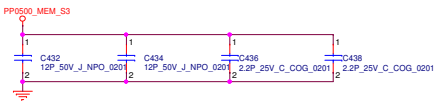
Date: Thursday, January 05, 2023 Sheet 18 of 44



CAD NOTE: PP0500_MEM_S3
4X 1UF PER DRAM, 2 PER SHORT EDGE CLOSE TO VDDQ
1X 10UF PER DRAM

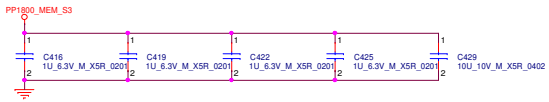
CAD NOTE: PP0500_MEM_S3 EMC CAPS
2X 12PF, 2X 2.2PF

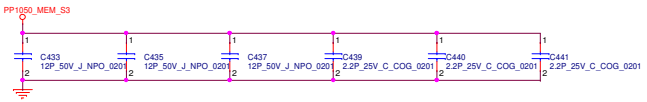




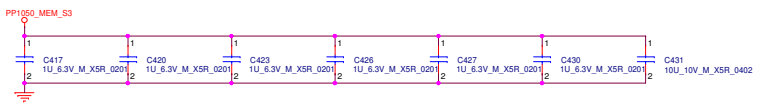
CAD NOTE: PP1800_MEM_S3
4X 1UF PER DRAM, 2 PER LONG EDGE CLOSE TO VDD1
1X 10UF PER DRAM

CAD NOTE: PP1050_MEM_S3 EMC CAPS
3X 12PF, 3X 2.2PF





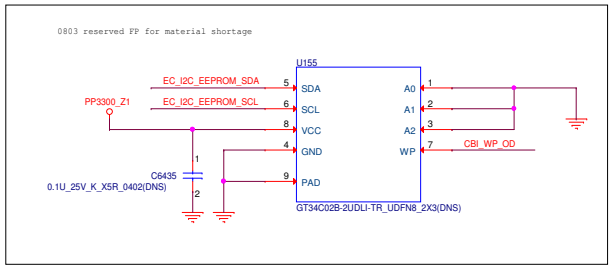
CAD NOTE: PP1050_MEM_S3
6X 1UF PER DRAM, 2 PER SHORT EDGE, 1 PER LONG EDGE, CLOSE TO VDD2H/VDD2L
1X 10UF PER DRAM



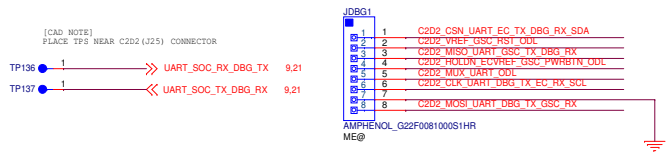
Document Number			LCFC
Size A2	Title LPDDR5: CH-A2		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 19 of 44		

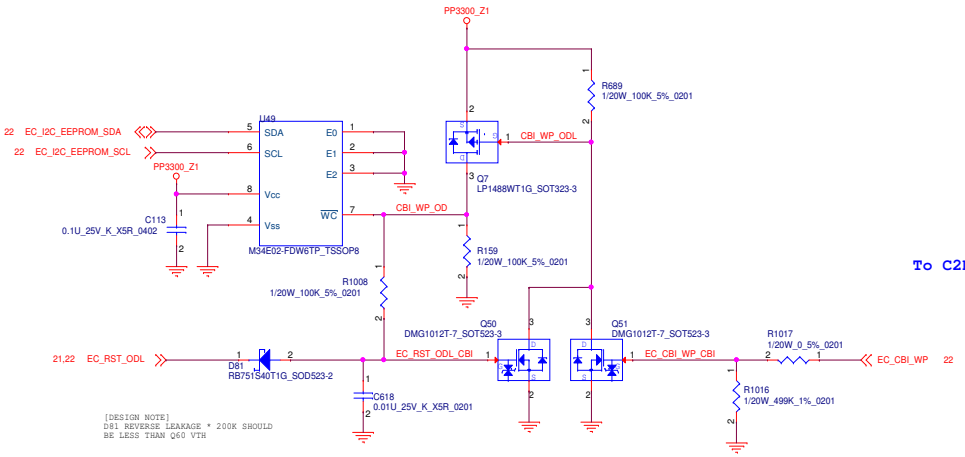
CBI EEPROM

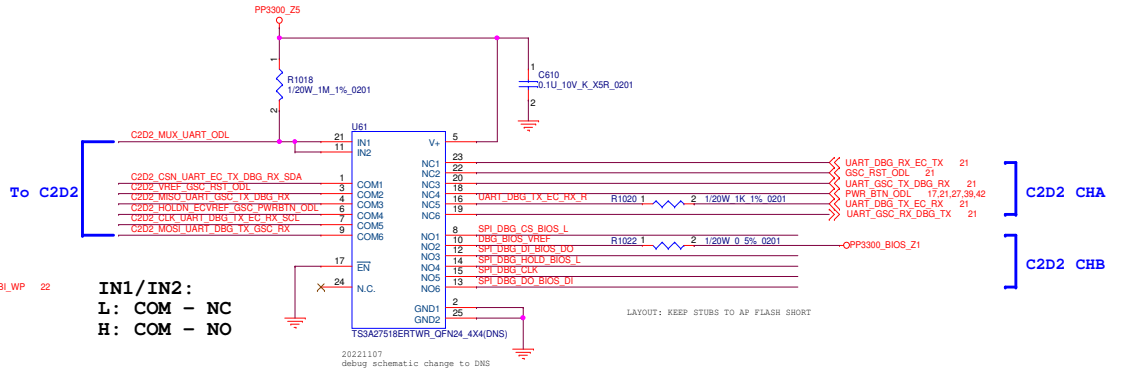
[Note_5/25]
EEPROM change to
SA0000AQ500 (M34E02-FDW6TP)



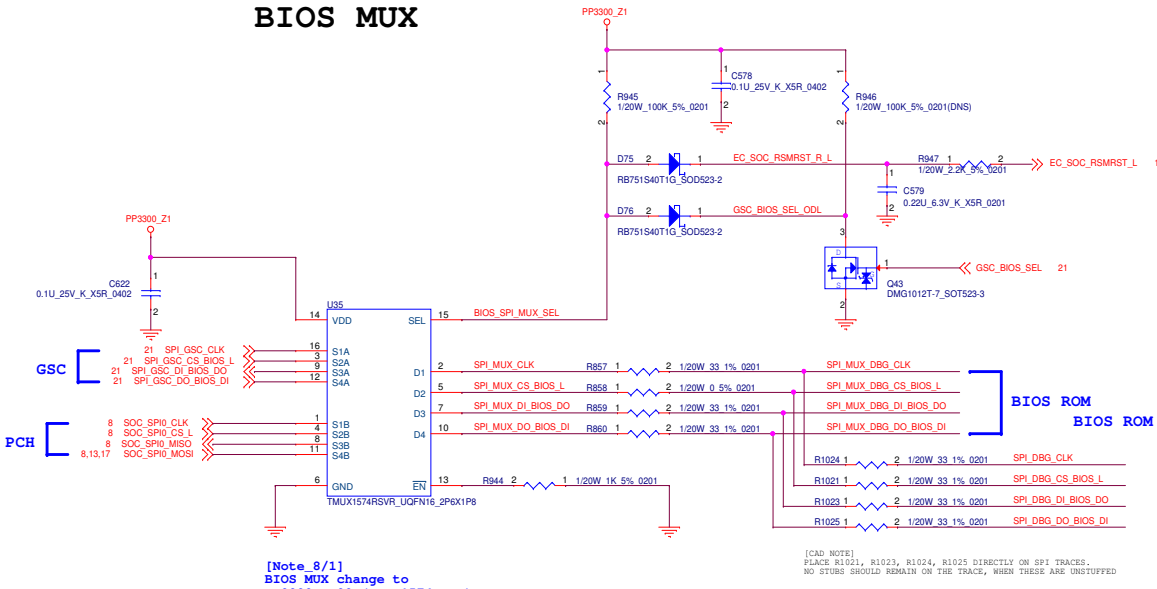
C2D2





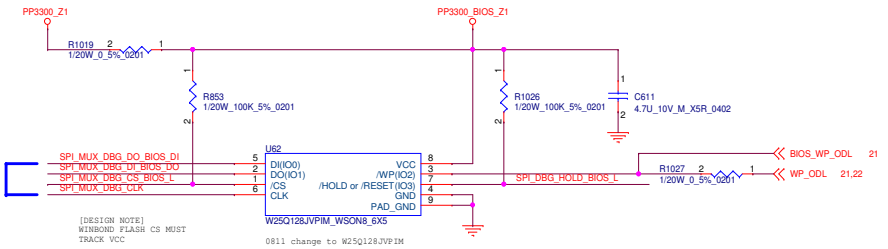


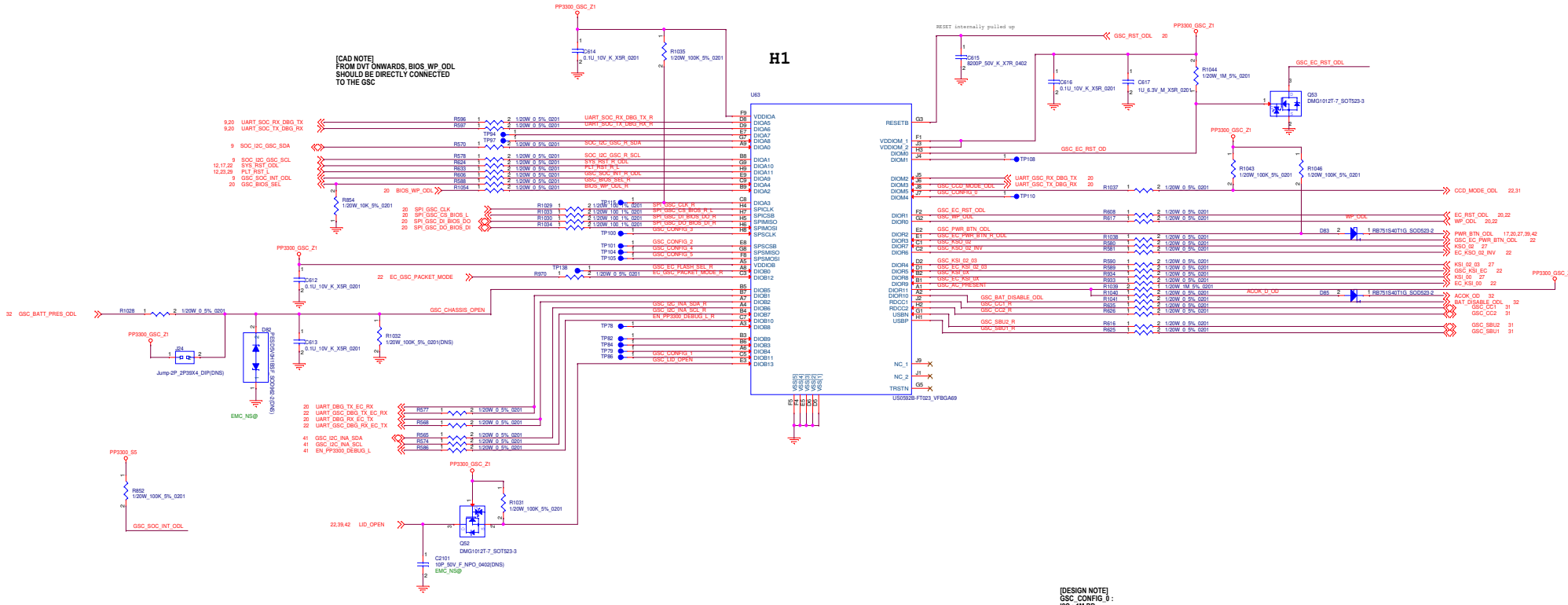
BIOS MUX



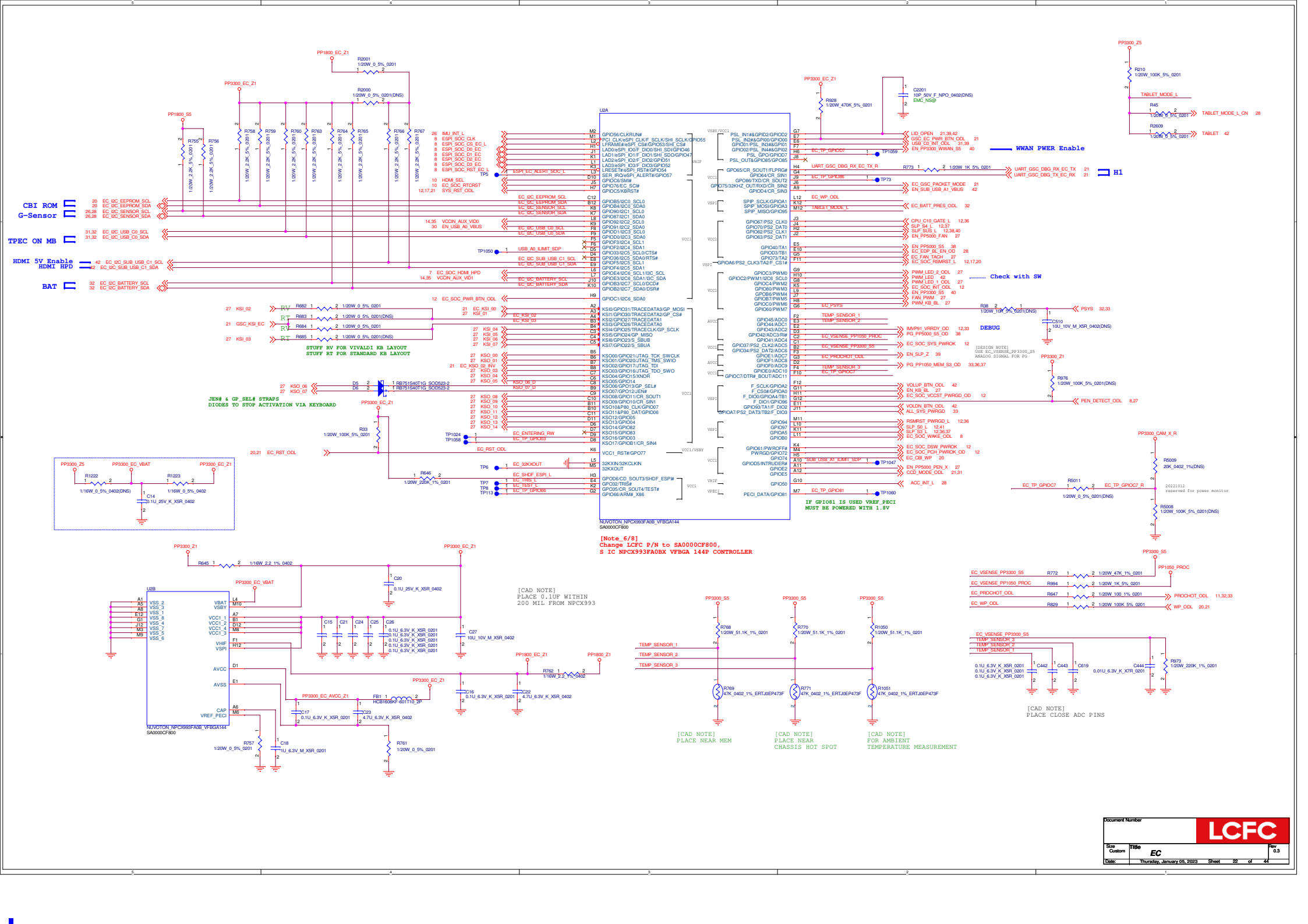
[Note_8/1]
BIOS MUX change to
SA0000BBE00 (TMUX1574RSVR)
Follow NIVVIKS

SPI FLASH (BIOS)

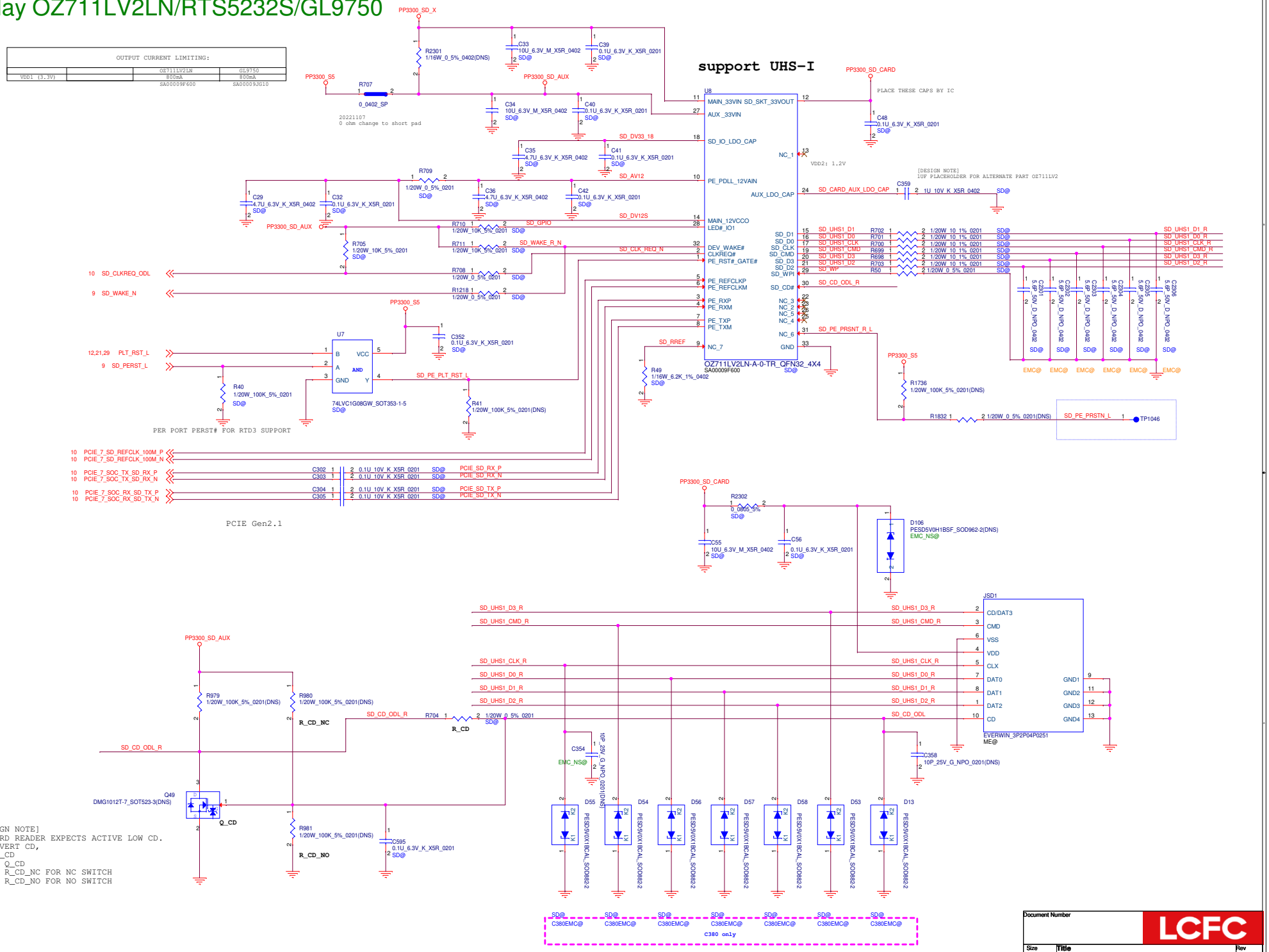


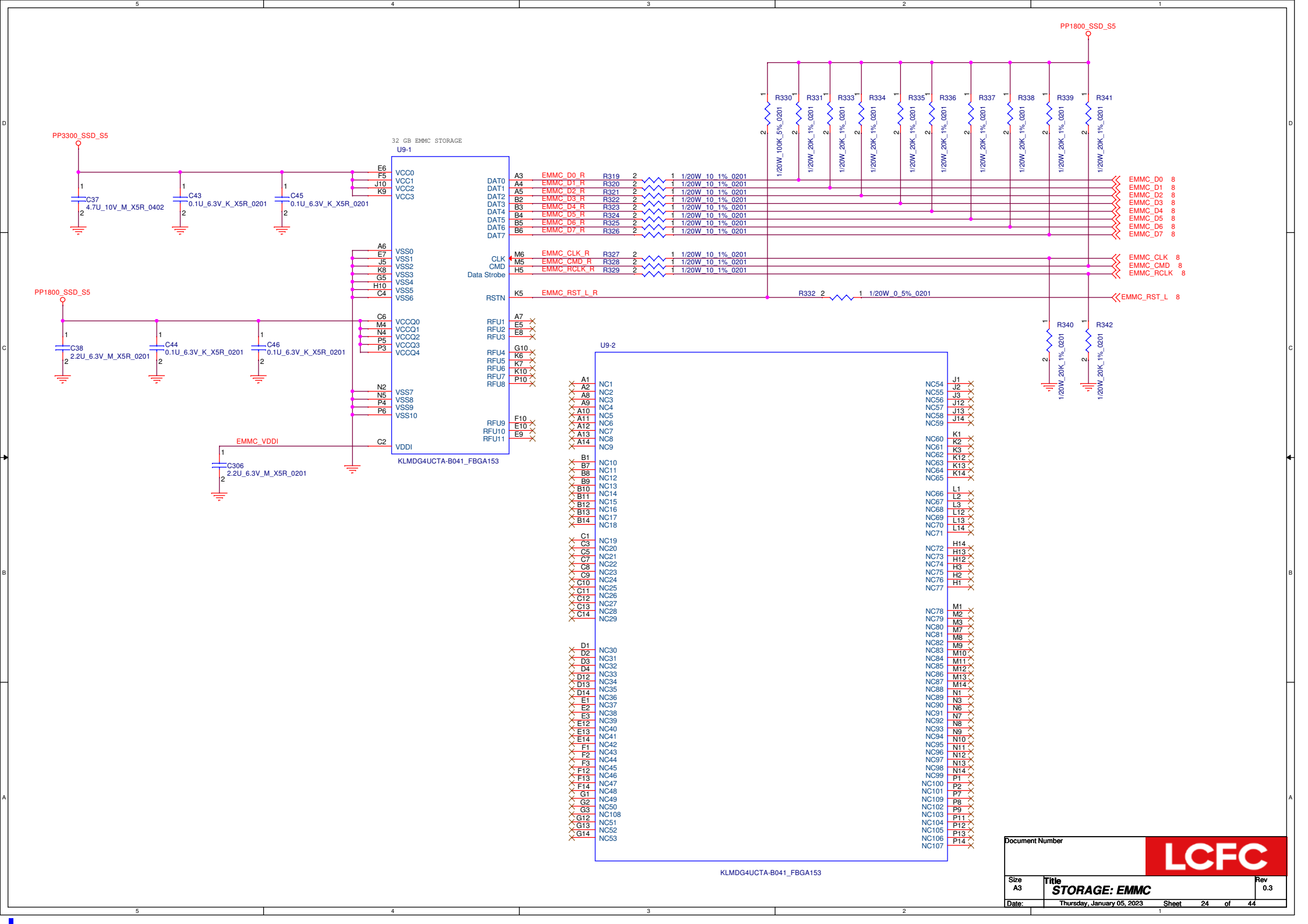


Document Number			LCFC
Size: Custom	Title: GSC		Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 21 of 44		


CBI ROM
G-Sensor
TPEC ON MB
HDMI 5V Enable
HDMI HPD
BAT
U2A
NUVOTON_NPCX993FA0B_VFBGA144
SA0000CF800
WWAN PWER Enable
H1
DEBUG
Check with SW
STUFF RV FOR VIVALDI KB LAYOUT
STUFF RT FOR STANDARD KB LAYOUT
JEN# & GP_SEL# STRAPS
DIODES TO STOP ACTIVATION VIA KEYBOARD
IF GPIO81 IS USED VREF_PECI
MUST BE POWERED WITH 1.8V
[Note_6/8]
Change LCFC P/N to SA0000CF800,
S IC NPCX993FA0BX VFBGA 144P CONTROLLER
[CAD NOTE]
PLACE 0.1UF WITHIN
200 MIL FROM NPCX993
[CAD NOTE]
PLACE NEAR MEM
[CAD NOTE]
PLACE NEAR
CHASSIS HOT SPOT
[CAD NOTE]
FOR AMBIENT
TEMPERATURE MEASUREMENT
[CAD NOTE]
PLACE CLOSE ADC PINS
Document Number
LCFC
Size
Custom
Title
EC
Rev
0.3
Date:
Thursday, January 05, 2023
Sheet
22
of
44

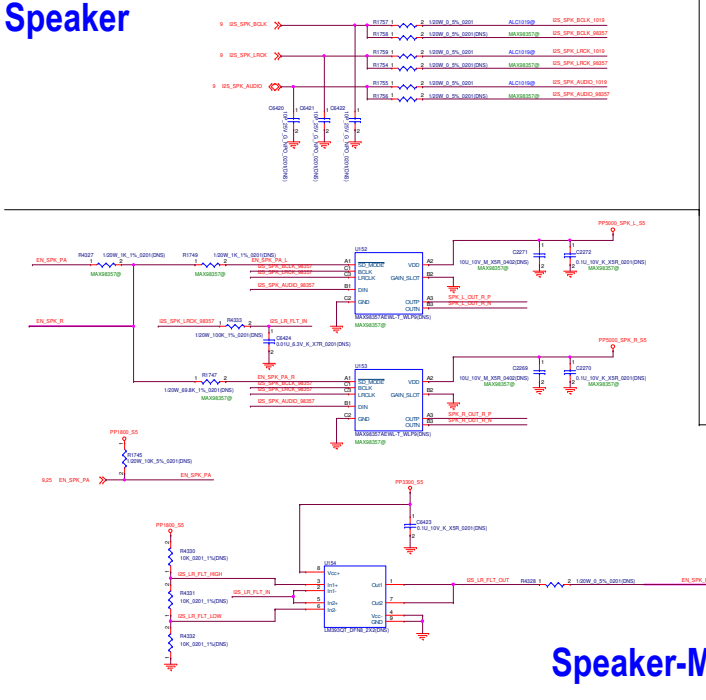
Colay OZ711LV2LN/RTS5232S/GL9750



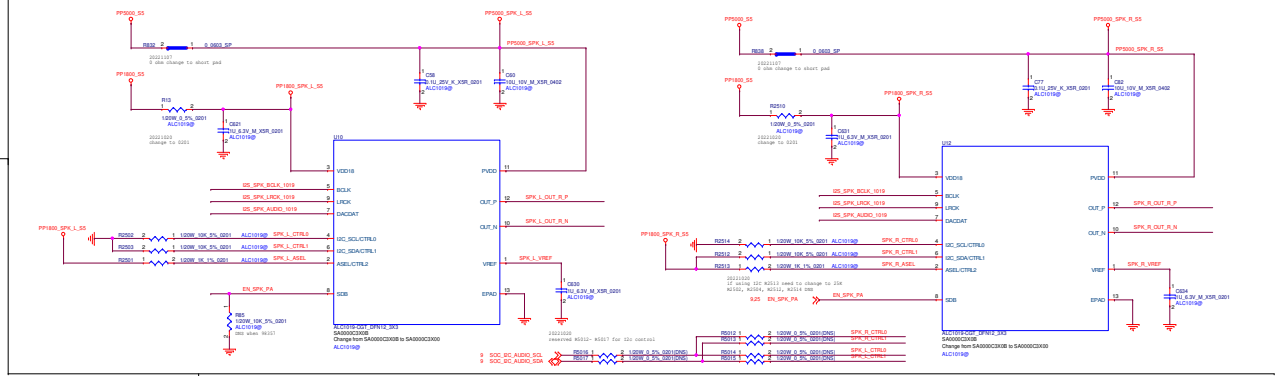


Document Number		LCFC
Size A3	Title STORAGE: EMMC	Rev 0.3
Date: Thursday, January 05, 2023	Sheet 24 of 44	

Speaker

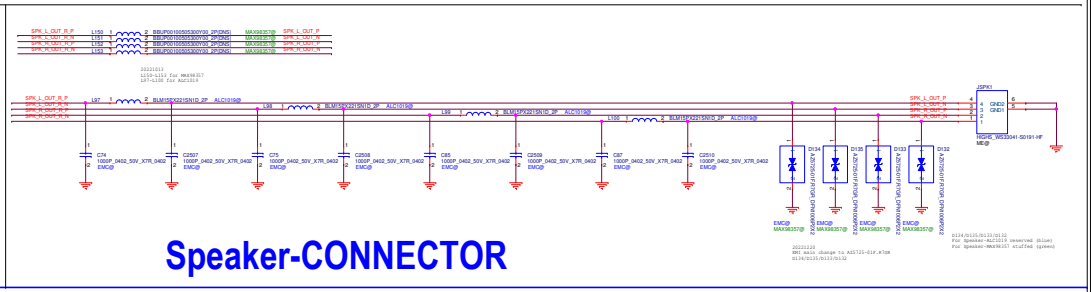


Speaker-ALC1019

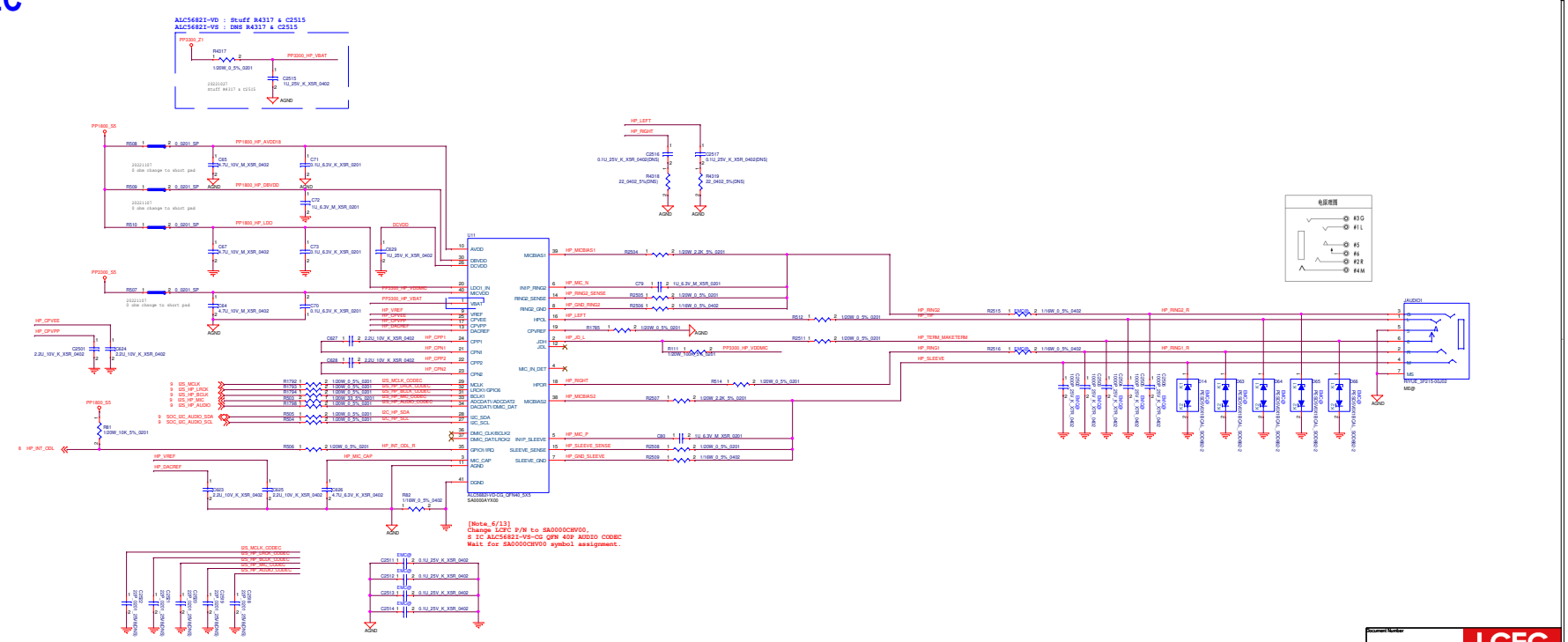


Speaker-MAX98357

Speaker-CONNECTOR

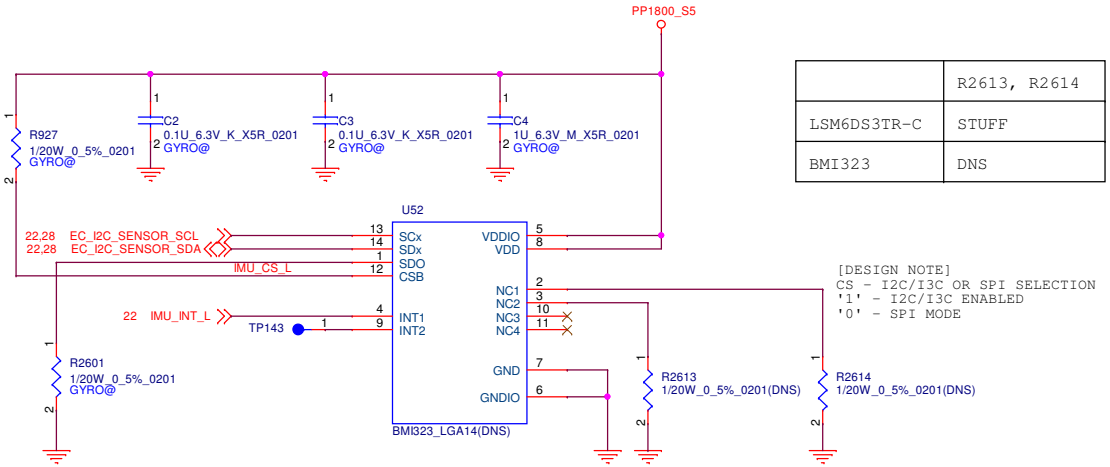


CODEC



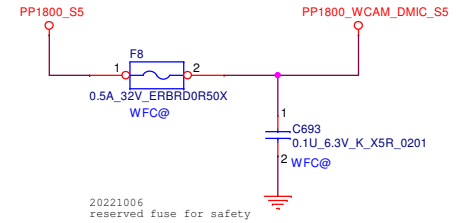
Sensor

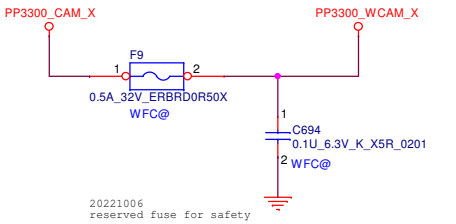
IMU 6 AXIS



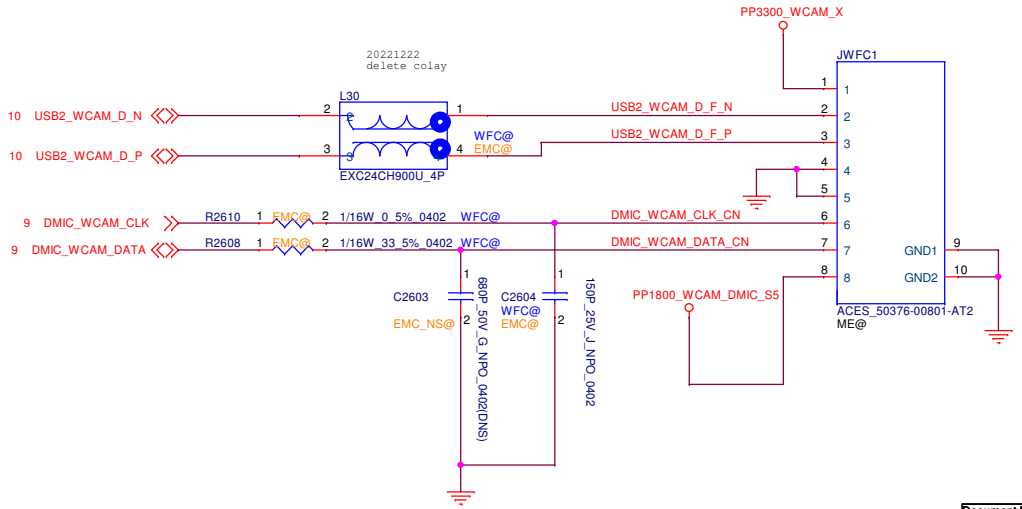
	R2613, R2614
LSM6DS3TR-C	STUFF
BMI323	DNS

WFC [USB]

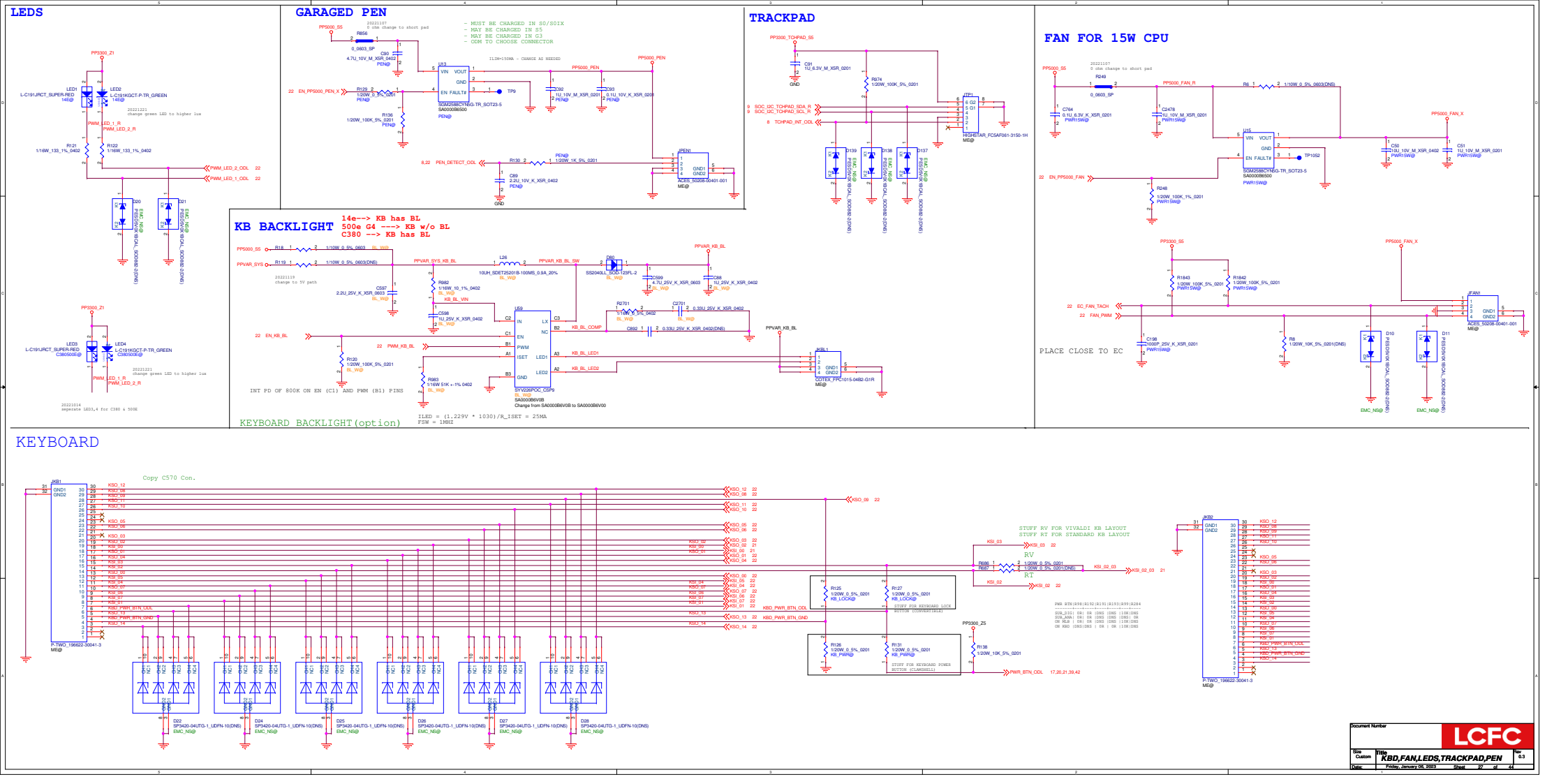


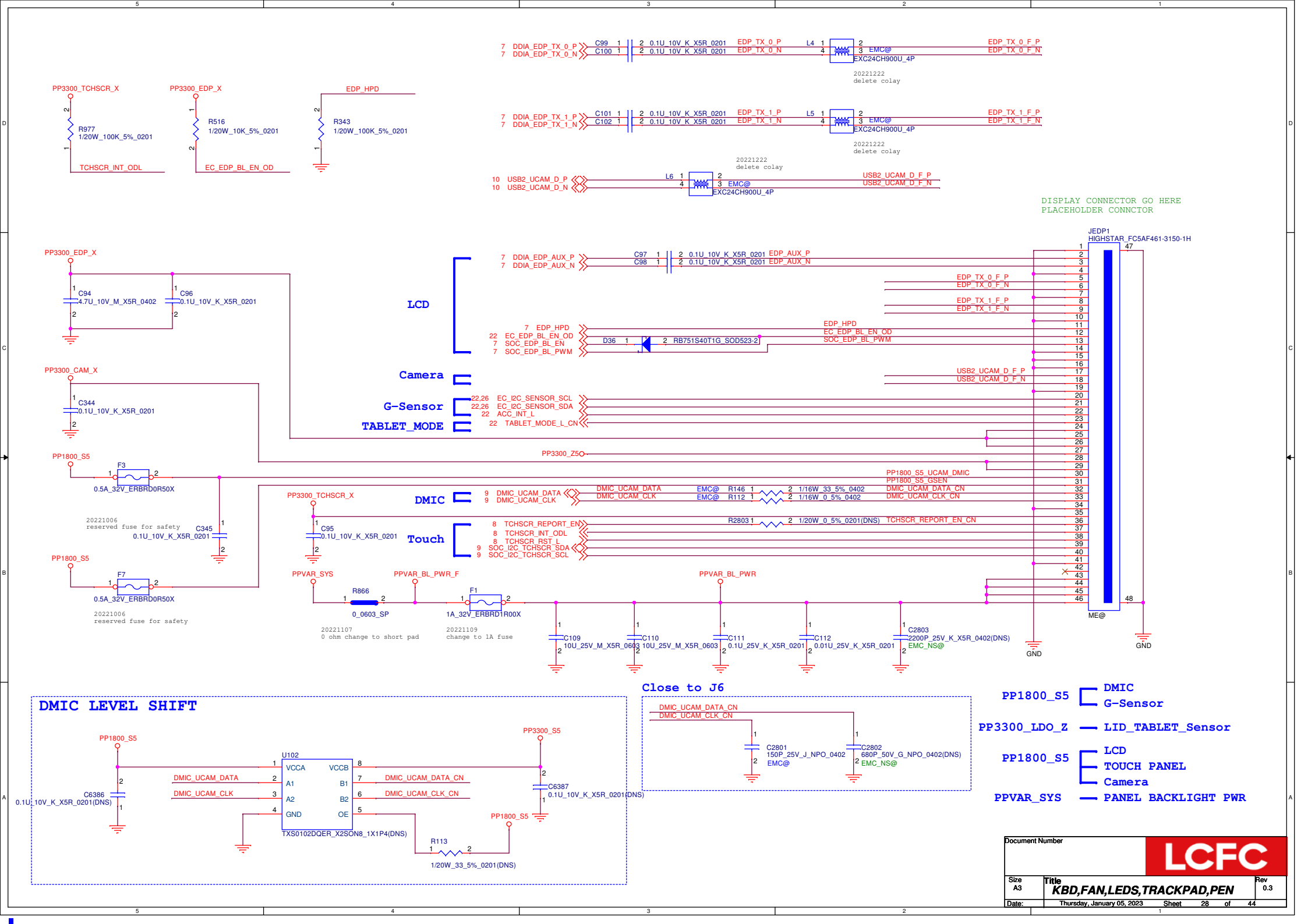


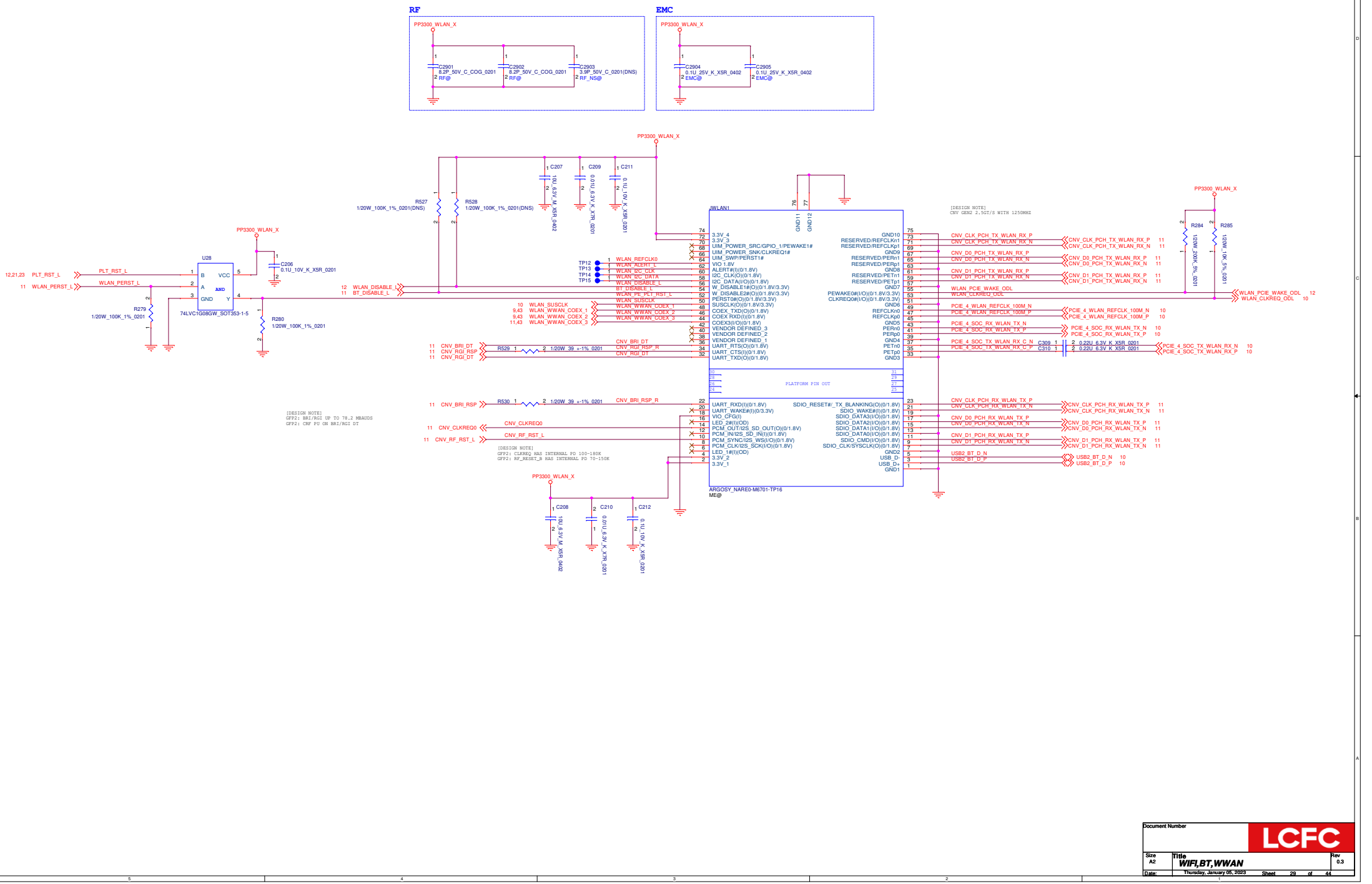
WFC [USB]



Document Number			LCFC
Size A3	Title SENSORS,WCAM		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 26 of 44		


LEDS
GARAGED PEN
- MUST BE CHARGED IN S0/S0IX
- MAY BE CHARGED IN S5
- MAY BE CHARGED IN G3
- ODM TO CHOOSE CONNECTOR
TRACKPAD
FAN FOR 15W CPU
KB BACKLIGHT
14e--> KB has BL
500e G4 ---> KB w/o BL
C380 --> KB has BL
KEYBOARD BACKLIGHT(option)
PLACE CLOSE TO EC
KEYBOARD
Copy C570 Con.
STUFF RV FOR VIVALDI KB LAYOUT
STUFF RT FOR STANDARD KB LAYOUT
Document Number
LCFC
KBD,FAN,LEDS,TRACKPAD,PEN
Rev 0.3
Friday, January 06, 2023
Sheet 27 of 44

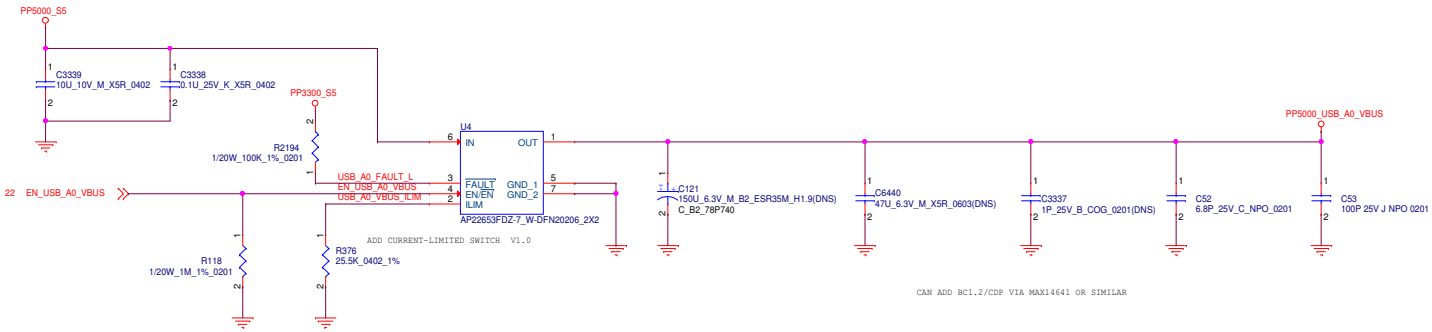

PP3300_TCHSCR_X
R977
1/20W_100K_5%_0201
TCHSCR_INT_ODL
PP3300_EDP_X
R516
1/20W_10K_5%_0201
EC_EDP_BL_EN_OD
EDP_HPD
R343
1/20W_100K_5%_0201
7 DDIA_EDP_TX_0_P
7 DDIA_EDP_TX_0_N
C99 0.1U_10V_K_X5R_0201
C100 0.1U_10V_K_X5R_0201
EDP_TX_0_P
EDP_TX_0_N
L4 EMC@ EXC24CH900U_4P
EDP_TX_0_F_P
EDP_TX_0_F_N
20221222
delete colay
7 DDIA_EDP_TX_1_P
7 DDIA_EDP_TX_1_N
C101 0.1U_10V_K_X5R_0201
C102 0.1U_10V_K_X5R_0201
EDP_TX_1_P
EDP_TX_1_N
L5 EMC@ EXC24CH900U_4P
EDP_TX_1_F_P
EDP_TX_1_F_N
20221222
delete colay
20221222
delete colay
10 USB2_UCAM_D_P
10 USB2_UCAM_D_N
L6 EMC@ EXC24CH900U_4P
USB2_UCAM_D_F_P
USB2_UCAM_D_F_N
DISPLAY CONNECTOR GO HERE
PLACEHOLDER CONNCTOR
JEDP1
HIGHSTAR_FC5AF461-3150-1H
PP3300_EDP_X
C94 4.7U_10V_M_X5R_0402
C96 0.1U_10V_K_X5R_0201
LCD
7 DDIA_EDP_AUX_P
7 DDIA_EDP_AUX_N
C97 0.1U_10V_K_X5R_0201
C98 0.1U_10V_K_X5R_0201
EDP_AUX_P
EDP_AUX_N
EDP_TX_0_F_P
EDP_TX_0_F_N
EDP_TX_1_F_P
EDP_TX_1_F_N
7 EDP_HPD
22 EC_EDP_BL_EN_OD
7 SOC_EDP_BL_EN
7 SOC_EDP_BL_PWM
D36 RB751S40T1G_SOD523-2
EDP_HPD
EC_EDP_BL_EN_OD
SOC_EDP_BL_PWM
PP3300_CAM_X
C344 0.1U_10V_K_X5R_0201
Camera
USB2_UCAM_D_F_P
USB2_UCAM_D_F_N
G-Sensor
22,26 EC_I2C_SENSOR_SCL
22,26 EC_I2C_SENSOR_SDA
22 ACC_INT_L
TABLET_MODE
22 TABLET_MODE_L_CN
PP3300_Z5
PP1800_S5
F3
0.5A_32V_ERBRD0R50X
20221006
reserved fuse for safety
C345 0.1U_10V_K_X5R_0201
PP1800_S5_UCAM_DMIC
PP1800_S5_GSEN
DMIC
9 DMIC_UCAM_DATA
9 DMIC_UCAM_CLK
DMIC_UCAM_DATA
DMIC_UCAM_CLK
EMC@ R146 1/16W_33_5%_0402
EMC@ R112 1/16W_0_5%_0402
DMIC_UCAM_DATA_CN
DMIC_UCAM_CLK_CN
PP3300_TCHSCR_X
C95 0.1U_10V_K_X5R_0201
Touch
8 TCHSCR_REPORT_EN
8 TCHSCR_INT_ODL
8 TCHSCR_RST_L
9 SOC_I2C_TCHSCR_SDA
9 SOC_I2C_TCHSCR_SCL
R2803 1/20W_0_5%_0201(DNS)
TCHSCR_REPORT_EN_CN
PP1800_S5
F7
0.5A_32V_ERBRD0R50X
20221006
reserved fuse for safety
PPVAR_SYS
PPVAR_BL_PWR_F
R866 0_0603_SP
F1 1A_32V_ERBRD1R00X
20221107
0 ohm change to short pad
20221109
change to 1A fuse
PPVAR_BL_PWR
C109 10U_25V_M_X5R_0603
C110 10U_25V_M_X5R_0603
C111 0.1U_25V_K_X5R_0201
C112 0.01U_25V_K_X5R_0201
C2803 2200P_25V_K_X5R_0402(DNS)
EMC_NS@
ME@
GND
GND
DMIC LEVEL SHIFT
PP1800_S5
C6386 0.1U_10V_K_X5R_0201(DNS)
U102
VCCA
A1
A2
GND
VCCB
B1
B2
OE
DMIC_UCAM_DATA
DMIC_UCAM_CLK
DMIC_UCAM_DATA_CN
DMIC_UCAM_CLK_CN
TXS0102DQER_X2SON8_1X1P4(DNS)
PP3300_S5
C6387 0.1U_10V_K_X5R_0201(DNS)
PP1800_S5
R113 1/20W_33_5%_0201(DNS)
Close to J6
DMIC_UCAM_DATA_CN
DMIC_UCAM_CLK_CN
C2801 150P_25V_J_NPO_0402 EMC@
C2802 680P_50V_G_NPO_0402(DNS) EMC_NS@
PP1800_S5
DMIC
G-Sensor
PP3300_LDO_Z
LID_TABLET_Sensor
PP1800_S5
LCD
TOUCH PANEL
Camera
PPVAR_SYS
PANEL BACKLIGHT PWR
Document Number
LCFC
Size A3
Title KBD,FAN,LEDS,TRACKPAD,PEN
Rev 0.3
Date: Thursday, January 05, 2023
Sheet 28 of 44


RF
EMC
PP3300_WLAN_X
C2901 8.2P_50V_C_COG_0201 RF@
C2902 8.2P_50V_C_COG_0201 RF@
C2903 3.9P_50V_C_0201(DNS) RF_NS@
C2904 0.1U_25V_K_X5R_0402 EMC@
C2905 0.1U_25V_K_X5R_0402 EMC@
U28
74LVC1G08GW_SOT353-1-5
PLT_RST_L
WLAN_PERST_L
C206 0.1U_10V_K_X5R_0201
R279 1/20W_100K_1%_0201
R280 1/20W_100K_1%_0201
R527 1/20W_100K_1%_0201(DNS)
R528 1/20W_100K_1%_0201(DNS)
C207 10U_6.3V_M_X5R_0402
C209 0.01U_6.3V_K_X7R_0201
C211 0.1U_10V_K_X5R_0201
C208 10U_6.3V_M_X5R_0402
C210 0.01U_6.3V_K_X7R_0201
C212 0.1U_10V_K_X5R_0201
JWLAN1
ARGOSY_NARE0-M6701-TP16
ME@
PLATFORM PIN OUT
WLAN_REFCLK0
WLAN_ALERT_L
WLAN_I2C_CLK
WLAN_I2C_DATA
WLAN_DISABLE_L
BT_DISABLE_L
WLAN_PE_PLT_RST_L
WLAN_SUSCLK
WLAN_WWAN_COEX_1
WLAN_WWAN_COEX_2
WLAN_WWAN_COEX_3
CNV_BRI_DT
CNV_RGI_RSP_R
CNV_RGI_DT
R529 1/20W_39_+-1%_0201
CNV_BRI_RSP
R530 1/20W_39_+-1%_0201
CNV_BRI_RSP_R
CNV_CLKREQ0
CNV_RF_RST_L
3.3V_4
3.3V_3
UIM_POWER_SRC/GPIO_1/PEWAKE1#
UIM_POWER_SNK/CLKREQ1#
UIM_SWP/PERST1#
VIO 1.8V
ALERT#(I)(0/1.8V)
I2C_CLK(O)(0/1.8V)
I2C_DATA(I/O)(0/1.8V)
W_DISABLE1#(O)(0/1.8V/3.3V)
W_DISABLE2#(O)(0/1.8V/3.3V)
PERST0#(O)(0/1.8V/3.3V)
SUSCLK(O)(0/1.8V/3.3V)
COEX_TXD(O)(0/1.8V)
COEX RXD(I)(0/1.8V)
COEX3(I/O)(0/1.8V)
VENDOR DEFINED_3
VENDOR DEFINED_2
VENDOR DEFINED_1
UART_RTS(O)(0/1.8V)
UART_CTS(I)(0/1.8V)
UART_TXD(O)(0/1.8V)
UART_RXD(I)(0/1.8V)
UART_WAKE#(I)(0/3.3V)
VIO_CFG(I)
LED_2#(I)(OD)
PCM_OUT/I2S_SD_OUT(O)(0/1.8V)
PCM_IN/I2S_SD_IN(I)(0/1.8V)
PCM_SYNC/I2S_WS(I/O)(0/1.8V)
PCM_CLK/I2S_SCK(I/O)(0/1.8V)
LED_1#(I)(OD)
3.3V_2
3.3V_1
GND10
RESERVED/REFCLKn1
RESERVED/REFCLKp1
GND9
RESERVED/PERn1
RESERVED/PERp1
GND8
RESERVED/PETn1
RESERVED/PETp1
GND7
PEWAKE0#(I/O)(0/1.8V/3.3V)
CLKREQ0#(I/O)(0/1.8V/3.3V)
GND6
REFCLKn0
REFCLKp0
GND5
PERn0
PERp0
GND4
PETn0
PETp0
GND3
SDIO_RESET#/_TX_BLANKING(O)(0/1.8V)
SDIO_WAKE#(I)(0/1.8V)
SDIO_DATA3(I/O)(0/1.8V)
SDIO_DATA2(I/O)(0/1.8V)
SDIO_DATA1(I/O)(0/1.8V)
SDIO_DATA0(I/O)(0/1.8V)
SDIO_CMD(I/O)(0/1.8V)
SDIO_CLK/SYSCLK(O)(0/1.8V)
GND2
USB_D-
USB_D+
GND1
GND11
GND12
[DESIGN NOTE]
CNV GEN2 2.5GT/S WITH 1250MHZ
CNV_CLK_PCH_TX_WLAN_RX_P
CNV_CLK_PCH_TX_WLAN_RX_N
CNV_D0_PCH_TX_WLAN_RX_P
CNV_D0_PCH_TX_WLAN_RX_N
CNV_D1_PCH_TX_WLAN_RX_P
CNV_D1_PCH_TX_WLAN_RX_N
WLAN_PCIE_WAKE_ODL
WLAN_CLKREQ_ODL
PCIE_4_WLAN_REFCLK_100M_N
PCIE_4_WLAN_REFCLK_100M_P
PCIE_4_SOC_RX_WLAN_TX_N
PCIE_4_SOC_RX_WLAN_TX_P
PCIE_4_SOC_TX_WLAN_RX_C_N
PCIE_4_SOC_TX_WLAN_RX_C_P
C309 0.22U_6.3V_K_X5R_0201
C310 0.22U_6.3V_K_X5R_0201
CNV_CLK_PCH_RX_WLAN_TX_P
CNV_CLK_PCH_RX_WLAN_TX_N
CNV_D0_PCH_RX_WLAN_TX_P
CNV_D0_PCH_RX_WLAN_TX_N
CNV_D1_PCH_RX_WLAN_TX_P
CNV_D1_PCH_RX_WLAN_TX_N
USB2_BT_D_N
USB2_BT_D_P
R284 1/20W_200K_5%_0201
R285 1/20W_10K_5%_0201
[DESIGN NOTE]
GFP2: BRI/RGI UP TO 78.2 MBAUDS
GFP2: CRF PU ON BRI/RGI DT
[DESIGN NOTE]
GFP2: CLKREQ HAS INTERNAL PD 100-180K
GFP2: RF_RESET_B HAS INTERNAL PD 70-150K
Document Number
LCFC
Size A2
Title WIFI,BT,WWAN
Rev 0.3
Date: Thursday, January 05, 2023
Sheet 29 of 44

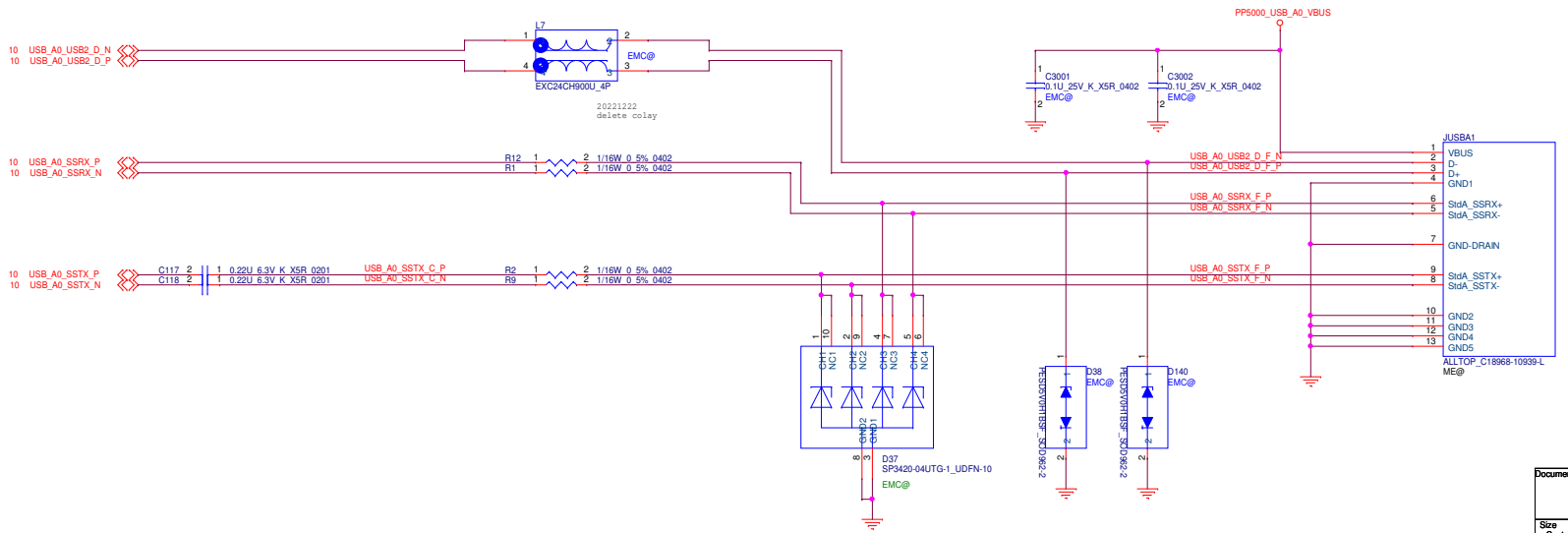
USB-A BC1.2

Option

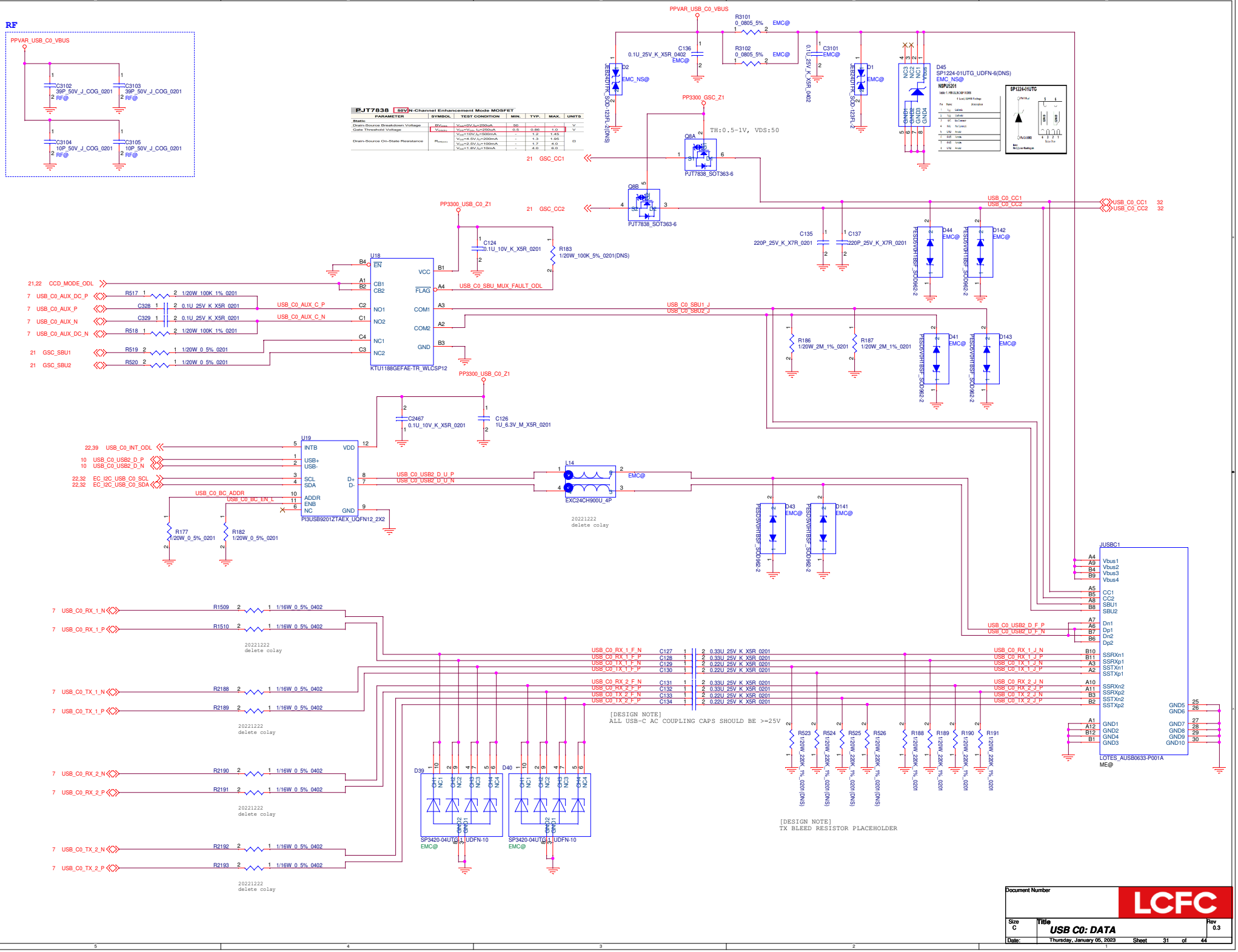
USB-A POWER

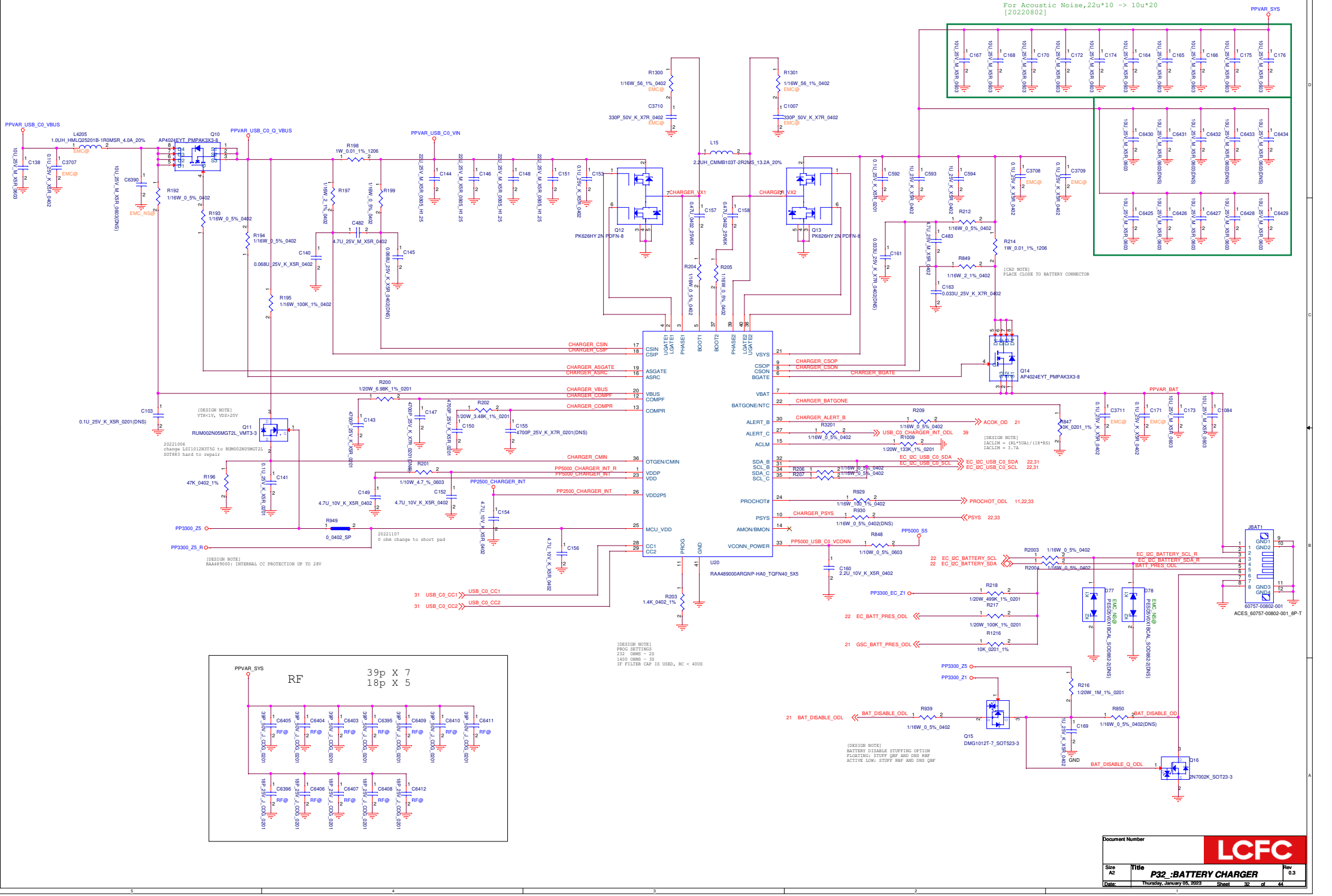


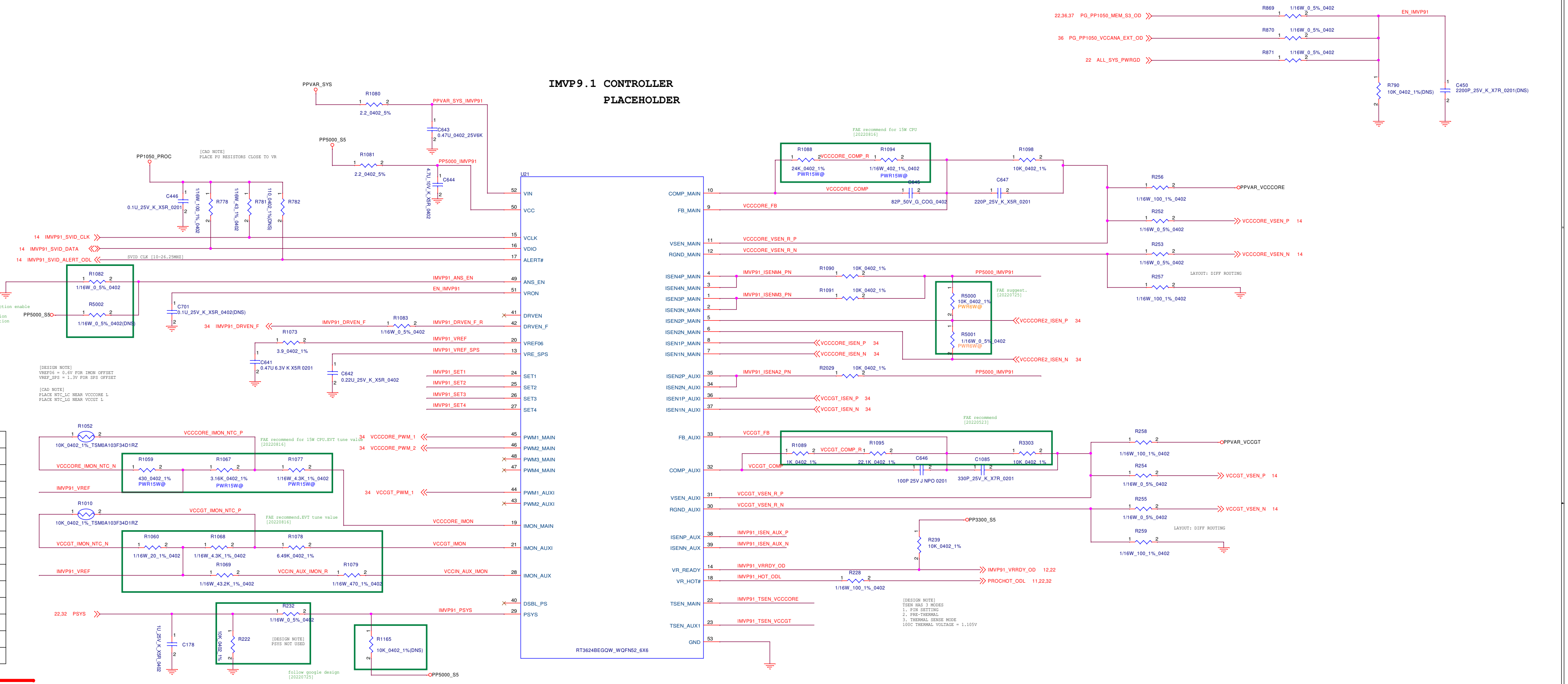
USB3.2 Gen1



Document Number	LCFC		
Size: Custom	Title: KBD,FAN,LEDS,TRACKPAD,PEN		Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 30 of 44		


RF
PPVAR_USB_C0_VBUS
C3102 39P_50V_J_COG_0201 RF@
C3103 39P_50V_J_COG_0201 RF@
C3104 10P_50V_J_COG_0201 RF@
C3105 10P_50V_J_COG_0201 RF@
PPVAR_USB_C0_VBUS
R3101 0_0805_5% EMC@
R3102 0_0805_5% EMC@
C136 0.1U_25V_K_X5R_0402 EMC@
C3101 0.1U_25V_K_X5R_0402 EMC@
D2 JEB24DTFK_SOD-123FL-2(DNS) EMC_NS@
D1 JEB24DTFK_SOD-123FL-2 EMC@
D45 SP1224-01UTG_UDFN-6(DNS) EMC_NS@
PJT7838 50V N-Channel Enhancement Mode MOSFET
PARAMETER SYMBOL TEST CONDITION MIN. TYP. MAX. UNITS
Static
Drain-Source Breakdown Voltage
Gate Threshold Voltage
Drain-Source On-State Resistance
PP3300_GSC_Z1
TH:0.5~1V, VDS:50
Q8A
PJT7838_SOT363-6
21 GSC_CC1
Q8B
PJT7838_SOT363-6
21 GSC_CC2
PP3300_USB_C0_Z1
C124 0.1U_10V_K_X5R_0201
R183 1/20W_100K_5%_0201(DNS)
USB_C0_CC1
USB_C0_CC2
USB_C0_CC1 32
USB_C0_CC2 32
C135 220P_25V_K_X7R_0201
C137 220P_25V_K_X7R_0201
D44 EMC@
D142 EMC@
U18
KTU1188GEFAE-TR_WLCSP12
21,22 CCD_MODE_ODL
7 USB_C0_AUX_DC_P
7 USB_C0_AUX_P
7 USB_C0_AUX_N
7 USB_C0_AUX_DC_N
21 GSC_SBU1
21 GSC_SBU2
R517 1/20W_100K_1%_0201
C328 0.1U_25V_K_X5R_0201
C329 0.1U_25V_K_X5R_0201
R518 1/20W_100K_1%_0201
R519 1/20W_0_5%_0201
R520 1/20W_0_5%_0201
USB_C0_AUX_C_P
USB_C0_AUX_C_N
USB_C0_SBU_MUX_FAULT_ODL
USB_C0_SBU1_J
USB_C0_SBU2_J
R186 1/20W_2M_1%_0201
R187 1/20W_2M_1%_0201
D41 EMC@
D143 EMC@
PP3300_USB_C0_Z1
C2467 0.1U_10V_K_X5R_0201
C126 1U_6.3V_M_X5R_0201
U19
PI3USB9201ZTAEX_UQFN12_2X2
22,39 USB_C0_INT_ODL
10 USB_C0_USB2_D_P
10 USB_C0_USB2_D_N
22,32 EC_I2C_USB_C0_SCL
22,32 EC_I2C_USB_C0_SDA
USB_C0_BC_ADDR
USB_C0_BC_EN_L
R177 1/20W_0_5%_0201
R182 1/20W_0_5%_0201
USB_C0_USB2_D_U_P
USB_C0_USB2_D_U_N
L14
EXC24CH900U_4P
EMC@
20221222
delete colay
D43 EMC@
D141 EMC@
JUSBC1
LOTES_AUSB0633-P001A
ME@
USB_C0_USB2_D_F_P
USB_C0_USB2_D_F_N
7 USB_C0_RX_1_N
7 USB_C0_RX_1_P
R1509 1/16W_0_5%_0402
R1510 1/16W_0_5%_0402
20221222
delete colay
7 USB_C0_TX_1_N
7 USB_C0_TX_1_P
R2188 1/16W_0_5%_0402
R2189 1/16W_0_5%_0402
20221222
delete colay
7 USB_C0_RX_2_N
7 USB_C0_RX_2_P
R2190 1/16W_0_5%_0402
R2191 1/16W_0_5%_0402
20221222
delete colay
7 USB_C0_TX_2_N
7 USB_C0_TX_2_P
R2192 1/16W_0_5%_0402
R2193 1/16W_0_5%_0402
20221222
delete colay
USB_C0_RX_1_F_N C127 0.33U_25V_K_X5R_0201
USB_C0_RX_1_F_P C128 0.33U_25V_K_X5R_0201
USB_C0_TX_1_F_N C129 0.22U_25V_K_X5R_0201
USB_C0_TX_1_F_P C130 0.22U_25V_K_X5R_0201
USB_C0_RX_2_F_N C131 0.33U_25V_K_X5R_0201
USB_C0_RX_2_F_P C132 0.33U_25V_K_X5R_0201
USB_C0_TX_2_F_N C133 0.22U_25V_K_X5R_0201
USB_C0_TX_2_F_P C134 0.22U_25V_K_X5R_0201
[DESIGN NOTE]
ALL USB-C AC COUPLING CAPS SHOULD BE >=25V
USB_C0_RX_1_J_N
USB_C0_RX_1_J_P
USB_C0_TX_1_J_N
USB_C0_TX_1_J_P
USB_C0_RX_2_J_N
USB_C0_RX_2_J_P
USB_C0_TX_2_J_N
USB_C0_TX_2_J_P
R523 R524 R525 R526 R188 R189 R190 R191
[DESIGN NOTE]
TX BLEED RESISTOR PLACEHOLDER
D39 SP3420-04UTG_1_UDFN-10 EMC@
D40 SP3420-04UTG_1_UDFN-10 EMC@
Document Number
LCFC
Size C
Title USB C0: DATA
Rev 0.3
Date: Thursday, January 05, 2023
Sheet 31 of 44


For Acoustic Noise,22u*10 -> 10u*20
[20220802]
PPVAR_SYS
PPVAR_USB_C0_VBUS
PPVAR_USB_C0_Q_VBUS
PPVAR_USB_C0_VIN
PPVAR_BAT
L4205
1.0UH_HMLQ25201B-1R0MSR_4.0A_20%
AP4024EYT_PMPAK3X3-8
Q10
L15
2.2UH_CMMB103T-2R2MS_13.2A_20%
CHARGER_VX1
CHARGER_VX2
Q12
PK626HY 2N PDFN-8
Q13
PK626HY 2N PDFN-8
Q14
AP4024EYT_PMPAK3X3-8
Q11
RUM002N05MGT2L_VMT3-3
Q15
DMG1012T-7_SOT523-3
Q16
2N7002K_SOT23-3
U20
RAA489000ARGNP-HA0_TQFN40_5X5
CHARGER_CSIN
CHARGER_CSIP
CHARGER_ASGATE
CHARGER_ASRC
CHARGER_VBUS
CHARGER_COMPF
CHARGER_COMPR
CHARGER_CMIN
PP5000_CHARGER_INT_R
PP5000_CHARGER_INT
PP2500_CHARGER_INT
CHARGER_PSYS
PP5000_USB_C0_VCONN
CHARGER_CSOP
CHARGER_CSON
CHARGER_BGATE
CHARGER_BATGONE
CHARGER_ALERT_B
USB_C0_CHARGER_INT_ODL
EC_I2C_USB_C0_SDA
EC_I2C_USB_C0_SCL
PROCHOT#
PROCHOT_ODL
PSYS
ACOK_OD
EC_I2C_BATTERY_SCL
EC_I2C_BATTERY_SDA
BATT_PRES_ODL
EC_BATT_PRES_ODL
GSC_BATT_PRES_ODL
BAT_DISABLE_ODL
BAT_DISABLE_Q_ODL
USB_C0_CC1
USB_C0_CC2
JBAT1
ACES_60757-00802-001_8P-T
60757-00802-001
D77
D78
PESD5V0X1BCAL_SOD882-2(DNS)
RF
39p X 7
18p X 5
[DESIGN NOTE]
VTH<1V, VDS>20V
20221006
change LSI1012N3TSG to RUM002N05MGT2L
SOT883 hard to repair
[DESIGN NOTE]
RAA489000: INTERNAL CC PROTECTION UP TO 28V
20221107
0 ohm change to short pad
[DESIGN NOTE]
PROG SETTINGS
232 OHMS - 2S
1400 OHMS - 3S
IF FILTER CAP IS USED, RC < 40US
[DESIGN NOTE]
IACLIM = (RL*5UA)/(18*RS)
IACLIM = 3.7A
[CAD NOTE]
PLACE CLOSE TO BATTERY CONNECTOR
[DESIGN NOTE]
BATTERY DISABLE STUFFING OPTION
FLOATING: STUFF QBF AND DNS RBF
ACTIVE LOW: STUFF RBF AND DNS QBF
Document Number
LCFC
Size A2
Title
P32_:BATTERY CHARGER
Rev 0.3
Date: Thursday, January 05, 2023
Sheet 32 of 44

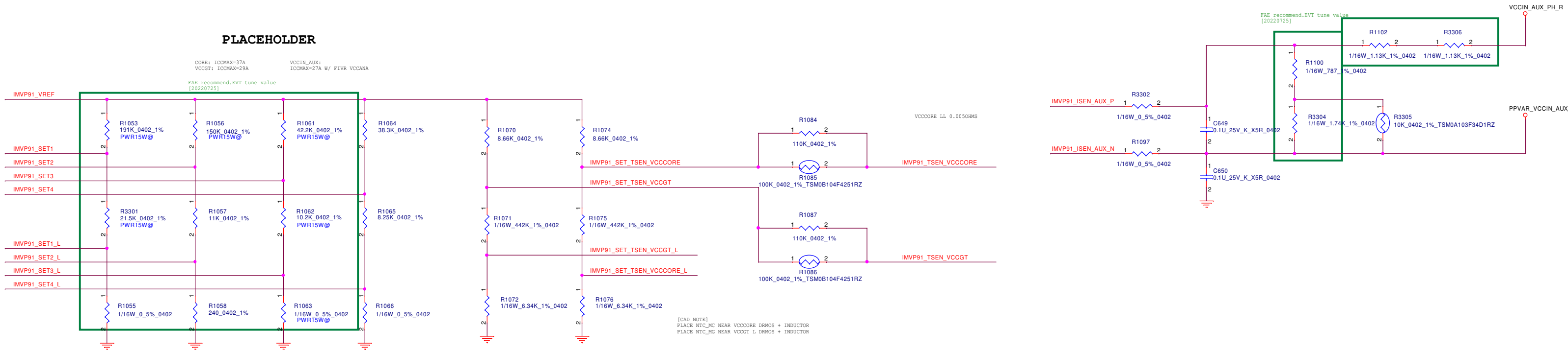


For Vboot = 0V
EVT tune value

Note		6W	15W
Core_IMON	R1059	270	470
	R1067	4.3K	3.16k
	R1077	6.2K	3.24K
SET1	R1053	80.6k	191k
	R3301	25.5k	21.5k
SET3	R1061	47.5k	42.2k
	R1062	11.5k	10.2k
	R1063	150	0
Core_comp	R1088	30K	24K
	R1094	160	402
Disable core phase2	R5000	10k	Dummy
	R5001	0	Dummy
SET2	R1056	196k	150k

For Vboot = 1.05V

	6W	15W
R1053	39.2k	54.9k
R3301	37.4k	29.4k
R1055	560	422
R1056	34.8k	33.2k
R1057	15k	15.4k



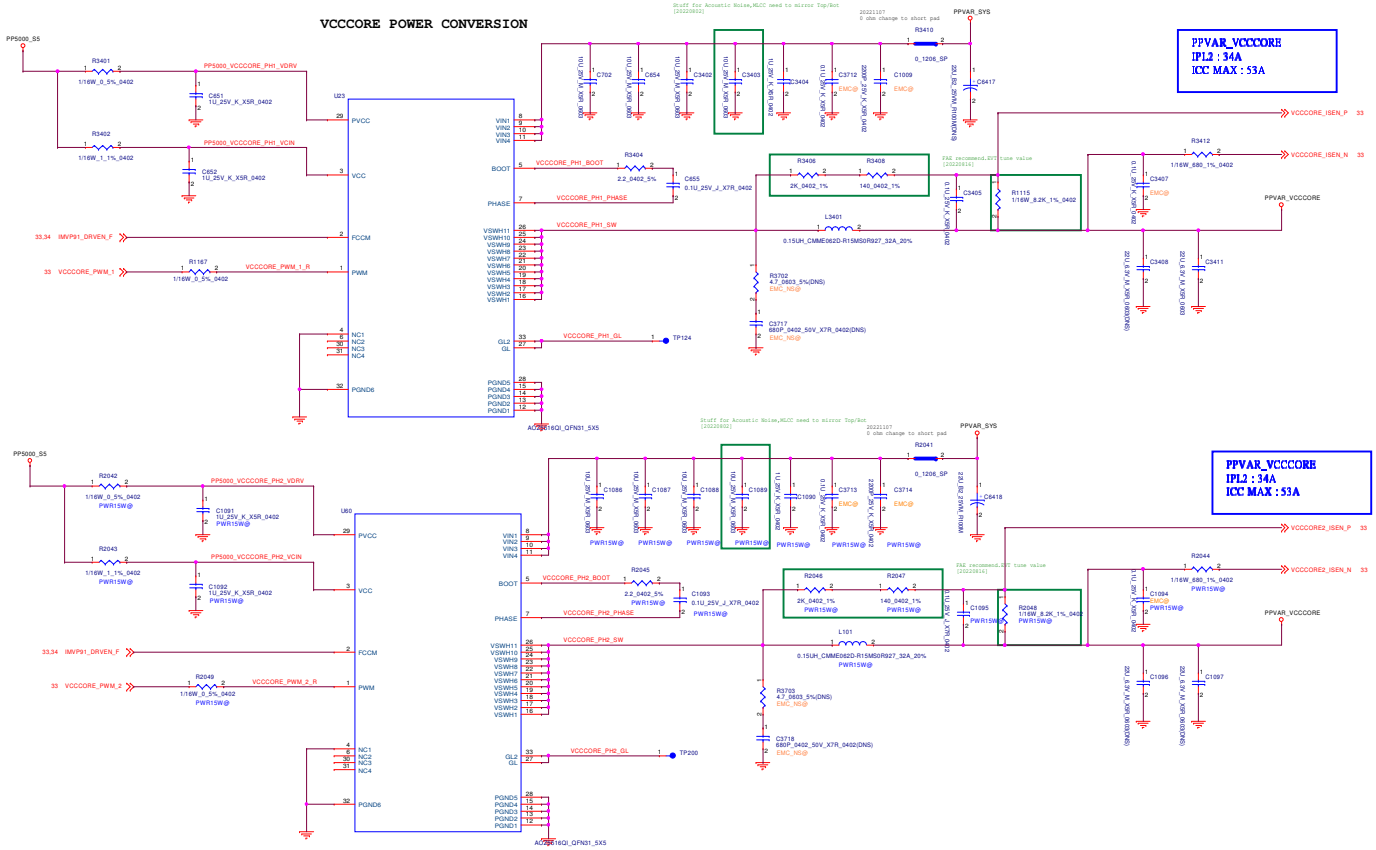
Document Number

LCFC

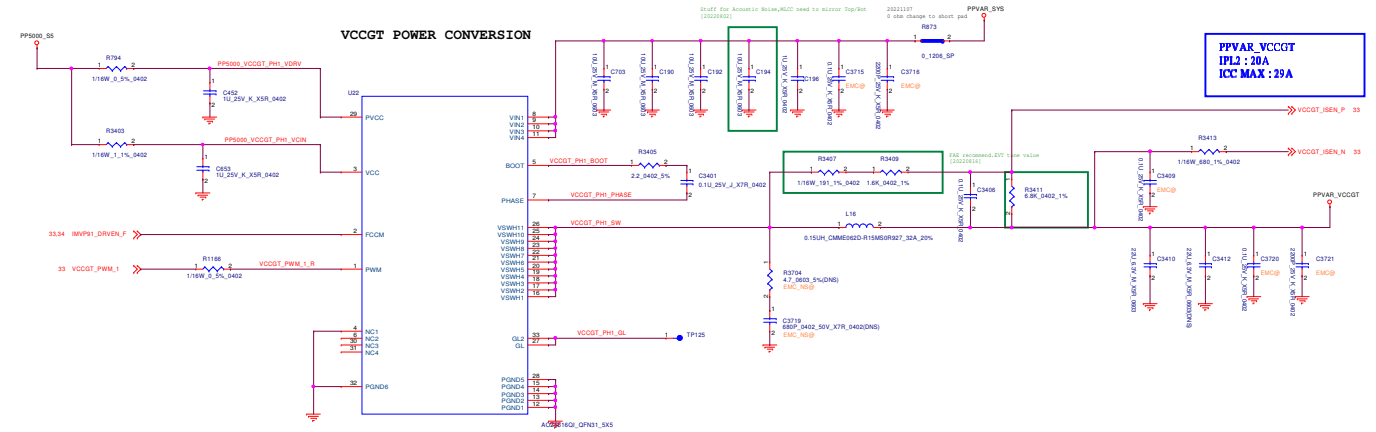
Size D | Title: **P33_Power SOC RAILS 1 (IMVP9.1)** | Rev 0.3

Date: Thursday, January 05, 2023 Sheet 33 of 44

VCCCORE POWER CONVERSION



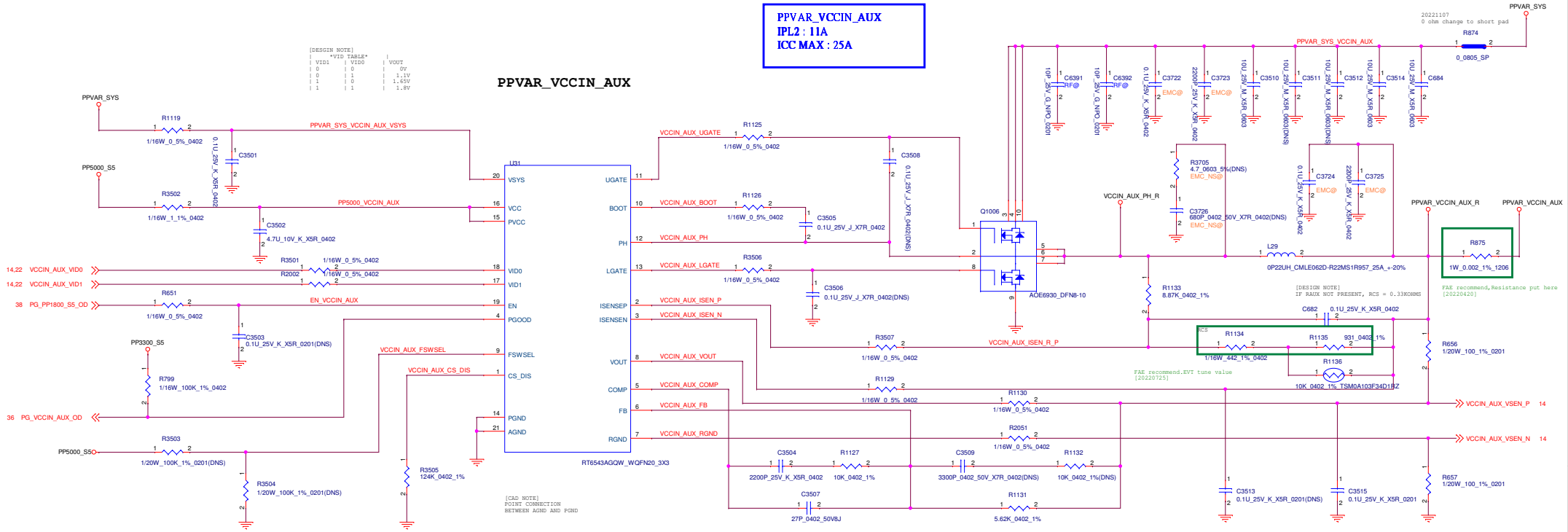
VCCGT POWER CONVERSION



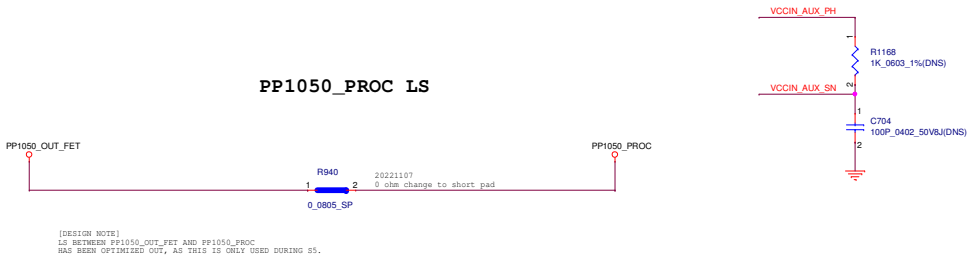
Document Number		LCFC	
Size: D	Title: P34_Power SOC RAILS 2		Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 34 of 44		

PPVAR_VCCIN_AUX
IPL2 : 11A
ICC MAX : 25A

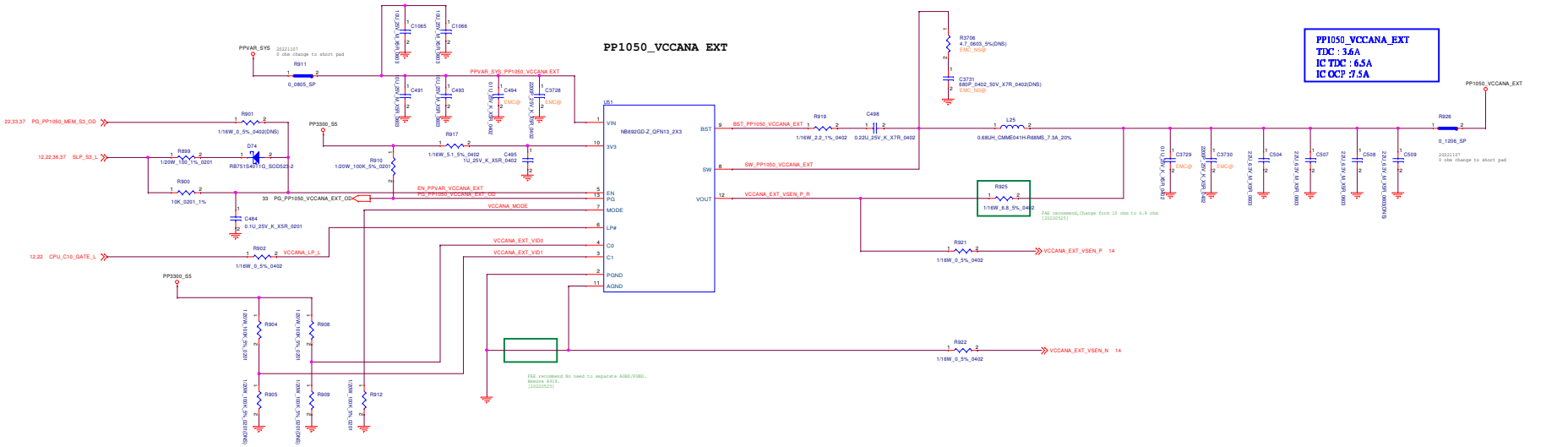
PPVAR_VCCIN_AUX



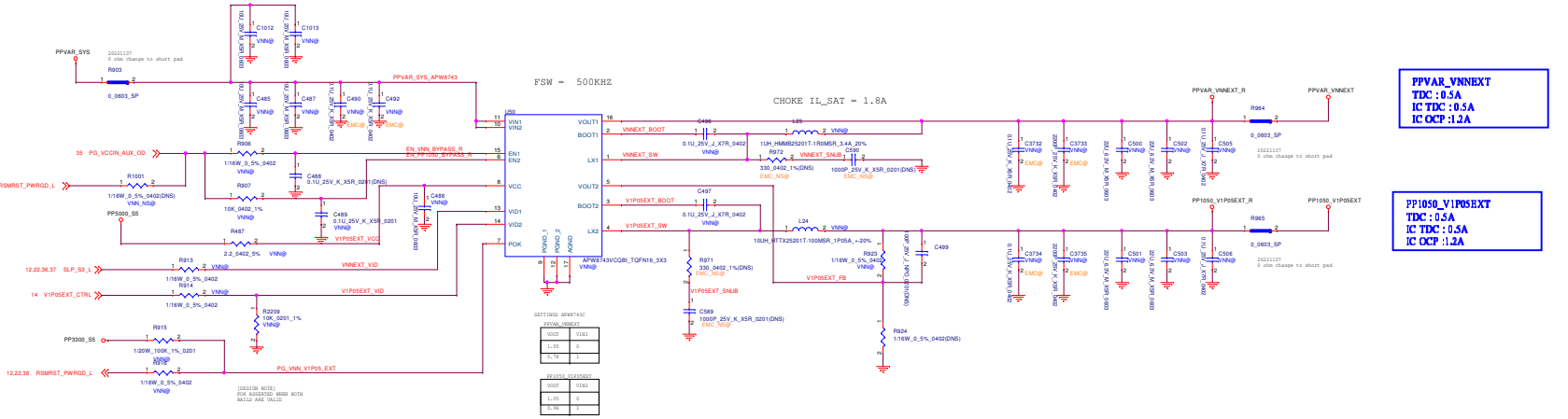
PP1050_PROC LS



Document Number			LCFC
Size: Custom	Title: P35_Power SOC RAILS 3		Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 35 of 44		



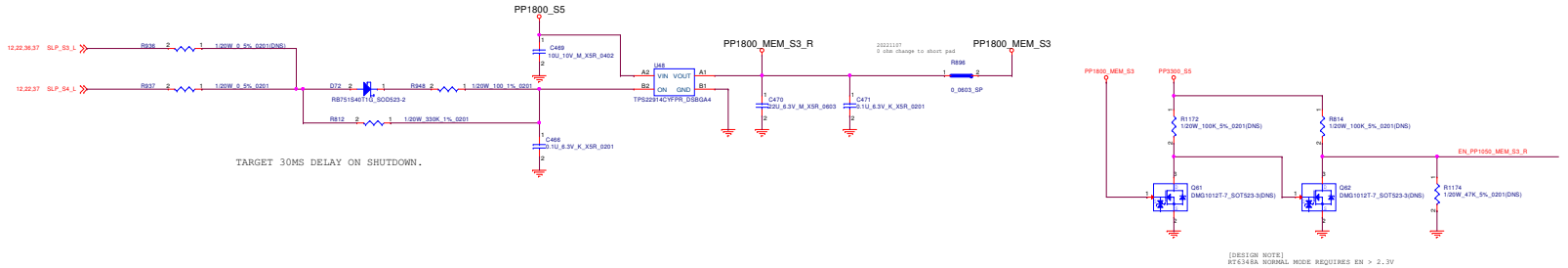
PPVAR_VNNEXT & PP1050_VP105EXT BYPASS RAILS

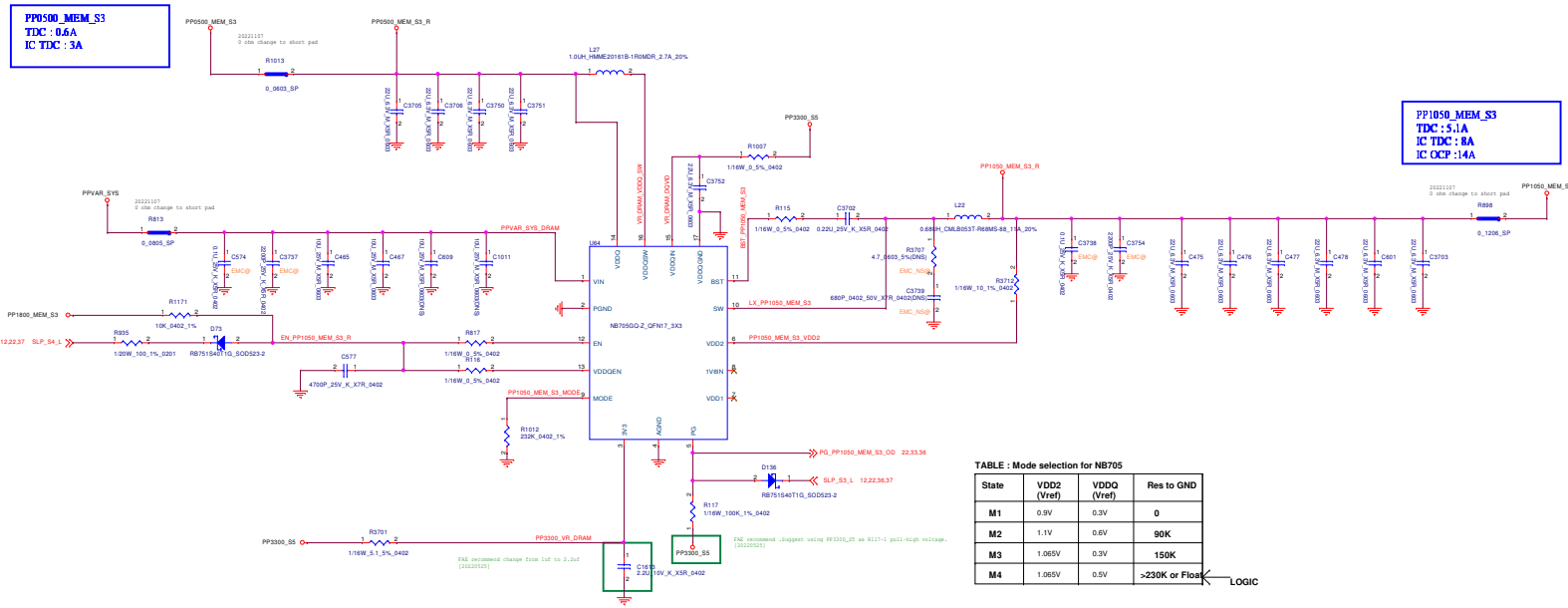


OCP AT ~5A

Document Number			
Size: D	Title: P36_Power SOC RAILS 4		Rev: 0.3
Date: Monday, January 09, 2023	Sheet 36 of 44		

HW/EE Portion





Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/06	Deciphered Date	2020/08/06

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: PWR_Memory PWR

LCFC

Size: D | Document Number: P37_Power LPDDR5 RAILS | Rev: 0.3

Date: Thursday, January 09, 2020 | Sheet 37 of 44

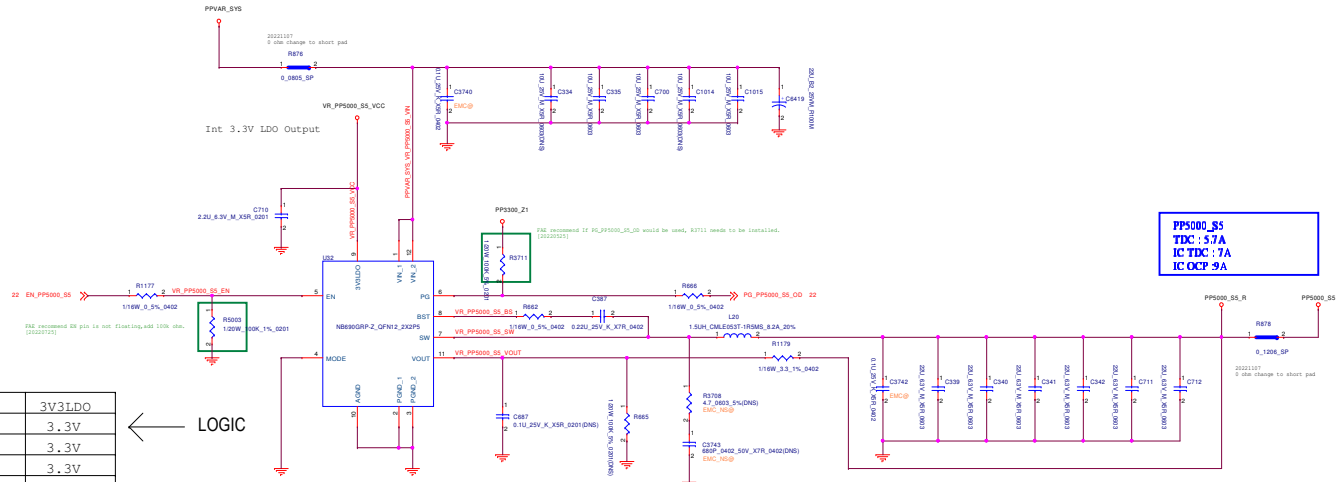
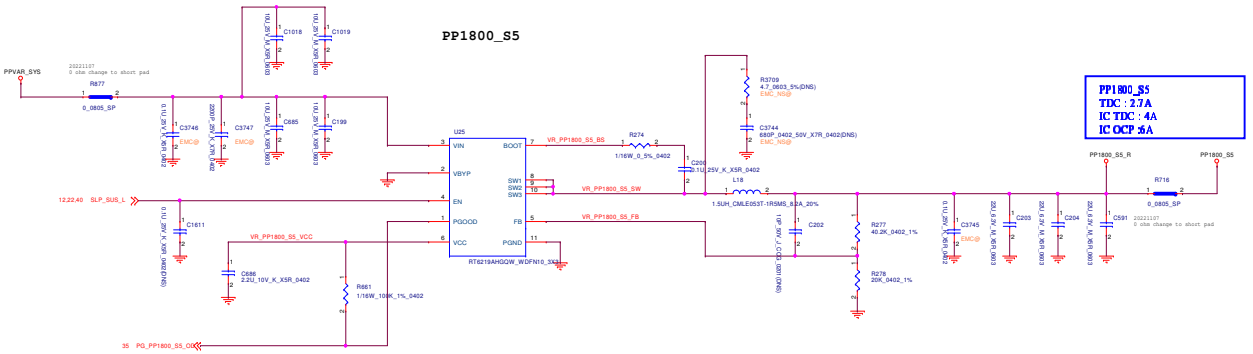


TABLE: NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

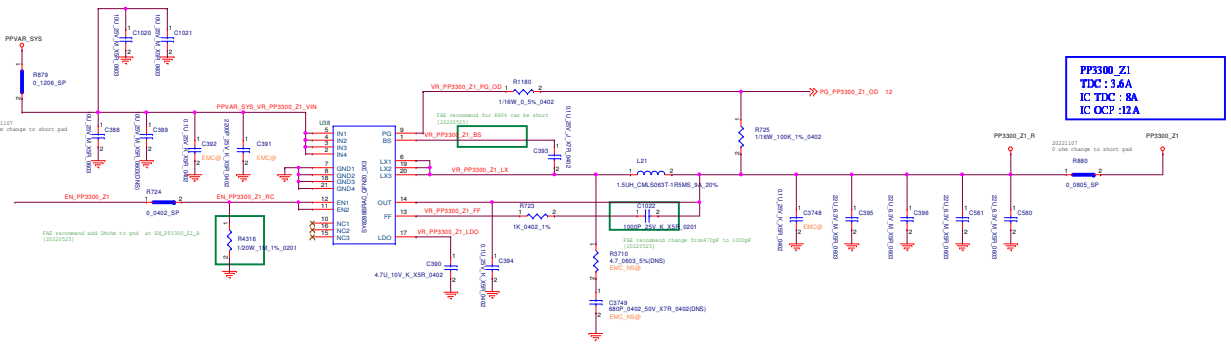
LOGIC



OCP AT ~5A

Document Number		LCFC
Size: D	Title: P38_Power SYS RAILS 1	Rev: 0.3
Date: Monday, January 16, 2023	Sheet 38 of 44	

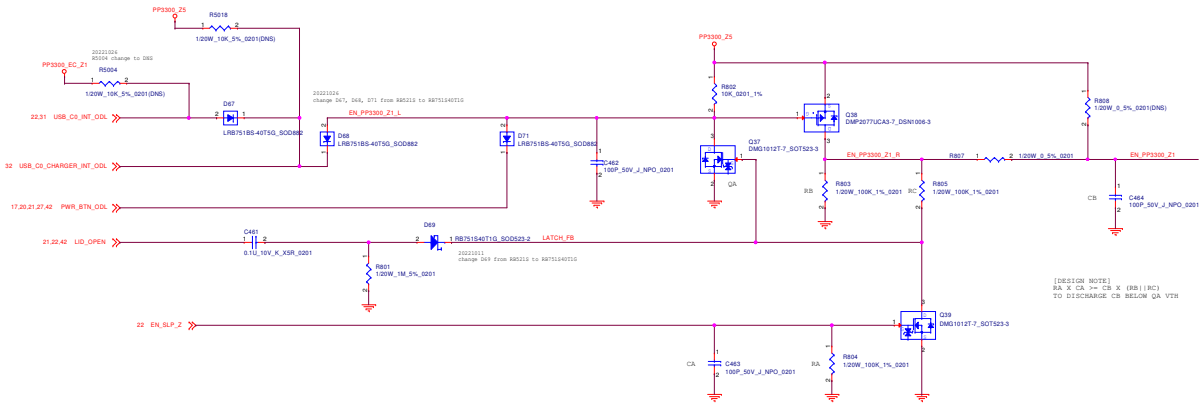
HW/PWR Portion



HW/EE Portion

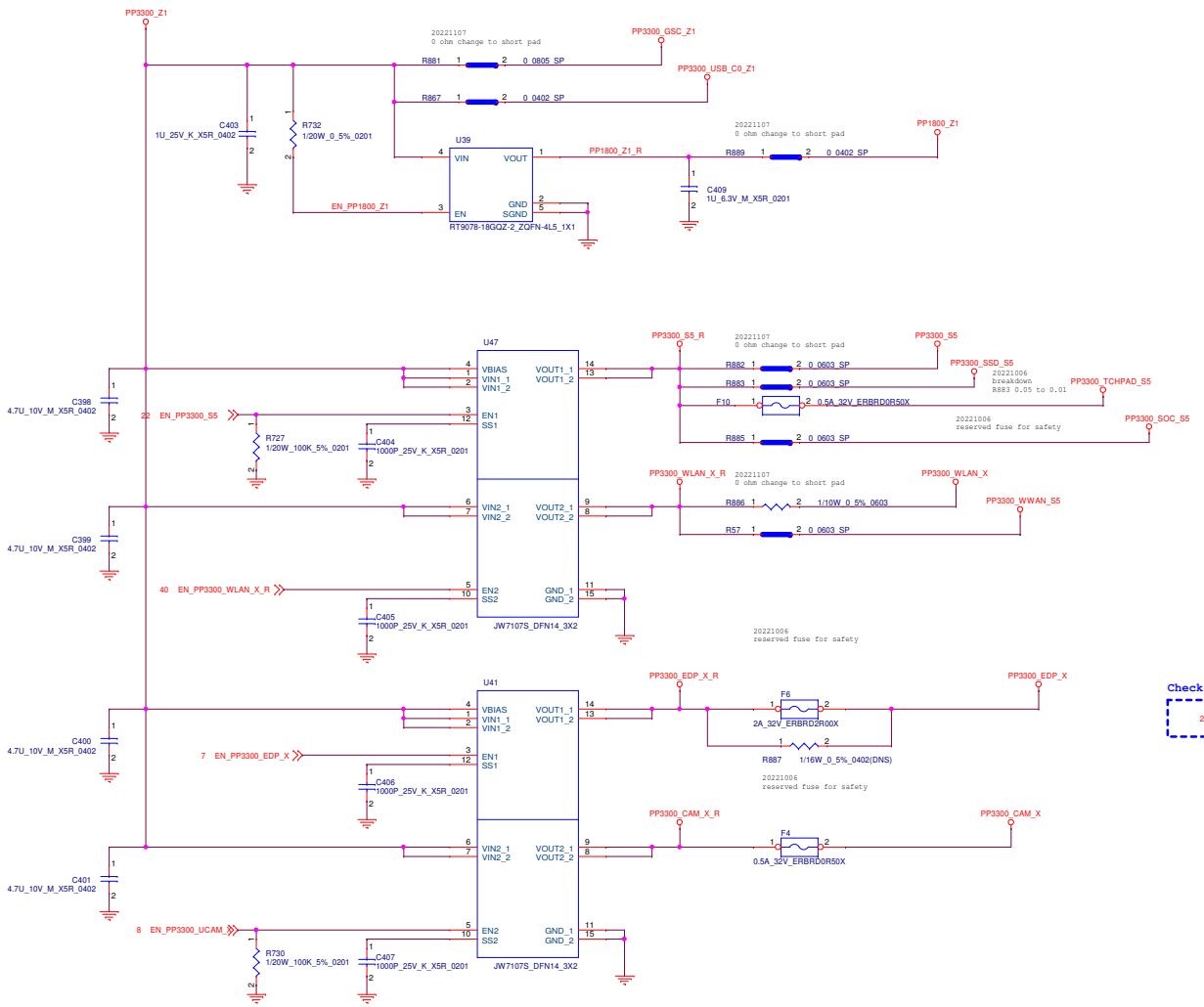
Z SLEEP STATE LOGIC

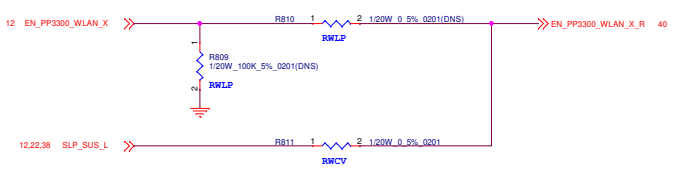
LOW POWER STATE WITH ONLY SOC RTC ENABLED.
WAKES FROM POWER BUTTON, LID, USB-C EVENTS



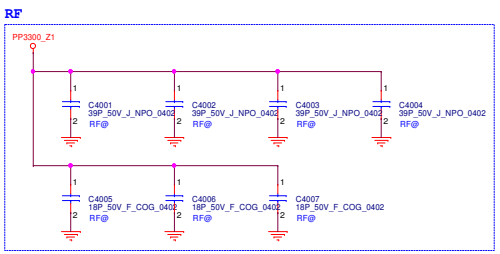
Size: D	Title: P39_Power SYS RAILS 2		Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 39 of 44		

PP3300_Z1 LS & LDOS

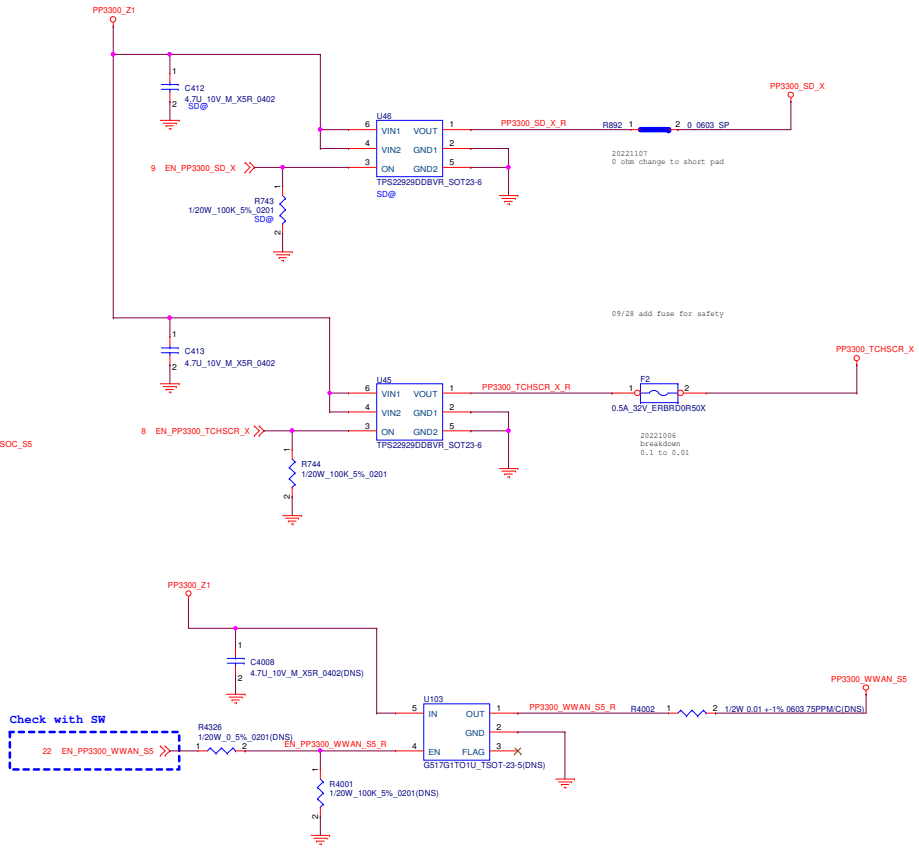




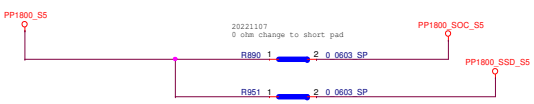
[CAD NOTE]
RWCV FOR BOTH CNVI AND PCIE WLAN MODULES



PP3300_Z1 LS & LDOS



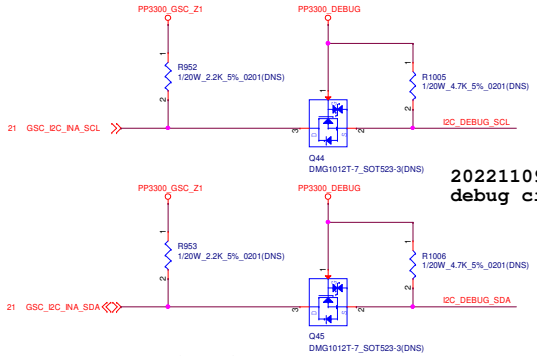
PP1800_Z1 LS & LDOS



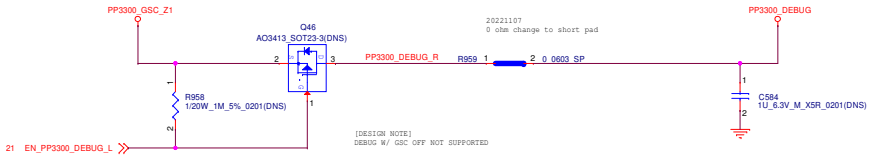
Document Number			LCFC
Size A2	Title Power SYS RAILS 3		Rev 0.3
Date: Thursday, January 05, 2023	Sheet 40 of 44		

POWER MONITORING

ODM MAY OPTIMIZE SENSE CONNECTIONS FOR LAYOUT AS REQUIRED

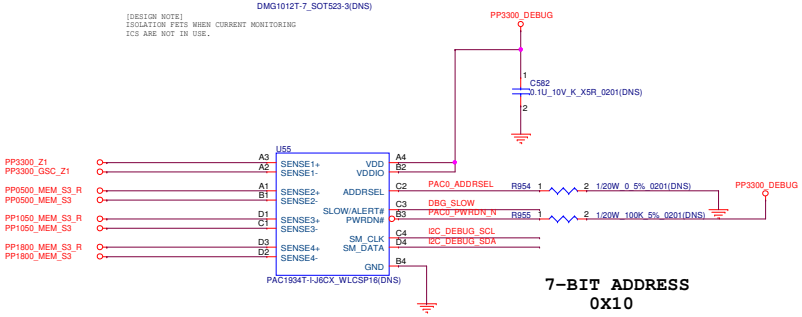


20221109
debug circuit change to DNS



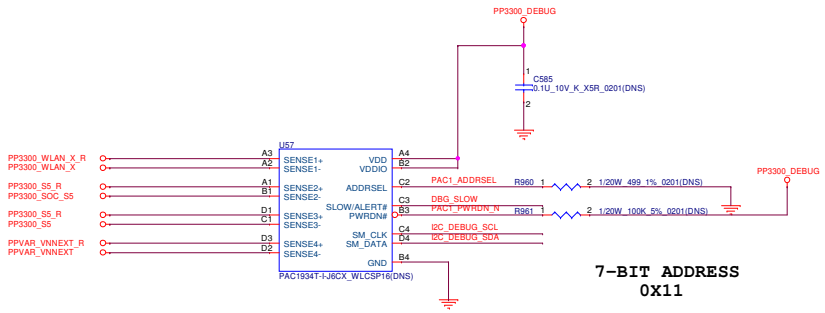
20221109
debug circuit change to DNS

[DESIGN NOTE]
ISOLATION FETS WHEN CURRENT MONITORING
ICS ARE NOT IN USE.



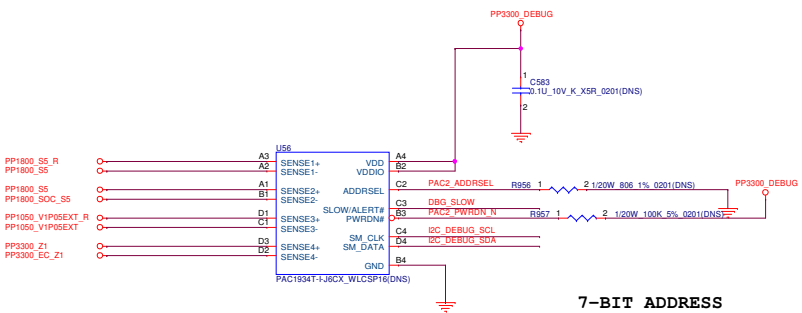
7-BIT ADDRESS
0X10

20221109
debug circuit change to DNS



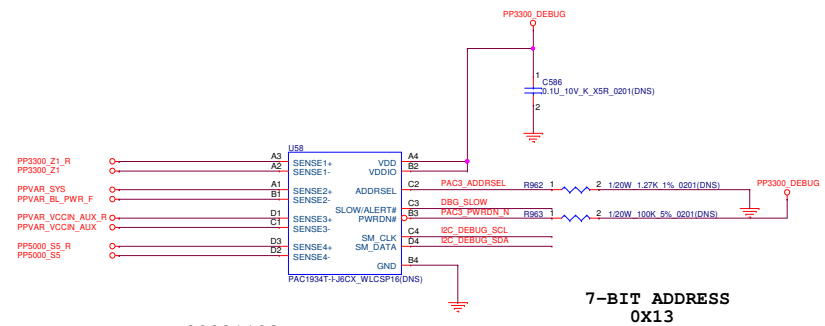
7-BIT ADDRESS
0X11

20221109
debug circuit change to DNS



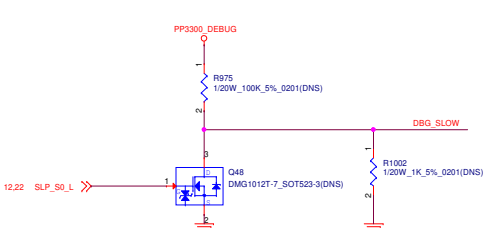
7-BIT ADDRESS
0X12

20221109
debug circuit change to DNS



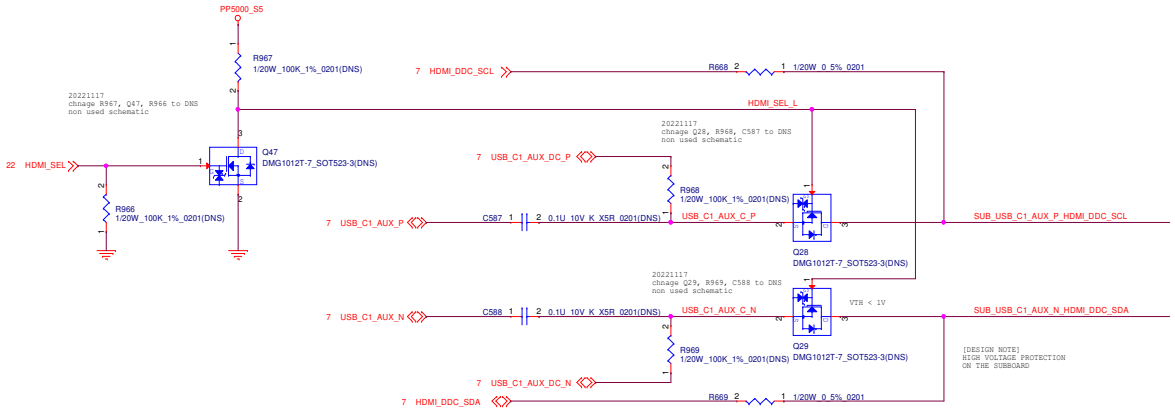
7-BIT ADDRESS
0X13

20221109
debug circuit change to DNS

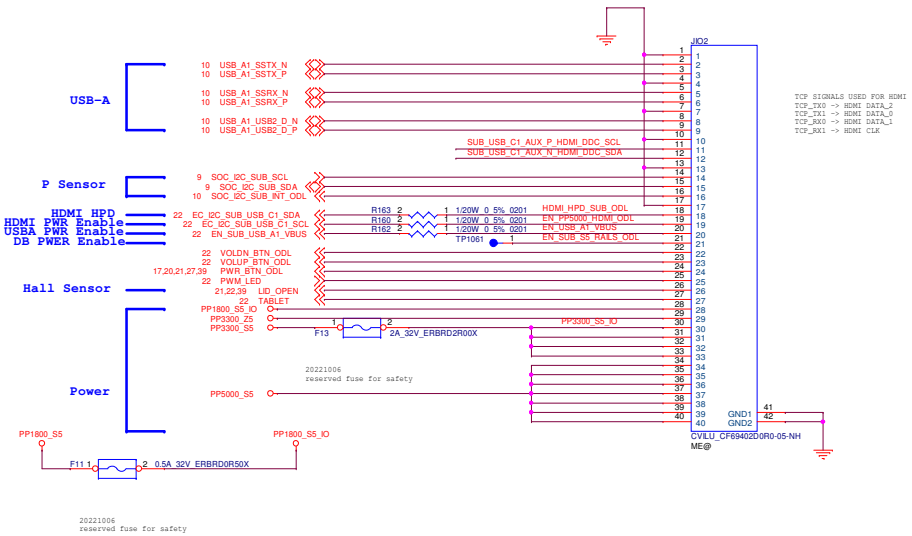


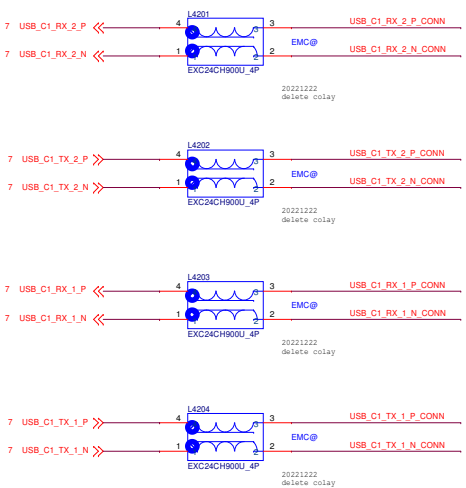
20221109
debug circuit change to DNS

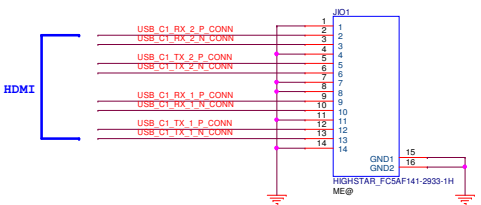
Document Number	LCFC	
Size A2	Title DEBUG: PWR MEASUREMENTS	Rev 0.3
Date: Thursday, January 05, 2023	Sheet 41 of 44	



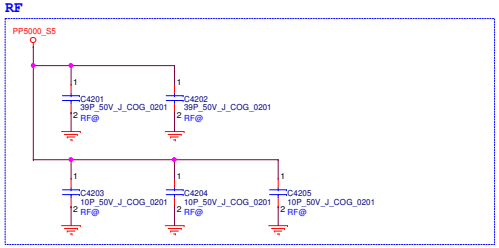
[SUB-BOARD CONNECTOR]







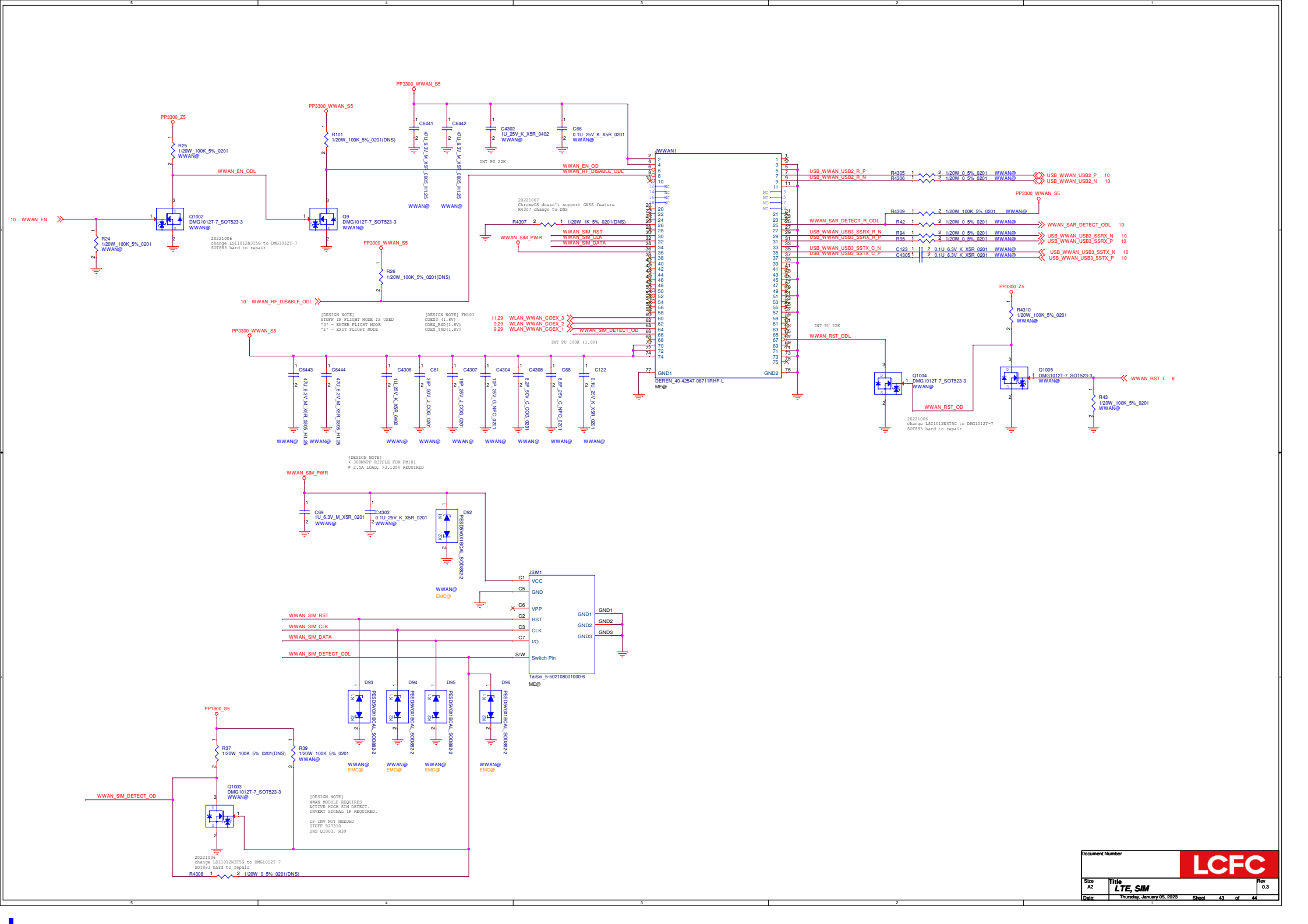
RF



TCP Port Signal Mapping for HDMI*

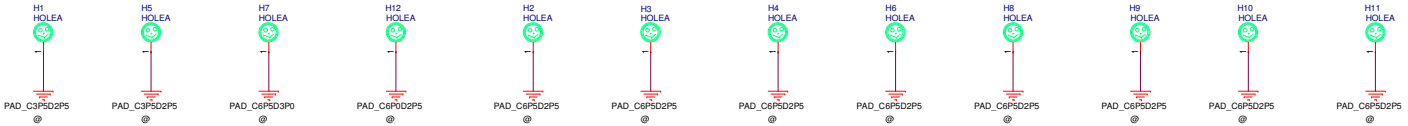
Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK
Note: Apply to TCP ports only.		

Document Number	LCFC	
Size A2	Title SUB-BOARD CONNECTORS	Rev 0.3
Date: Thursday, January 05, 2023	Sheet 42 of 44	

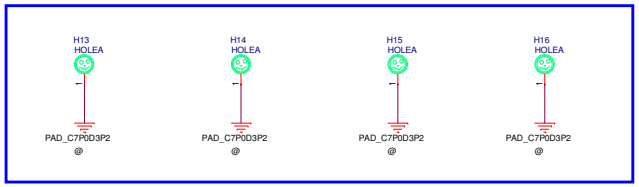

PP3300_WWAN_S5
PP3300_Z5
R25 1/20W_100K_5%_0201 WWAN@
WWAN_EN_ODL
10 WWAN_EN
Q1002 DMG1012T-7_SOT523-3 WWAN@
R24 1/20W_100K_5%_0201 WWAN@
20221006 change LSI1012N3T5G to DMG1012T-7 SOT883 hard to repair
R101 1/20W_100K_5%_0201(DNS)
Q9 DMG1012T-7_SOT523-3 WWAN@
R26 1/20W_100K_5%_0201(DNS)
10 WWAN_RF_DISABLE_ODL
C6441 47U_6.3V_M_X5R_0805_H1.25 WWAN@
C6442 47U_6.3V_M_X5R_0805_H1.25 WWAN@
C4302 1U_25V_K_X5R_0402 WWAN@
C66 0.1U_25V_K_X5R_0201 WWAN@
INT PU 22K
WWAN_EN_OD
WWAN_RF_DISABLE_ODL
20221007 ChromeOS doesn't support GNSS feature R4307 change to DNS
R4307 1/20W_1K_5%_0201(DNS)
WWAN_SIM_PWR
WWAN_SIM_RST
WWAN_SIM_CLK
WWAN_SIM_DATA
[DESIGN NOTE] STUFF IF FLIGHT MODE IS USED '0' - ENTER FLIGHT MODE '1' - EXIT FLIGHT MODE
[DESIGN NOTE] FM101 COEX3 (1.8V) COEX_RXD(1.8V) COEX_TXD(1.8V)
11,29 WLAN_WWAN_COEX_3
9,29 WLAN_WWAN_COEX_2
9,29 WLAN_WWAN_COEX_1
WWAN_SIM_DETECT_OD
INT PU 390K (1.8V)
JWWAN1
GND1
GND2
DEREN_40-42547-06711RHF-L
ME@
USB_WWAN_USB2_R_P
USB_WWAN_USB2_R_N
R4305 1/20W_0_5%_0201 WWAN@
R4306 1/20W_0_5%_0201 WWAN@
USB_WWAN_USB2_P 10
USB_WWAN_USB2_N 10
R4309 1/20W_100K_5%_0201 WWAN@
WWAN_SAR_DETECT_R_ODL
R42 1/20W_0_5%_0201 WWAN@
WWAN_SAR_DETECT_ODL 10
USB_WWAN_USB3_SSRX_R_N
USB_WWAN_USB3_SSRX_R_P
R94 1/20W_0_5%_0201 WWAN@
R95 1/20W_0_5%_0201 WWAN@
USB_WWAN_USB3_SSRX_N 10
USB_WWAN_USB3_SSRX_P 10
USB_WWAN_USB3_SSTX_C_N
USB_WWAN_USB3_SSTX_C_P
C123 0.1U_6.3V_K_X5R_0201 WWAN@
C4305 0.1U_6.3V_K_X5R_0201 WWAN@
USB_WWAN_USB3_SSTX_N 10
USB_WWAN_USB3_SSTX_P 10
WWAN_RST_ODL
Q1004 DMG1012T-7_SOT523-3 WWAN@
WWAN_RST_OD
20221006 change LSI1012N3T5G to DMG1012T-7 SOT883 hard to repair
R4310 1/20W_100K_5%_0201 WWAN@
Q1005 DMG1012T-7_SOT523-3 WWAN@
R43 1/20W_100K_5%_0201 WWAN@
WWAN_RST_L 8
C6443 47U_6.3V_M_X5R_0805_H1.25 WWAN@
C6444 47U_6.3V_M_X5R_0805_H1.25 WWAN@
C4306 1U_25V_K_X5R_0402 WWAN@
C61 39P_50V_J_COG_0201 WWAN@
C4307 18P_25V_J_COG_0201 WWAN@
C4304 10P_25V_G_NPO_0201 WWAN@
C4308 8.2P_50V_C_COG_0201 WWAN@
C68 6.8P_25V_C_NPO_0201 WWAN@
C122 0.1U_25V_K_X5R_0201 WWAN@
[DESIGN NOTE] < 300MVPP RIPPLE FOR FM101 @ 2.5A LOAD, >3.135V REQUIRED
C69 1U_6.3V_M_X5R_0201 WWAN@
C4303 0.1U_25V_K_X5R_0201 WWAN@
D92 PESD5V0X1BCAL_SOD882-2 WWAN@ EMC@
JSIM1
C1 VCC
C5 GND
C6 VPP
C2 RST
C3 CLK
C7 I/O
S/W Switch Pin
GND1
GND2
GND3
TaiSol_5-502108001000-6
ME@
D93 PESD5V0X1BCAL_SOD882-2 WWAN@ EMC@
D94 PESD5V0X1BCAL_SOD882-2 WWAN@ EMC@
D95 PESD5V0X1BCAL_SOD882-2 WWAN@ EMC@
D96 PESD5V0X1BCAL_SOD882-2 WWAN@ EMC@
PP1800_S5
R37 1/20W_100K_5%_0201(DNS)
R39 1/20W_100K_5%_0201 WWAN@
WWAN_SIM_DETECT_OD
Q1003 DMG1012T-7_SOT523-3 WWAN@
[DESIGN NOTE] WWAN MODULE REQUIRES ACTIVE HIGH SIM DETECT. INVERT SIGNAL IF REQUIRED. IF INV NOT NEEDED STUFF R27310 DNS Q1003, R39
20221006 change LSI1012N3T5G to DMG1012T-7 SOT883 hard to repair
R4308 1/20W_0_5%_0201(DNS)
Document Number
LCFC
Size A2
Title LTE, SIM
Rev 0.3
Date: Thursday, January 05, 2023
Sheet 43 of 44

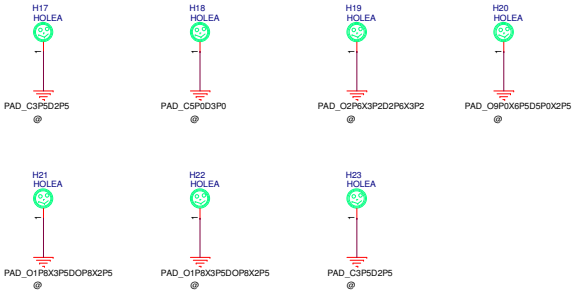
SCREW HOLES AND SHIELDS

QTHER HOLES



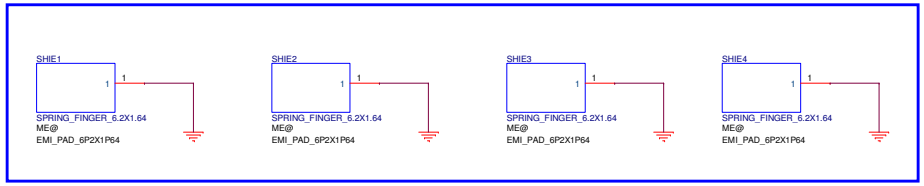
CPU SCREW HOLES





Need to change symbol to EMI_PAD_4P4X0P8

LPDDR5 SHIELDS



Document Number: 14e Gen3		LCFC
Size: Custom	Title: SCREW HOLES AND SHIELDS	Rev: 0.3
Date: Thursday, January 05, 2023	Sheet 44 of 44	