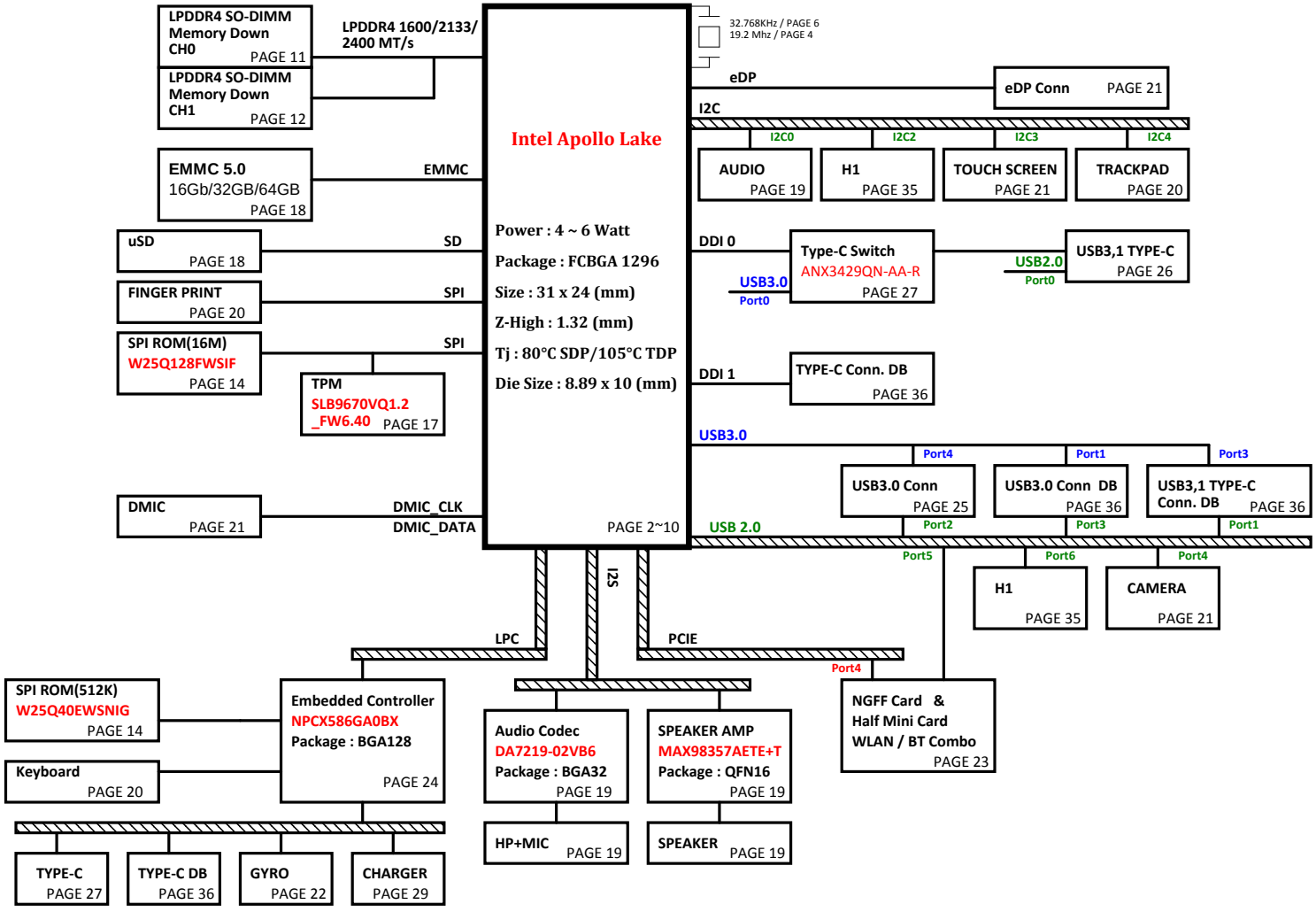
Intel Apollo Platform Block Diagram

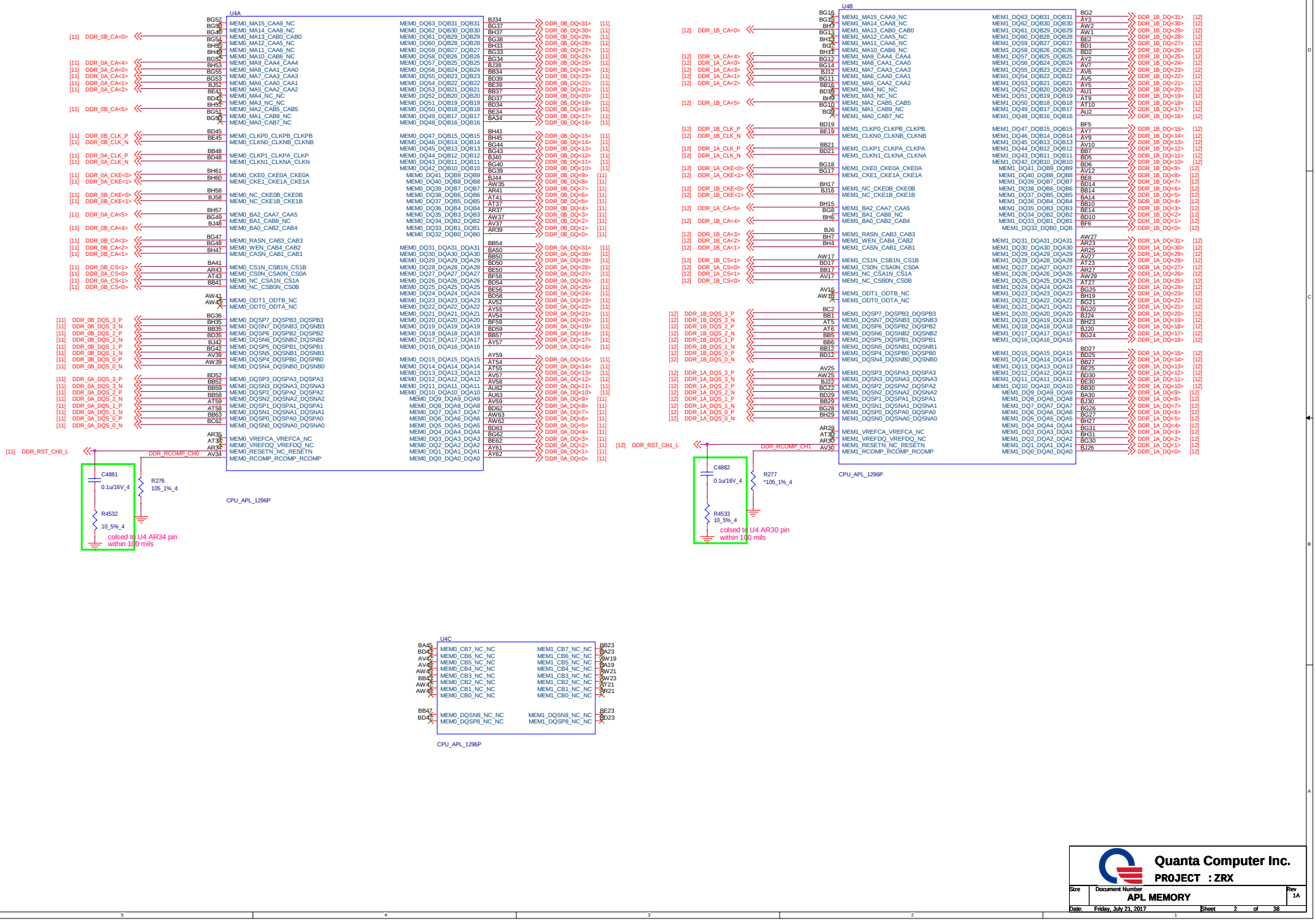
PCB 6L STACK UP

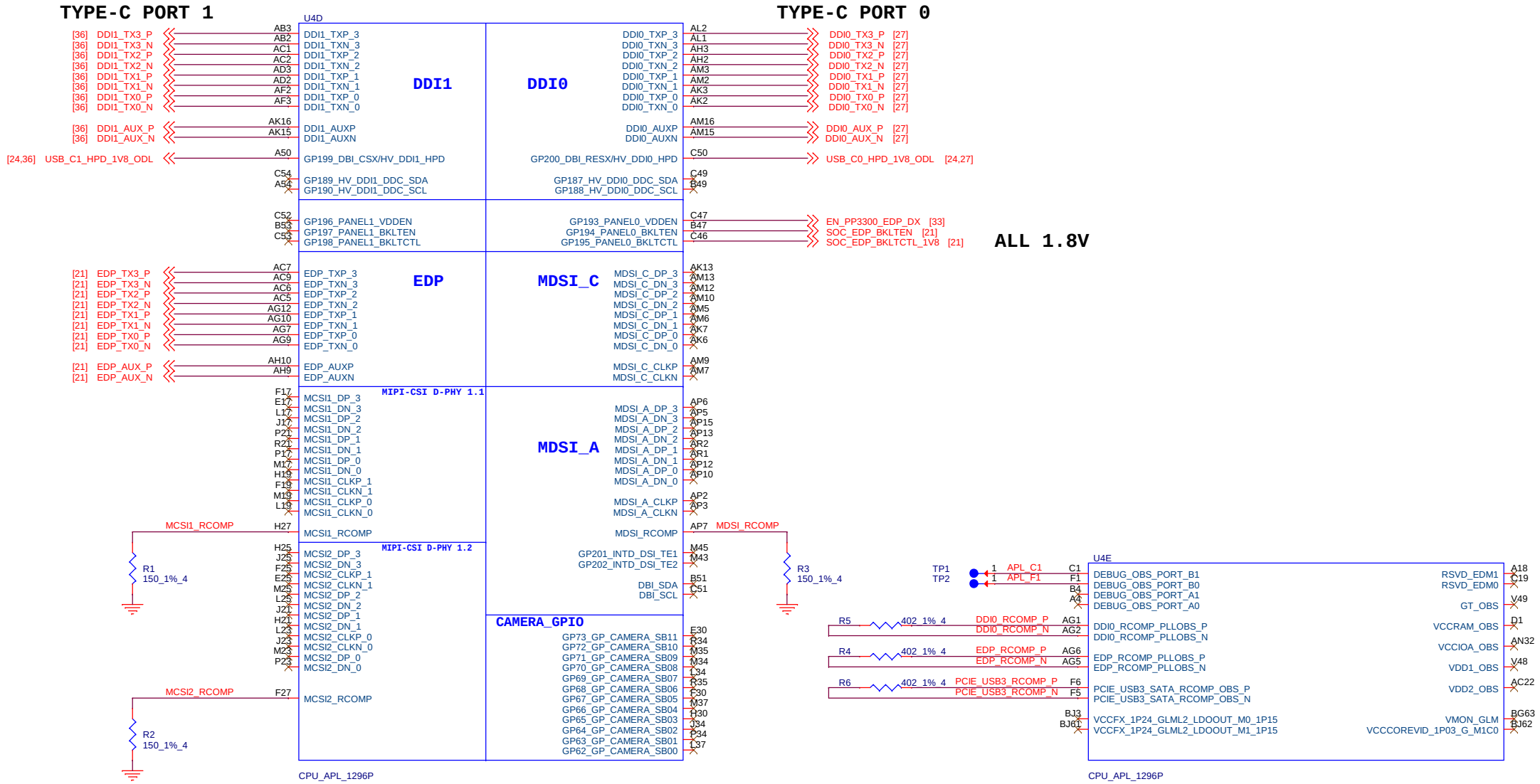
LAYER 1 : TOP
LAYER 2 : VCC
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6: BOT

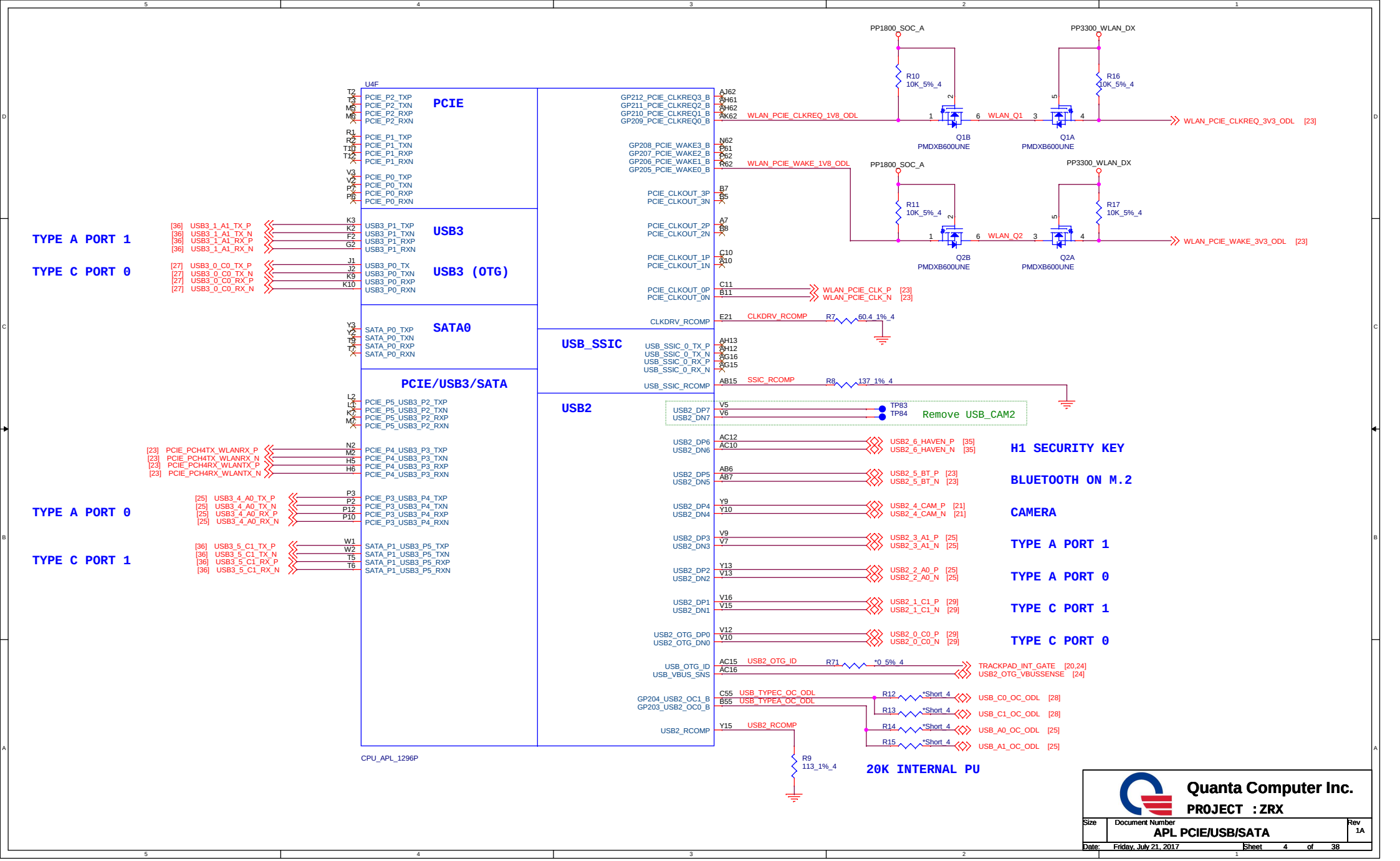


Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Friday, July 21, 2017	Sheet 1 of 38	


U4A
U4B
U4C
CPU_APL_1296P
C4881
0.1u/16V_4
R276
105_1%_4
R4532
10_5%_4
colsed to U4 AR34 pin
within 100 mils
C4882
R277
*105_1%_4
R4533
colsed to U4 AR30 pin
DDR_RCOMP_CH0
DDR_RCOMP_CH1
DDR_RST_CH0_L
DDR_RST_CH1_L
Quanta Computer Inc.
PROJECT : ZRX
APL MEMORY
Size
Document Number
Rev
1A
Date: Friday, July 21, 2017
Sheet 2 of 38

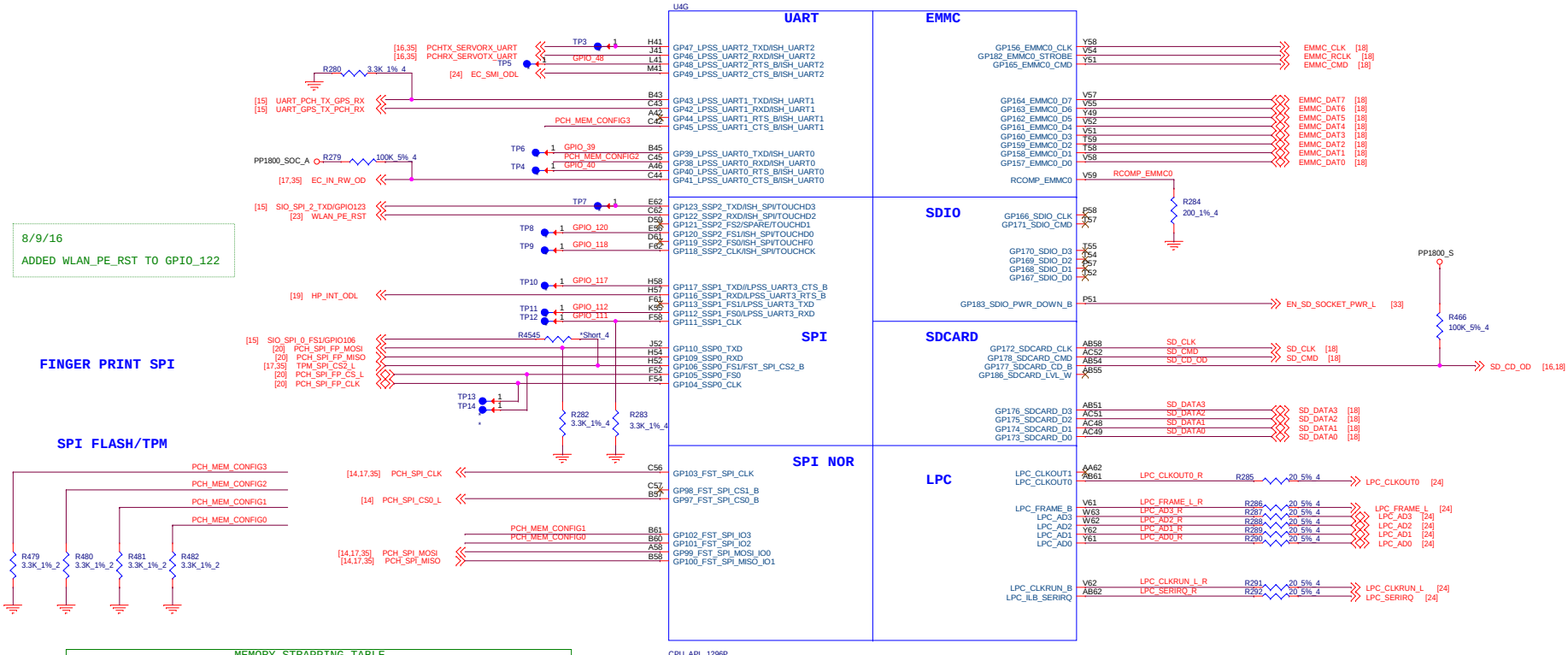

TYPE-C PORT 1
TYPE-C PORT 0
ALL 1.8V
U4D
DDI1
DDI0
EDP
MDSI_C
MDSI_A
CAMERA_GPIO
MIPI-CSI D-PHY 1.1
MIPI-CSI D-PHY 1.2
DDI1_TXP_3
DDI1_TXN_3
DDI1_TXP_2
DDI1_TXN_2
DDI1_TXP_1
DDI1_TXN_1
DDI1_TXP_0
DDI1_TXN_0
DDI1_AUXP
DDI1_AUXN
GP199_DBI_CSX/HV_DDI1_HPD
GP189_HV_DDI1_DDC_SDA
GP190_HV_DDI1_DDC_SCL
GP196_PANEL1_VDDEN
GP197_PANEL1_BKLTEN
GP198_PANEL1_BKLTCTL
DDI0_TXP_3
DDI0_TXN_3
DDI0_TXP_2
DDI0_TXN_2
DDI0_TXP_1
DDI0_TXN_1
DDI0_TXP_0
DDI0_TXN_0
DDI0_AUXP
DDI0_AUXN
GP200_DBI_RESX/HV_DDI0_HPD
GP187_HV_DDI0_DDC_SDA
GP188_HV_DDI0_DDC_SCL
GP193_PANEL0_VDDEN
GP194_PANEL0_BKLTEN
GP195_PANEL0_BKLTCTL
EDP_TXP_3
EDP_TXN_3
EDP_TXP_2
EDP_TXN_2
EDP_TXP_1
EDP_TXN_1
EDP_TXP_0
EDP_TXN_0
EDP_AUXP
EDP_AUXN
MDSI_C_DP_3
MDSI_C_DN_3
MDSI_C_DP_2
MDSI_C_DN_2
MDSI_C_DP_1
MDSI_C_DN_1
MDSI_C_DP_0
MDSI_C_DN_0
MDSI_C_CLKP
MDSI_C_CLKN
MCSI1_DP_3
MCSI1_DN_3
MCSI1_DP_2
MCSI1_DN_2
MCSI1_DP_1
MCSI1_DN_1
MCSI1_DP_0
MCSI1_DN_0
MCSI1_CLKP_1
MCSI1_CLKN_1
MCSI1_CLKP_0
MCSI1_CLKN_0
MCSI1_RCOMP
MDSI_A_DP_3
MDSI_A_DN_3
MDSI_A_DP_2
MDSI_A_DN_2
MDSI_A_DP_1
MDSI_A_DN_1
MDSI_A_DP_0
MDSI_A_DN_0
MDSI_A_CLKP
MDSI_A_CLKN
MDSI_RCOMP
GP201_INTD_DSI_TE1
GP202_INTD_DSI_TE2
DBI_SDA
DBI_SCL
MCSI2_DP_3
MCSI2_DN_3
MCSI2_CLKP_1
MCSI2_CLKN_1
MCSI2_DP_2
MCSI2_DN_2
MCSI2_DP_1
MCSI2_DN_1
MCSI2_CLKP_0
MCSI2_CLKN_0
MCSI2_DP_0
MCSI2_DN_0
MCSI2_RCOMP
GP73_GP_CAMERA_SB11
GP72_GP_CAMERA_SB10
GP71_GP_CAMERA_SB09
GP70_GP_CAMERA_SB08
GP69_GP_CAMERA_SB07
GP68_GP_CAMERA_SB06
GP67_GP_CAMERA_SB05
GP66_GP_CAMERA_SB04
GP65_GP_CAMERA_SB03
GP64_GP_CAMERA_SB02
GP63_GP_CAMERA_SB01
GP62_GP_CAMERA_SB00
CPU_APL_1296P
R1 150_1%_4
R2 150_1%_4
R3 150_1%_4
R4 402_1%_4
R5 402_1%_4
R6 402_1%_4
TP1
TP2
APL_C1
APL_F1
U4E
DEBUG_OBS_PORT_B1
DEBUG_OBS_PORT_B0
DEBUG_OBS_PORT_A1
DEBUG_OBS_PORT_A0
DDI0_RCOMP_P
DDI0_RCOMP_N
DDI0_RCOMP_PLLOBS_P
DDI0_RCOMP_PLLOBS_N
EDP_RCOMP_P
EDP_RCOMP_N
EDP_RCOMP_PLLOBS_P
EDP_RCOMP_PLLOBS_N
PCIE_USB3_RCOMP_P
PCIE_USB3_RCOMP_N
PCIE_USB3_SATA_RCOMP_OBS_P
PCIE_USB3_SATA_RCOMP_OBS_N
VCCFX_1P24_GLML2_LDOOUT_M0_1P15
VCCFX_1P24_GLML2_LDOOUT_M1_1P15
RSVD_EDM1
RSVD_EDM0
GT_OBS
VCCRAM_OBS
VCCIOA_OBS
VDD1_OBS
VDD2_OBS
VMON_GLM
VCCCOREVID_1P03_G_M1C0
CPU_APL_1296P
Quanta Computer Inc.
PROJECT : ZRX
Size
Document Number
APL eDP/RCOMP
Rev
1A
Date: Friday, July 21, 2017
Sheet 3 of 38



Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	APL PCIE/USB/SATA	1A
Date: Friday, July 21, 2017	Sheet 4 of 38	



8/9/16

ADDED WLAN_PE_RST TO GPIO_122

MEMORY STRAPPING TABLE

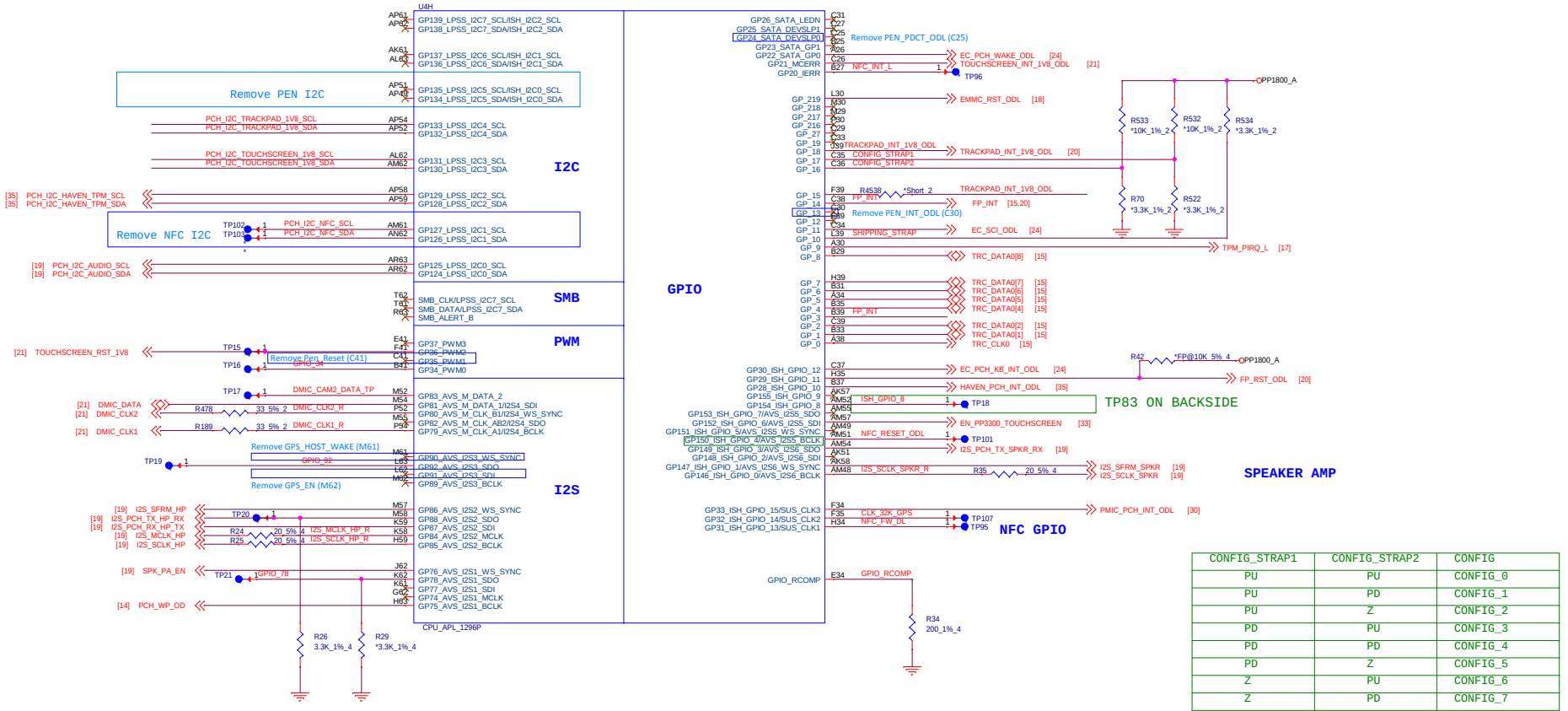
Q PN	CONFIG PIN	3	2	1	0
AKD5QZST507	SAMSUNG 8GB K4F8E304HB-MGCJ LF+HF	0	0	0	0
AKD5RZST515	SAMSUNG 4GB K4F6E304HB-MGCJ LF+HF	0	0	0	1
AKD5FWSTL04	MICRON 8GB MT53B512M32D2NP-062WT:C	0	0	1	0
AKD5JWSTL04	MICRON 4GB MT53B256M32D1NP-062 WT:C	0	0	1	1
AKD5RG0TW09	HYNIX 8GB H9HCNNNBPUMLHR-NME	0	1	0	0
AKD5RG0TW08	HYNIX 4GB H9HCNNN8KUMLHR-NME	0	1	0	1
		1	1	1	1

HARDWARE STRAPS (* = SYSTEM STRAP SELECTION)

GPIO_39: INTERNAL 20K PD *DISABLE CSE ROM BYPASS: 0 ENABLE CSE ROM BYPASS: 1	GPIO_47: INTERNAL 20K PD *DON'T FORCE DNX FW LOAD: 0 FORCE DNX FW LOAD: 1	GPIO_106: INTERNAL 20K PU *MUST BE HIGH WHEN RSM_RST_N DEASSERTS	GPIO_117: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_120: INTERNAL 20K PD *TOP SWAP OVERRIDE DISABLE: 0 TOP SWAP OVERRIDE ENABLE: 1
GPIO_40: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_48: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_111: INTERNAL 20K PU DO NOT BOOT FROM SPI: 1 *BOOT FROM SPI: 0	GPIO_123: INTERNAL 20K PU MUST BE HIGH WHEN RSM_RST_N DEASSERTS	GPIO_121: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS
GPIO_43: INTERNAL 20K PU ENABLE BOOT FROM EMMC: 1 *DISABLE BOOT FROM EMMC: 0	GPIO_104: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_118: INTERNAL 20K PD *NO FLASH DESCRIPTOR OVERRIDE: 0 OVERRIDE FLASH DESCRIPTOR: 1	GPIO_112: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	
GPIO_44: INTERNAL 20K PU *ENABLE BOOT FROM SPI: 1 DISABLE BOOT FROM SPI: 0	GPIO_105: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	GPIO_110: INTERNAL 20K PU LPC BUFFERS AT 1.8V: 1 *LPC BUFFERS AT 3.3V: 0	GPIO_113: INTERNAL 20K PD *MUST BE LOW WHEN RSM_RST_N DEASSERTS	

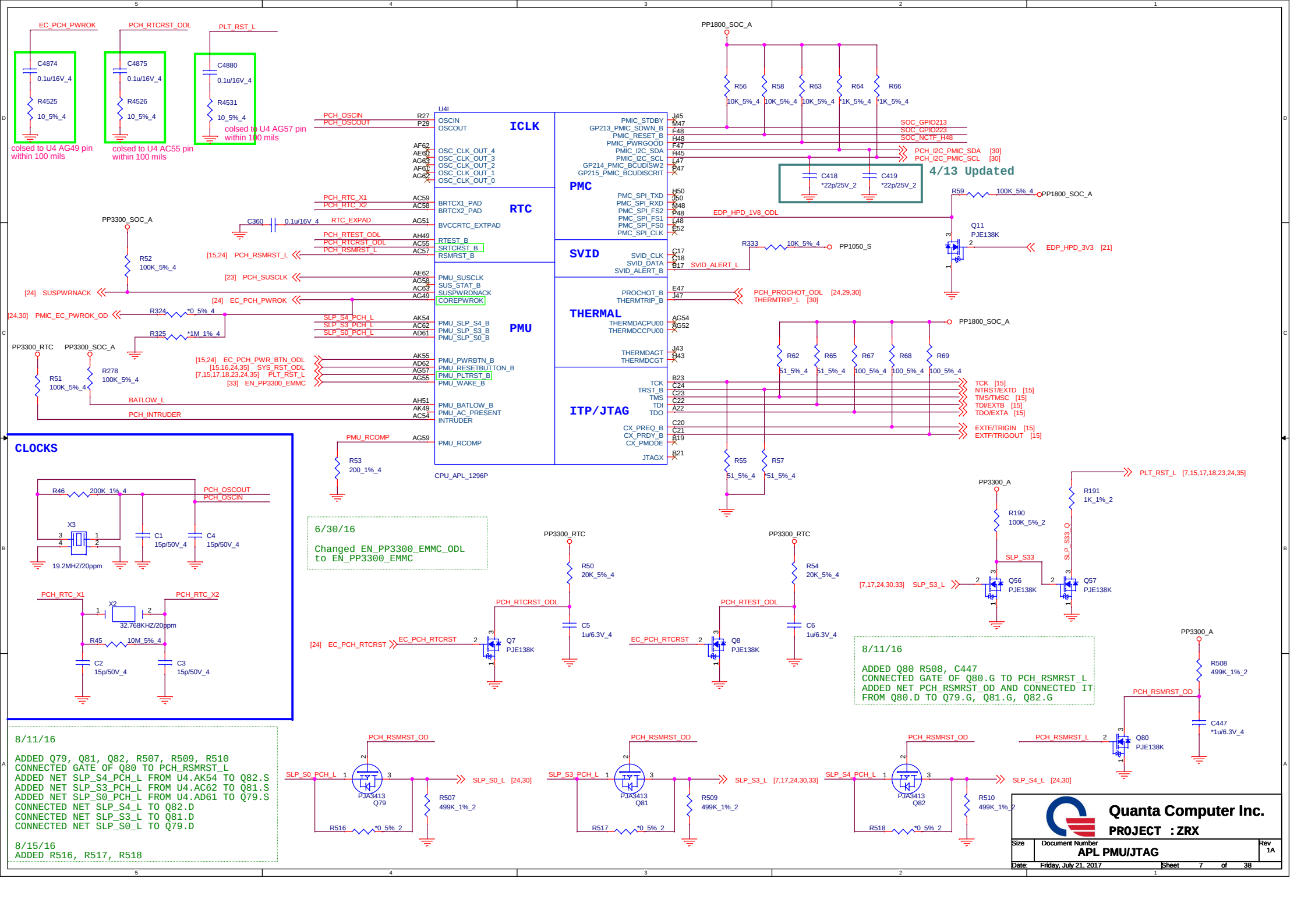
Quanta Computer Inc.
PROJECT : ZRX

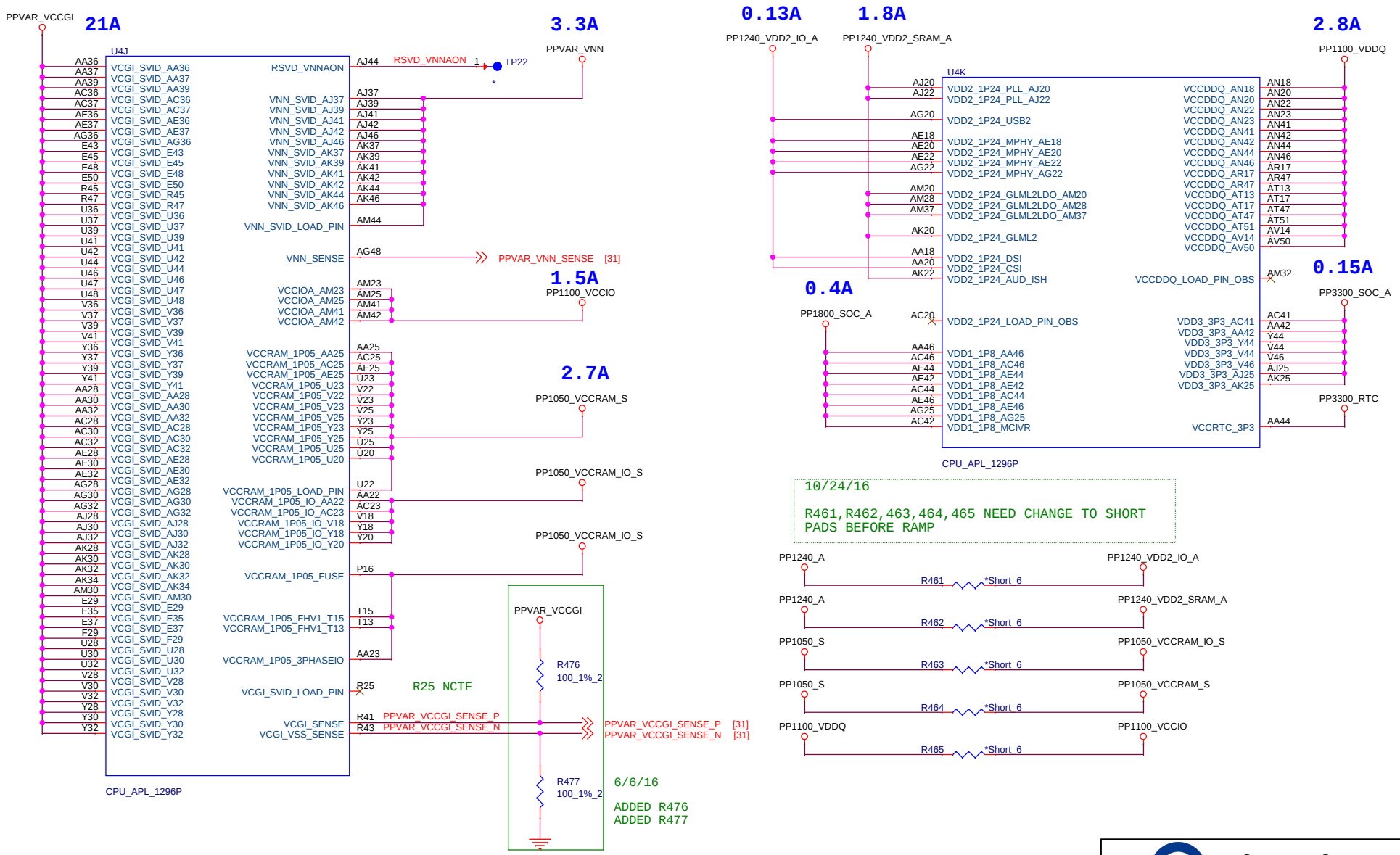
Size	Document Number	Rev
	APL UART/SPI/EMMC/SD/LPC	1A
Date: Friday, July 21, 2017	Sheet 5 of 38	

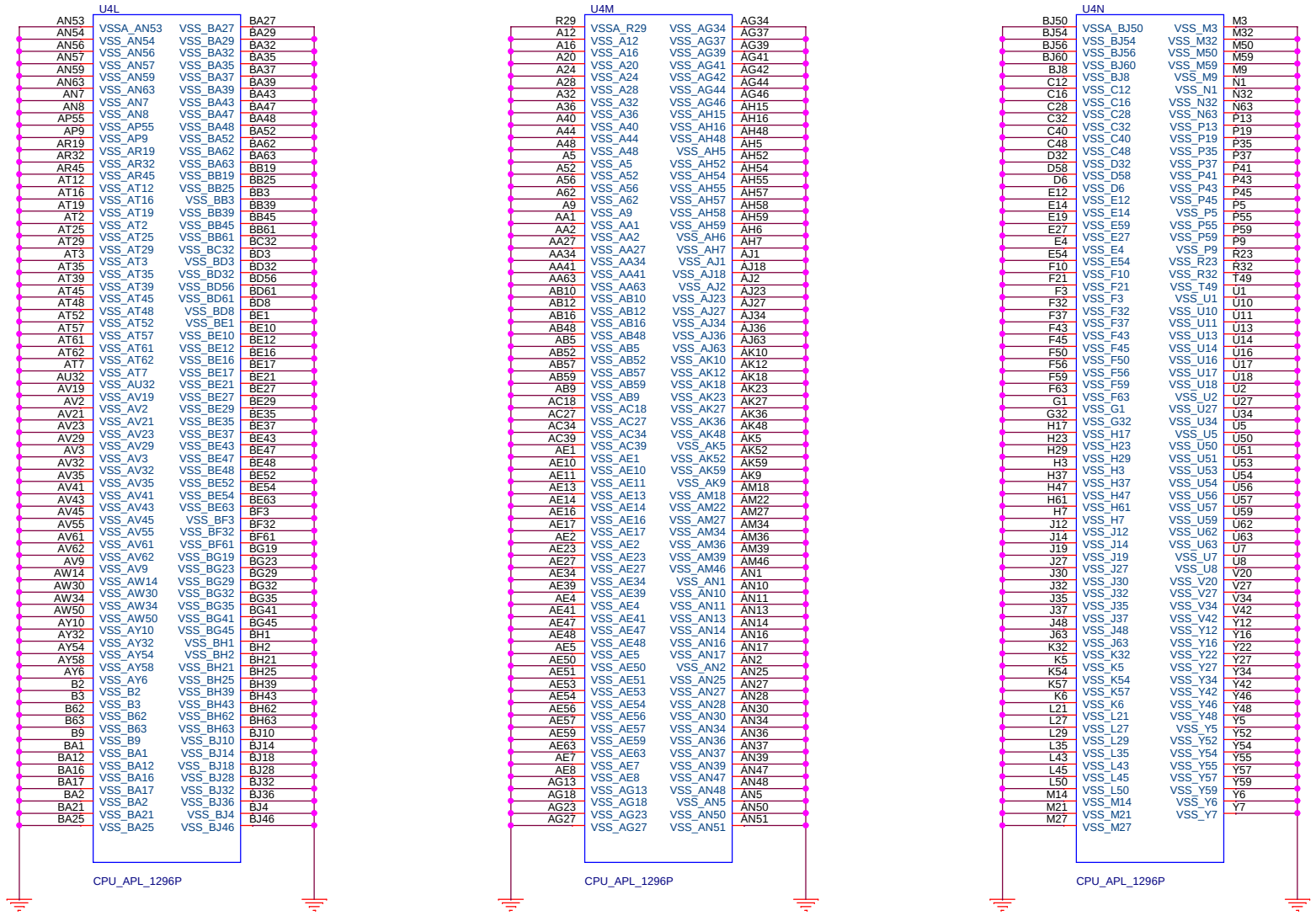


CONFIG_STRAP1	CONFIG_STRAP2	CONFIG
PU	PU	CONFIG_0
PU	PD	CONFIG_1
PU	Z	CONFIG_2
PD	PU	CONFIG_3
PD	PD	CONFIG_4
PD	Z	CONFIG_5
Z	PU	CONFIG_6
Z	PD	CONFIG_7
*Z	*Z	CONFIG_8

Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: APL I2C/I2S/GPIO	Rev: 1A
Date: Friday, July 21, 2017	Sheet 6 of 38	


EC_PCH_PWROK
PCH_RTCRST_ODL
PLT_RST_L
C4874
C4875
C4880
0.1u/16V_4
R4525
R4526
R4531
10_5%_4
colsed to U4 AG49 pin within 100 mils
colsed to U4 AC55 pin within 100 mils
colsed to U4 AG57 pin within 100 mils
U4I
ICLK
RTC
SVID
PMU
THERMAL
ITP/JTAG
PMC
CPU_APL_1296P
PP1800_SOC_A
PP3300_SOC_A
PP3300_RTC
PP1050_S
R56
R58
R63
R64
R66
10K_5%_4
*1K_5%_4
SOC_GPIO213
SOC_GPIO223
SOC_NCTF_H48
PCH_I2C_PMIC_SDA [30]
PCH_I2C_PMIC_SCL [30]
C418
C419
*22p/25V_2
4/13 Updated
R59
100K_5%_4
EDP_HPD_1V8_ODL
Q11
PJE138K
EDP_HPD_3V3 [21]
R333
10K_5%_4
SVID_ALERT_L
PCH_PROCHOT_ODL [24,29,30]
THERMTRIP_L [30]
R62
R65
R67
R68
R69
51_5%_4
100_5%_4
TCK [15]
NTRST/EXTD [15]
TMS/TMSC [15]
TDI/EXTB [15]
TDO/EXTA [15]
EXTE/TRIGIN [15]
EXTF/TRIGOUT [15]
R55
R57
*51_5%_4
C360
0.1u/16V_4
RTC_EXPAD
R52
100K_5%_4
[24] SUSPWRNACK
[24] EC_PCH_PWROK
[24,30] PMIC_EC_PWROK_OD
R324
*0_5%_4
R325
*1M_1%_4
[23] PCH_SUSCLK
[15,24] PCH_RSMRST_L
[15,24] EC_PCH_PWR_BTN_ODL
[15,16,24,35] SYS_RST_ODL
[7,15,17,18,23,24,35] PLT_RST_L
[33] EN_PP3300_EMMC
BATLOW_L
PCH_INTRUDER
R51
R278
100K_5%_4
PMU_RCOMP
R53
200_1%_4
CLOCKS
R46
200K_1%_4
PCH_OSCOUT
PCH_OSCIN
X3
19.2MHZ/20ppm
C1
C4
15p/50V_4
PCH_RTC_X1
PCH_RTC_X2
X2
32.768KHZ/20ppm
R45
10M_5%_4
C2
C3
6/30/16
Changed EN_PP3300_EMMC_ODL
to EN_PP3300_EMMC
R50
R54
20K_5%_4
[24] EC_PCH_RTCRST
EC_PCH_RTCRST
Q7
Q8
PJE138K
C5
C6
1u/6.3V_4
PP3300_A
R190
100K_5%_2
R191
1K_1%_2
SLP_S33
[7,17,24,30,33] SLP_S3_L
Q56
Q57
PLT_RST_L [7,15,17,18,23,24,35]
8/11/16
ADDED Q80 R508, C447
CONNECTED GATE OF Q80.G TO PCH_RSMRST_L
ADDED NET PCH_RSMRST_OD AND CONNECTED IT
FROM Q80.D TO Q79.G, Q81.G, Q82.G
R508
499K_1%_2
C447
*1u/6.3V_4
Q80
8/11/16
ADDED Q79, Q81, Q82, R507, R509, R510
CONNECTED GATE OF Q80 TO PCH_RSMRST_L
ADDED NET SLP_S4_PCH_L FROM U4.AK54 TO Q82.S
ADDED NET SLP_S3_PCH_L FROM U4.AC62 TO Q81.S
ADDED NET SLP_S0_PCH_L FROM U4.AD61 TO Q79.S
CONNECTED NET SLP_S4_L TO Q82.D
CONNECTED NET SLP_S3_L TO Q81.D
CONNECTED NET SLP_S0_L TO Q79.D
8/15/16
ADDED R516, R517, R518
PCH_RSMRST_OD
SLP_S0_PCH_L
SLP_S0_L [24,30]
SLP_S3_PCH_L
SLP_S3_L [7,17,24,30,33]
SLP_S4_PCH_L
SLP_S4_L [24,30]
PJA3413
Q79
Q81
Q82
R507
R509
R510
499K_1%_2
R516
R517
R518
*0_5%_2
Quanta Computer Inc.
PROJECT : ZRX
Size
Document Number
APL PMU/JTAG
Rev
1A
Date: Friday, July 21, 2017
Sheet 7 of 38


PPVAR_VCCGI
21A
U4J
3.3A
PPVAR_VNN
RSVD_VNNAON
TP22
VNN_SENSE
PPVAR_VNN_SENSE [31]
1.5A
PP1100_VCCIO
2.7A
PP1050_VCCRAM_S
PP1050_VCCRAM_IO_S
PP1050_VCCRAM_IO_S
R25 NCTF
PPVAR_VCCGI
R476
100_1%_2
R477
100_1%_2
PPVAR_VCCGI_SENSE_P [31]
PPVAR_VCCGI_SENSE_N [31]
CPU_APL_1296P
6/6/16
ADDED R476
ADDED R477
0.13A
1.8A
PP1240_VDD2_IO_A
PP1240_VDD2_SRAM_A
2.8A
PP1100_VDDQ
U4K
0.4A
PP1800_SOC_A
0.15A
PP3300_SOC_A
PP3300_RTC
CPU_APL_1296P
10/24/16
R461,R462,463,464,465 NEED CHANGE TO SHORT
PADS BEFORE RAMP
PP1240_A
PP1240_VDD2_IO_A
R461
*Short_6
PP1240_A
PP1240_VDD2_SRAM_A
R462
*Short_6
PP1050_S
PP1050_VCCRAM_IO_S
R463
*Short_6
PP1050_S
PP1050_VCCRAM_S
R464
*Short_6
PP1100_VDDQ
PP1100_VCCIO
R465
*Short_6
Quanta Computer Inc.
PROJECT : ZRX
Size
Document Number
APL POWER
Rev
1A
Date: Friday, July 21, 2017
Sheet 8 of 38

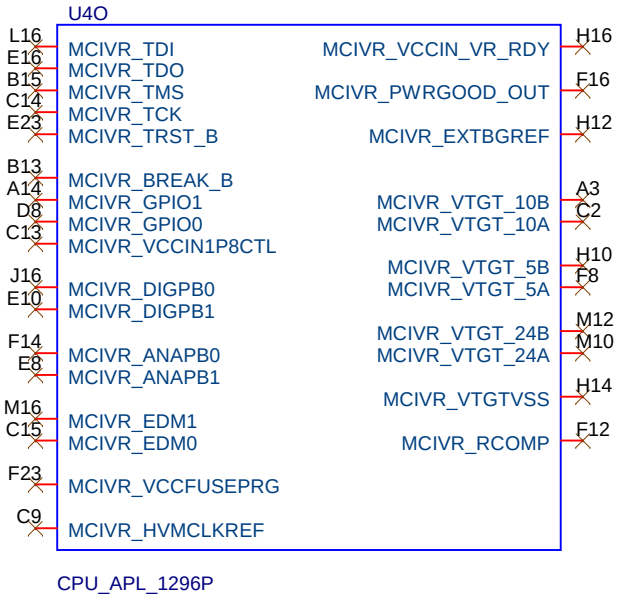


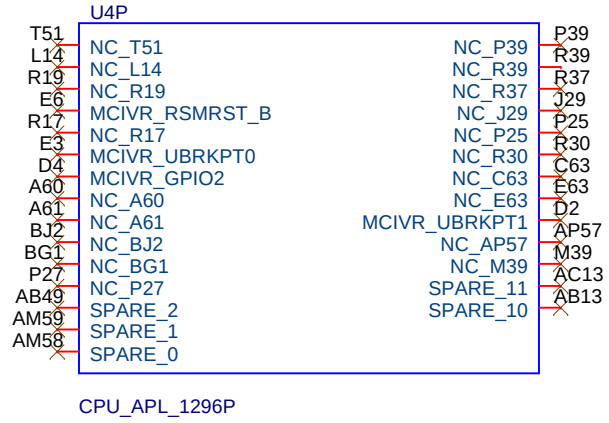
Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	APL GROUND	1A

Date: Friday, July 21, 2017 Sheet 9 of 38

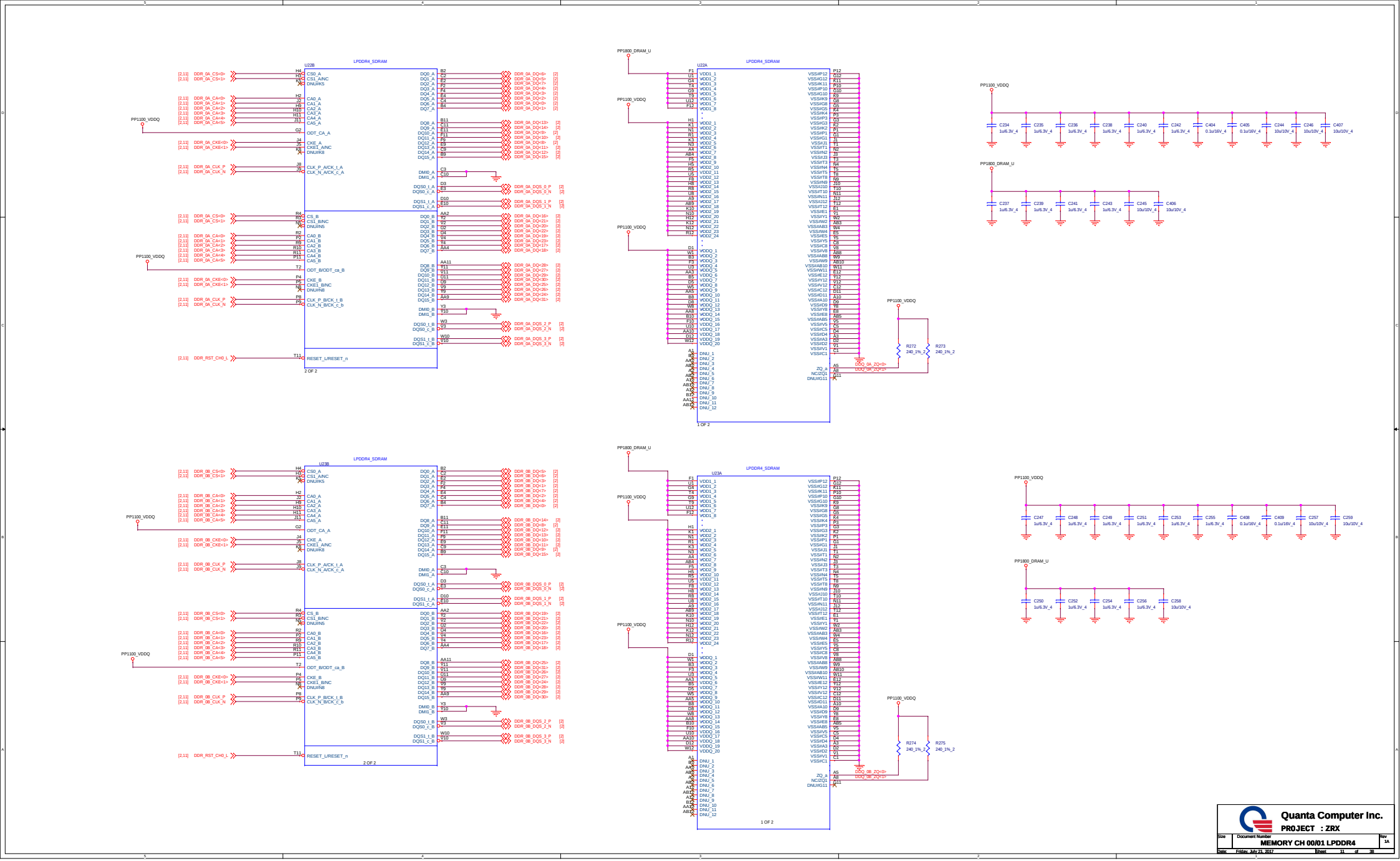




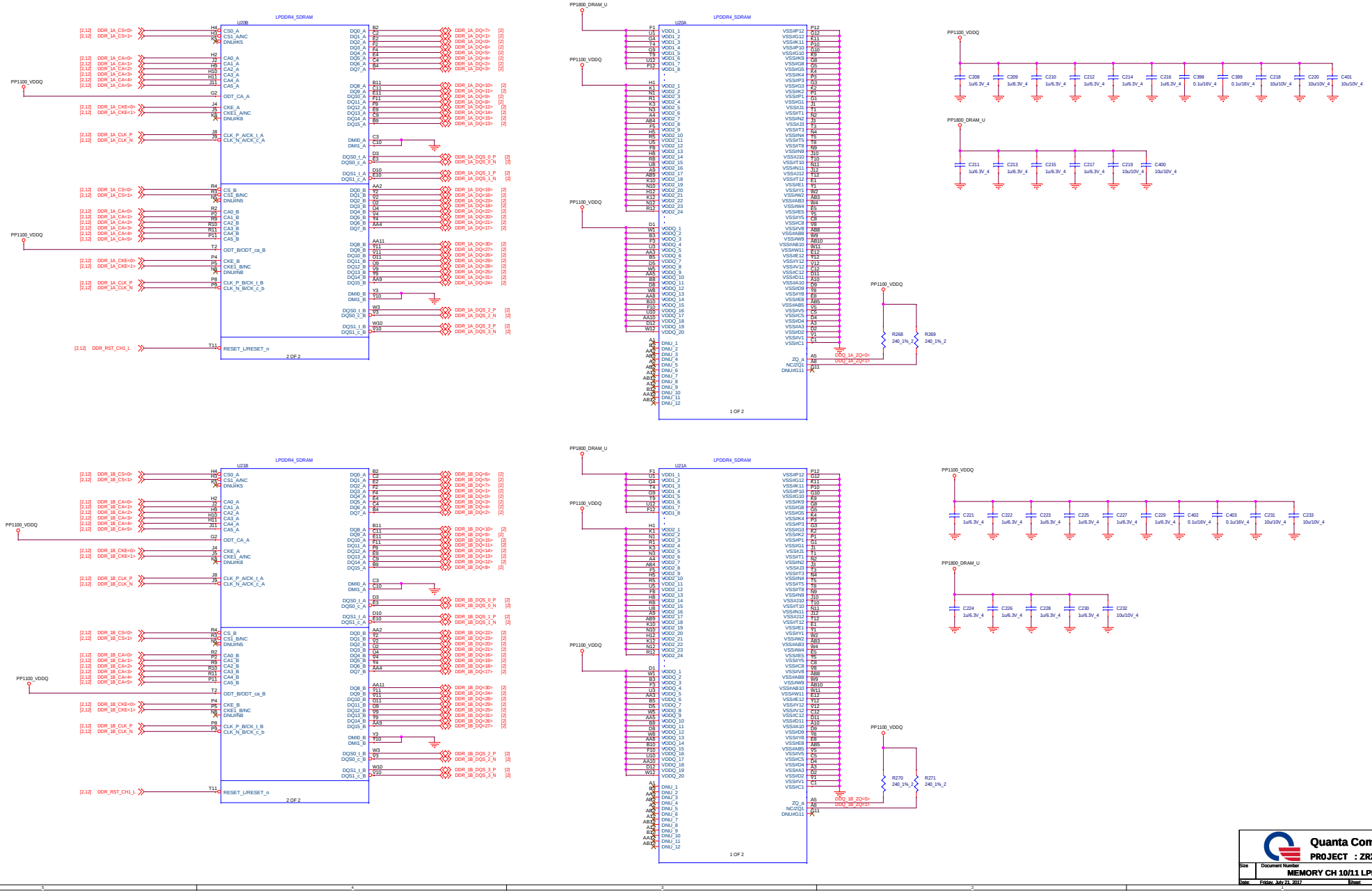
Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	APL NO CONNECT	1A
Date: Friday, July 21, 2017	Sheet 10 of 38	



Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	MEMORY CH 00/01 LPDDR4		1A
Date: Friday, July 21, 2017	Sheet 11 of 38		



Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	MEMORY CH 10/11 LPDDR4	1A
Date: Friday, July 21, 2017	Sheet 12 of 38	


PPVAR_VCCGI
C26 1u/6.3V_4
C35 1u/6.3V_4
C44 1u/6.3V_4
C49 1u/6.3V_4
C54 1u/6.3V_4
C58 1u/6.3V_4
C62 1u/6.3V_4
C65 1u/6.3V_4
C68 1u/6.3V_4
C70 1u/6.3V_4
C72 1u/6.3V_4
C74 1u/6.3V_4
BACKSIDE
PPVAR_VCCGI
C27 22u/6.3V_6
C36 22u/6.3V_6
C45 22u/6.3V_6
C50 22u/6.3V_6
C55 22u/6.3V_6
C59 22u/6.3V_6
C63 22u/6.3V_6
C66 22u/6.3V_6
TOPSIDE
EDGE CAP
PP1050_VCCRAM_IO_S
C79 1u/6.3V_4
C84 1u/6.3V_4
C80 1u/6.3V_4
C85 1u/6.3V_4
BACKSIDE
PP1050_VCCRAM_IO_S
C88 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR VCCRAM_1P05_IO PINS
PP1240_VDD2_IO_A
C93 1u/6.3V_4
C101 1u/6.3V_4
C94 1u/6.3V_4
BACKSIDE
PP1240_VDD2_IO_A
C104 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR AE20,AE18,AE22,AG22
VDD2_1P24_MPHY
PPVAR_VNN
C28 1u/6.3V_4
C37 1u/6.3V_4
C46 1u/6.3V_4
BACKSIDE
PPVAR_VNN
C29 22u/6.3V_6
C38 22u/6.3V_6
C47 22u/6.3V_6
C51 22u/6.3V_6
C274 *22u/6.3V_6
C275 *22u/6.3V_6
TOPSIDE
EDGE CAP
PP1240_VDD2_SRAM_A
C81 1u/6.3V_4
C86 1u/6.3V_4
C82 1u/6.3V_4
BACKSIDE
PP1240_VDD2_SRAM_A
C89 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR AM20,AK20,AM37
VDD2_1P24_GLM
PP1240_VDD2_IO_A
C95 1u/6.3V_4
BACKSIDE
PP1240_VDD2_IO_A
C96 1u/6.3V_4
C105 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR AA18,AA20
VDD2_1P24_DSI_CSI
PP1100_VCCIO
C52 22u/6.3V_6
C56 22u/6.3V_6
TOPSIDE
EDGE CAP
AM42,AM25,AM23,AM41
PP1100_VCCIO
C30 1u/6.3V_4
C39 1u/6.3V_4
BACKSIDE
PP1240_VDD2_SRAM_A
C83 1u/6.3V_4
BACKSIDE
PLACE NEAR AM28
VDD2_1P24_GLM
PP3300_RTC
C99 1u/6.3V_4
C198 0.1u/16V_4
TOPSIDE
AA44
VCCRTC_3P3V
PP1100_VDDQ
C31 1u/6.3V_4
C40 1u/6.3V_4
BACKSIDE
PP1100_VDDQ
C32 22u/6.3V_6
C41 22u/6.3V_6
C48 22u/6.3V_6
C53 22u/6.3V_6
C60 22u/6.3V_6
C64 22u/6.3V_6
C67 22u/6.3V_6
C69 22u/6.3V_6
TOPSIDE
EDGE CAP
PP1240_VDD2_SRAM_A
C76 1u/6.3V_4
C77 1u/6.3V_4
BACKSIDE
PP1240_VDD2_SRAM_A
C87 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR AJ20,AJ22,AK22
VDD2_1P24_AUD_ISH_PLL
PP1800_SOC_A
C97 1u/6.3V_4
C100 1u/6.3V_4
C98 1u/6.3V_4
BACKSIDE
PP1800_SOC_A
PP1800_SOC_A
C102 1u/6.3V_4
C106 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR VDD_1P8V_A
PP1050_VCCRAM_S
C33 1u/6.3V_4
C42 1u/6.3V_4
C34 1u/6.3V_4
C43 1u/6.3V_4
BACKSIDE
PP1050_VCCRAM_S
C57 22u/6.3V_6
C61 22u/6.3V_6
TOPSIDE
EDGE CAP
PLACE NEAR VCCRAM_1P05 PINS
PP1240_VDD2_IO_A
C78 1u/6.3V_4
BACKSIDE
PLACE NEAR AG20
VDD2_1P24_USB2
BACKSIDE
PP3300_SOC_A
C90 1u/6.3V_4
BACKSIDE
PP3300_SOC_A
C107 1u/6.3V_4
AK25,AJ25
TOPSIDE
PP3300_SOC_A
C91 1u/6.3V_4
C92 1u/6.3V_4
C103 22u/6.3V_6
EDGE CAP
AC41,AA42,Y44,V44,V46
PLACE NEAR VDD_3P3V_A
Quanta Computer Inc.
PROJECT : ZRX
Size
Document Number
SOC DECOUPLING
Rev
1A
Date: Friday, July 21, 2017
Sheet 13 of 38

PCH SPI FLASH

8/31/16

ADDED D40, R520
ADDED HAVEN_AP_FLASH_SEL_33A_ODL

PDG IS NOT CLEAR IF CS0 NEEDS PULL-UP
33 OHMS ON SPI SIDE BASED ON PDG

WINBOND: W25Q128FWPIF
GIGADEVICES: 25LQ128CWIG
16MB PCH FLASH
STANDBY CURRENT: 50 UA
MAX CURRENT: 25MA

8/11/16

CHANGED R471 PULLUP TO PP3300_EC
CHANGED U5 TO W25Q128FWPIF

74LVC1G07
1.65-5.5V

KEEP NEAR H1(U95) TO MINIMIZE SPI STUBS

EC SPI FLASH

DO WE WANT DO USE THE 1.8V LDO?
ADD 1.8V SPI PART

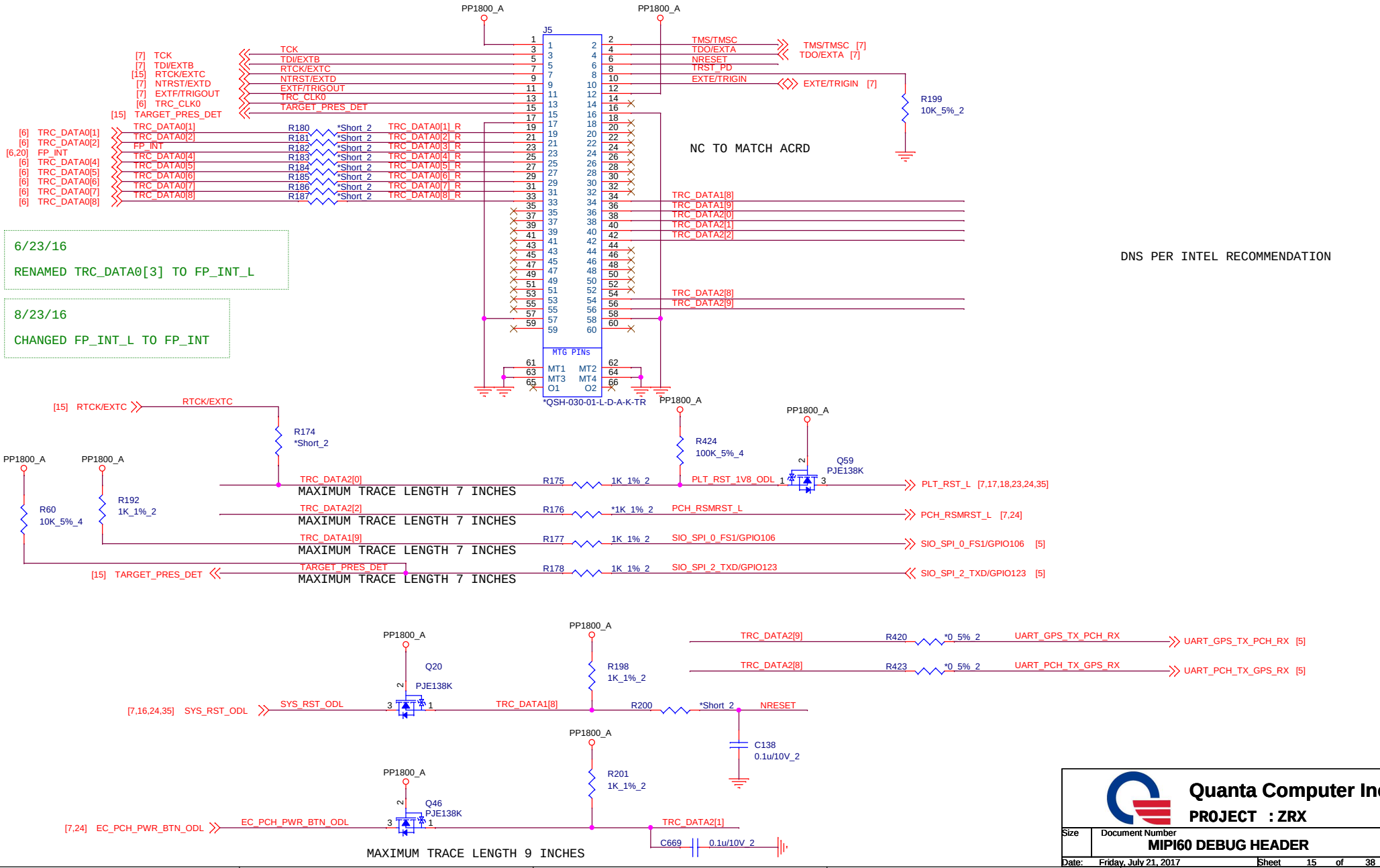
DSW STANDBY CURRENT: 10-50 UA
DSW POWERDOWN CURRENT: 1-5 UA

512KB EC FLASH
MAX CURRENT: 15MA

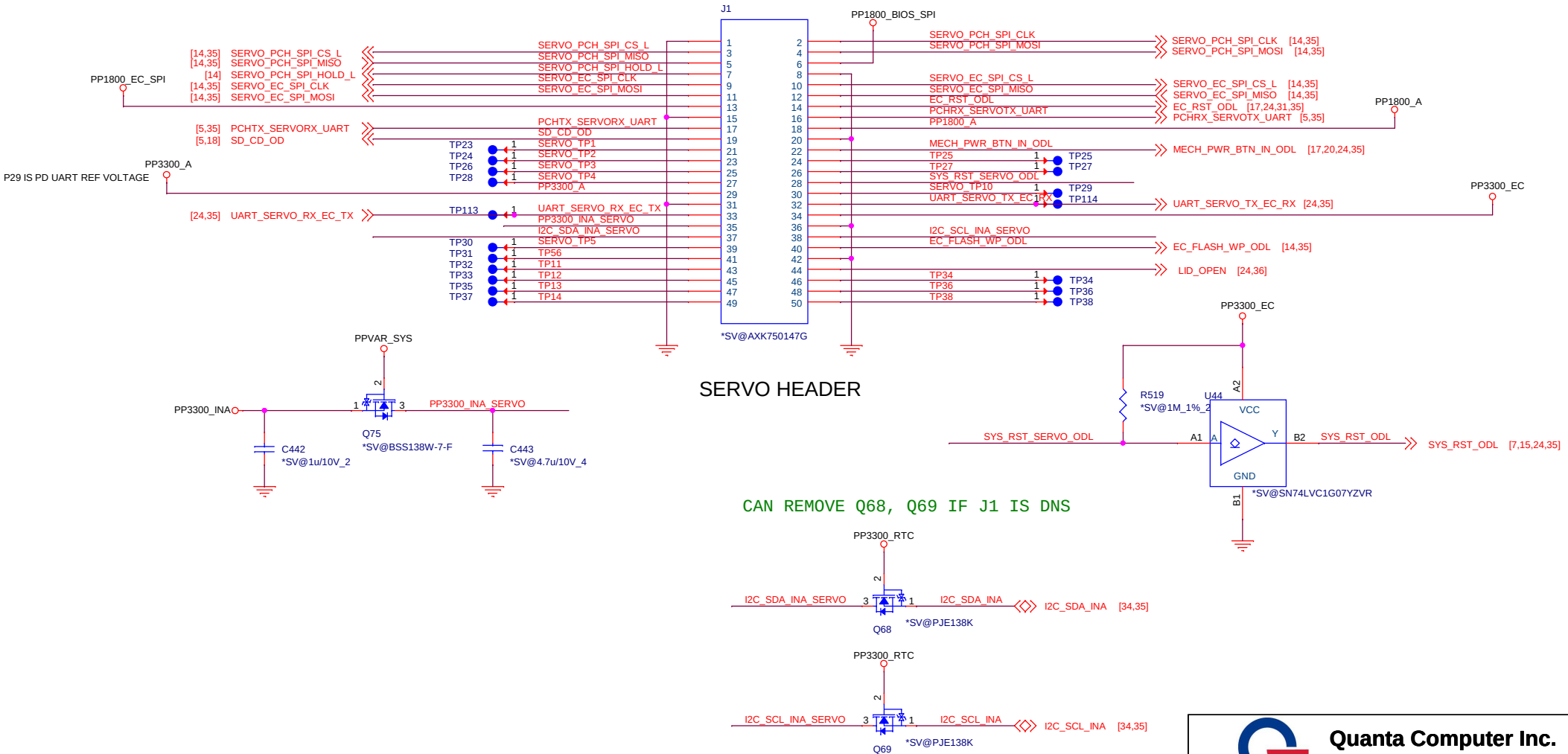
8/11/16

REMOVED R89, MT1
(Hole1 change to normal hole)

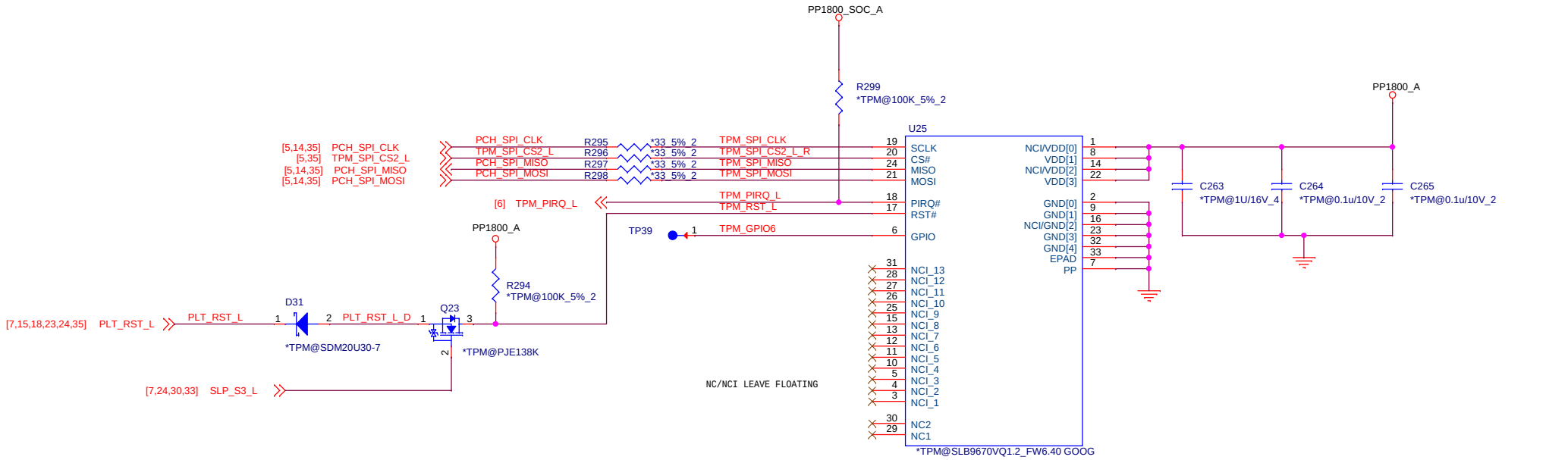
Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	SPI ROM		1A
Date: Friday, July 21, 2017		Sheet 14 of 38	



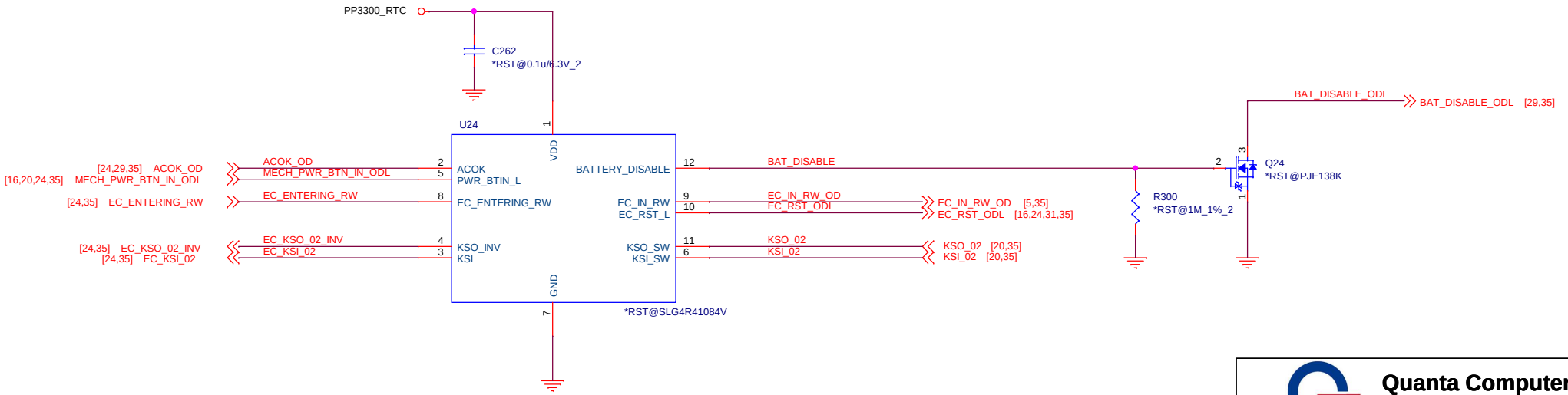
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: MIPI60 DEBUG HEADER	Rev: 1A
Date: Friday, July 21, 2017	Sheet 15 of 38	



Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number	Rev
	SERVO	1A
Date: Friday, July 28, 2017	Sheet 16 of 38	



RESET IC



Quanta Computer Inc.

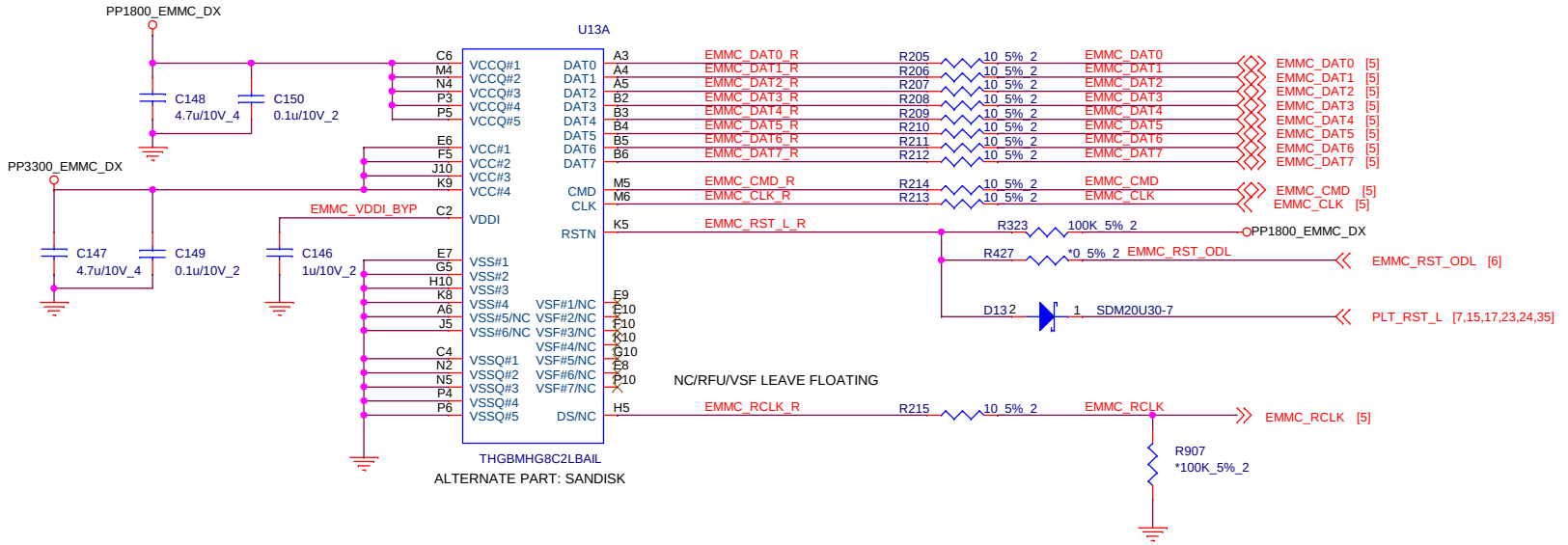
PROJECT : ZRX

Size	Document Number	Rev
	TPM/SILEGO	1A

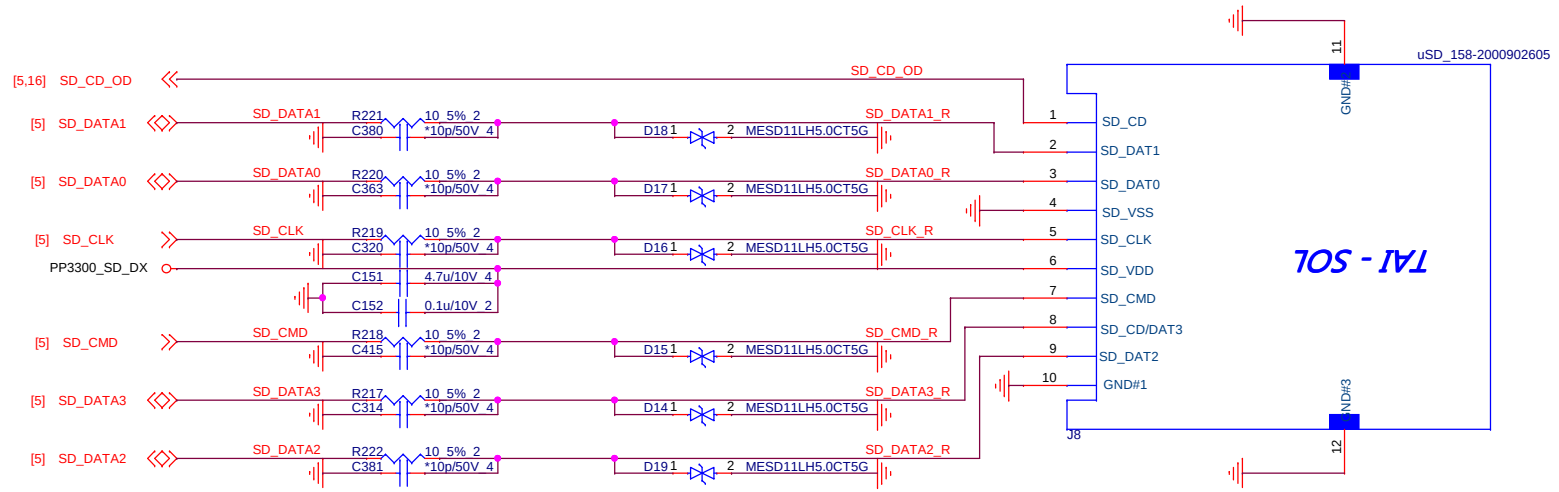
Date: Friday, July 21, 2017 Sheet 17 of 38

32 GB EMMC SD STORAGE

150 UA SLEEP CURRENT



SD Connetcor

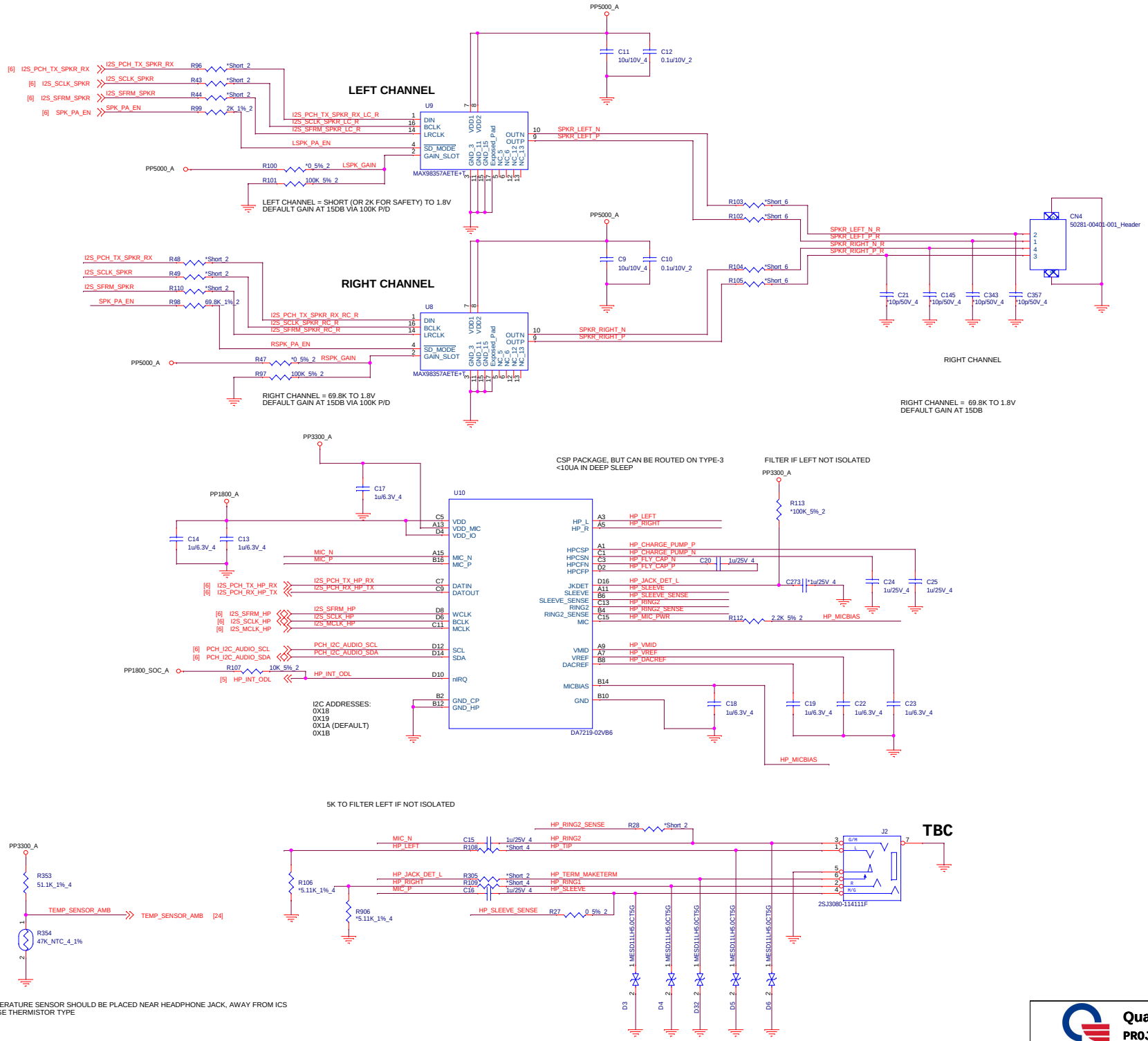


Quanta Computer Inc.

PROJECT : ZRX

Size	Document Number	Rev
	eMMC/SD	1A

Date: Friday, July 21, 2017 Sheet 18 of 38

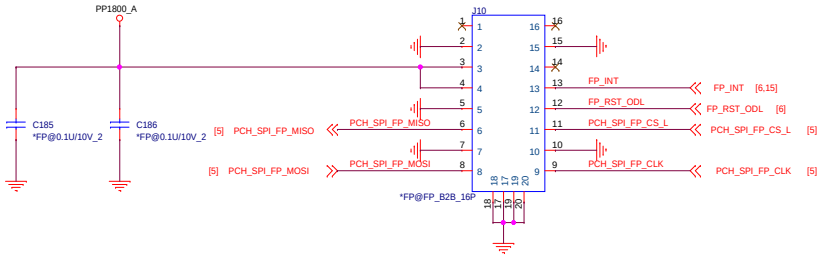


Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	AUDIO		1A
Date:	Friday, July 21, 2017	Sheet 19 of 38	

FINGER PRINT CONNECTOR

Not - Ready

Modify the pins assignment to meet Quanta's layout symbol rule.



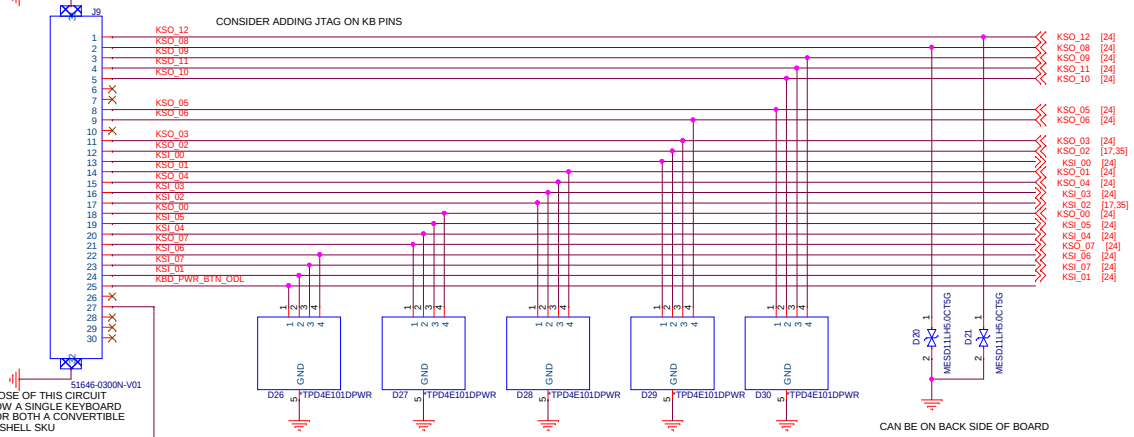
NFC CONNECTOR

SUBJECT TO CHANGE PER QUANTA REQUEST

Remove This Function

BSW REF DESIGN ERRATA MENTIONED
A LEAKAGE PROBLEM INTO THE EC
VIA THE KSO PINS. THE FIX WAS
TO ADD 100K PULLUPS TO 3P3A_EC
ON THE KSO SIGNALS
0C2A COMPATIBLE

CONSIDER ADDING JTAG ON KB PINS

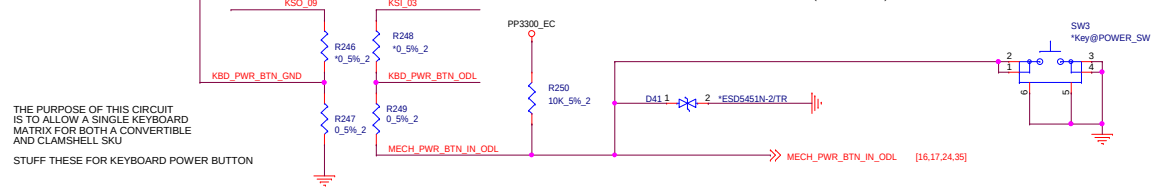


THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHELL SKU

CAN BE ON BACK SIDE OF BOARD

STUFF THESE FOR KEYBOARD LOCK BUTTON

STUFF FOR POWER BUTTON (DETACHABLE)



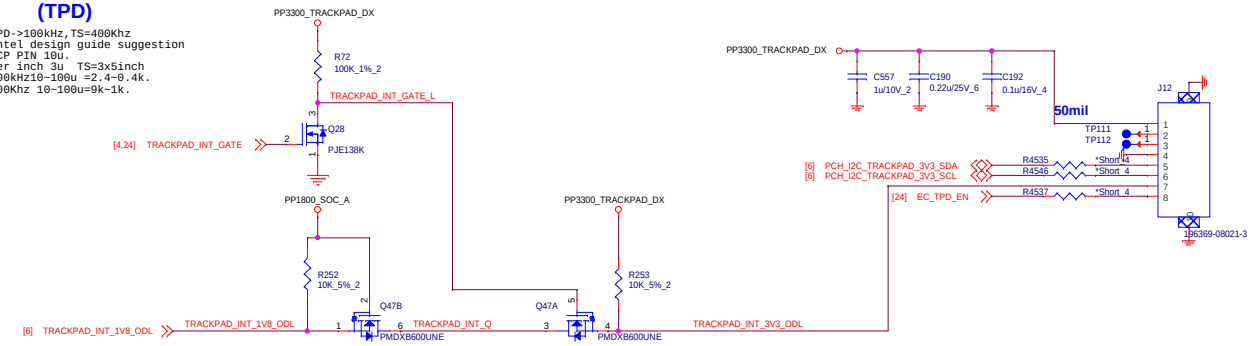
THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHELL SKU

STUFF THESE FOR KEYBOARD POWER BUTTON

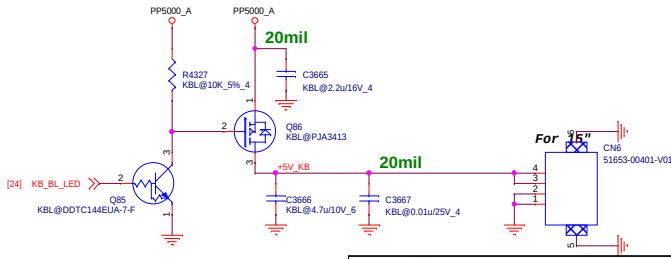
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)

(TPD)

TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.



KB_BL Control



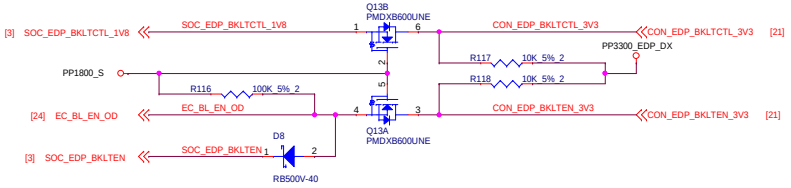
11/3/16

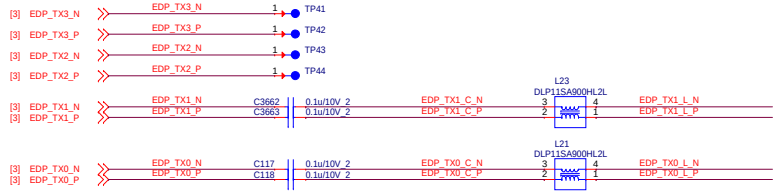
Remove Pen connector
Add KB backlight circuit

Quanta Computer Inc.
PROJECT : ZRX

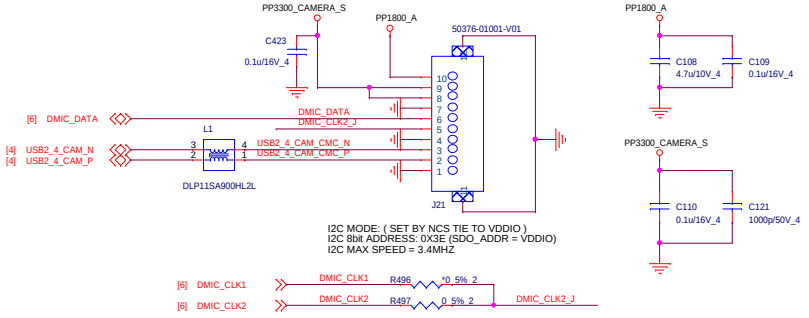
Size	Document Number	Rev
	BASE: KB, TP, NFC, FINGER	1A
Date: Friday, July 21, 2017	Sheet 20 of 38	

EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR





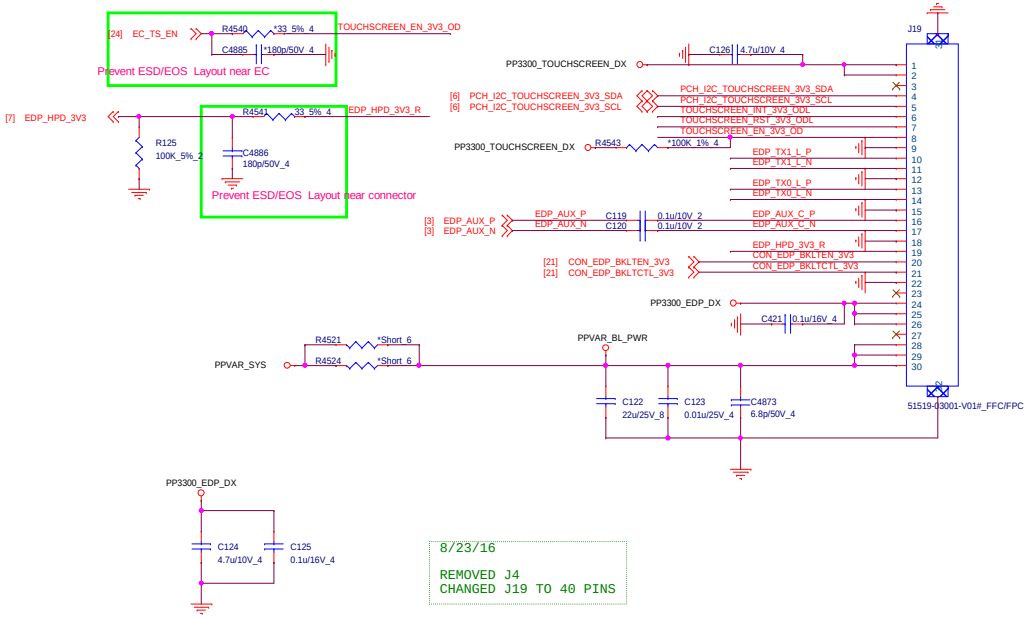
CCD/DMIC BOARD (KX022+DMIC)



Sensor I2C Level shift

Remove This Function

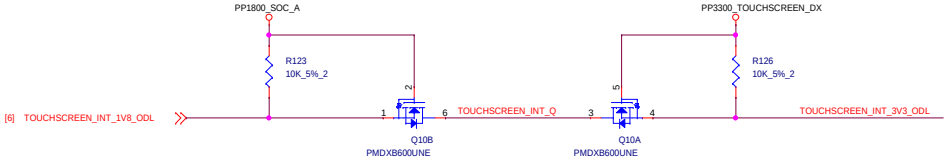
EDP + TouchScreen Connector

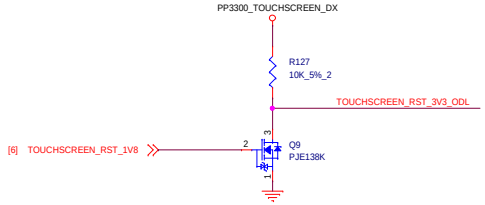


8/23/16

REMOVED J4
CHANGED J19 TO 40 PINS

TOUCH SCREEN





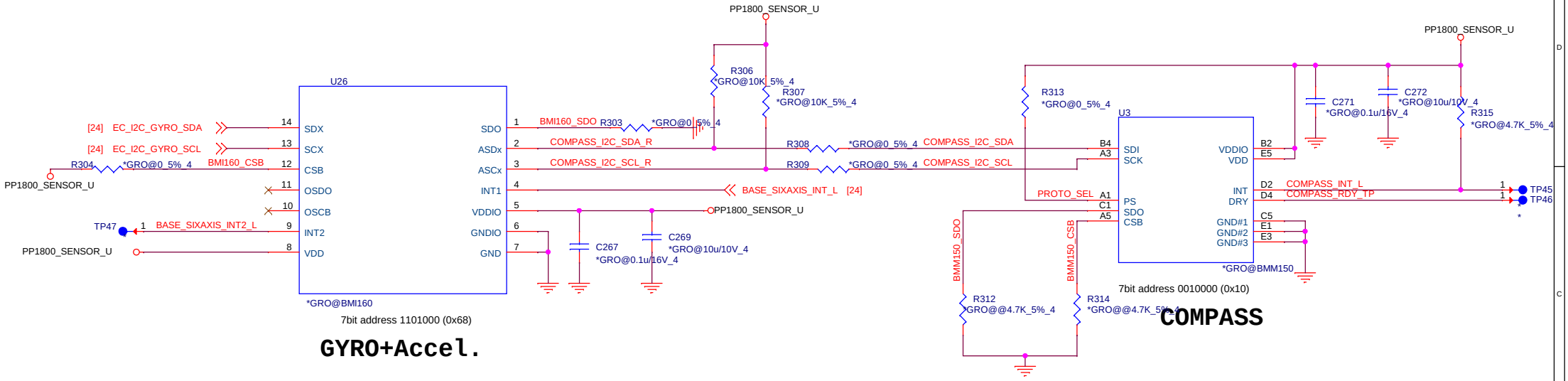
C-PANEL CAMERA

Remove This Function

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	LID: eDP, CAM, TOUCH, SEN	1A

Date: Friday, July 21, 2017 Sheet 21 of 38



BAROMETER

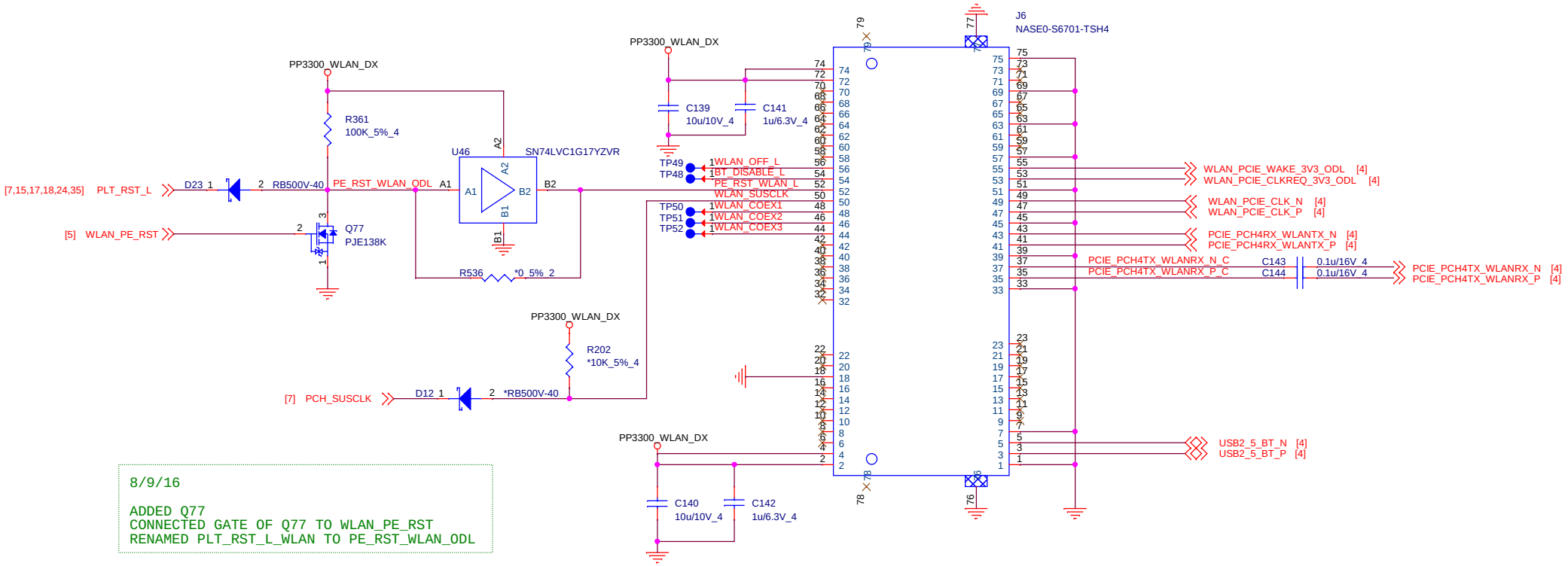
Remove This Function

CHARGE/BATTERY LED

TO Sub Board

Quanta Computer Inc. PROJECT : ZRX		
Size	Document Number: COMPASS, BARO, GYRO, LID	Rev: 1A
Date: Friday, July 21, 2017	Sheet 22 of 38	

M.2 connector (Wifi+BT)



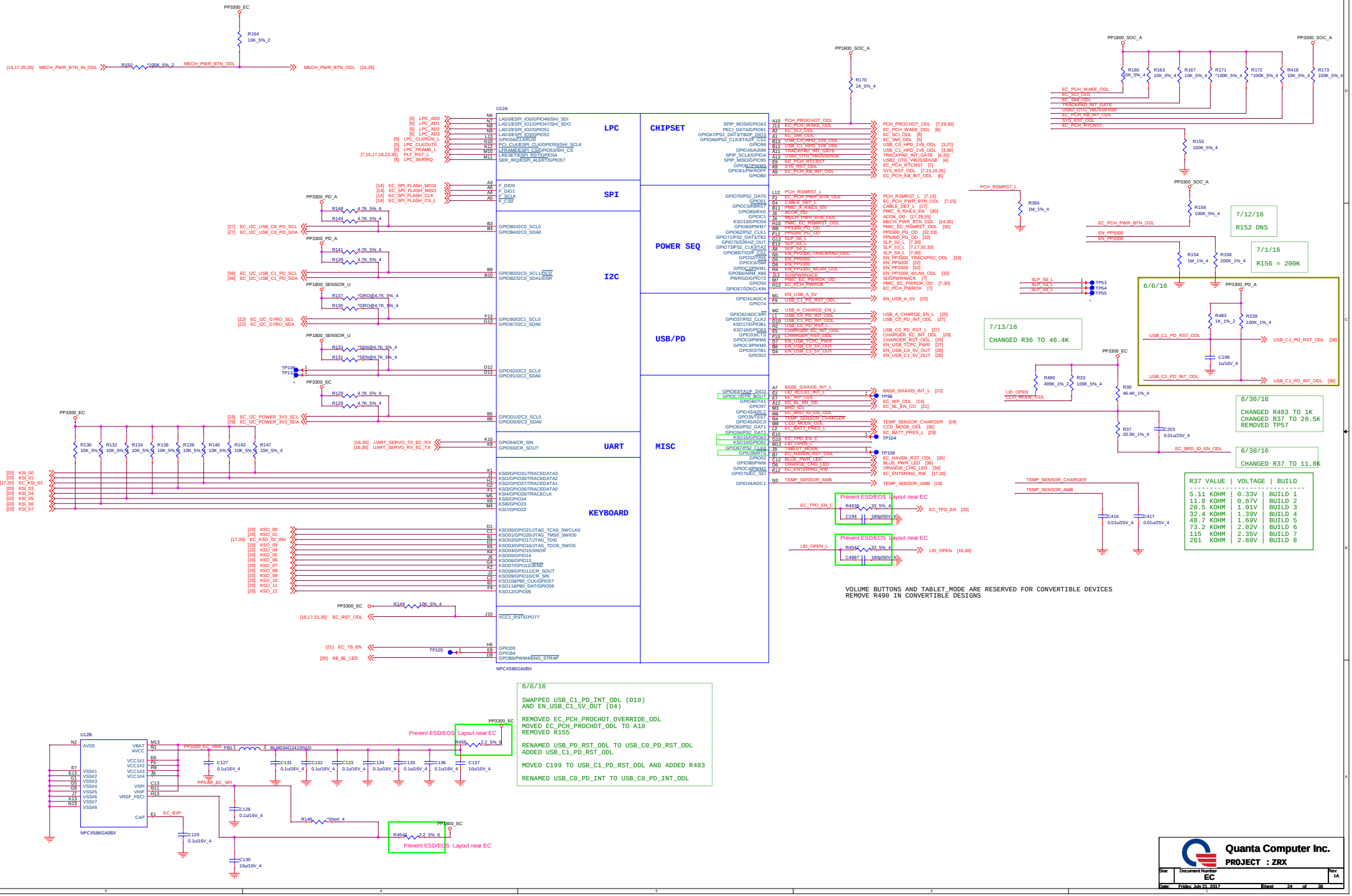
8/9/16

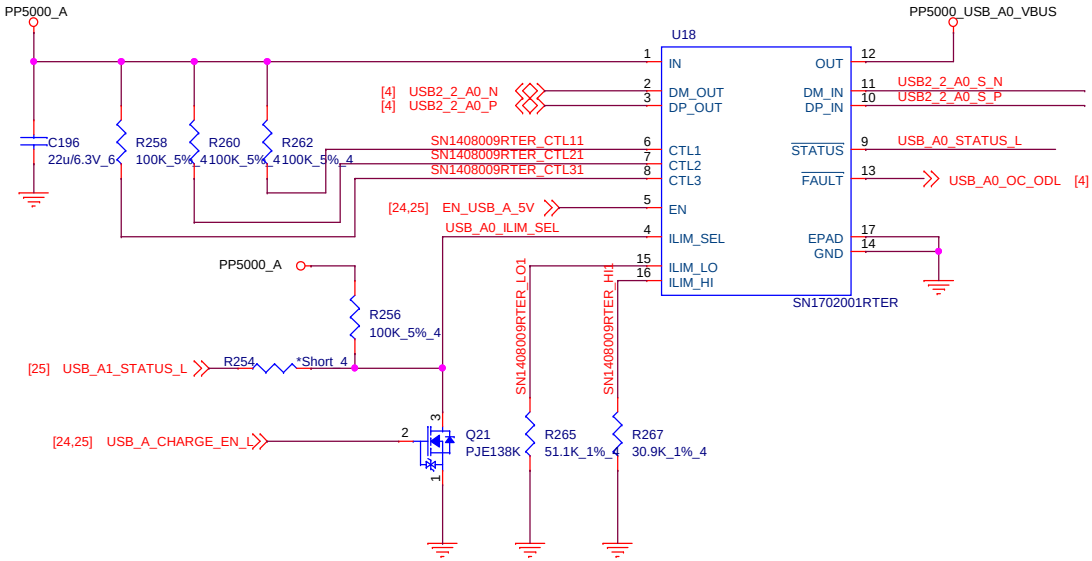
ADDED Q77
CONNECTED GATE OF Q77 TO WLAN_PE_RST
RENAMED PLT_RST_L_WLAN TO PE_RST_WLAN_ODL

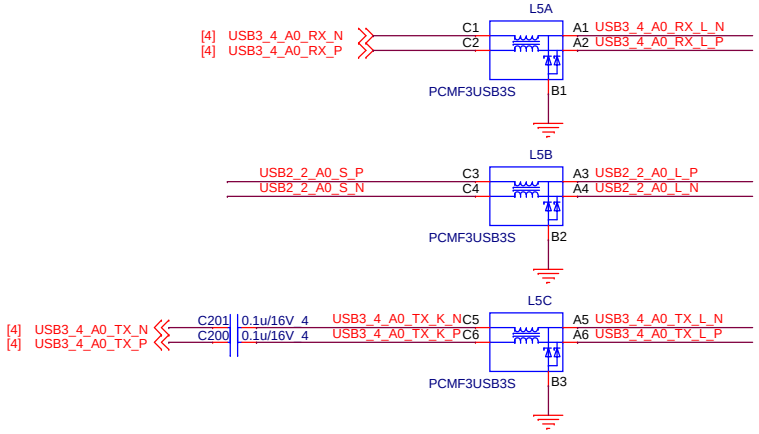
GPS connector

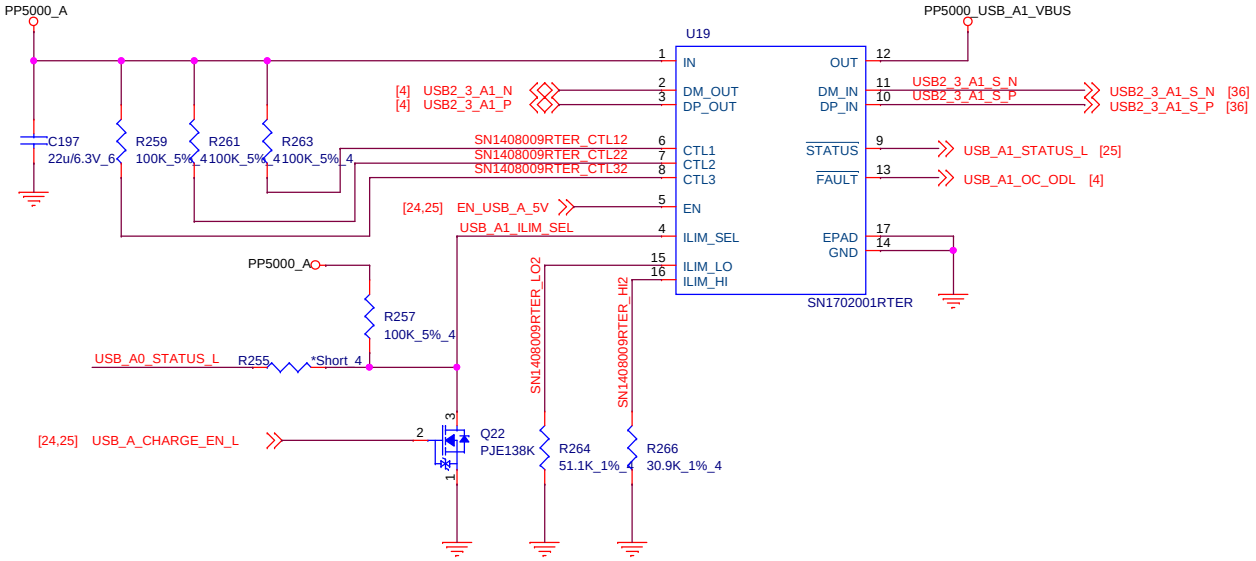
Remove This Function

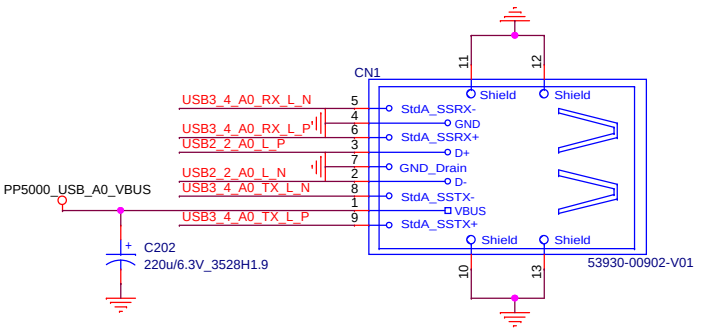
Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: WIFI,GPS CONNTECOR	Rev: 1A
Date: Friday, July 21, 2017	Sheet 23 of 38	


PP3300_EC
R164 10K_5%_2
[16,17,20,35] MECH_PWR_BTN_IN_ODL
R150 *100K_5%_2
MECH_PWR_BTN_ODL
MECH_PWR_BTN_ODL [24,35]
U12A
NPCX586GA0BX
LPC
SPI
I2C
UART
KEYBOARD
CHIPSET
POWER SEQ
USB/PD
MISC
[5] LPC_AD0
[5] LPC_AD1
[5] LPC_AD2
[5] LPC_AD3
[5] LPC_CLKRUN_L
[5] LPC_CLKOUT0
[5] LPC_FRAME_L
[7,15,17,18,23,35] PLT_RST_L
[5] LPC_SERIRQ
[14] EC_SPI_FLASH_MOSI
[14] EC_SPI_FLASH_MISO
[14] EC_SPI_FLASH_CLK
[14] EC_SPI_FLASH_CS_L
PP3300_PD_A
R148 4.7K_5%_4
R144 4.7K_5%_4
[27] EC_I2C_USB_C0_PD_SCL
[27] EC_I2C_USB_C0_PD_SDA
R141 4.7K_5%_4
R139 4.7K_5%_4
[36] EC_I2C_USB_C1_PD_SCL
[36] EC_I2C_USB_C1_PD_SDA
PP1800_SENSOR_U
R137 *GRO@4.7K_5%_4
R135 *GRO@4.7K_5%_4
[22] EC_I2C_GYRO_SCL
[22] EC_I2C_GYRO_SDA
R133 *SEN@4.7K_5%_4
R131 *SEN@4.7K_5%_4
TP106
TP110
R129 4.7K_5%_4
R128 4.7K_5%_4
[29] EC_I2C_POWER_3V3_SCL
[29] EC_I2C_POWER_3V3_SDA
R130 10K_5%
R132 10K_5%
R134 10K_5%
R136 10K_5%
R138 10K_5%
R140 10K_5%
R143 10K_5%
R147 10K_5%
[20] KSI_00
[20] KSI_01
[17,35] EC_KSI_02
[20] KSI_03
[20] KSI_04
[20] KSI_05
[20] KSI_06
[20] KSI_07
[20] KSO_00
[20] KSO_01
[17,35] EC_KSO_02_INV
[20] KSO_03
[20] KSO_04
[20] KSO_05
[20] KSO_06
[20] KSO_07
[20] KSO_08
[20] KSO_09
[20] KSO_10
[20] KSO_11
[20] KSO_12
R149 10K_5%_4
[16,17,31,35] EC_RST_ODL
[21] EC_TS_EN
TP105
[20] KB_BL_LED
[16,35] UART_SERVO_TX_EC_RX
[16,35] UART_SERVO_RX_EC_TX
F_DIO0
F_DIO1
F_SCLK
F_CS0
GPIOB5/I2C0_SCL0
GPIOB4/I2C0_SDA0
GPIOB3/I2C0_SCL1/DCD
GPIOB2/I2C0_SDA1/DSR
GPIO92/I2C2_SCL0
GPIO91/I2C2_SDA0
GPIOD1/I2C3_SCL0
GPIOD0/I2C3_SDA0
GPIO64/CR_SIN
GPIO65/CR_SOUT
KSI0/GPIO31/TRACEDATA3
KSI1/GPIO30/TRACEDATA2
KSI2/GPIO27/TRACEDATA1
KSI3/GPIO26/TRACEDATA0
KSI4/GPIO25/TRACECLK
KSI5/GPIO24
KSI6/GPIO23
KSI7/GPIO22
KSO0/GPIO21/JTAG_TCK0_SWCLK0
KSO1/GPIO20/JTAG_TMS0_SWIO0
KSO2/GPIO17/JTAG_TDI
KSO3/GPIO16/JTAG_TDO0_SWO0
KSO4/GPIO15/ENOR
KSO5/GPIO14
KSO6/GPIO13
KSO7/GPO12/IEN0
KSO8/GPIO11/CR_SOUT
KSO9/GPIO10/CR_SIN
KSO10&P80_CLK/GPIO07
KSO11&P80_DAT/GPIO06
KSO12/GPIO05
VCC1_RST/GPO77
GPIO00
GPIO84
GPOB6/PWM4/ENG_STRAP
SPIP_MOSI/GPIOA3
PECI_DATA/GPIO81
GPIOA7/PS2_DAT3/TB2/F_DIO3
GPIOA6/PS2_CLK3/TA2/F_CS1
GPIO94
GPIO5A/A20M
SPIP_SCLK/GPIOA
SPIP_MISO/GPIO95
GPIOB7/PWM5
GPIO61/PWROFF
GPIOB0
GPIO70/PS2_DAT0
GPIO01
GPIOC5/KBRST
GPIO85/RXD
GPIOC1
KSO13/GPIO04
GPIO60/PWM7
GPIO62/PS2_CLK1
GPIO71/PS2_DAT3/TB2
GPIO75/32KHZ_OUT
GPIO73/PS2_CLK3/TA2
GPIO86/TXD/F_CS1
GPO32/TRST
GPIOC6/SMI
GPIOC2/PWM1
GPO66/ARM_X86
PWRGD/GPIO77
GPIO50
GPIOE7/32KCLKIN
GPIO41/ADC4
GPIO74
GPIO42/ADC3/RI
GPIO37/PS2_CLK2
KSO17/GPIOB1
KSO16/GPIO09
GPIO33/CTS
GPIOC0/PWM6
GPIOC3/PWM0
GPIOD3/TB1
GPIOD2
GPIO93/TA1/F_DIO2
GPIOC7/DTR_BOUT
GPIO40/TA1
GPIO97
GPIO43/ADC2
GPO35/TEST
GPIO45/ADC0
GPIO63/PS2_DAT1
GPIO34/PS2_DAT2
KSO15/GPIO03
KSO14/GPIO02
GPIO67/PS2_CLK1
GPIO38/RTS
GPIO02
GPIO80/PWM
GPIOC4/PWM2
GPIO76/EC_SCI
GPIO44/ADC1
PCH_PROCHOT_ODL [7,29,30]
EC_PCH_WAKE_ODL [6]
EC_SCI_ODL [6]
EC_SMI_ODL [6]
USB_C0_HPD_1V8_ODL [3,27]
USB_C1_HPD_1V8_ODL [3,36]
TRACKPAD_INT_GATE [4,20]
USB2_OTG_VBUSSENSE [4]
EC_PCH_RTCRST [7]
SYS_RST_ODL [7,15,16,35]
EC_PCH_KB_INT_ODL [6]
PCH_RSMRST_L [7,15]
EC_PCH_PWR_BTN_ODL [7,15]
CABLE_DET_L [27]
PMIC_A_RAILS_EN [30]
ACOK_OD [17,29,35]
MECH_PWR_BTN_ODL [24,35]
PMIC_EC_RSMRST_ODL [30]
PP3300_PG_OD [32,33]
PP5000_PG_OD [32]
SLP_S0_L [7,30]
SLP_S3_L [7,17,30,33]
SLP_S4_L [7,30]
EN_PP3300_TRACKPAD_ODL [33]
EN_PP5000 [32]
EN_PP3300 [32]
EN_PP3300_WLAN_ODL [33]
SUSPWRNACK [7]
PMIC_EC_PWROK_OD [7,30]
EC_PCH_PWROK [7]
EN_USB_A_5V
USB_C1_PD_RST_ODL
USB_A_CHARGE_EN_L [25]
USB_C0_PD_INT_ODL [27]
USB_C1_PD_INT_ODL [27]
USB_C0_PD_RST_L
USB_C0_PD_RST_L [27]
CHARGER_EC_INT_ODL [29]
CHARGER_RST_ODL [29]
EN_USB_TCPC_PWR [27]
EN_USB_C0_5V_OUT [28]
EN_USB_C1_5V_OUT [28]
BASE_SIXAXIS_INT_L [22]
LID_ACCEL_INT_L
EC_WP_ODL [14]
EC_BL_EN_OD [21]
BRD_ID1
EC_PRD_ID_EN_ODL
TEMP_SENSOR_CHARGER [29]
CCD_MODE_ODL [35]
EC_BATT_PRES_L [29]
EC_TPD_EN_C
LID_OPEN_L
EC_HAVEN_RST_ODL [35]
BLUE_PWR_LED [36]
ORANGE_CHG_LED [36]
EC_ENTERING_RW [17,35]
TEMP_SENSOR_AMB [19]
TP98
TP104
TP108
R170 1K_5%_4
PP1800_SOC_A
PP3300_SOC_A
R160 10K_5%_4
R163 10K_5%_4
R167 10K_5%_4
R171 *100K_5%_4
R172 *100K_5%_4
R419 10K_5%_4
R173 100K_5%_4
EC_PCH_WAKE_ODL
EC_SCI_ODL
EC_SMI_ODL
TRACKPAD_INT_GATE
USB2_OTG_VBUSSENSE
EC_PCH_RSTCRST
SYS_RST_ODL
R153 100K_5%_4
PCH_RSMRST_L
R394 1M_1%_4
R158 100K_5%_4
EC_PCH_PWR_BTN_ODL
EN_PP5000
EN_PP3300
R154 1M_1%_4
R156 200K_1%_4
SLP_S0_L
SLP_S3_L
SLP_S4_L
TP53
TP54
TP55
PP3300_PD_A
R483 1K_1%_2
R239 100K_1%_4
C199 1u/16V_4
USB_C1_PD_RST_ODL
USB_C1_PD_RST_ODL [36]
USB_C1_PD_INT_ODL
USB_C1_PD_INT_ODL [36]
R490 499K_1%_2
R33 100K_5%_4
LID_OPEN
CCD_MODE_ODL
R36 46.4K_1%_4
R37 20.5K_1%_4
C203 0.01u/25V_4
EC_BRD_ID_EN_ODL
TEMP_SENSOR_CHARGER
TEMP_SENSOR_AMB
C416 0.01u/25V_4
C417 0.01u/25V_4
Prevent ESD/EOS Layout near EC
R4532 33_5%_4
C194 180p/50V_4
R4542 33_5%_4
C4887 180p/50V_4
U12B
VBAT
AVCC
VCC1#1
VCC1#2
VCC1#3
VCC1#4
VSPI
VHIF
VREF_PECI
CAP
VSS#1
VSS#2
VSS#3
VSS#4
VSS#5
VSS#6
VSS#7
VSS#8
PP3300_EC_ANA
FB1 BLM03AG241SN1D
R459 2.2_5%_6
C127 0.1u/16V_4
C131 0.1u/16V_4
C132 0.1u/16V_4
C133 0.1u/16V_4
C134 0.1u/16V_4
C135 0.1u/16V_4
C136 0.1u/16V_4
C137 10u/10V_4
PPVAR_EC_SPI
C128 0.1u/16V_4
C129 0.1u/16V_4
C130 10u/10V_4
EC_BYP
R146 *Short_4
R4544 2.2_5%_6
PP1800_EC
Prevent ESD/ECS Layout near EC
VOLUME BUTTONS AND TABLET_MODE ARE RESERVED FOR CONVERTIBLE DEVICES
REMOVE R490 IN CONVERTIBLE DESIGNS
7/12/16
R152 DNS
7/1/16
R156 = 200K
6/6/16
7/13/16
CHANGED R36 TO 46.4K
8/30/16
CHANGED R483 TO 1K
CHANGED R37 TO 20.5K
REMOVED TP57
6/30/16
CHANGED R37 TO 11.8K
R37 VALUE | VOLTAGE | BUILD
5.11 KOHM | 0.33V | BUILD 1
11.8 KOHM | 0.67V | BUILD 2
20.5 KOHM | 1.01V | BUILD 3
32.4 KOHM | 1.39V | BUILD 4
48.7 KOHM | 1.69V | BUILD 5
73.2 KOHM | 2.02V | BUILD 6
115 KOHM | 2.35V | BUILD 7
261 KOHM | 2.80V | BUILD 8
6/6/16
SWAPPED USB_C1_PD_INT_ODL (D10)
AND EN_USB_C1_5V_OUT (D4)
REMOVED EC_PCH_PROCHOT_OVERRIDE_ODL
MOVED EC_PCH_PROCHOT_ODL TO A10
REMOVED R155
RENAMED USB_PD_RST_ODL TO USB_C0_PD_RST_ODL
ADDED USB_C1_PD_RST_ODL
MOVED C199 TO USB_C1_PD_RST_ODL AND ADDED R483
RENAMED USB_C0_PD_INT TO USB_C0_PD_INT_ODL
Quanta Computer Inc.
PROJECT : ZRX
Size
Document Number
EC
Rev 1A
Date: Friday, July 21, 2017
Sheet 24 of 38









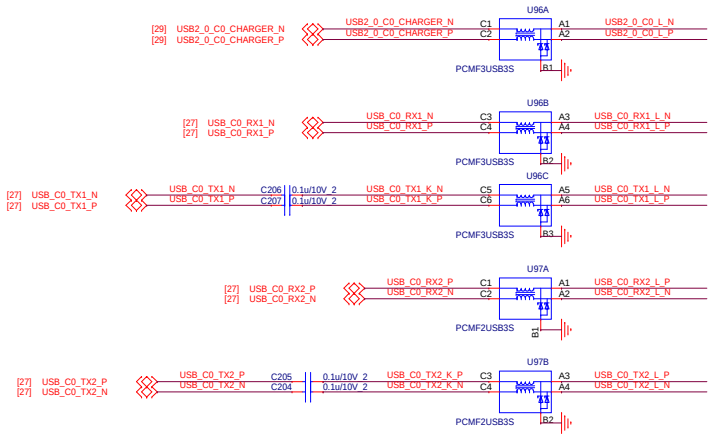
Quanta Computer Inc.

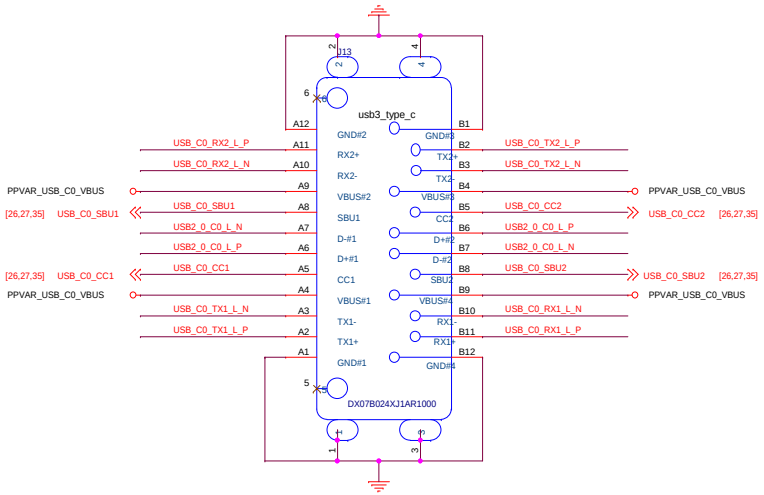
PROJECT : ZRX

Size	Document Number	Rev
	USB A CONNECTORS	1A

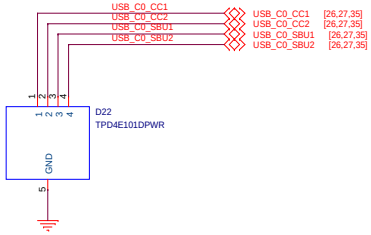
Date: Friday, July 21, 2017 Sheet 25 of 38

PORT 0 TYPE-C MLB

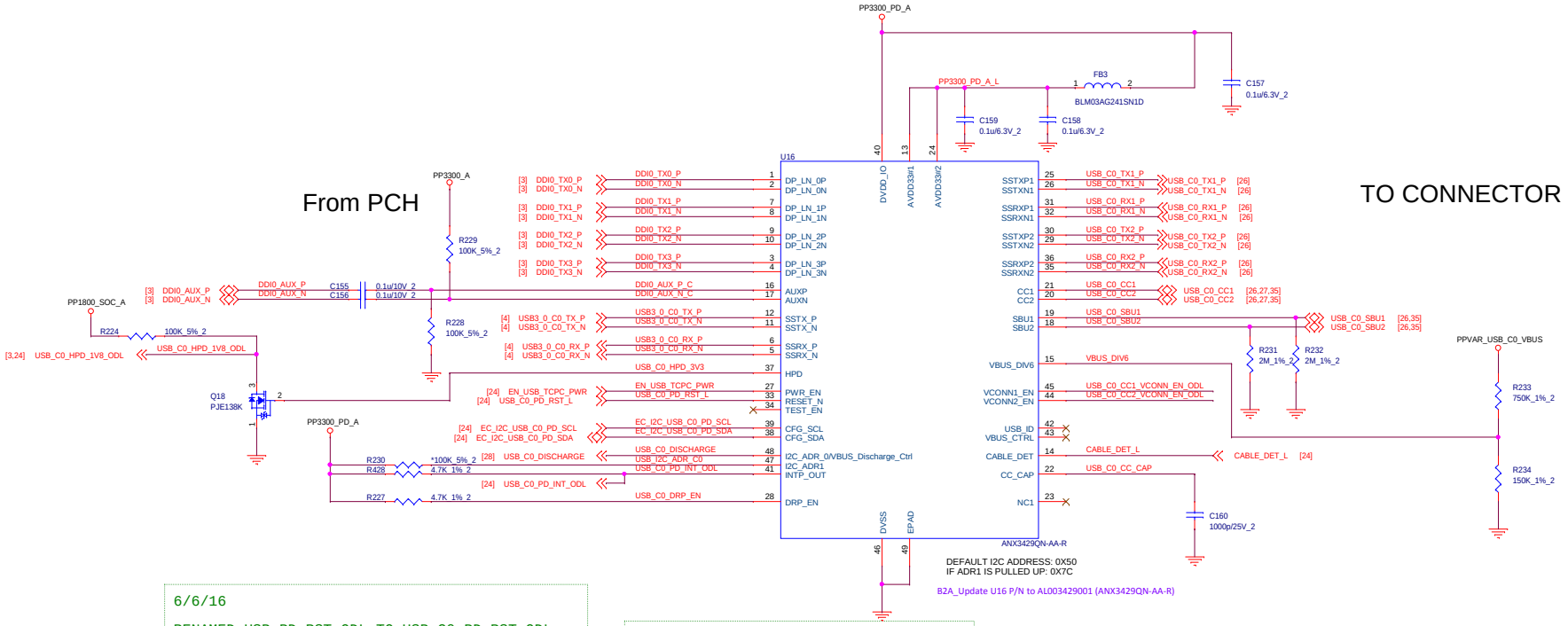




ESD Protection



Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: USB C CONNECTORS	Rev: 1A
Date: Friday, July 21, 2017	Sheet 26 of 38	



6/6/16

RENAMED USB_PD_RST_ODL TO USB_C0_PD_RST_ODL

8/9/16

RENAMED USB_C0_PD_RST_ODL TO USB_C0_PD_RST_L
MOVED PIN 13 TO PP3300_PD_ANA
MOVED C158 TO PP3300_PD_ANA

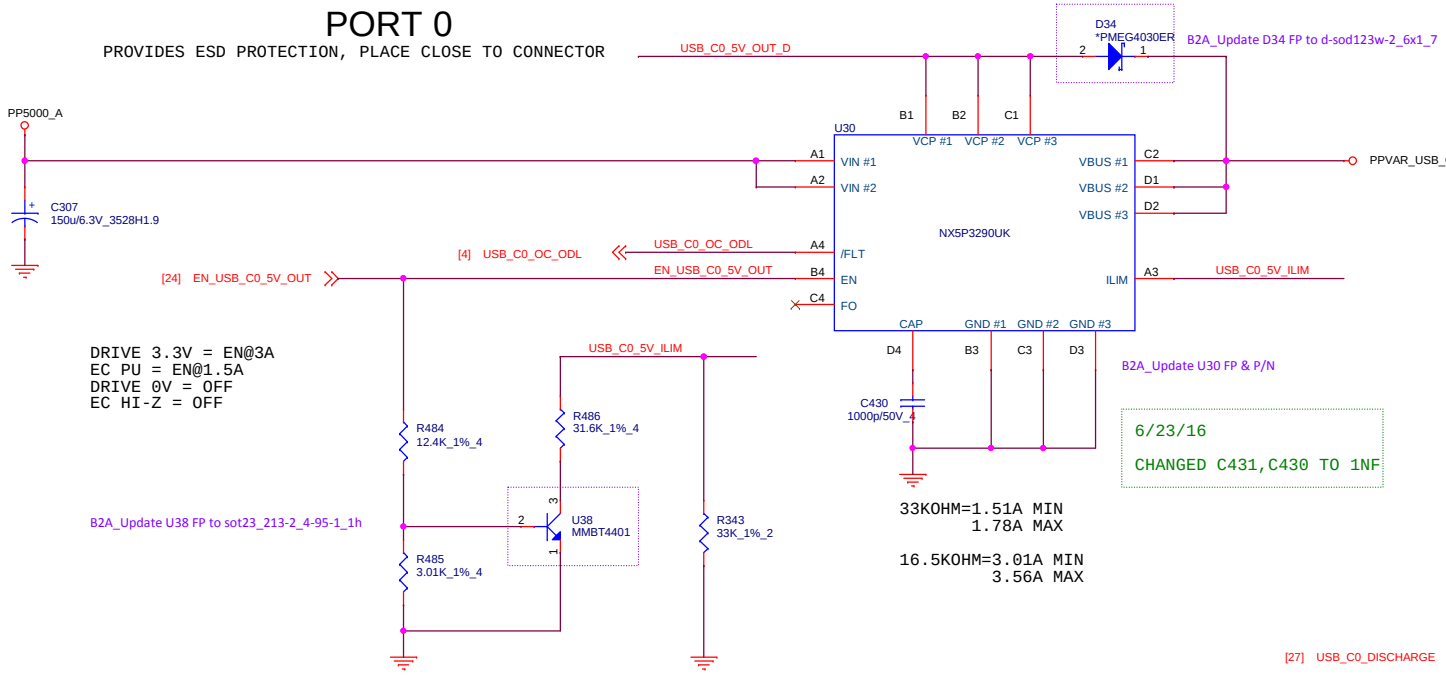
8/15/16
FLOATED TEST_EN

MOTHERBOARD PORT

Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	USB C TCPC/MUX		1A
Date: Friday, July 21, 2017		Sheet 27 of 38	

PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



DRIVE 3.3V = EN@3A
EC PU = EN@1.5A
DRIVE 0V = OFF
EC HI-Z = OFF

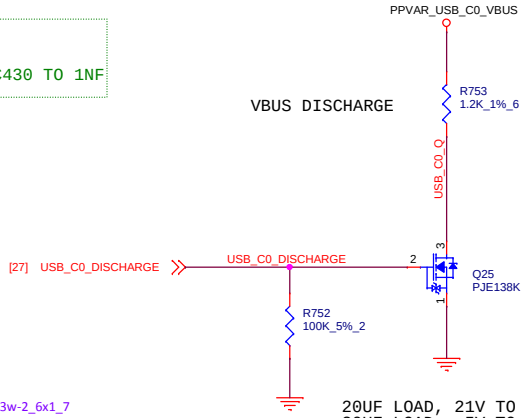
33KOHM=1.51A MIN
1.78A MAX

16.5KOHM=3.01A MIN
3.56A MAX

6/23/16

CHANGED C431,C430 TO 1NF

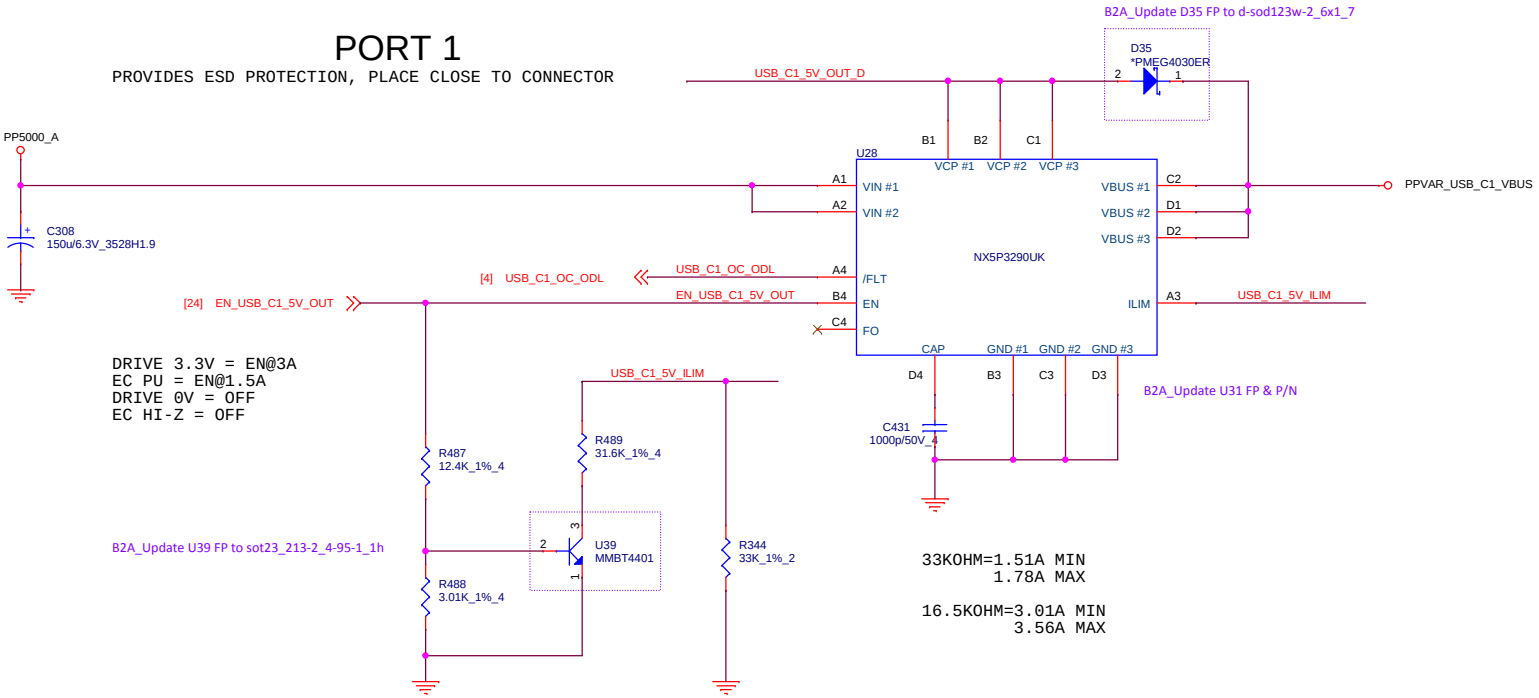
VBUS DISCHARGE



20UF LOAD, 21V TO <0.8V IN <80MS
20UF LOAD, 5V TO <0.8V IN <45MS
0402 CAN DISSIPATE 400MW FOR 80MS
0603 CAN DISSIPATE 400MW FOR 500MS
0805 CAN DISSIPATE 400MW FOR 2000MS

PORT 1

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR



DRIVE 3.3V = EN@3A
EC PU = EN@1.5A
DRIVE 0V = OFF
EC HI-Z = OFF

33KOHM=1.51A MIN
1.78A MAX

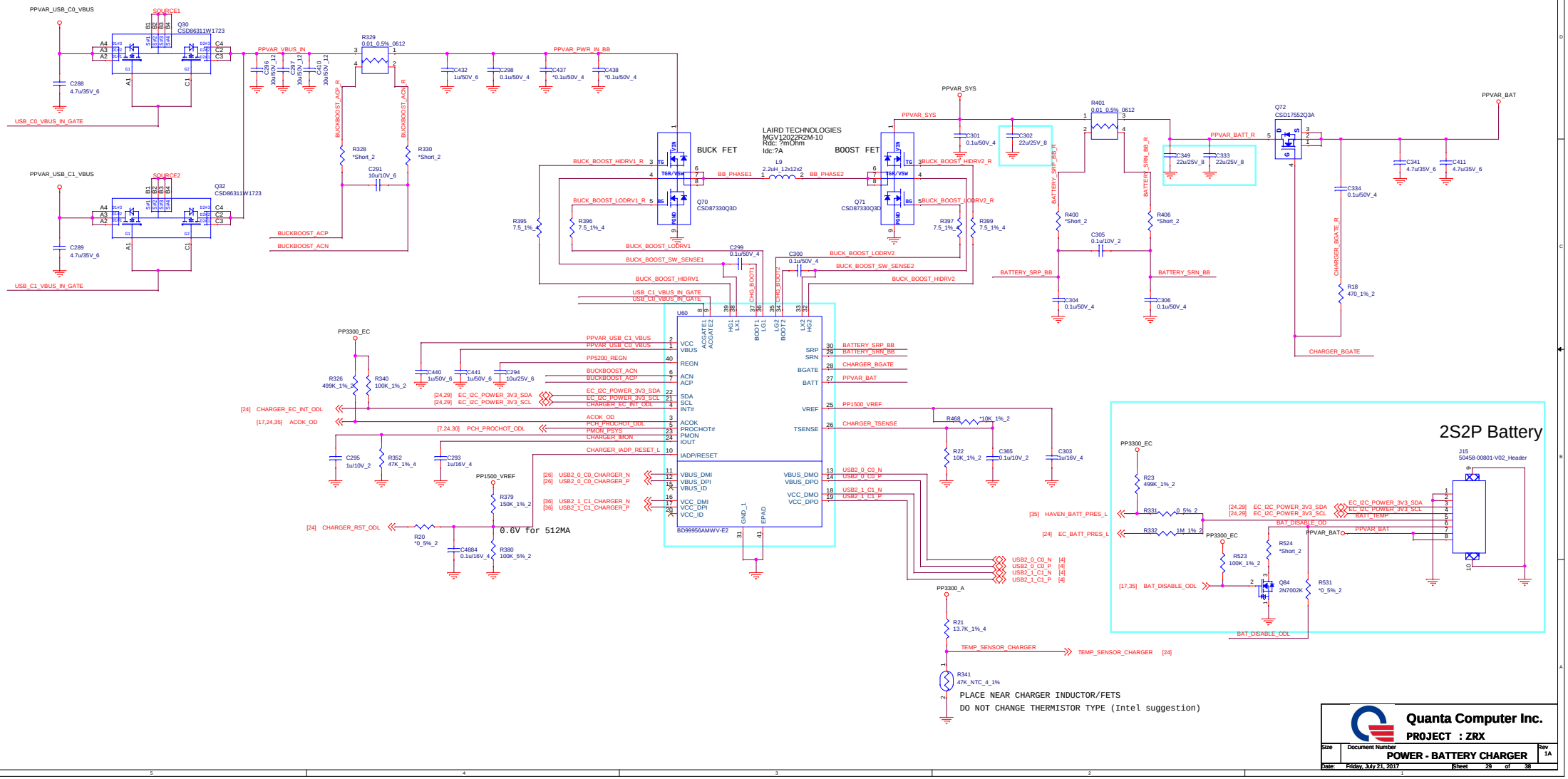
16.5KOHM=3.01A MIN
3.56A MAX

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	USB C 5V OUT	1A
Date: Friday, July 21, 2017	Sheet 28 of 38	

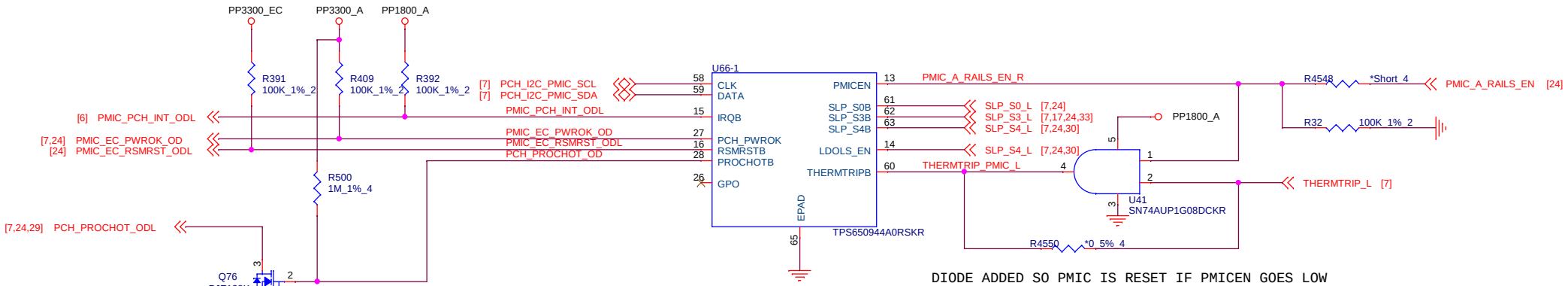
POWER - BATTERY CHARGER

ROHM BUCK-BOOST CHARGER

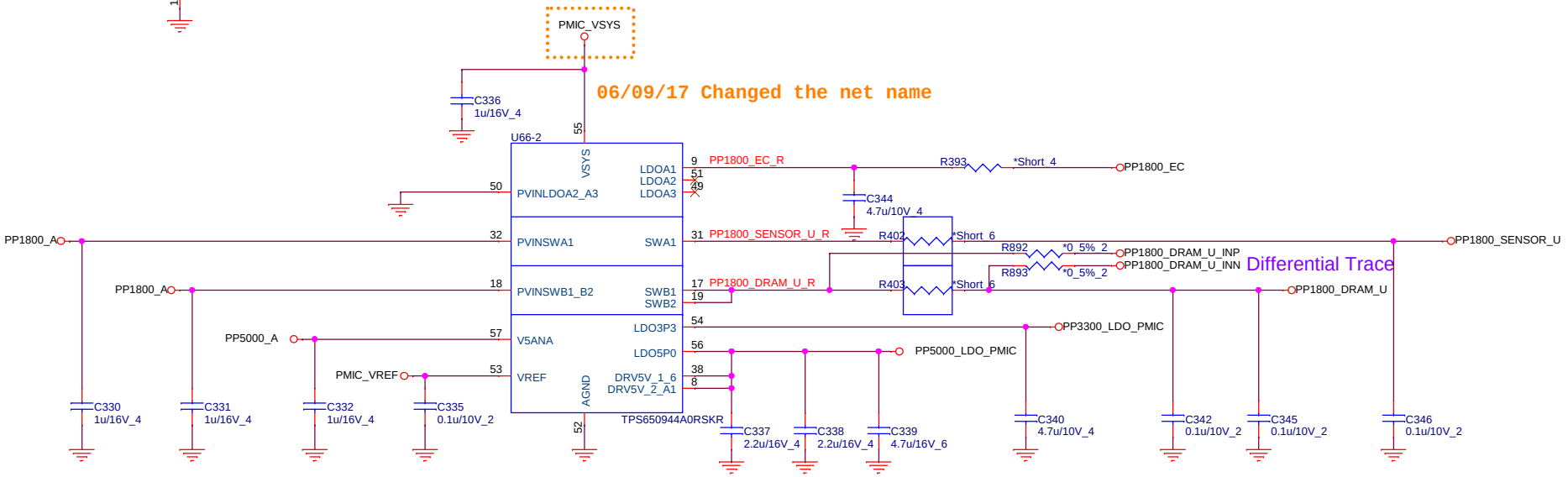


Quanta Computer Inc.		
PROJECT : ZRX		
Size	Document Number: POWER - BATTERY CHARGER	Rev: 1A
Date: Friday, July 21, 2017	Sheet 29 of 38	

POWER - PMIC LOGIC



DIODE ADDED SO PMIC IS RESET IF PMICEN GOES LOW

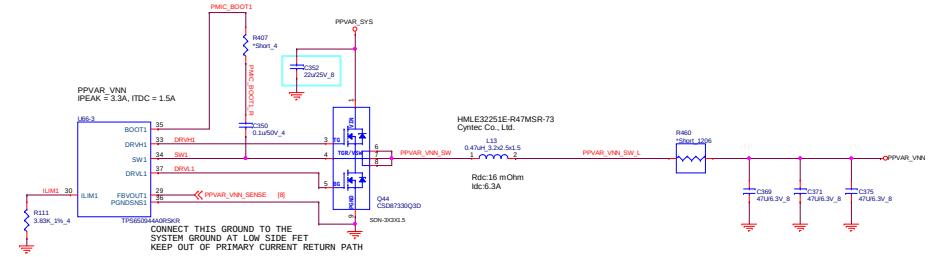


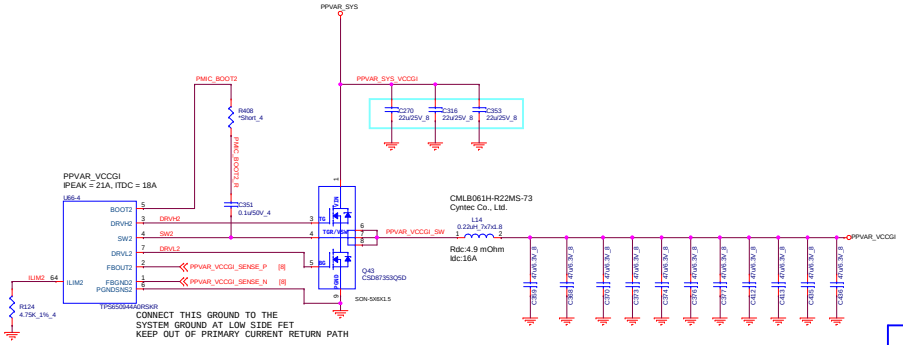
4.7UF ON LDO5P0
2.2UF ON DRV5V5_1_6
2.2UF ON DRV5V_2_A1

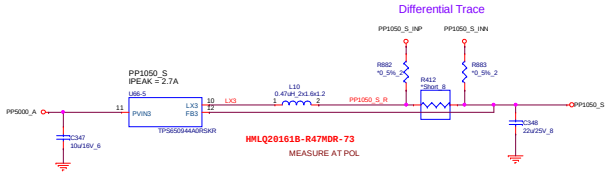
Quanta Computer Inc.
PROJECT : ZRX

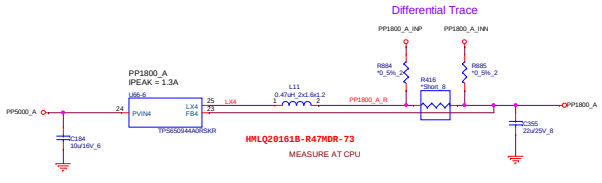
Size	Document Number	Rev
	POWER - PMIC LOGIC	1A
Date: Friday, July 21, 2017	Sheet 30 of 38	

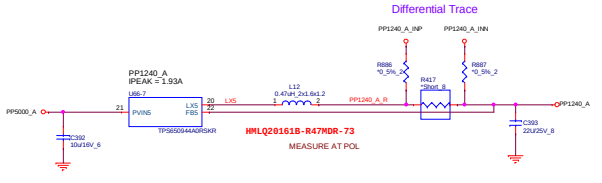
POWER - PMIC RAILS

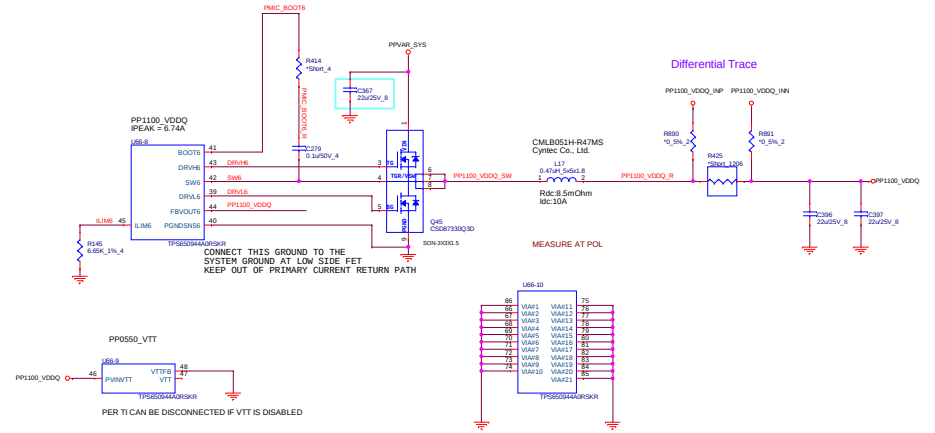




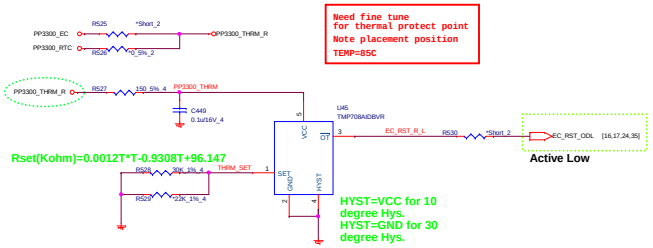






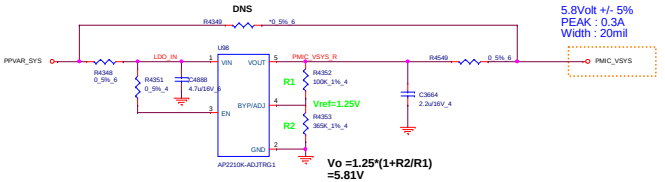


Thermal Protector



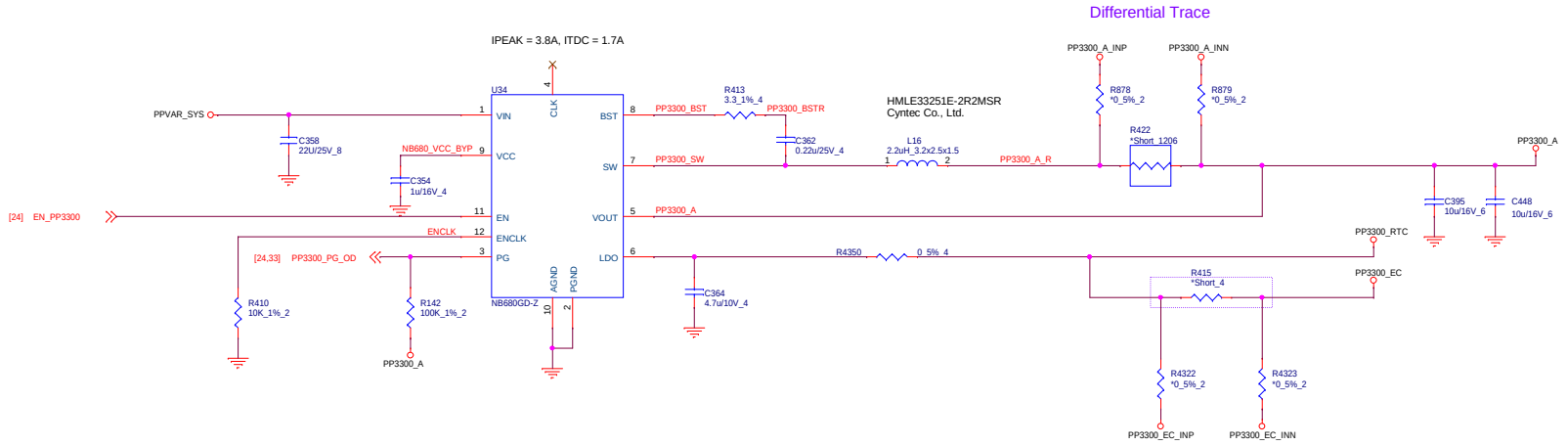
PMIC_VSYS

06/09/17 Add AP2210

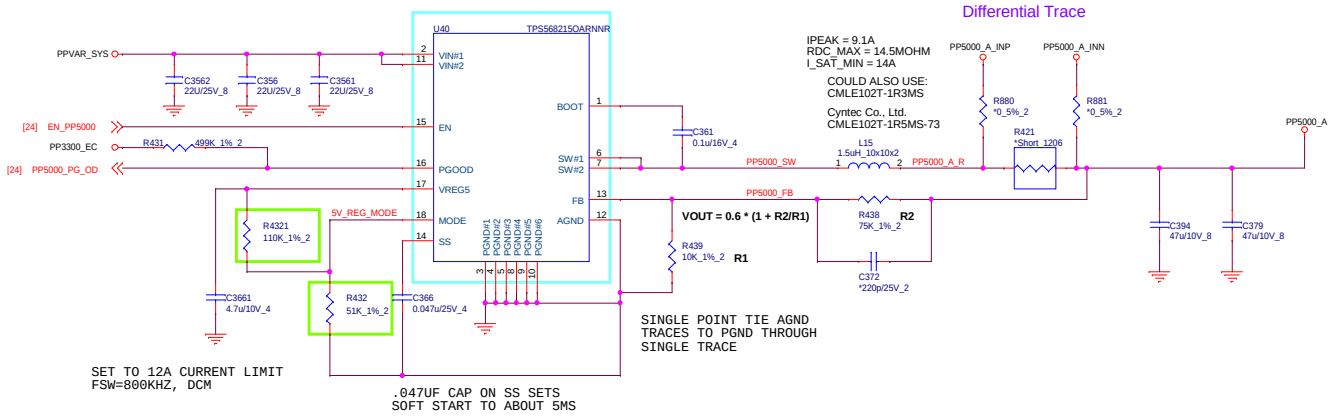


Quanta Computer Inc.
PROJECT : ZRX
Size | Document Number | Rev 1A
POWER - PMIC RAILS
Date: Friday, July 21, 2017 | Sheet 31 of 38

PP3300_A



PP5000_A



7/1/16

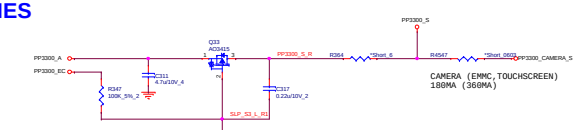
Fixed note to say "Soft start to about 5ms"

Quanta Computer Inc.

PROJECT : ZRX

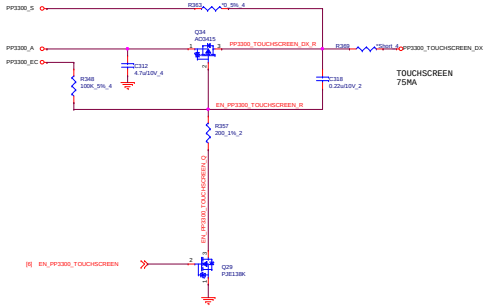
Size	Document Number	Rev
	POWER: 3.3V AND 5V	1A
Date: Friday, July 21, 2017	Sheet 32 of 38	

POWER - LOAD SWITCHES

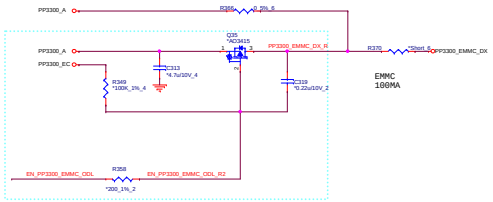


CAMERA (EMMC,TOUCHSCREEN)
180MA (360MA)

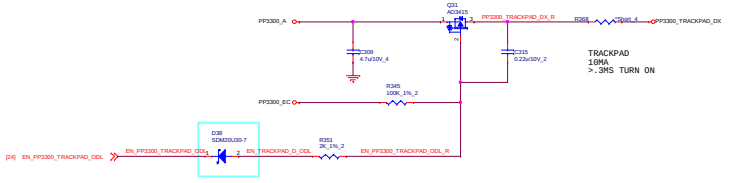
TRY TO REMOVE LOAD SWITCH



TOUCHSCREEN
75MA

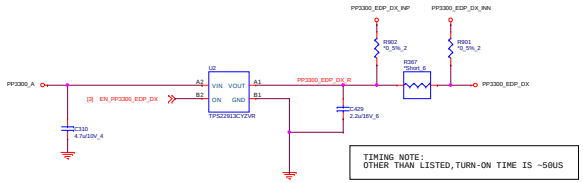


EMMC
100MA



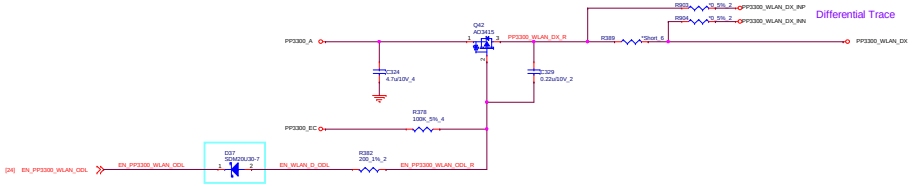
TRACKPAD
10MA
>.3MS TURN ON

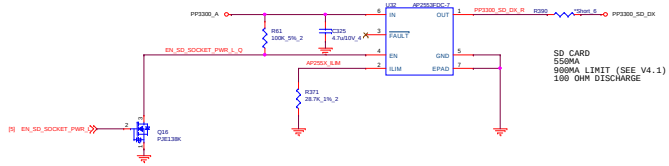
Differential Trace



TIMING NOTE:
OTHER THAN LISTED,TURN-ON TIME IS ~50US

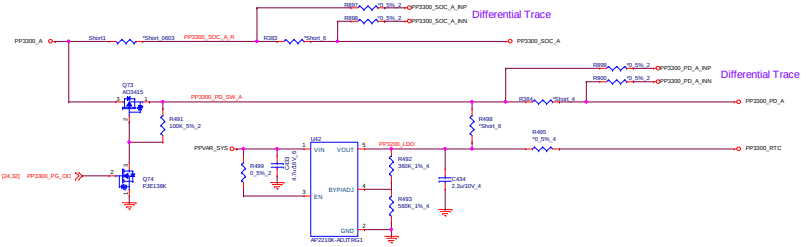
Differential Trace

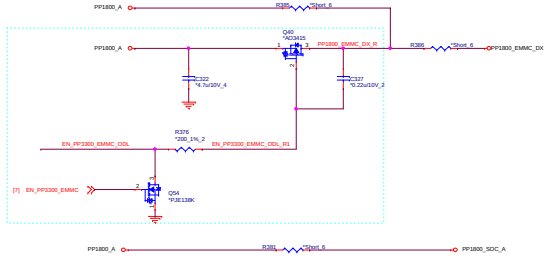


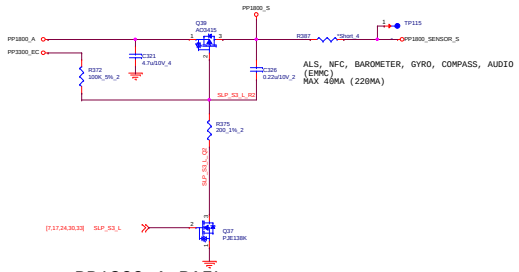


SD CARD
550MA
500MA LIMIT (SEE V4.1)
100 OHM DISCHARGE

Differential Trace







ALS, NFC, BAROMETER, GYRO, COMPASS, AUDIO (EMMC)
MAX 40MA (220MA)

PP1800_A RAIL

NFC

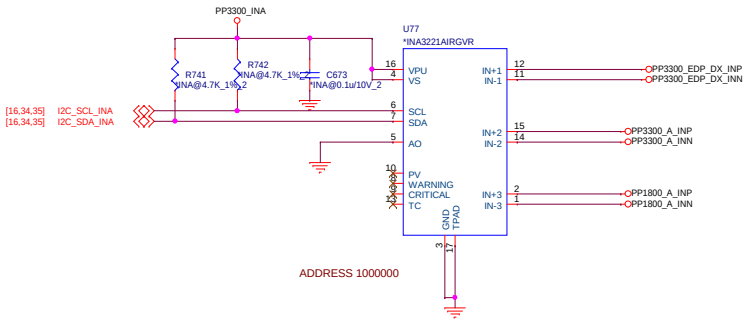
Remove This Function

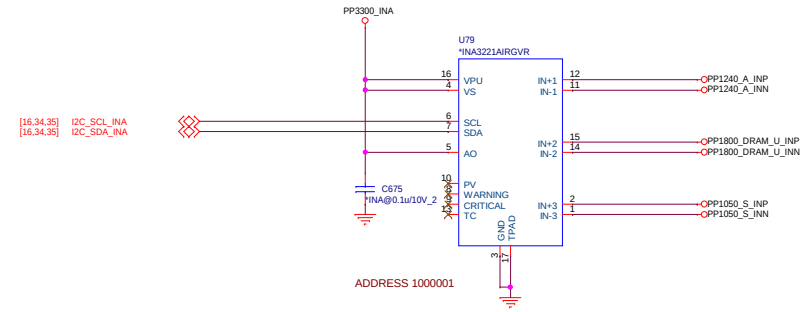
PP5000_A RAIL

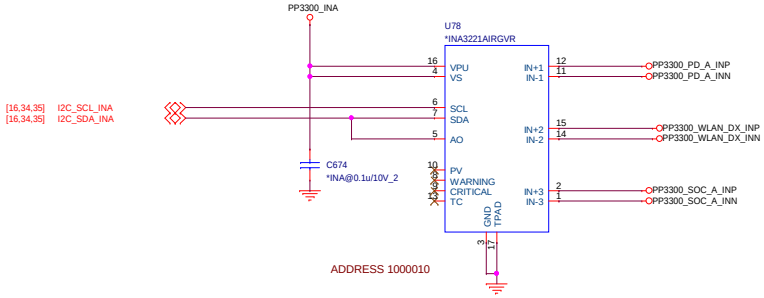
Quanta Computer Inc.
PROJECT : ZRX

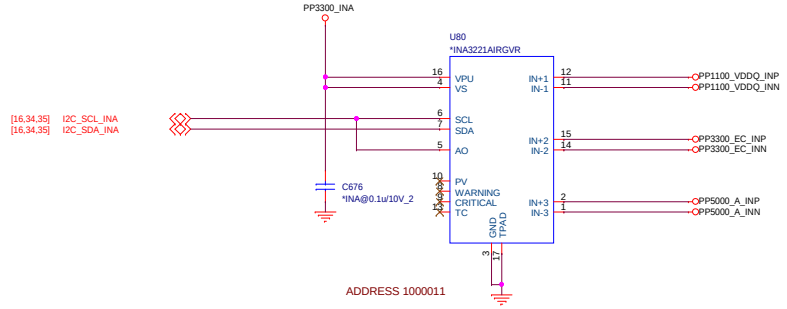
Size	Document Number	Rev
	POWER - LOAD SWITCHES	1A
Date: Friday, July 21, 2017	Sheet 38 of 38	

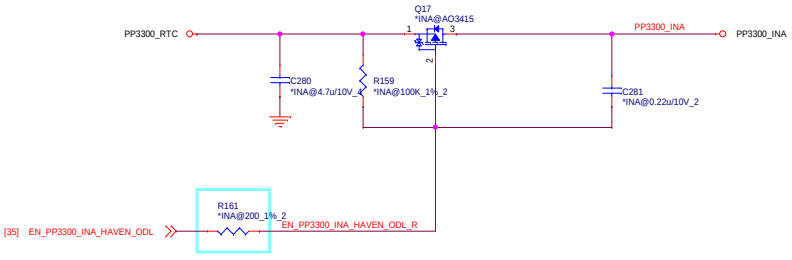
INAs



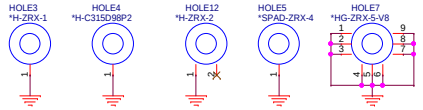


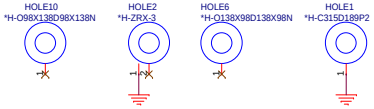


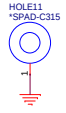


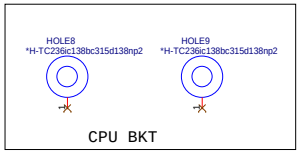


HOLES





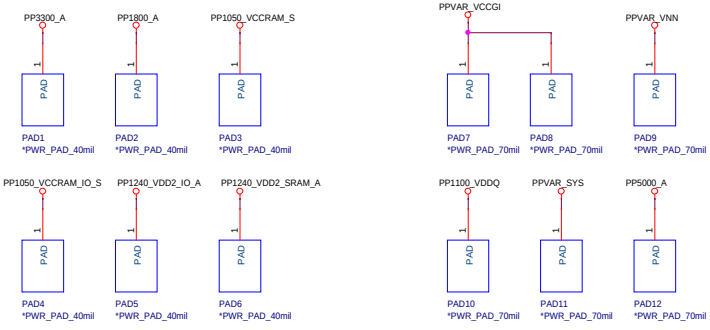




POWER TEST PAD

6/6/16
Remove solder mask on PAD 1 - PAD12

6/29/16
Add solder mask on PAD 1 - PAD12



Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	INAs	1A
Date: Friday, July 21, 2017	Sheet 34 of 38	

Locate with TPM(Page 21)

8/9/16

CHANGED DIOM3 TO PLT_RST_L
STUFFED R501
MADE R867 = 1K
REPLACED R877 WITH TP84

7/12/16

R501 DNS

6/30/16

ADDED R501

6/30/16

MADE R440, R441, R442,
R447, R448, R449 TO 0OHM

8/11/16

ADDED U43, C445
ADDED R502, Q78

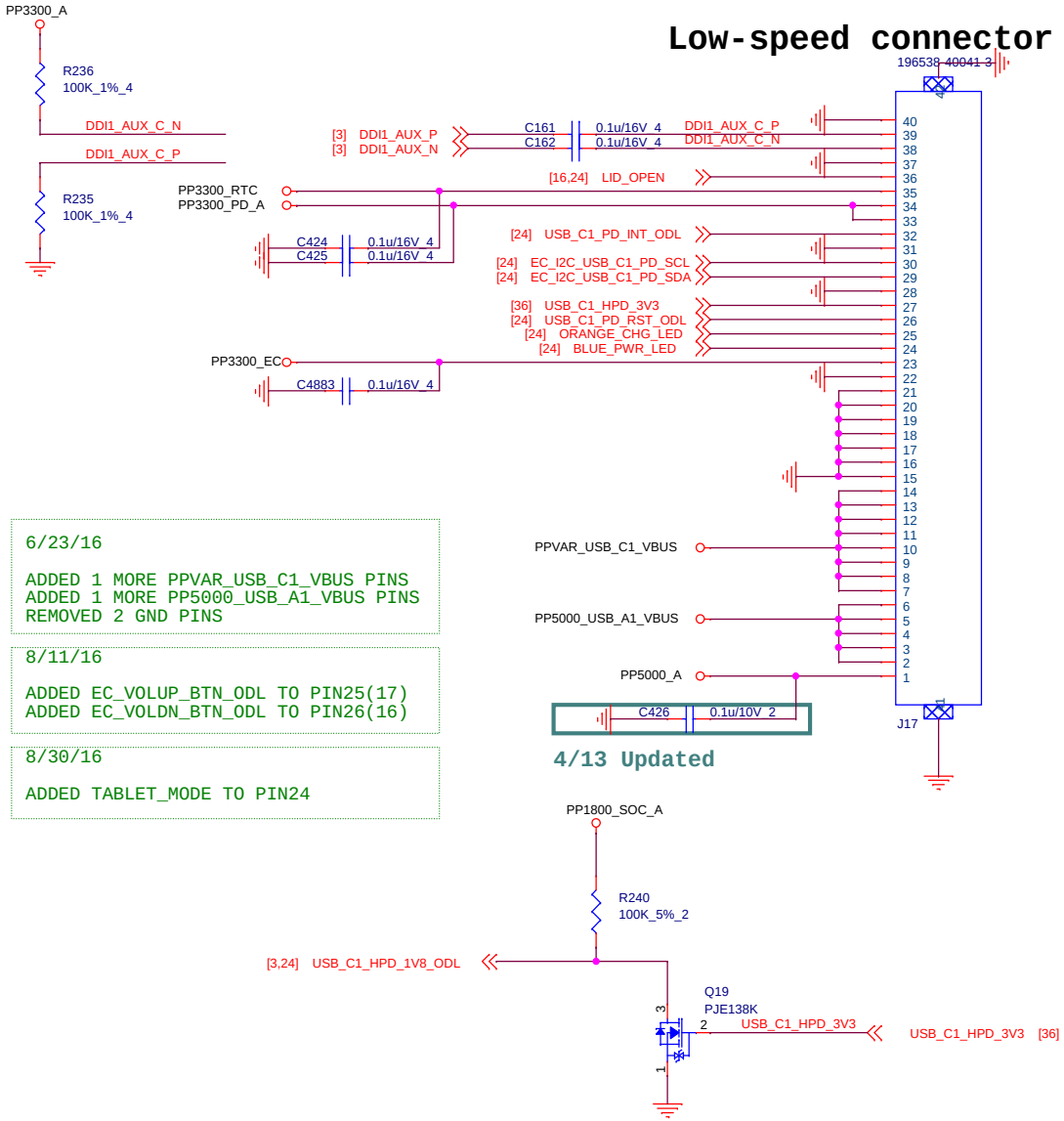
REMOVED Q63, Q28, Q50, Q64, Q36, Q51
Q48, Q52, Q49, Q53, R440, R447
R441, R448, R442, R449

ADDED R503, R504, R505, R506
ADDED HAVEN_USBA_N/P NETS

8/23/16
ADDED GND PAD TO U43

Quanta Computer Inc.			
PROJECT : ZRX			
Size	Document Number		Rev
	H1 SECURE MICROCONTROLLER		1A
Date: Friday, July 21, 2017		Sheet 35 of 38	

Low-speed connector



6/23/16

ADDED 1 MORE PPVAR_USB_C1_VBUS PINS
ADDED 1 MORE PP5000_USB_A1_VBUS PINS
REMOVED 2 GND PINS

8/11/16

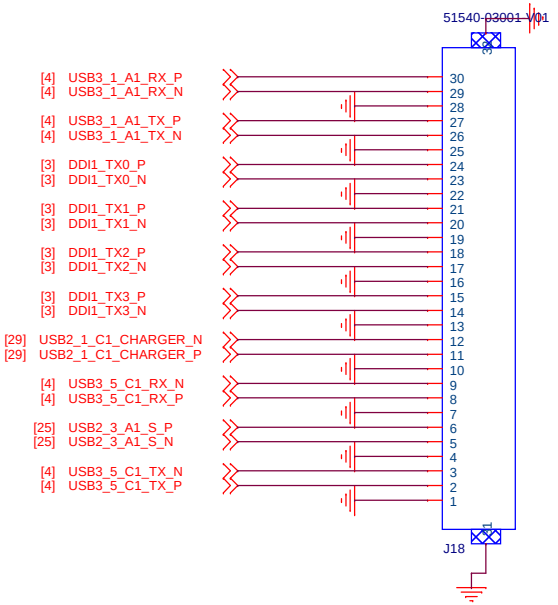
ADDED EC_VOLUP_BTN_ODL TO PIN25(17)
ADDED EC_VOLDN_BTN_ODL TO PIN26(16)

8/30/16

ADDED TABLET_MODE TO PIN24

4/13 Updated

High-speed connector



Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	MLB CONNECTORS	1A
Date: Friday, July 21, 2017	Sheet 36 of 38	

Model	Version	CHANGE LIST
ZRX	B	2017/3/7 page 20 Change U18 U19 P/N to SN1702001RTER page 23 Change J6 footprint to ngff-nase0-s6701-tsh4-ke-smt 2017/3/9 page 24 Change R37 from 5.11K ohm to 11.8K ohm for Build 2 page 31 Change R528 to 30Kohm for thermal protect when temp is 76.3C page 20 Change U18 U19 P/N to SLGC55545VTR page 36 Change J18 P/N form DFFC30FR181 to DFFC30FR172
	C	2017/4/6 page 29 DNI R20 , Add C4884 0.1uF Cap to GND on CHARGER_IADP_RESET_L page 06 Changed R38 and R39 pull-up value to 1K 2017/4/11 page 24 Add EOSD/ESD solution (R4539 33ohm and C194 180pF) on EC_TPD_EN Change EC_TS_EN from EC_GPIO83 to EC_GPIO00 Add EOSD/ESD solution (R4542 33ohm and C4887 180pF) on LID_OPEN page 21 Change EC_TS_EN from J19 Pin23 to J19 Pin8 , Add EOSD/ESD solution (R4540 33ohm and C4885 180pF) on EC_TS_EN Add EOSD/ESD solution (R4541 33ohm and C4886 180pF) on EDP_HPD_3V3 Add pull High Registor (R4543 100k ohm) on TOUCHSCREEN_EN_3V3_OD page 20 Add ESD solution (D41) on MECH_PWR_BTN_IN_ODL page 24 Change R37 to 20.5K (BUILD 3) 2017/4/12 page 24 Add EOSD/ESD solution (R459 2.2ohm and R4544 2.2ohm) on Embed Controller Power (U12.M13/U12.N1 and U12.C13/U12.H13 page 07 change Q79,Q81,Q82 P/N to PJA3413 2017/5/04 page 21 DNI R4543 2017/5/11 page 20 DNI SW3 (Hardware power Key) 2017/5/15 Change 0-ohm to short pad page 04 R12,R13,R14,R15 page 05 R281 page 08 R461,R462,R463,R464 page 14 R77,R78,R79,R80,R84,R85,R86,R87 page 15 R180~R187,R174,R200 page 19 R96,R43,R44,R48,R49,R110,R102,R103,R104,R105,R28,R108,R305,R109 page 20 R4535,R4536,R4537 page 21 R4521,R4524 page 24 R146 page 25 R254,R255 page 29 R328,R330,R400,R406,R524 page 31 R407,R408,R414,R525,R530 page 33 R498 page 35 R813,R818 ~ R823,R826,R827,R828,R841,R842,R847 ~ R853,R855,R856,R334 ~ R338,R450 ~ R452,R503,R504,R873,R874,R876,R859 ~ R866,R869~R872 2017/5/17 Change milli-ohm to short pad page 30 R393/0.51ohm 2017/5/18 DNI INAs Function page 16 Q68,Q69,Q75,C442,C443 page 30 R892,R893 page 31 R882,R883,R884,R885,R886,R887,R890,R891 page 32 R878,R879,R880,R881,R4322,R4323 page 33 R897,R898,R899,R900,R901,R902,R903,R904 Change milli-ohm to short pad page 30 R402/0.02ohm,R403/0.02ohm page 31 R460/0.002,R412/0.01,R416/0.02,R417/0.02,R425/0.002 page 32 R422/0.002,R415/0.51,R421/0.002 page 33 R364/0.02,R367/0.02,R368/0.1,R369/0.1,R370/0.02,R381/0.02,R383/0.02,R384/0.1,R386/0.02,R387/0.1,R389/0.02,R390/0.02 2017/5/24 ADD PMIC Power Issue Debug page 30 Add R4548, R4348 0 ohm resistor and change R393 to 0 ohm. page 31 Add R4350 0 ohm resistor. 2017/6/02 page 25 Change U18,U19 P/N to TI-SN1702001RTER 2017/6/12 page 30 Change the net name at 55 pin of PMIC to PMIC_VSYS. page 31 Add U98 group for PMIC issue in PMIC_VSYS
	Ramp	2017/6/15 page 30 Add R4550 bypass to avoid U41 Logic unit

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	CHANGE LIST	1A

Date: Friday, July 21, 2017 Sheet 37 of 38

Model	Version	CHANGE LIST
ZRX	C Ramp	2017/6/19 page 6 Add R4538 on GP_15 for S3 issue. It can using TP to wake up on S3 2017/6/19 Change 0-ohm to short pad page 30 R4548 ,R393 page 33 R385 2017/7/28 page 30 DNI J1, R519 ,U44 ; Remove SERVO Function

Quanta Computer Inc.
PROJECT : ZRX

Size	Document Number	Rev
	CHANGE LIST	1A
Date: Monday, July 31, 2017	Sheet 38 of 38	