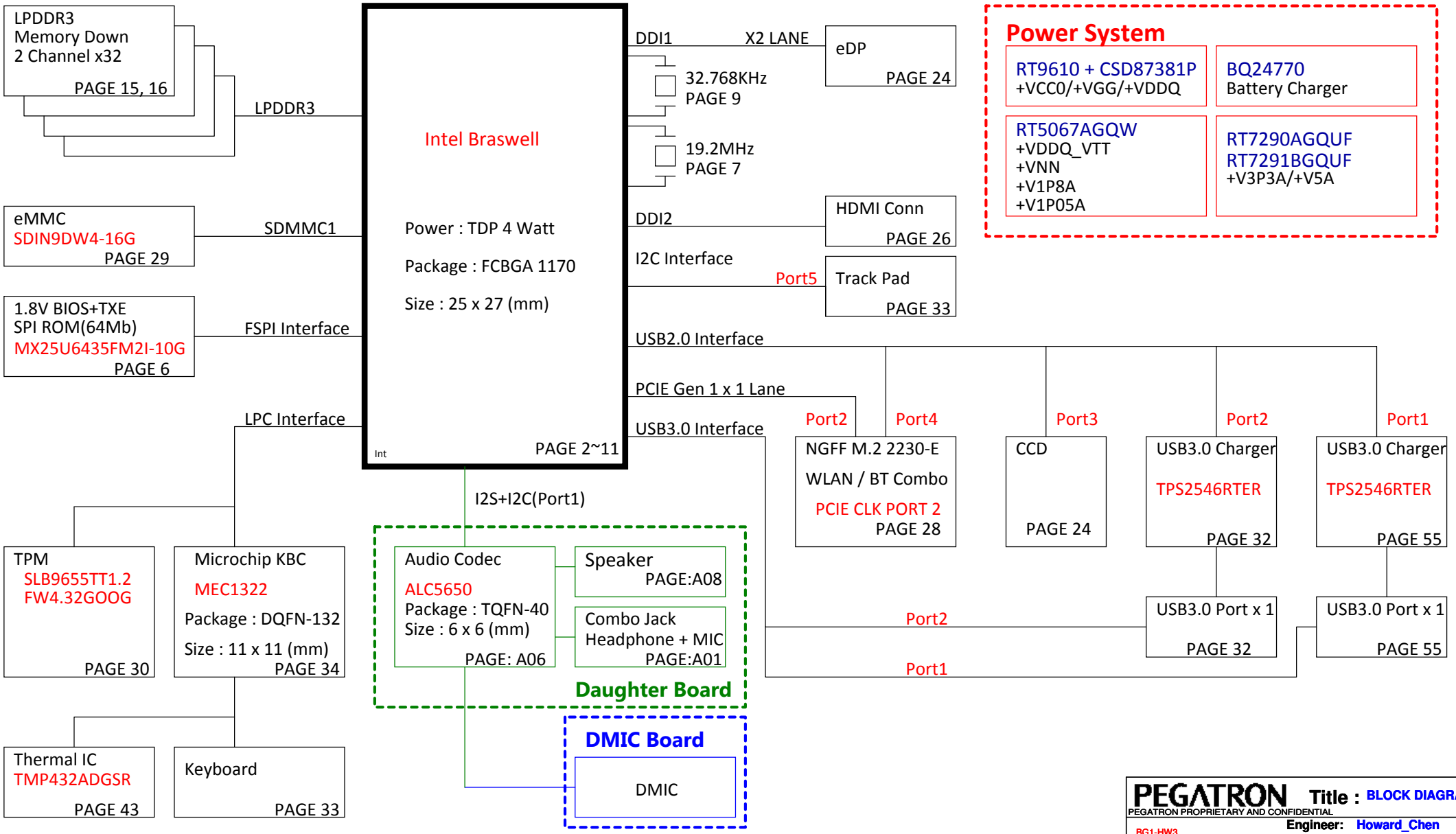
Intel Braswell Platform Block Diagram



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Title : BLOCK DIAGRAM

BG1-HW3

Engineer: Howard_Chen

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 1 of 68

Braswell
GPIO

CFIO Name	Use As	Signal Name	Internal Pull-up/down	External Pull-up/down	Power
GP_CAMERASB00	Native	XDP	20K PD		1.8VA
GP_CAMERASB01	Native	XDP	20K PD		1.8VA
GP_CAMERASB10		NC	20K PD		1.8VA
GP_CAMERASB11	Native	HW SETTING	20K PD		1.8VA
GP_CAMERASB02	Native	XDP	20K PD		1.8VA
GP_CAMERASB03	Native	XDP	20K PD		1.8VA
GP_CAMERASB04	Native	XDP	20K PD		1.8VA
GP_CAMERASB05	Native	XDP	20K PD		1.8VA
GP_CAMERASB06	Native	XDP	20K PD		1.8VA
GP_CAMERASB07	Native	XDP	20K PD		1.8VA
GP_CAMERASB08	Native	XDP	20K PD		1.8VA
GP_CAMERASB09	Native	HW SETTING	20K PD		1.8VA
HV_DDI0_HPD	Native	USB_C	20K PD		1.8VA
HV_DDI0_DDC_SCL		NC	20K PU		1.8VA
HV_DDI0_DDC_SDA		NC	20K PU		1.8VA
PANEL0_BKLTCTL		NC	0		1.8VA
PANEL0_BKLTEN		NC	0		1.8VA
PANEL0_VDDEN		NC	0		1.8VA
HV_DDI1_HPD	Native	EDP_HPD_L	20K PD		1.8VA
PANEL1_BKLTCTL	Native	EDP_BKLTCTL	0		1.8VA
PANEL1_BKLTEN	Native	EDP_BKLTEN	0		1.8VA
PANEL1_VDDEN	Native	EDP_VDDEN	0		1.8VA
HV_DDI2_HPD	Native	INT_HDMI_HPD	20K PD		1.8VA
HV_DDI2_DDC_SCL	Native	HDMI_DDCCLK_SW	20K PU		1.8VA
HV_DDI2_DDC_SDA	Native	HDMI_DDCDATA_SW	20K PU		1.8VA
SDMMC1_CLK	Native	EMMC_CLK	0(20K PD)		1.8VA
SDMMC1_CMD	Native	EMMC_CMD	Z(20K PU)		1.8VA
SDMMC1_D0	Native	EMMC_D0	Z(20K PU)		1.8VA
SDMMC1_D1	Native	EMMC_D1	Z(20K PU)		1.8VA
SDMMC1_D2	Native	EMMC_D2	Z(20K PU)		1.8VA
SDMMC1_D3_CD_N	Native	EMMC_D3	Z(20K PU)		1.8VA
MMC1_D4_SD_WE	Native	EMMC_D4	Z(20K PU)		1.8VA
SDMMC1_D5	Native	EMMC_D5	Z(20K PU)		1.8VA
SDMMC1_D6	Native	EMMC_D6	Z(20K PU)		1.8VA
SDMMC1_D7	Native	EMMC_D7	Z(20K PU)		1.8VA
SDMMC1_RCLK	Native	EMMC_RCLK_R	Z(20K PD)		1.8VA
FST_SPI_CLK	Native	FAST_SPI_CLK	OUTPUT*		1.8VA
FST_SPI_CS0_N	Native	FAST_SPI_CS0	OUTPUT*		1.8VA
FST_SPI_CS1_N		NC	OUTPUT*		1.8VA
FST_SPI_CS2_N	GPO	LTE_DISABLE#	OUTPUT*		1.8VA
FST_SPI_D0	Native	FAST_SPI_D0	20K PU		1.8VA
FST_SPI_D1	Native	FAST_SPI_D1	20K PU		1.8VA
FST_SPI_D2		NC	20K PU		1.8VA
FST_SPI_D3		NC	20K PU		1.8VA
GPIO_DFX0	Native	XDP	20K PD		1.8VA
GPIO_DFX1	Native	XDP	20K PD		1.8VA
GPIO_DFX2	Native	XDP	20K PD		1.8VA
GPIO_DFX3	Native	XDP	20K PD		1.8VA
GPIO_DFX4	Native	XDP	20K PD		1.8VA
GPIO_DFX5	Native	XDP	20K PU		1.8VA
GPIO_DFX6	Native	XDP	20K PU		1.8VA
GPIO_DFX7	Native	XDP	20K PU		1.8VA
GPIO_DFX8	Native	XDP	20K PU		1.8VA
GPIO_SUS0	Native	HW SETTING	20K PD		1.8VA
GPIO_SUS1	Native	HW SETTING	20K PD		1.8VA
GPIO_SUS2	Native	HW SETTING	20K PU		1.8VA
GPIO_SUS3	Native	HW SETTING	20K PD		1.8VA
GPIO_SUS4	Native	HW SETTING	20K PU		1.8VA
GPIO_SUS5	Native	HW SETTING	20K PU		1.8VA
GPIO_SUS6	Native	HW SETTING	20K PU		1.8VA
GPIO_SUS7	Native	HW SETTING	20K PU		1.8VA
SEC_GPIO_SUS8	Native	HW SETTING	20K PU		1.8VA
SEC_GPIO_SUS9	Native	HW SETTING	20K PD		1.8VA
SEC_GPIO_SUS10	Native	HW SETTING	20K PD		1.8VA
SEC_GPIO_SUS11	GPI	SIM_DET_C	0(20K PD)		1.8VA
MF_HDA_CLK		NC	0(20K PD)		1.8VA/1.5VA
MF_HDA_DOCKEN_N	GPI	MIC_PRESENT_L_SOC	20K PD		1.8VA/1.5VA
MF_HDA_DOCKRST_N	GPO	AUDIO_SWITCH_INT_N	0(20K PD)		1.8VA/1.5VA
MF_HDA_RST_N		NC	20K PD		1.8VA/1.5VA
MF_HDA_SDI0		NC	20K PD		1.8VA/1.5VA
MF_HDA_SDI1		NC	20K PD		1.8VA/1.5VA
MF_HDA_SDO		NC	20K PD		1.8VA/1.5VA
MF_HDA_SYNC		NC	20K PD		1.8VA/1.5VA
UART1_CTS_N		NC	20K PU		1.8VA
UART1_RTS_N		NC	1(20K PU)		1.8VA
UART1_RXD	Native	SOC_UART_RX	20K PU		1.8VA
UART1_TXD	Native	SOC_UART_TX	1(20K PU)		1.8VA
UART2_CTS_N		NC	20K PU		1.8VA
UART2_RTS_N		NC	1(20K PU)		1.8VA
UART2_RXD		NC	20K PU		1.8VA
UART2_TXD		NC	1(20K PU)		1.8VA
GPIO_ALERT	Native	AJACK_PRESENT_SOC	0(20K PU)*		1.8VA
I2C0_SCL	Native	I2C_0_SCL	Z(1K PU,OD)		1.8VA
I2C0_SDA	Native	I2C_0_SDA	Z(1K PU,OD)		1.8VA
I2C1_SCL	Native	I2C_1_SCL	Z(20K PU,OD)		1.8VA
I2C1_SDA	Native	I2C_1_SDA	Z(20K PU,OD)		1.8VA
I2C2_SCL	Native	I2C_NFC_SCL	Z(20K PU,OD)		1.8VA
I2C2_SDA	Native	I2C_NFC_SDA	Z(20K PU,OD)		1.8VA
I2C3_SCL	GPI	RAM_ID1	Z(20K PU,OD)		1.8VA
I2C3_SDA	GPI	RAM_ID3	Z(20K PU,OD)		1.8VA
I2C4_SCL		NC	Z(20K PU,OD)		1.8VA
I2C4_SDA		NC	Z(20K PU,OD)		1.8VA
I2C5_SCL	Native	I2C_5_SCL	Z(20K PU,OD)		1.8VA
I2C5_SDA	Native	I2C_5_SDA	Z(20K PU,OD)		1.8VA

CFIO Name	Use As	Signal Name	Internal Pull-up/down	External Pull-up/down	Power
I2C6_SCL	Native	I2C_6_SCL	Z(20K PU,OD)		1.8VA
I2C6_SDA	Native	I2C_6_SDA	Z(20K PU,OD)		1.8VA
MF_ISH_GPIO_0		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_1		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_2		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_3		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_4	GPI	PCH_SPI_WP_D	Z(20K PU)*		1.8VA
MF_ISH_GPIO_5		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_6		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_7		NC	Z(20K PU)*		1.8VA
MF_ISH_GPIO_8		NC	Z(20K PU,OD)		1.8VA
MF_ISH_GPIO_9		NC	Z(20K PU,OD)		1.8VA
MF_ISH_I2C1_SDA		NC	Z(20K PU,OD)		1.8VA
MF_ISH_I2C1_SCL		NC	Z(20K PU,OD)		1.8VA
CX_PRDY_N	Native	XDP	Z(5K PU,OD)		1.8VA
CX_PREQ_N	Native	XDP	5K PU,OD		1.8VA
TCK	Native	XDP	5K PD		1.8VA
TDI	Native	XDP	5K PU		1.8VA
TDO	Native	XDP	Z		1.8VA
TMS	Native	XDP	5K PU		1.8VA
TRST_N	Native	XDP	5K PU		1.8VA
ILB_SERIRQ	Native	ILB_SERIRQ	20K PU		1.8VA
MF_LPC_CLKOUT0	Native	CLK_PCI_EC_SOC	SLP*		3.3VA/1.8VA
MF_LPC_CLKOUT1		NC	20K PD		3.3VA/1.8VA
MF_LPC_AD0	Native	LPC_AD0	20K PU		3.3VA/1.8VA
MF_LPC_AD1	Native	LPC_AD1	20K PU		3.3VA/1.8VA
MF_LPC_AD2	Native	LPC_AD2	20K PU		3.3VA/1.8VA
MF_LPC_AD3	Native	LPC_AD3	20K PU		3.3VA/1.8VA
LPC_CLKRUN_N	Native	LPC_CLKRUN_L	20K PU		3.3VA/1.8VA
LPC_FRAME_N	Native	LPC_LFRAME#	1(20K PU)		3.3VA/1.8VA
GP_SSP_2_CLK	Native	I2S_BCLK_R	20K PD		1.8VA
GP_SSP_2_FS	Native	I2S_LRCLK_R	20K PD		1.8VA
GP_SSP_2_RXD	Native	I2S_DIN_R	20K PD		1.8VA
GP_SSP_2_TXD	Native	I2S_DOUT_R	0(20K PD)		1.8VA
PCIE_CLKREQ0_N	Native	PCIE_CLKREQ_IMAGE#	20K PU		1.8VA
PCIE_CLKREQ1_N	Native	LTE_WAKE#	20K PU		1.8VA
PCIE_CLKREQ2_N	Native	PCIE_CLKREQ_WLAN#	20K PU		1.8VA
PCIE_CLKREQ3_N	Native	AUDIO_CODEC_IRQ	20K PU		1.8VA
MF_PLT_CLK0	Native	I2S_MCLK_R	CLK(20K PD)		1.8VA
MF_PLT_CLK1	GPI	RAM_ID2	CLK(20K PD)		1.8VA
MF_PLT_CLK2		NC	CLK(20K PD)		1.8VA
MF_PLT_CLK3		NC	CLK(20K PD)		1.8VA
MF_PLT_CLK4		NC	CLK(20K PD)		1.8VA
MF_PLT_CLK5		NC	CLK(20K PD)		1.8VA
PMU_AC_PRESENT	Native	ACPRESENT	20K PD		1.8VA
PMU_BATLOW_N	Native	PMC_BATLOW#	20K PU		1.8VA
PMU_PLTRST_N	Native	SOC_PLTRST#	1(20K PU)*		1.8VA
PMU_PWRBTN_N	Native	SOC_PWRBTN#	20K PU		1.8VA
PMU_RESETBUTTON_N	Native	SOC_REST_BTN#	20K PU		1.8VA
PMU_SLP_LAN_N		NC	0*		1.8VA
PMU_SLP_S0IX_N	Native	SLP_S0IX#	1*		1.8VA
PMU_SLP_S3_N	Native	SLP_S3#	1*		1.8VA
PMU_SLP_S4_N	Native	SLP_S4#	1*		1.8VA
PMU_SUSCLK	Native	PMC_SUSCLK0	CLK		1.8VA
PMU_WAKE_N	Native	PCH_WAKE_L	20K PU		1.8VA
PMU_WAKE_LAN_N		NC	20K PU		1.8VA
SUS_STAT_N	Native	PMC_SUS_STAT#	1*		1.8VA
SUSPWRDNACK	Native	PMC_SUSPWRDNACK	0(20K PD)		1.8VA
PWM0		NC	0(20K PD)		1.8VA
PWM1		NC	0(20K PD)		1.8VA
SATA_GP0	GPO	WIFI_DISABLE#	20K PD		1.8VA
SATA_GP1	GPI	TS_INT1#	20K PD		1.8VA
SATA_GP2	Native	SATA_DEVSLP_C	0(20K PD)		1.8VA
SATA_GP3	GPI	RAM_ID0	0(20K PD)		1.8VA
SATA_LEDN	GPI	EC_IN_RW_Q	PRG*		1.8VA
SDMMC3_1P8_EN	Native	SDMMC3_1P8_EN	0(20K PD)		1.8VA
SDMMC3_CD_N	Native	SD3_CD#	20K PU		1.8VA
SDMMC3_CLK	Native	SD3_CLK	0(20K PD)		3.3VA/1.8VA
SDMMC3_CMD	Native	SD3_CMD	Z(20K PU)		3.3VA/1.8VA
SDMMC3_D0	Native	SD3_D0	Z(20K PU)		3.3VA/1.8VA
SDMMC3_D1	Native	SD3_D1	Z(20K PU)		3.3VA/1.8VA
SDMMC3_D2	Native	SD3_D2	Z(20K PU)		3.3VA/1.8VA
SDMMC3_D3	Native	SD3_D3	Z(20K PU)		3.3VA/1.8VA
SDMMC3_PWR_EN_N	Native	SDMMC3_PWR_EN_N	1*		1.8VA
SDMMC2_CLK		NC	0(20K PD)		1.8VA
SDMMC2_CMD		NC	Z(20K PU)		1.8VA
SDMMC2_D0		NC	Z(20K PU)		1.8VA
SDMMC2_D1		NC	Z(20K PU)		1.8VA
SDMMC2_D2		NC	Z(20K PU)		1.8VA
SDMMC2_D3_CD_N		NC	Z(20K PU)		1.8VA
MF_SMB_ALERT_N		NC	20K PU		1.8VA
MF_SMB_CLK	Native	SMB_SOC_CLK	20K PU		1.8VA
MF_SMB_DATA	Native	SMB_SOC_DATA	20K PU		1.8VA
SPKR		NC	PRG		1.8VA
SPI1_CLK	Native	SOC_SPI_CLK	0*		1.8VA
SPI1_CS0_N	Native	SOC_SPI_CS#	1		1.8VA
SPI1_CS1_N		NC	1		1.8VA
SPI1_MISO	Native	SOC_SPI_MISO	20K PU*		1.8VA
SPI1_MOSI	Native	SOC_SPI_MOSI	0*		1.8VA
SVID0_ALERT_N	Native	SVID_ALERT#			1.8VA
SVID0_CLK	Native	SVID_CLK			1.8VA
SVID0_DATA	Native	SVID_DATA			1.8VA
USB_OC0_N	Native	USB_OC0#	20K PU		1.8VA
USB_OC1_N	Native	USB_OC1#	20K PU		1.8VA

EC
MEC1322

EC GPIO	Signal Name
GP112	LPC_LAD0
GP114	LPC_LAD1
GP113	LPC_LAD2
GP111	LPC_LAD3
GP117	CLK_PCI_EC
GP120	LPC_LFRAME#
GP116	PLTRST#
GP014	LPC_CLKRUN_L
GP125	KB_COL00
GP126	KB_COL01
GP144	KB_COL02
GP032	KB_COL03
GP142	KB_COL04
GP040	KB_COL05
GP042	KB_COL06
GP043	KB_COL07
GP000	EC_JTAG_TCK
GP100	EC_JTAG_TMS
GP101	EC_JTAG_TDO
GP102	EC_JTAG_TDI
GP103	KB_ROW00
GP104	KB_ROW01
GP001	KB_ROW02
GP002	KB_ROW03
GP003	KB_ROW04
GP106	KB_ROW05
GP004	KB_ROW06
GP107	KB_ROW07
GP005	KB_ROW08
GP006	KB_ROW09
GP007	KB_ROW10
GP010	KB_ROW11
GP011	KB_ROW12
GP012	USBPD_BOOT0_EC (TP)
GP115	IRQ_SERIRQ
GP044	EC_SMI_3P3_L
GP026	EC_SOC_WAKE_SCI_N
GP121	VCC1_RST#
GP131	EC_RST#
GP143	PCH_RSMRST_L
GP063	RSMRST_N_PWRGD
GP162	EC_UART0_RX
GP165	EC_UART0_TX
GP046	DP_USB_C_HPD_Q (TP)
GP047	USB_PD_EC_INT (TP)
GP050	OTG_SW_EN (TP)
GP065	DELAY_ALL_SYS_PWRGD
GP051	PCH_SUS_STAT_L
GP052	EC_ACDET_CTRL (TP)
GP053	TRACKPAD_PWREN
GP152	EC_KBD_IRQ#
GP127	WAKE_INT (TP)
GP130	ALL_SYS_PWRGD
GP132	EC_PLUG_DETECT
GP133	EC_PWM0
GP135	USBPD_MCU_RST (TP)
GP136	EC_PWM1
GP140	THERMAL_PROBE_EN_L
GP141	EC_PWM3
GP145	EC_KBD_ALERT
GP147	ALS_INT# (TP)

EC GPIO	Signal Name
GP013	USB_ILIM_SEL
GP027	LID_OPEN_OUT1_R
GP030	EC_ACIN
GP031	VOLUME_UP (TP)
GP033	EC_SPI_WP_ME#
GP034	VOLUME_DOWN (TP)
GP035	SMC_ONOFF_N
GP036	USB2_PWR_EN
GP041	EC_ENTERING_RW
GP045	USB_OC1_L
GP056	EC_TEMP_SENSOR_1
GP057	EC_TEMP_SENSOR_2
GP060	BC_PMON
GP061	EC_ADC0
GP062	EC_TEMP_SENSOR_3
GP066	PCH_WAKE_EC_L
GP105	USB_CTL1
GP110	EC_REST_L
GP067	USB3_PWR_EN
GP055	USB_OC0_L
GP210	SUSPWRDNACK_SOC_EC
GP211	PCH_SLP_SX_L
GP200	PCH_SLP_S4_L
GP015	SMB_BC_CLK
GP016	SMB_BC_DATA
GP134	BOARD_ID1
GP017	BOARD_ID2
GP022	EC_SENSOR_I2C1_SCL (TP)
GP023	EC_SENSOR_I2C1_SDA (TP)
GP020	EC_I2C_USBPD_SCL_R (TP)
GP021	EC_I2C_USBPD_SDA_R (TP)
GP025	SMB_THRM_DATA
GP024	SMB_THRM_CLK
GP151	PROCHOT_EC
GP154	BOARD_ID0
GP155	EC_PERICOM_INT (TP)
GP156	PWR_BTN_SELECT
GP157	PCH_SUSPWRDNACK
GP160	PCH_PWRBTN_L
GP161	GYRO_INT1 (TP)
GP163	VP9_CODEC_RESET#
GP206	PCH_SLP_S3_L
GP123	EC_STRAP_GPIO1
GP202	EC_BL_DISABLE_L
GP201	STARTUP_LATCH_SET
GP203	SMC_SHUTDOWN
GP204	USBPD_BST_OFF (TP)
GP054	EC_SPI_MOSI_R
GP164	EC_SPI_MISO_R
GP153	EC_SPI_CLK_R
GP146	EC_SPI_CS#_R
GP064	EC_HIB_L
GP124	EC_VNN_ALERT_N (TP)
GP122	EC_VNN_VCLK (TP)
GP150	WLAN_OFF_L

PCIE Port Assignment

Port#	
PCIE 0~1	VIDEO CODEC
PCIE 2	WLAN

USB Port Assignment

Port#	
USB 0	Reserved
USB 1	External port (DB)
USB 2	External port (MB)
USB 3	Camera
USB 4	WIFI/BT module
USB3 Port 2	External port (MB)

I2C Port Assignment

Port#	
I2C 0	Reserved
I2C 1	Audio Codec
I2C 2	Reserved
I2C 3	Reserved
I2C 4	Reserved
I2C 5	Touch Pad
I2C 6	EC

Option Table

Optional	
@	Unmount
TS	Touch Screen part
TS@	Touch Screen reserved
GD	Google Debug
GD@	Google Debug Reserved
APS	Intel PWR debug Part
XDP	Intel Debug Conn Part
XDP@	Intel Debug Conn Part Reversed
LTE	LTE Sku part
LTE_@	LTE Sku reserved
Non_LTE	Non LTE Sku part
EMI	EMI part
EMI@	EMI part Reserved
S0IX	S0IX support part
S0IX@	S0IX support reserved
MEMCH0	MEM Channel 0 Part
MEMCH1	MEM Channel 1 Part

2015/08/24
Update Option table

Item	Optional	A Build Define
1	@	nustuff
2	XDP	
3	N/A	
4	GD	
5	GD@	nustuff
6	MEMCH0	
7	MEMCH0_@	nustuff
8	MEMCH1	
9	MEMCH1_@	nustuff
10	HDMI_ALS	nustuff
11	HDMI_PLS	

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Title: System Setting
Engineer: Howard_Chen
Size: B | Project Name: Sanance | Rev: 1.1
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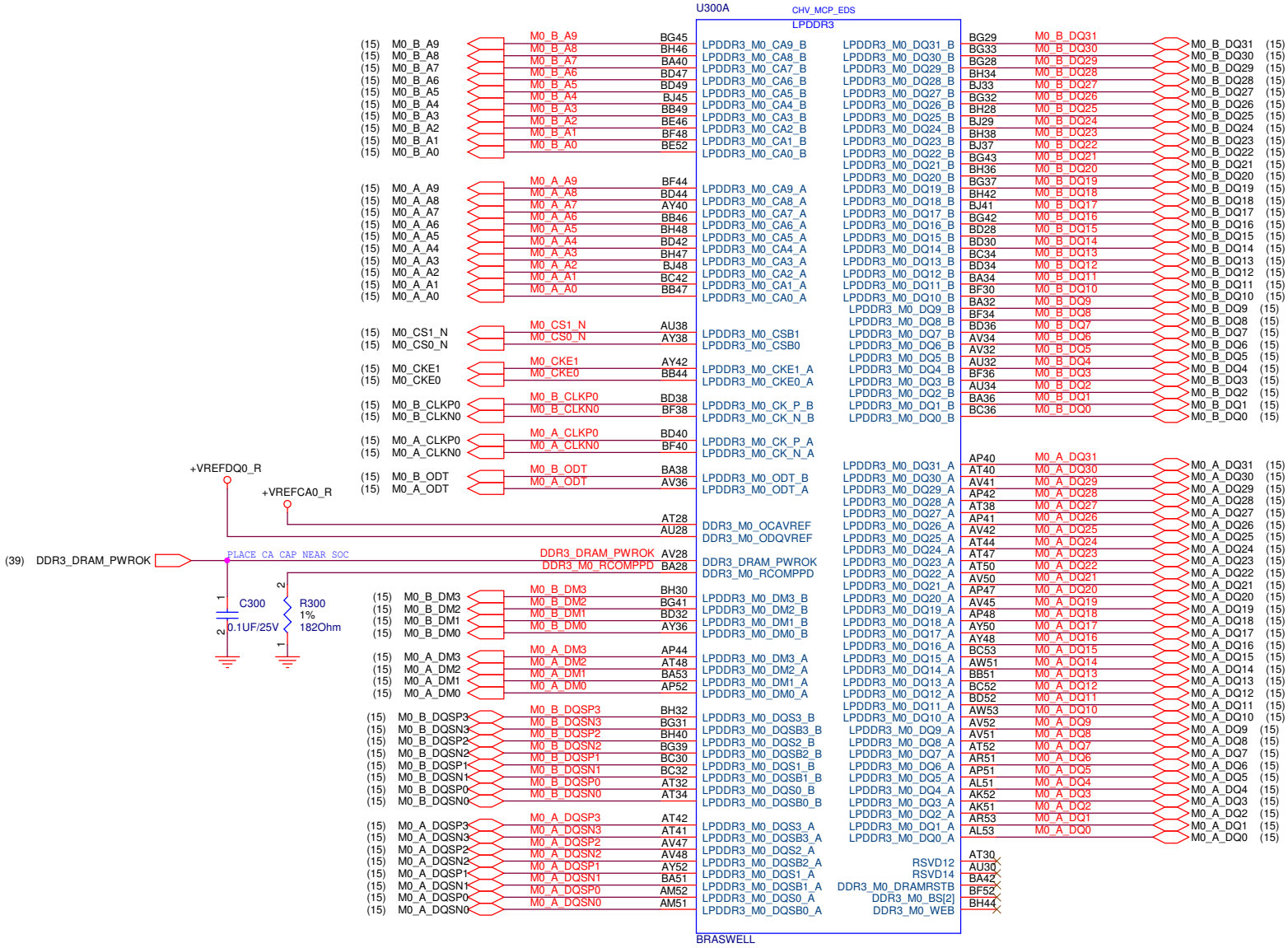


PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

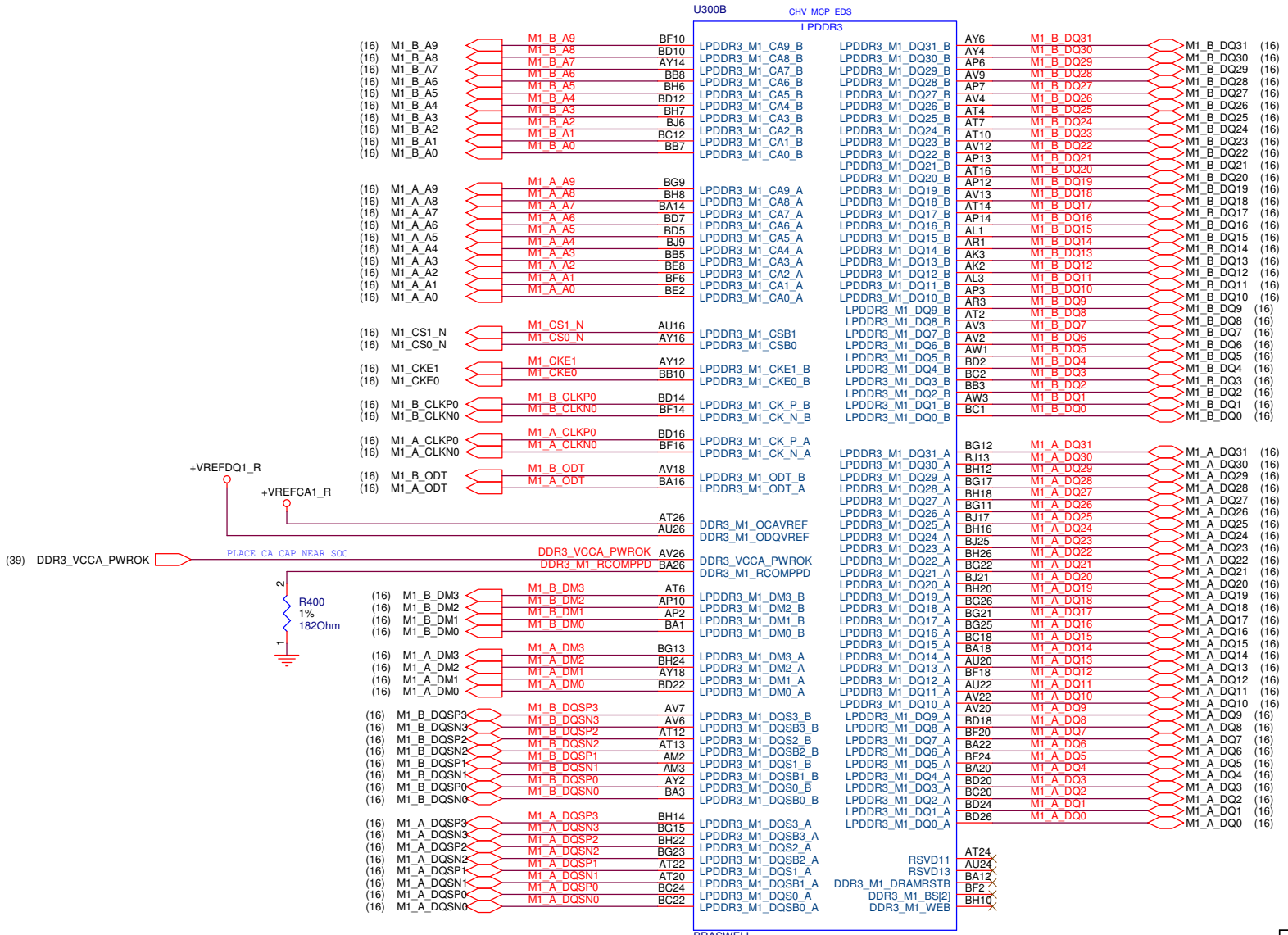
Title : CPU(1)_MEM_LPDDR3_C

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 3 of 68



PEGATRON	Title : CPU(2)_MEM_LPDDR3_CHB
PEGATRON PROPRIETARY AND CONFIDENTIAL	
BG1-HW3	Engineer: Howard_Chen
Size: B	Project Name: Sanance
Rev: 1.1	
Date: Friday, February 19, 2016	Sheet 4 of 68

DISPLAY, XDP, EMMC, SD

DISPLAY MAPPING	
DDI0	DP - type C
DDI1	eDP
DDI2	HDMI

SD MAPPING	
SDMMC1	EMMC
SDMMC2	NC
SDMMC3	SD card

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DISPLAY, XDP, EMMC, SD

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
C	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 5 of 68

SATA MAPPING	
SATA0	NC
SATA1	SSD

PCIe MAPPING	
PCIE0	Video Codec
PCIE1	Video Codec
PCIE2	WLAN
PCIE3	NC

CHV_MCP_EDS U300D

SATA_TXP0 C31
SATA_TXN0 B30
SATA_RXP0 N28
SATA_RXN0 M28
SATA_TXP1 C29
SATA_TXN1 A29
SATA_RXP1 J28
SATA_RXN1 K28
SATA_LEDN AH3
SATA_GP0 AH2
SATA_GP1 AG3
SATA_GP2 AG1
SATA_GP3/SATA_DEVSLP1 AF3
SATA_RCOMP_P N30
SATA_RCOMP_N M30
FST_SPI_CLK W3
FST_SPI_CS0_B V4
FST_SPI_CS1_B V6
FST_SPI_CS2_B V7
FST_SPI_D0 V2
FST_SPI_D1 V3
FST_SPI_D2 U1
FST_SPI_D3 U3
MF_HDA_RSTB AF13
MF_HDA_SDI1 AD6
MF_HDA_CLK AD9
MF_HDA_SDI0 AD7
MF_HDA_SYNC AF12
MF_HDA_SDO AF14
MF_HDA_DOCKENB AB9
MF_HDA_DOCKRSTB AB7
SPKR H4
GP_SSP_2_CLK AK9
GP_SSP_2_FS AK10
GP_SSP_2_TXD AK12
GP_SSP_2_RXD AK13

SATA

PCIE_TXP0 C24
PCIE_TXN0 B24
PCIE_RXP0 G20
PCIE_RXN0 J20
PCIE_TXP1 A25
PCIE_TXN1 C25
PCIE_RXP1 D20
PCIE_RXN1 F20
PCIE_TXP2 B26
PCIE_TXN2 C26
PCIE_RXP2 D22
PCIE_RXN2 F22
PCIE_TXP3 A27
PCIE_TXN3 C27
PCIE_RXP3 G24
PCIE_RXN3 J24
PCIE_CLKREQ0B AM10
PCIE_CLKREQ1B AM12
PCIE_CLKREQ2B AK14
PCIE_CLKREQ3B AM14

PCIe

CLK_DIFF_P[0] A21
CLK_DIFF_N[0] C21
CLK_DIFF_P[1] C19
CLK_DIFF_N[1] B20
CLK_DIFF_P[2] C18
CLK_DIFF_N[2] B18
CLK_DIFF_P[3] C17
CLK_DIFF_N[3] A17
CLK_DIFF_P[4] C16
CLK_DIFF_N[4] B16
PCIE_RCOMP_P D26
PCIE_RCOMP_N F26

SPI1_CLK V14
SPI1_CS0_B Y13
SPI1_CS1_B Y12
SPI1_MISO V13
SPI1_MOSI V12

SPI

BRASWELL

(46) EC_IN_RW_Q
(46) WIFI_DISABLE#
TS_INT1#
SATA_DEVSLP_C
(7) RAM_ID0
R625 1 2 402Ohm 1% SATA_RCOMP_DP SATA_RCOMP_DN

level shift to LTE
add 10k pull up to v1p8a
and change to U300.V7

LTE_DISABLE#

FAST_SPI_CLK
FAST_SPI_CS0
FAST_SPI_D0
FAST_SPI_D1

FAST SPI

MIC_PRESENT_L_SOC
AUDIO_SWITCH_INT_N

AUDIO

(31) I2S_BCLK_R
(31) I2S_LRCLK_R
(31) I2S_DOUT_R
(31) I2S_DIN_R
R634 1 2 0Ohm
I2S_LRCLK

C608 @ 10PF/50V
I2S_LRCLK_R
EMI modify 1112

PCIE_TX2_WLAN_C_DP C604 1 2 0.1UF/25V
PCIE_TX2_WLAN_C_DN C605 1 2 0.1UF/25V
PCIE_TX2_WLAN_DP (28)
PCIE_TX2_WLAN_DN (28)
PCIE_RX2_WLAN_DP (28)
PCIE_RX2_WLAN_DN (28)

PCIE_CLKREQ_IMAGE#
LTE_WAKE#
PCIE_CLKREQ_WLAN# (46)
AUDIO_CODEC_IRQ (31)

CLK_PCIE_WLANP_DP (28)
CLK_PCIE_WLANN_DN (28)

SOC_PCIE_COMP_DP 1% 402Ohm 2 1 R603
SOC_PCIE_COMN_DN

SOC_SPI_CLK 1 T600
SOC_SPI_CS# 1 T601
PMIC_IRQ_N
PMIC_IRQ_N (39)
SOC_SPI_MISO_DB_R R628 1 @ 2 0Ohm SOC_SPI_MISO 1 T603
SOC_SPI_MOSI 1 T604

+V1P8A

PCIE_CLKREQ_IMAGE# R609 1 @ 2 10KOhm
PCIE_CLKREQ_WLAN# R626 1 @ 2 10KOhm
SATA_DEVSLP_C R601 1 2 10KOhm
EC_IN_RW_Q R602 1 2 10KOhm
LTE_WAKE# R629 1 2 10KOhm
LTE_DISABLE# R630 1 2 10KOhm
TS_INT1# R631 1 2 10KOhm
MIC_PRESENT_L_SOC R632 1 2 10KOhm
AUDIO_SWITCH_INT_N R633 1 2 10KOhm

From Google debug Conn

+V1P8A_ME +V3P3A_EC
R620 100KOhm
R619 @ 100KOhm
U602
A VCC
B
GND Y
SN74AUC1G08DCKR
+V1P8A_ME
C607 0.1UF/25V

(25) GPIO_SPI_WP
R604 1 2 0Ohm R606 1 2 0Ohm
modify 0118

From Screw

(44) SPI_WP_ME
Q601 BSS138W-7-F

SPI NOR FLASH

SPI_WP_ME_ROM_Q (34)
PCH_SPI_WP_D (7)
To SoC

SOC_SPI_WP# (34)

R613 100KOhm
modify 1109

SOC_SPI_HOLD#
R615 @ 0Ohm

+V1P8A_ME
C606 0.1UF/25V

U603
VCC
WP#/SIO2
RESET#/SIO3 GND
SI/SIO0
SO/SIO1
CS#
SCLK
MX25U6435FM2I-10G

SOC_SPI_MOSI_R
SOC_SPI_MISO_R
SOC_SPI_CS#_R
SOC_SPI_CLK_R

R607 1 2 10Ohm 1% FAST_SPI_D0
R608 1 2 10Ohm 1% FAST_SPI_D1
R627 1 2 10Ohm 1% FAST_SPI_CS0
R610 1 2 10Ohm 1% FAST_SPI_CLK

R611 1 GD 2 0Ohm GD_SPI_SI_R (25)
R612 1 GD 2 0Ohm GD_SPI_SO_R (25)
R614 1 GD 2 0Ohm GD_SPI_CS0#_R (25)
R616 1 GD 2 0Ohm GD_SPI_CLK_R (25)

+V1P8A_ME
FAST_SPI_CS0 R622 1 @ 2 3.3KOhm
SOC_SPI_WP# R618 1 @ 2 3.3KOhm
SOC_SPI_HOLD# R621 1 @ 2 3.3KOhm
SOC_SPI_MOSI_R R623 1 @ 2 3.3KOhm
SOC_SPI_MISO_R R624 1 @ 2 3.3KOhm
SOC_SPI_CLK_R R617 1 @ 2 3.3KOhm

From Google debug Conn

(25) SPI_HOLD#_BIOS

Q602 BSS138W-7-F
+V1P8A_ME
+V1P8A
+V3P3A

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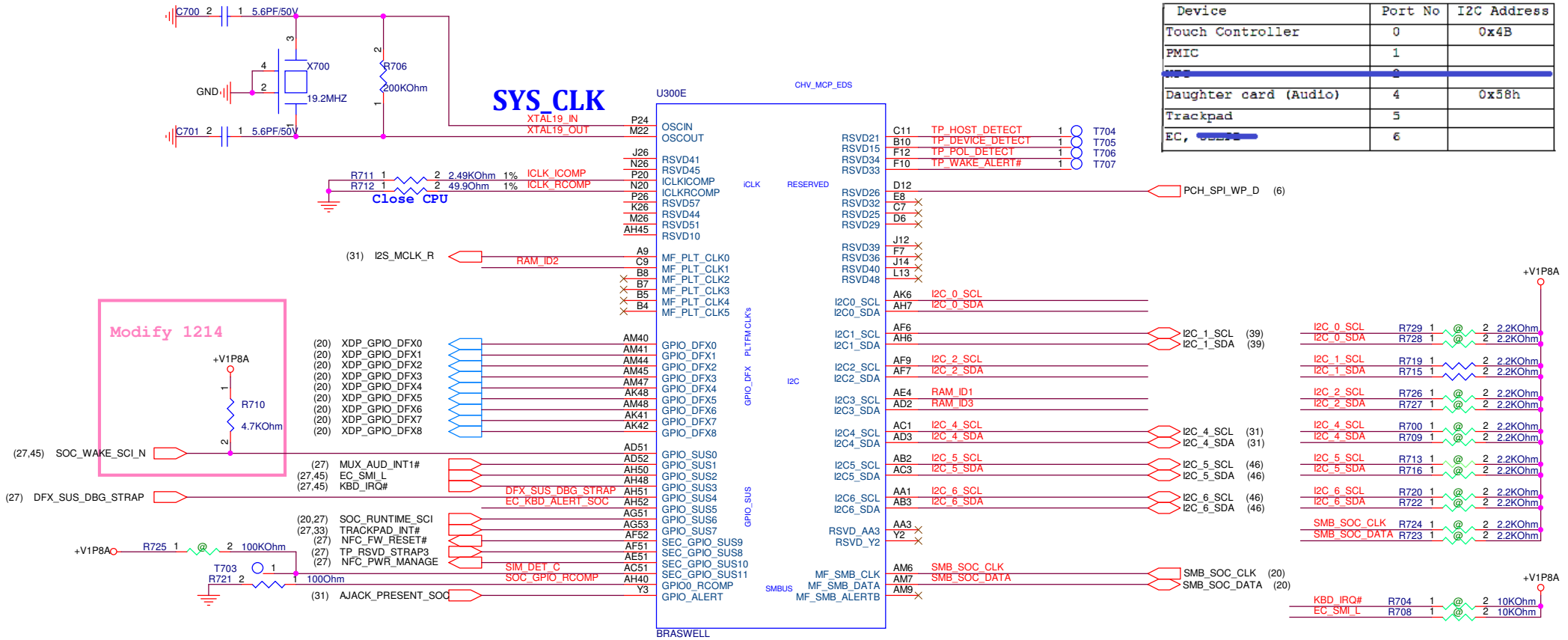
Title : CPU(4)_SATA_PCIe_SPI_
Engineer: Howard_Chen
BG1-HW3
Size B
Project Name Sanance
Rev 1.1
Date: Friday, February 19, 2016
Sheet 6 of 68

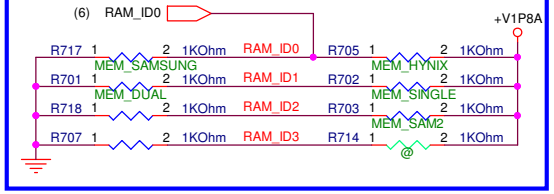
I2C PORT MAPPING

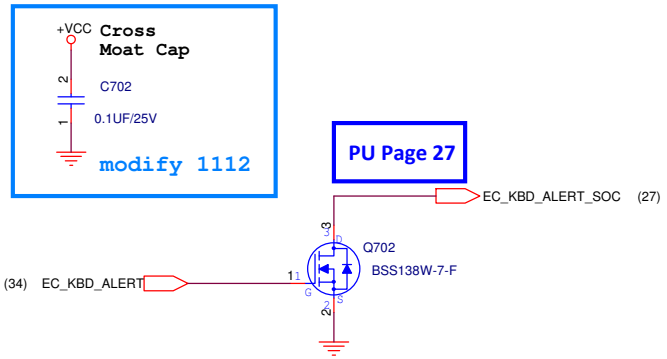
Device	Port No	I2C Address
Touch Controller	0	0x4B
PMIC	1	
[redacted]	2	
Daughter card (Audio)	4	0x58h
Trackpad	5	
EC, [redacted]	6	



RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0	VENDOR	PEGA P/N	Note
0	0	0	0	SAMSUNG/K4E8E304EE-EGCE	0315-01960PB	4pcs -> 4GB
0	0	0	1	SK HYNIX/H9CCNNN8JTBLAR-NUD	0315-01GR0PB	4pcs -> 4GB
0	0	1	0	SAMSUNG/K4E8E304EE-EGCE	0315-01960PB	2pcs -> 2GB
0	0	1	1	SK HYNIX/H9CCNNN8JTBLAR-NUD	0315-01GR0PB	2pcs -> 2GB
0	1	0	0	SAMSUNG/K4E8E324EB-EGCF	0315-01M90PB	4pcs -> 4GB
0	1	0	1			
0	1	1	0	SAMSUNG/K4E8E324EB-EGCF	0315-01M90PB	2pcs -> 2GB

RAM ID SETTING





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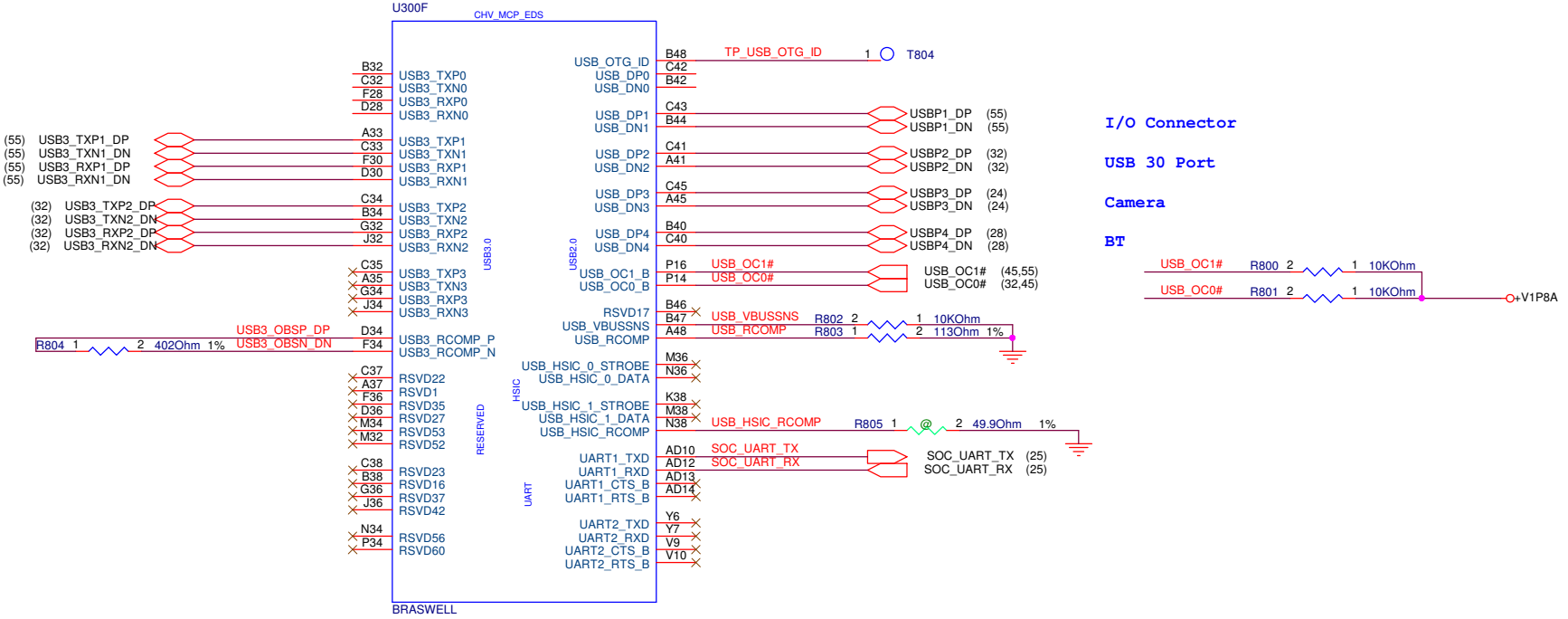
Title : CPU(5)_I2C_XDP_SM BUS

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 7 of 68



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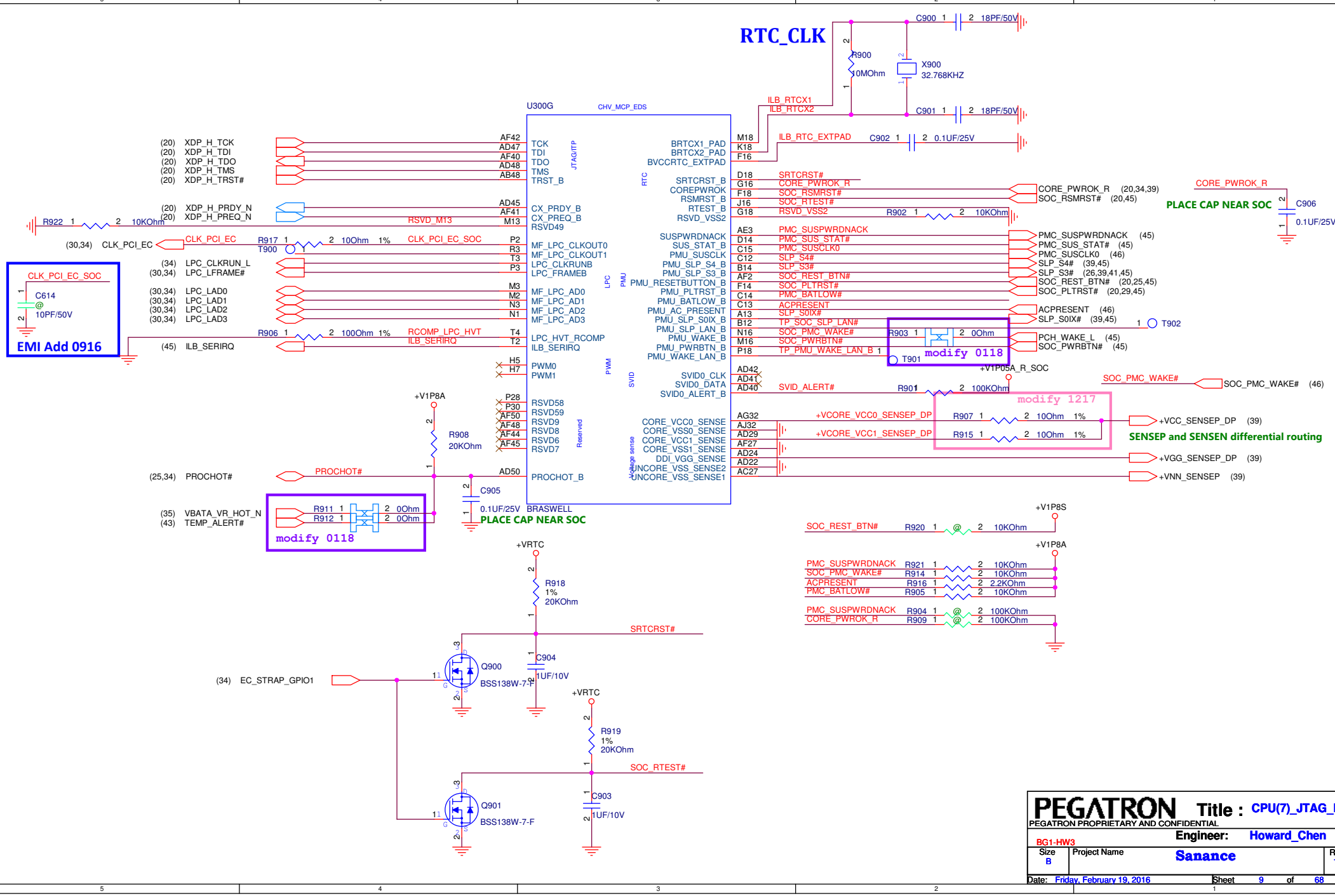
Title : CPU(6)_USB INTERFACE

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 8 of 68


RTC_CLK
C900 1 2 18PF/50V
R900 10MOhm
X900 32.768KHZ
C901 1 2 18PF/50V
ILB_RTCX1
ILB_RTCX2
ILB_RTC_EXTPAD
C902 1 2 0.1UF/25V
U300G
CHV_MCP_EDS
JTAG/ITP
RTC
LPC
PMU
SVID
PWM
Reserved
Voltage sense
BRASWELL
(20) XDP_H_TCK
(20) XDP_H_TDI
(20) XDP_H_TDO
(20) XDP_H_TMS
(20) XDP_H_TRST#
(20) XDP_H_PRDY_N
(20) XDP_H_PREQ_N
R922 1 2 10KOhm
RSVD_M13
(30,34) CLK_PCI_EC
CLK_PCI_EC
R917 1 2 10Ohm 1%
T900
CLK_PCI_EC_SOC
CLK_PCI_EC_SOC
C614 @ 10PF/50V
EMI Add 0916
(34) LPC_CLKRUN_L
(30,34) LPC_LFRAME#
(30,34) LPC_LAD0
(30,34) LPC_LAD1
(30,34) LPC_LAD2
(30,34) LPC_LAD3
R906 1 2 100Ohm 1%
RCOMP_LPC_HVT
ILB_SERIRQ
(45) ILB_SERIRQ
+V1P8A
R908 20KOhm
PROCHOT#
(25,34) PROCHOT#
C905 0.1UF/25V
PLACE CAP NEAR SOC
(35) VBATA_VR_HOT_N
(43) TEMP_ALERT#
R911 1 2 0Ohm
R912 1 2 0Ohm
modify 0118
+VRTC
R918 1% 20KOhm
SRTCRST#
(34) EC_STRAP_GPIO1
Q900 BSS138W-7-F
C904 1UF/10V
R919 1% 20KOhm
SOC_RTEST#
Q901 BSS138W-7-F
C903 1UF/10V
CORE_PWROK_R (20,34,39)
SOC_RSMRST# (20,45)
R902 1 2 10KOhm
PMC_SUSPWRDNACK (45)
PMC_SUS_STAT# (45)
PMC_SUSCLK0 (46)
SLP_S4# (39,45)
SLP_S3# (26,39,41,45)
SOC_REST_BTN# (20,25,45)
SOC_PLTRST# (20,29,45)
ACPRESENT (46)
SLP_S0IX# (39,45)
T902
PCH_WAKE_L (45)
SOC_PWRBTN# (45)
R903 1 2 0Ohm
T901
modify 0118
+V1P05A_R_SOC
SOC_PMC_WAKE#
SOC_PMC_WAKE# (46)
R901 2 100KOhm
modify 1217
+VCORE_VCC0_SENSEP_DP
+VCORE_VCC1_SENSEP_DP
R907 1 2 10Ohm 1%
R915 1 2 10Ohm 1%
+VCC_SENSEP_DP (39)
SENSEP and SENSEN differential routing
+VGG_SENSEP_DP (39)
+VNN_SENSEP (39)
CORE_PWROK_R
PLACE CAP NEAR SOC
C906 0.1UF/25V
+V1P8S
SOC_REST_BTN# R920 1 @ 2 10KOhm
+V1P8A
PMC_SUSPWRDNACK R921 1 2 10KOhm
SOC_PMC_WAKE# R914 1 2 10KOhm
ACPRESENT R916 1 2 2.2KOhm
PMC_BATLOW# R905 1 2 10KOhm
PMC_SUSPWRDNACK R904 1 @ 2 100KOhm
CORE_PWROK_R R909 1 @ 2 100KOhm
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Title : CPU(7)_JTAG_LPC_TH
BG1-HW3
Engineer: Howard_Chen
Size B
Project Name Sanance
Rev 1.1
Date: Friday, February 19, 2016
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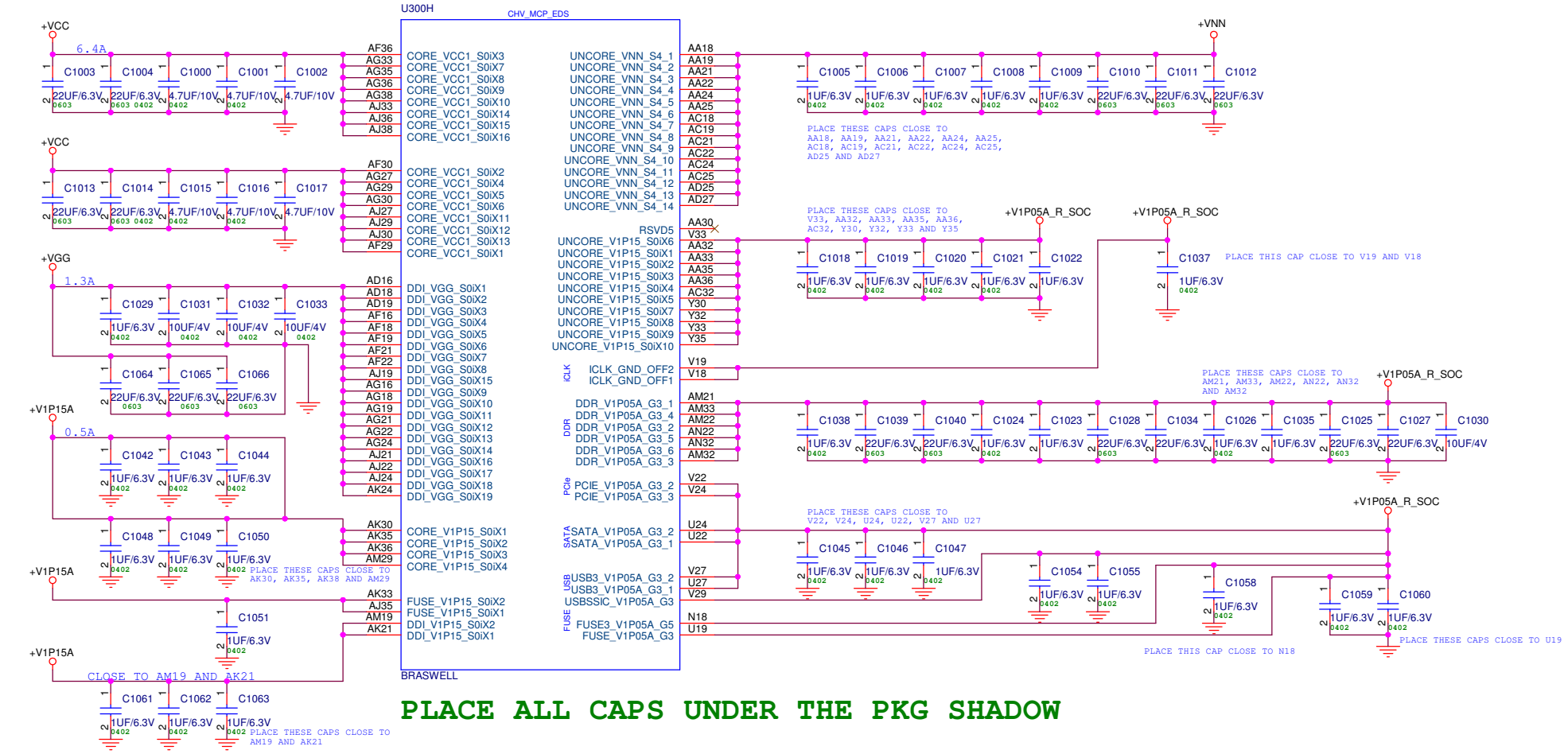
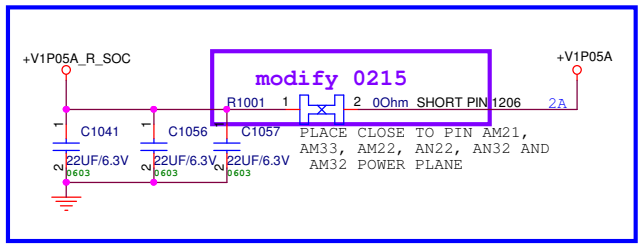


PLACE ALL CAPS UNDER THE PKG SHADOW



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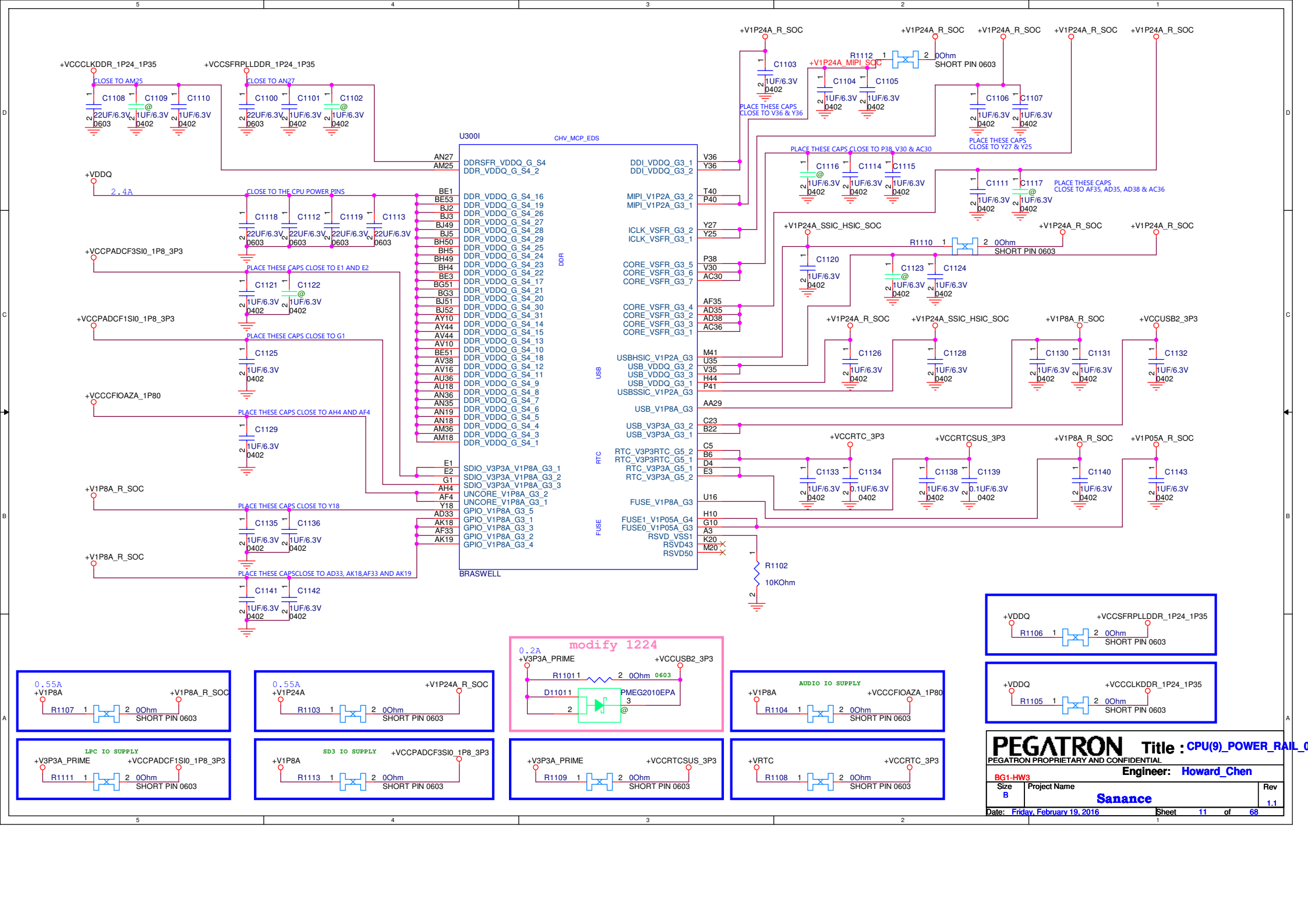
Title : CPU(8)_POWER_RAIL_0

BG1-HW3

Engineer: Howard_Chen

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 10 of 68


+VCCCLKDDR_1P24_1P35
+VCCSFRPLLDDR_1P24_1P35
CLOSE TO AM25
CLOSE TO AN27
C1108 22UF/6.3V 0603
C1109 @ 1UF/6.3V 0402
C1110 1UF/6.3V 0402
C1100 22UF/6.3V 0603
C1101 1UF/6.3V 0402
C1102 @ 1UF/6.3V 0402
+VDDQ
2.4A
CLOSE TO THE CPU POWER PINS
C1118 C1112 C1119 C1113 22UF/6.3V 0603
+VCCPADCF3SI0_1P8_3P3
PLACE THESE CAPS CLOSE TO E1 AND E2
C1121 1UF/6.3V 0402
C1122 @ 1UF/6.3V 0402
+VCCPADCF1SI0_1P8_3P3
PLACE THESE CAPS CLOSE TO G1
C1125 1UF/6.3V 0402
+VCCCFIOAZA_1P80
PLACE THESE CAPS CLOSE TO AH4 AND AF4
C1129 1UF/6.3V 0402
+V1P8A_R_SOC
PLACE THESE CAPS CLOSE TO Y18
C1135 C1136 1UF/6.3V 0402
+V1P8A_R_SOC
PLACE THESE CAPSCLOSE TO AD33, AK18,AF33 AND AK19
C1141 C1142 1UF/6.3V 0402
U300I
CHV_MCP_EDS
BRASWELL
DDR
USB
RTC
FUSE
AN27 AM25 DDRSFR_VDDQ_G_S4 DDR_VDDQ_G_S4_2
BE1 BE53 BJ2 BJ3 BJ49 BJ5 BH50 BH5 BH49 BH4 BE3 BG51 BG3 BJ51 BJ52 AY10 AY44 AV44 AV10 BE51 AV38 AV16 AU36 AU18 AN36 AN35 AN19 AN18 AM36 AM18 DDR_VDDQ_G_S4_16 DDR_VDDQ_G_S4_19 DDR_VDDQ_G_S4_26 DDR_VDDQ_G_S4_27 DDR_VDDQ_G_S4_28 DDR_VDDQ_G_S4_29 DDR_VDDQ_G_S4_25 DDR_VDDQ_G_S4_24 DDR_VDDQ_G_S4_23 DDR_VDDQ_G_S4_22 DDR_VDDQ_G_S4_17 DDR_VDDQ_G_S4_21 DDR_VDDQ_G_S4_20 DDR_VDDQ_G_S4_30 DDR_VDDQ_G_S4_31 DDR_VDDQ_G_S4_14 DDR_VDDQ_G_S4_15 DDR_VDDQ_G_S4_13 DDR_VDDQ_G_S4_10 DDR_VDDQ_G_S4_18 DDR_VDDQ_G_S4_12 DDR_VDDQ_G_S4_11 DDR_VDDQ_G_S4_9 DDR_VDDQ_G_S4_8 DDR_VDDQ_G_S4_7 DDR_VDDQ_G_S4_6 DDR_VDDQ_G_S4_5 DDR_VDDQ_G_S4_4 DDR_VDDQ_G_S4_3 DDR_VDDQ_G_S4_1
E1 E2 G1 AH4 AF4 Y18 AD33 AK18 AF33 AK19 SDIO_V3P3A_V1P8A_G3_1 SDIO_V3P3A_V1P8A_G3_2 SDIO_V3P3A_V1P8A_G3_3 UNCORE_V1P8A_G3_2 UNCORE_V1P8A_G3_1 GPIO_V1P8A_G3_5 GPIO_V1P8A_G3_1 GPIO_V1P8A_G3_3 GPIO_V1P8A_G3_2 GPIO_V1P8A_G3_4
V36 Y36 DDI_VDDQ_G3_1 DDI_VDDQ_G3_2
T40 P40 MIPI_V1P2A_G3_2 MIPI_V1P2A_G3_1
Y27 Y25 ICLK_VSFR_G3_2 ICLK_VSFR_G3_1
P38 V30 AC30 CORE_VSFR_G3_5 CORE_VSFR_G3_6 CORE_VSFR_G3_7
AF35 AD35 AD38 AC36 CORE_VSFR_G3_4 CORE_VSFR_G3_2 CORE_VSFR_G3_3 CORE_VSFR_G3_1
M41 U35 V35 H44 P41 AA29 USBHSIC_V1P2A_G3 USB_VDDQ_G3_2 USB_VDDQ_G3_3 USB_VDDQ_G3_1 USBSSIC_V1P2A_G3 USB_V1P8A_G3
C23 B22 USB_V3P3A_G3_2 USB_V3P3A_G3_1
C5 B6 D4 E3 RTC_V3P3RTC_G5_2 RTC_V3P3RTC_G5_1 RTC_V3P3A_G5_1 RTC_V3P3A_G5_2
U16 FUSE_V1P8A_G3
H10 G10 A3 K20 M20 FUSE1_V1P05A_G4 FUSE0_V1P05A_G3 RSVD_VSS1 RSVD43 RSVD50
R1102 10KOhm
+V1P24A_R_SOC
C1103 1UF/6.3V 0402
PLACE THESE CAPS CLOSE TO V36 & Y36
+V1P24A_MIPI_SOC
C1104 1UF/6.3V 0402
C1105 1UF/6.3V 0402
R1112 0Ohm SHORT PIN 0603
C1106 C1107 1UF/6.3V 0402
PLACE THESE CAPS CLOSE TO Y27 & Y25
PLACE THESE CAPS CLOSE TO P38, V30 & AC30
C1116 @ 1UF/6.3V 0402
C1114 C1115 1UF/6.3V 0402
C1111 C1117 @ 1UF/6.3V 0402
PLACE THESE CAPS CLOSE TO AF35, AD35, AD38 & AC36
+V1P24A_SSIC_HSIC_SOC
R1110 0Ohm SHORT PIN 0603
C1120 1UF/6.3V 0402
C1123 @ 1UF/6.3V 0402
C1124 1UF/6.3V 0402
C1126 1UF/6.3V 0402
C1128 1UF/6.3V 0402
C1130 C1131 1UF/6.3V 0402
C1132 1UF/6.3V 0402
+VCCRTC_3P3
C1133 1UF/6.3V 0402
C1134 0.1UF/6.3V 0402
+VCCRTCSUS_3P3
C1138 C1139 1UF/6.3V 0402
C1140 1UF/6.3V 0402
+V1P05A_R_SOC
C1143 1UF/6.3V 0402
modify 1224
0.2A
+V3P3A_PRIME
+VCCUSB2_3P3
R11011 0Ohm 0603
D11011 PMEG2010EPA
0.55A
+V1P8A
+V1P8A_R_SOC
R1107 0Ohm SHORT PIN 0603
+V1P24A
R1103 0Ohm SHORT PIN 0603
AUDIO IO SUPPLY
R1104 0Ohm SHORT PIN 0603
+VDDQ
+VCCSFRPLLDDR_1P24_1P35
R1106 0Ohm SHORT PIN 0603
+VCCCLKDDR_1P24_1P35
R1105 0Ohm SHORT PIN 0603
LPC IO SUPPLY
R1111 0Ohm SHORT PIN 0603
SD3 IO SUPPLY
+VCCPADCF3SI0_1P8_3P3
R1113 0Ohm SHORT PIN 0603
R1109 0Ohm SHORT PIN 0603
+VRTC
+VCCRTC_3P3
R1108 0Ohm SHORT PIN 0603
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : CPU(9)_POWER_RAIL_0
Engineer: Howard_Chen
BG1-HW3
Size B
Project Name
Sanance
Rev 1.1
Date: Friday, February 19, 2016
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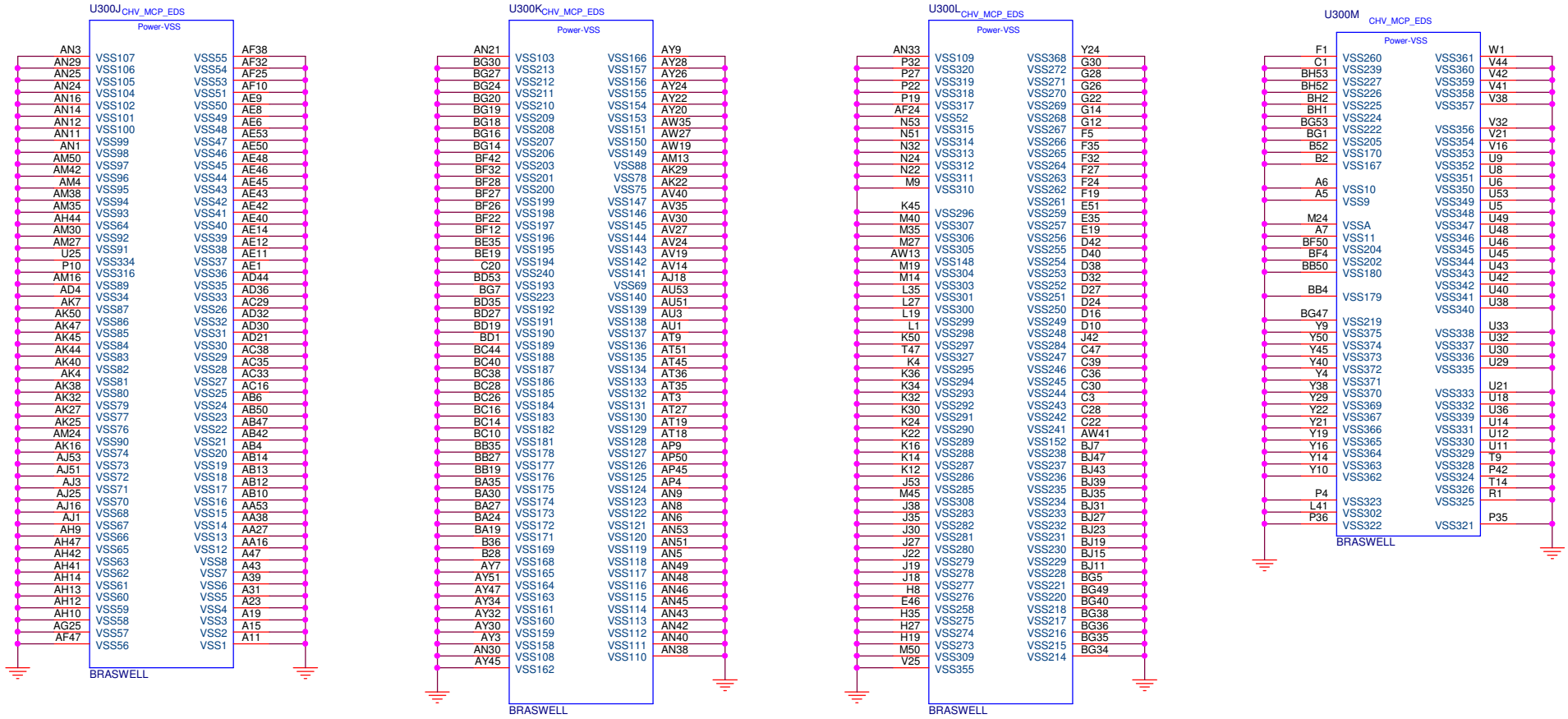

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Title :CPU(10)_CPU_GROUND

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 12 of 68

PEGATRON Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 13 of 68

PEGATRON

Title : **********

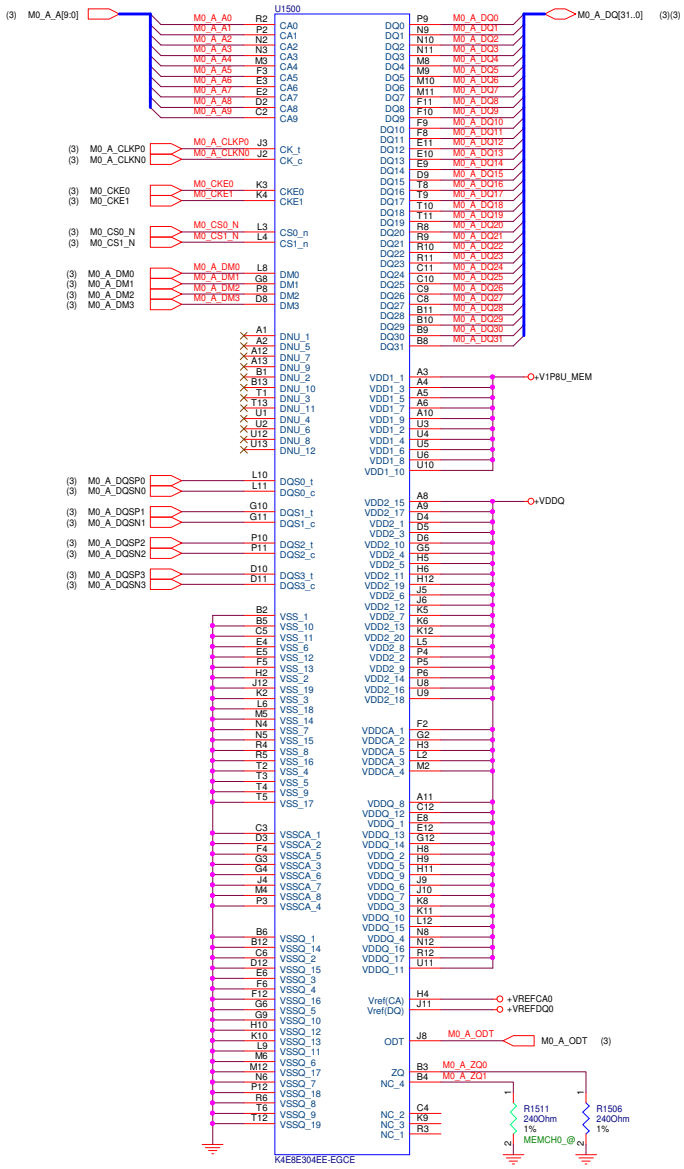
PEGATRON PROPRIETARY AND CONFIDENTIAL

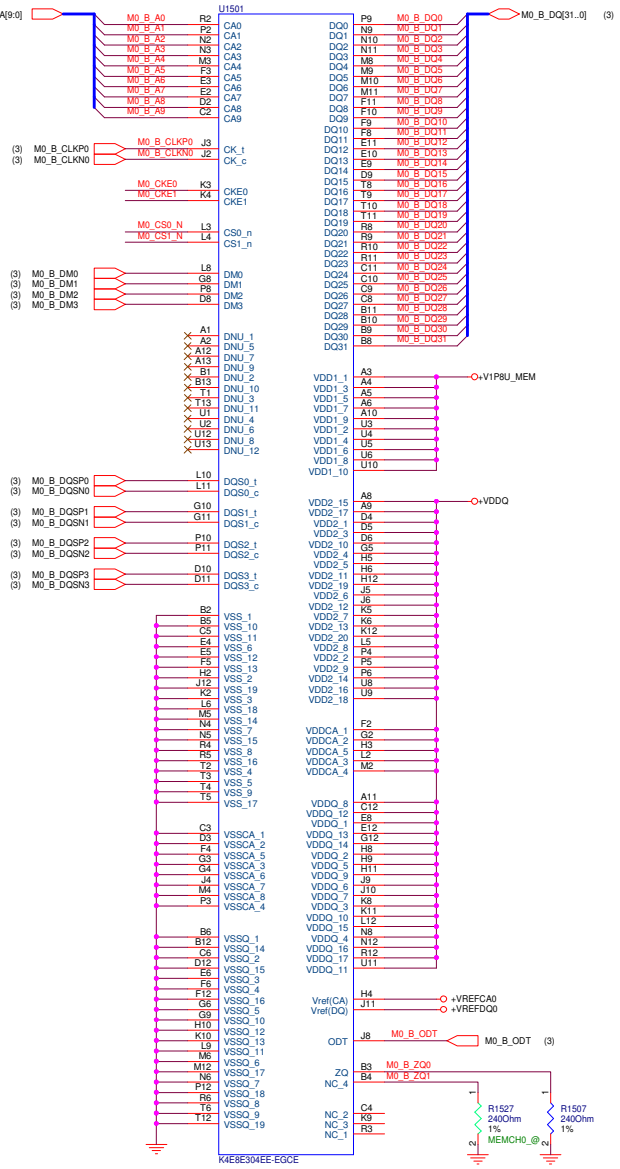
Engineer:

BG1-HW3

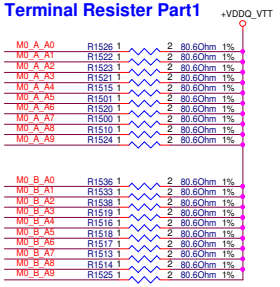
Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 14 of 68



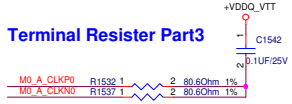


Terminal Resister Part1

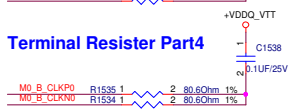


Terminal Resister Part2

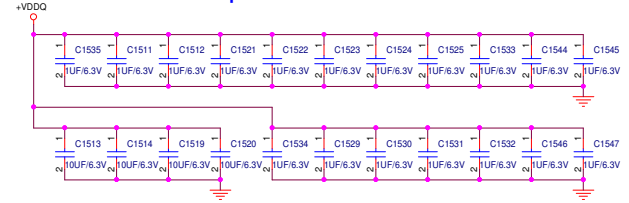
Terminal Resister Part3



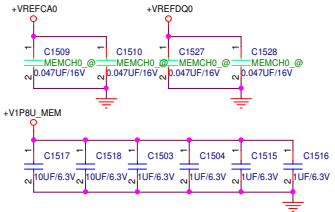
Terminal Resister Part4



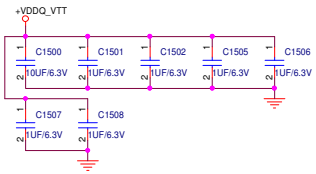
U1201/U1202 Power Decouple



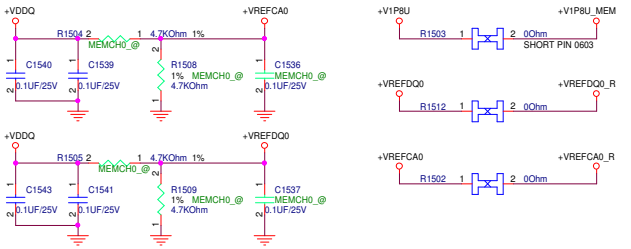
Reference Power



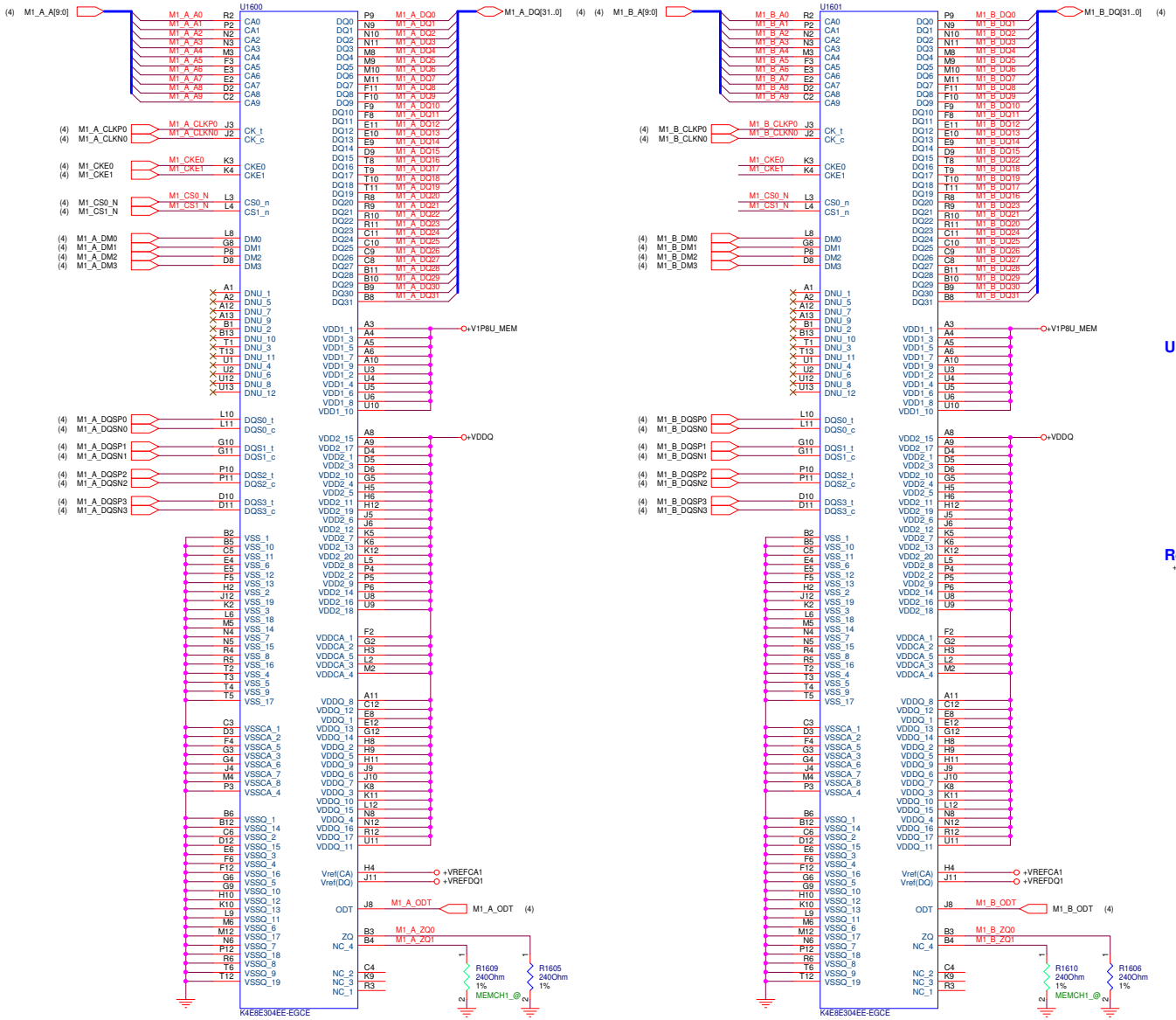
VTT Power Decouple



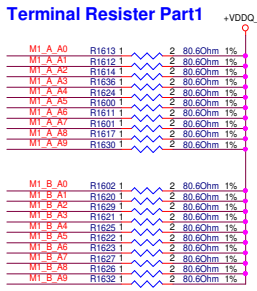
Branch Power



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : LPDDR3 MEMORY CHANNEL A
Engineer: Howard_Chen
BG1-HW3
Size C
Project Name Sanance
Rev 1.1
Date: Friday, February 19, 2016
Sheet 15 of 68



Terminal Resister Part1

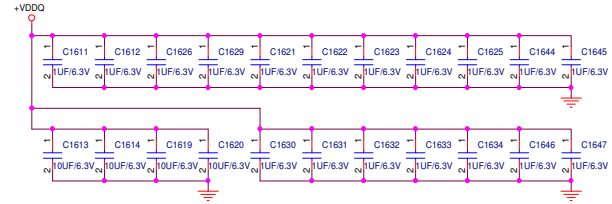


Terminal Resister Part2

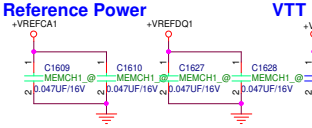
Terminal Resister Part3

Terminal Resister Part4

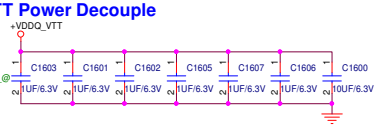
U1600/U1601 Power Decouple

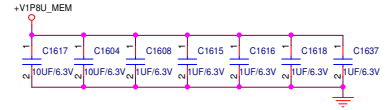


Reference Power

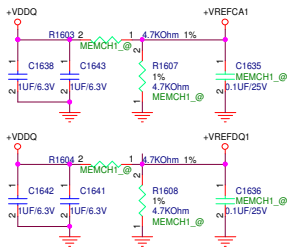


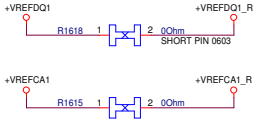
VTT Power Decouple





Reference Power





PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LPDDR3 MEMORY CHANNEL A

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
C	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 16 of 68

PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 17 of 68

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : **********

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 18 of 68

PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

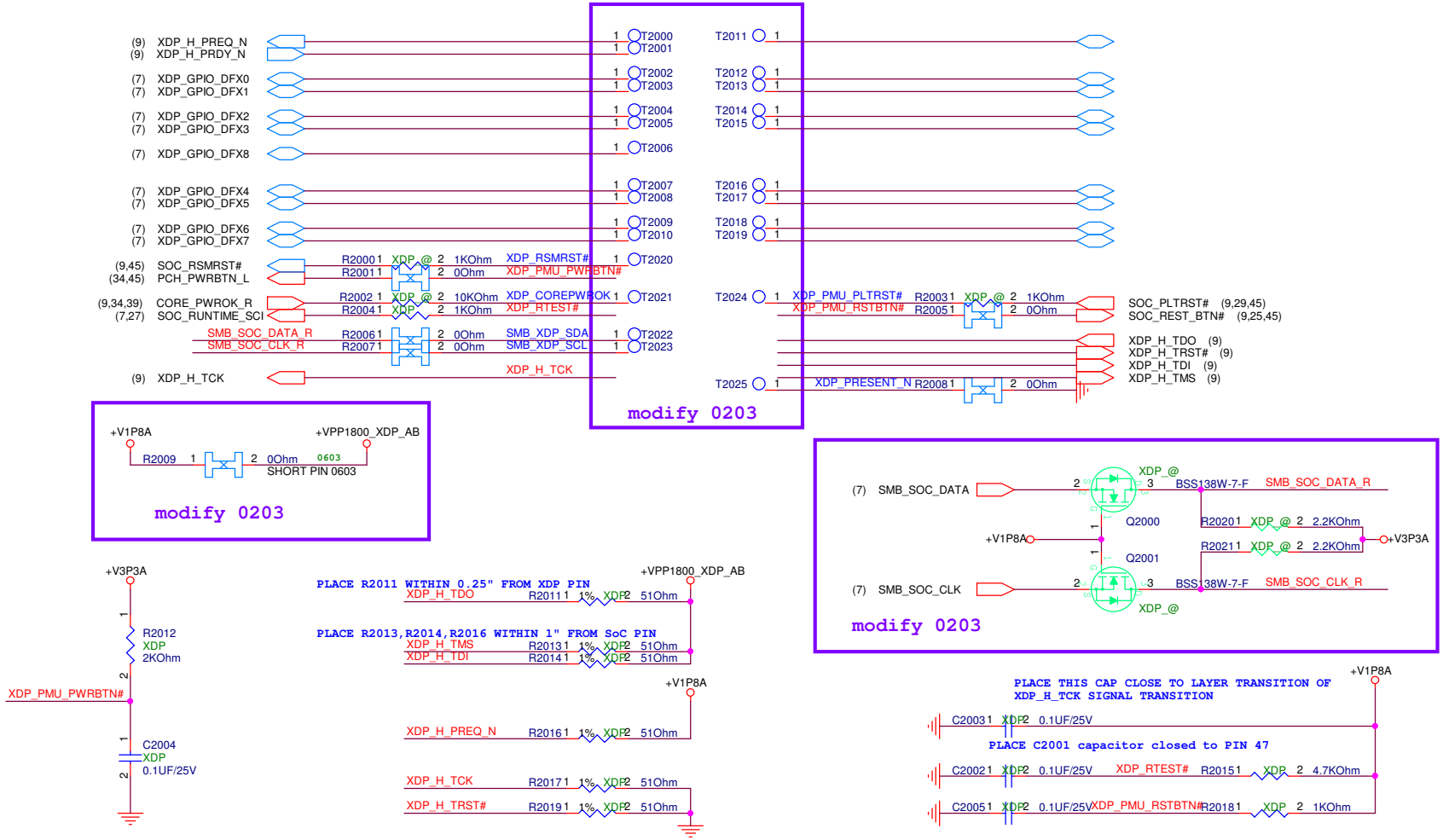
Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 19 of 68

INTEL Debug Port (CPU)



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : INTEL XDP CONN

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 20 of 68

PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 21 of 68

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : **********

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 22 of 68

PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

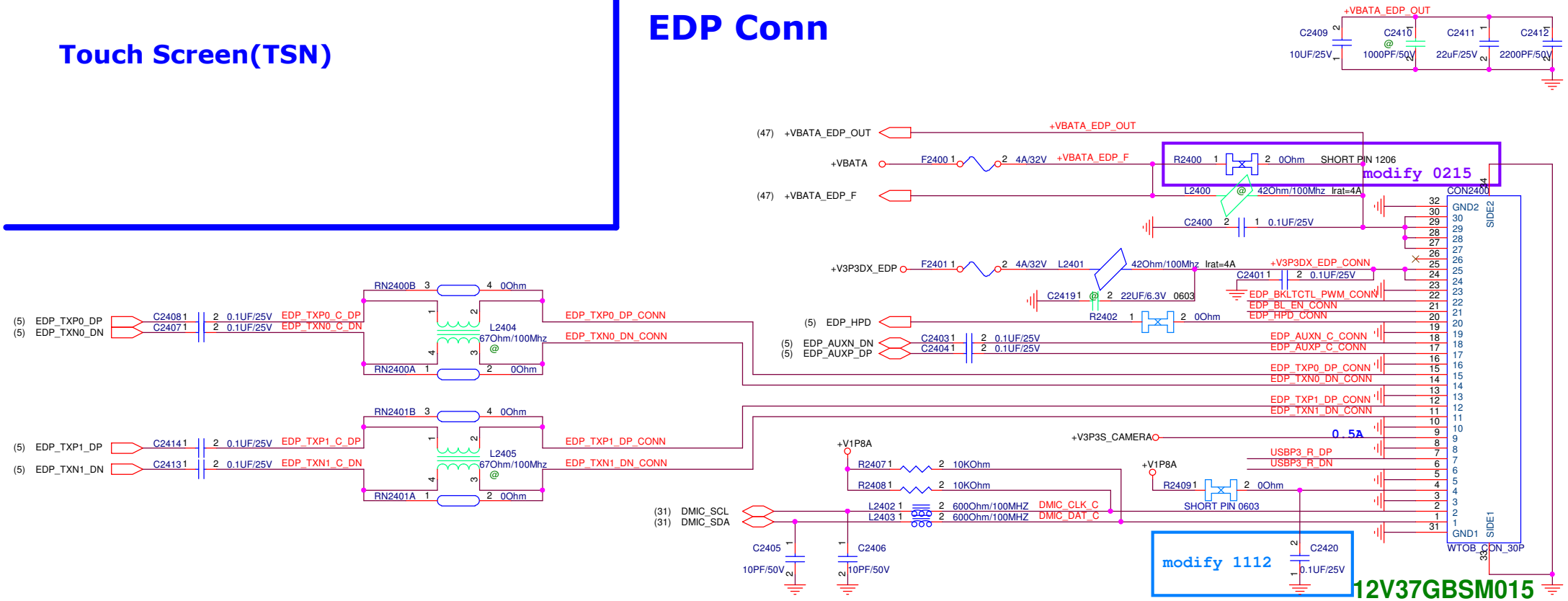
BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

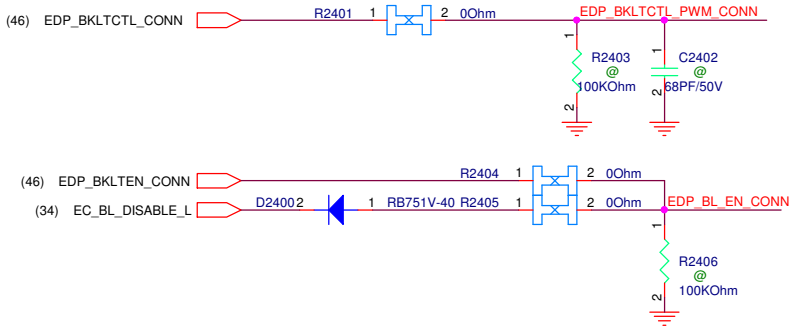
Date: Friday, February 19, 2016 Sheet 23 of 68

Touch Screen(TSN)

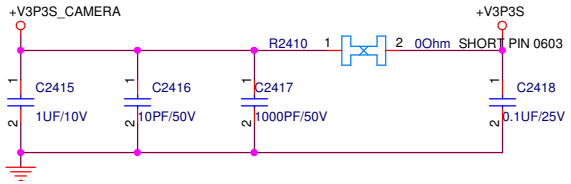
EDP Conn



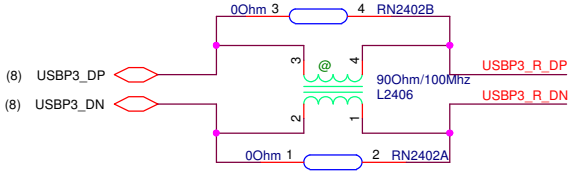
LCD Panel Control



CCD power(FCM)



CCD USB(FCM)



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : EDP _CAMERA_DMIC

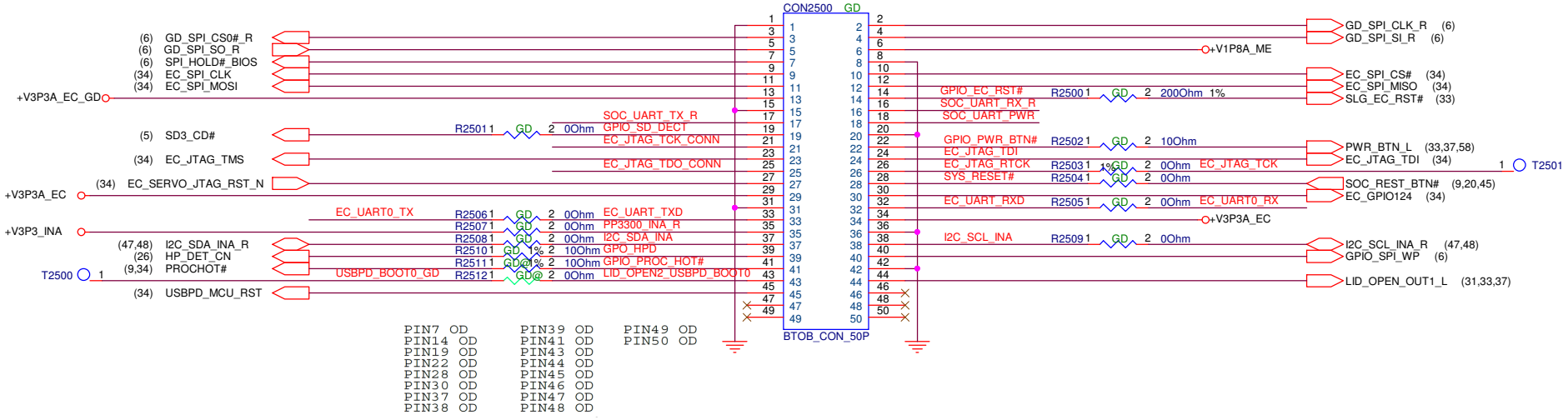
Engineer: Howard_Chen

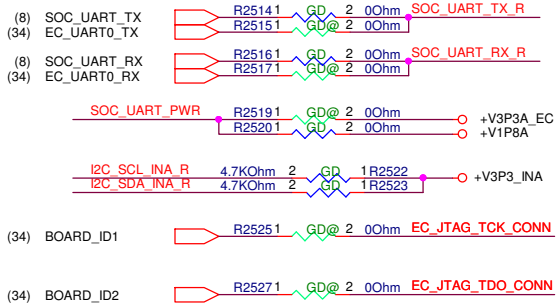
BG1-HW3

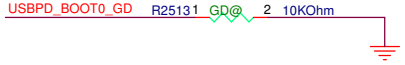
Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 24 of 68

Google Debug Connector







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GOOGLE_DEBUG_CONN

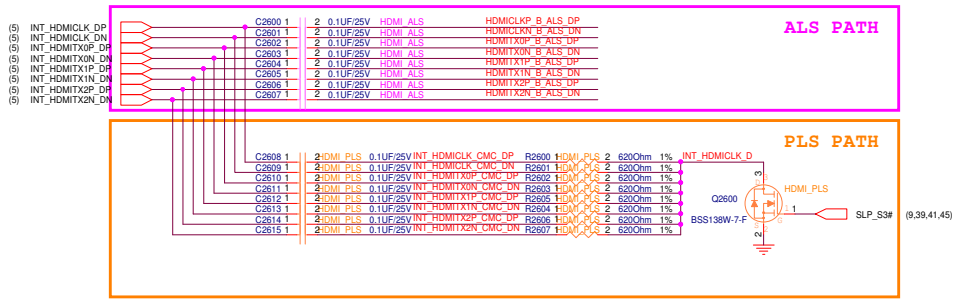
BG1-HW3

Engineer: Howard_Chen

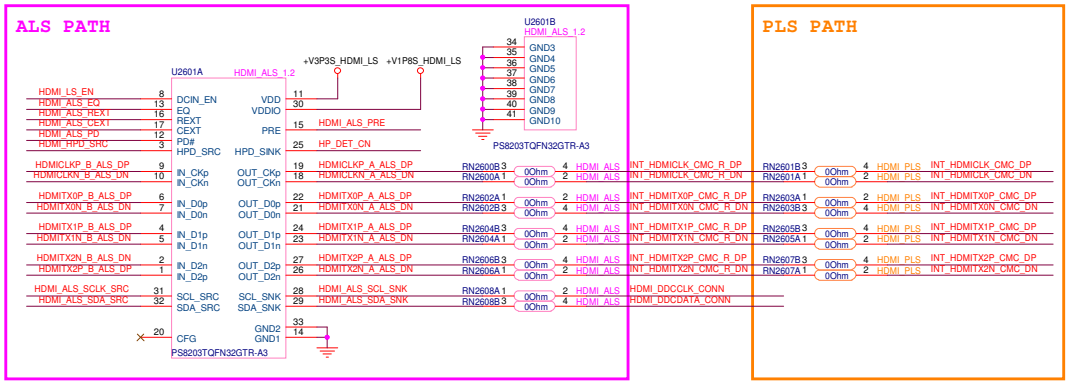
Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 25 of 68

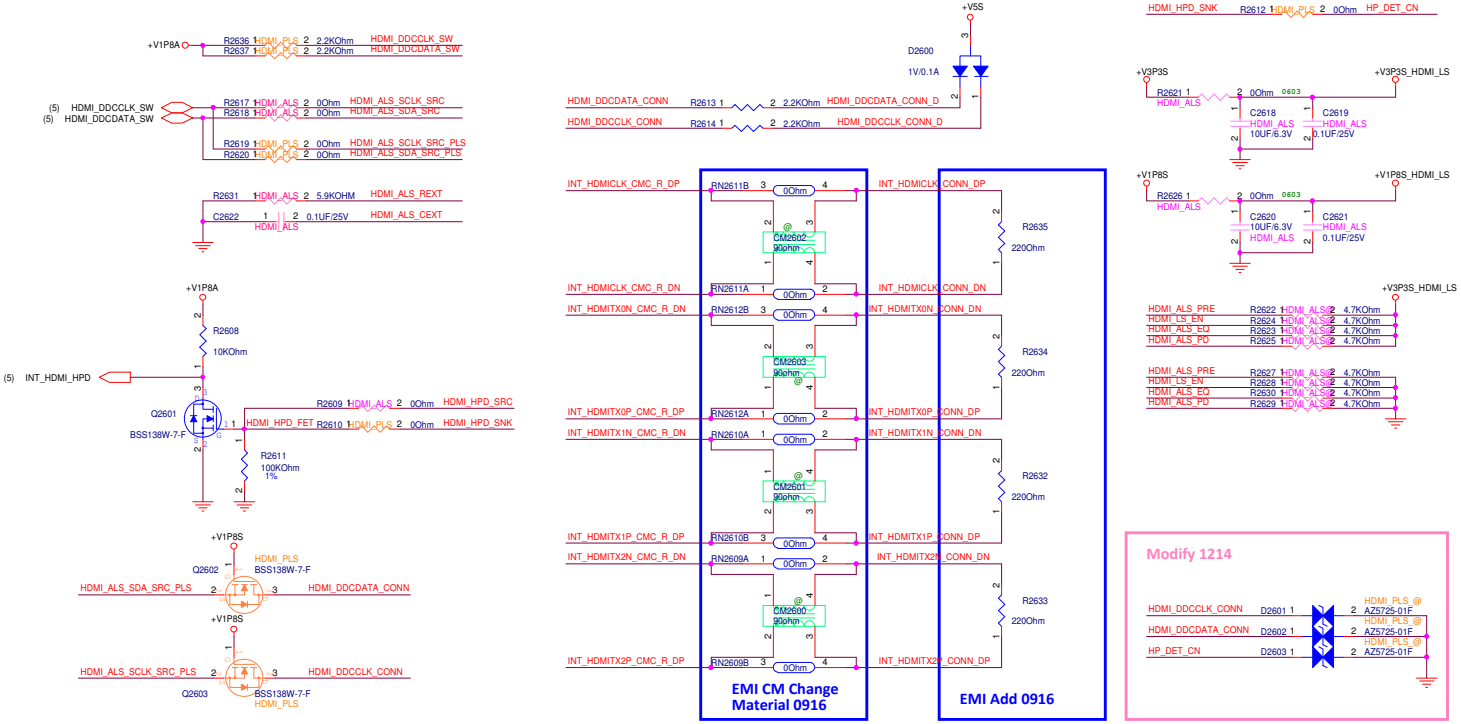
HDMI Cost Reduced level shift (HDM)



HDMI Repeater Optional



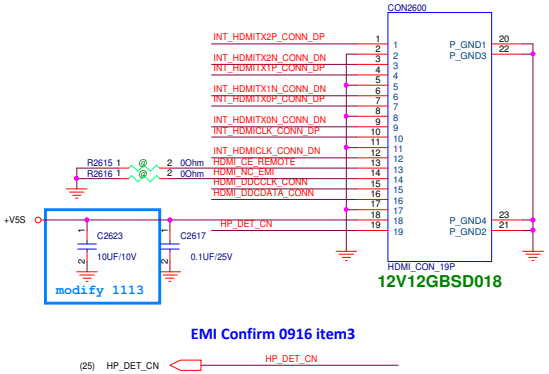
PULL-UPS, PULL-DOWNS, CMC AND LEVEL TRANSLATOR



NOTE:
WHEN USING ACTIVE LEVEL SHIFTER - ESD DIODES are in-built in PS8203.
WHEN USING PASSIVE LEVEL SHIFTER - It is recommended to add external ESD DIODES on board for the below signals

1) HDMI_DDCCLK_CONN
2) HDMI_DDCDATA_CONN
3) HP_DET_CN

HDMI- CONNECTOR



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : HDMI_DISPLAY_CONN
Engineer: Howard_Chen
BG1-HW3
Size: C
Project Name: Sanance
Rev: 1.1
Date: Friday, February 19, 2016
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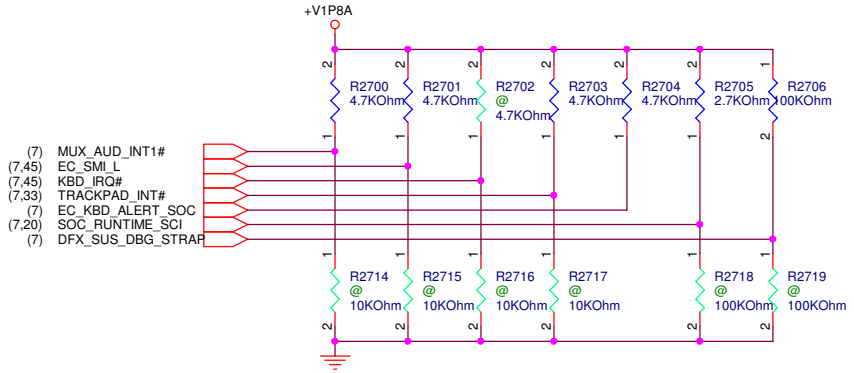
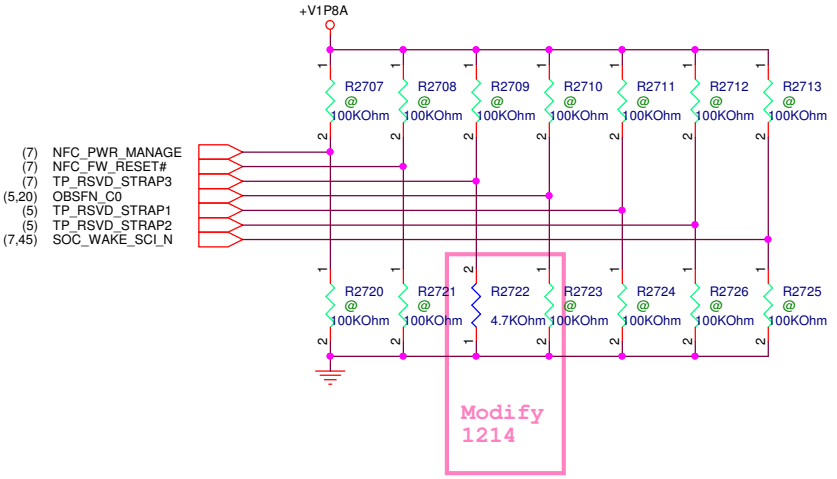
Straps -- strap detect @ RSMRST# assertion				
Purpose	Pin Name	Pull-Up/Pull Down	Polarity	Default State on board?
DDI0 Detected	GPIO_SUS0	Weak internal pull down	When '1'-Port DDI0 is Detected When '0'- PortB is not detected (could be overwritten by BIOS incased it used as GPIO)	High
DDI1 Detected	GPIO_SUS1	Weak internal pull down	When '1'-Port DDI1 is Detected When '0'- PortC is not detected(could be overwritten by BIOS incased it used as GPIO)	High
A16 swap override	GPIO_SUS2	Weak internal pull up	A16 override if sampled low. (Changes bootloader address)	High
DSI Display Detected	GPIO_SUS3	Weak internal pull down	When '1' DSI Port is Detected (could be overwritten by BIOS incased it used as GPIO)	Low
Boot BIOS Strap BBS	GPIO_SUS4	Weak internal pull up	Boot BIOS from LPC if sampled low	High
Flash Descriptor Security Override	GPIO_SUS5	Weak internal pull up	Security measures defined in the Flash Descriptor is overridden if sampled low	High
DFX Boot Halt Strap & VISA Early POSM Debug Enable	GPIO_SUS6	Weak Internal Pull Up	0 = Halt Boot and Early POSM Debug 1 = Normal operation.	High
DFX Sus Debug Strap	GPIO_SUS7	Weak Internal Pull Up	0 = SUS Debug 1= No SUS Debug	High
ICLK, USB2, DDI SFR Supply Select-	SEC_GPIO_SUS8	Weak Internal Pull Up	**0: supply is 1.25V**; 1: supply is 1.35V	**Low**
ICLK SFR Bypass	SEC_GPIO_SUS9	Weak Internal Pull Down	0- no bypass; 1: bypass with 1.05V	Low
POSM Select	SEC_GPIO_SUS10	Weak Internal Pull Down	Selects which POSM will be observed at time 0. 0 = Fuse Controller 1 - PMC	Don't care, if GPIO_SUS6 is pulled high.
ICLK Xtal OSC Bypass	GP_CAMERASB08	Weak Internal Pull Down	0- no bypass; 1: bypass	Low
CCU SUS RO Bypass	GP_CAMERASB09	Weak Internal Pull Down	0- no bypass; 1: bypass	Low
RTC OSC Bypass	GP_CAMERASB11	Weak Internal Pull Down	0- no bypass; 1: bypass	Low





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : STRAP_SETTINGS

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 27 of 68

WIFI/BT COMBO (NGFF E KEY)

BT

PQC modify 1113

RN2800A 2 1 0Ohm
RN2800B 4 3 0Ohm
CM2800 90Ohm/100MHz

(8) USBP4_DP
(8) USBP4_DN

USBP4_BT_DP
USBP4_BT_DN

WLAN

(6) PCIE_TX2_WLAN_DP
(6) PCIE_TX2_WLAN_DN
(6) PCIE_RX2_WLAN_DP
(6) PCIE_RX2_WLAN_DN
(6) CLK_PCIE_WLANP_DP
(6) CLK_PCIE_WLANN_DN
modify 1217 (46) PCIE_CLKREQ_WLAN_N
(46) WLAN_WAKE_L

C2810 @ 0.1UF/25V

EMI Add 0916

CON2800
NP_NC1
SIDE1
NP_NC2
SIDE2
NGFF_67P
12V44GBSD010

+V3P3A_WIFI

WIFI_SUSCLK (46)
WLAN_OFF_L (34)
RF_EN (46)
WLAN_PERST# (45)

C2809 @ 0.1UF/25V

+V3P3A

modify 0215
R2801 2 1 0Ohm SHORT PIN 0805

C2800 22UF/6.3V
C2801 22UF/6.3V
C2802 0.1UF/25V
C2803 10UF/6.3V
C2804 0.1UF/25V
C2805 @ 0.1UF/25V
C2806 @ 0.1UF/25V
C2807 10UF/6.3V
C2808 10UF/6.3V

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : NGFF_WLAN/BT_CONN

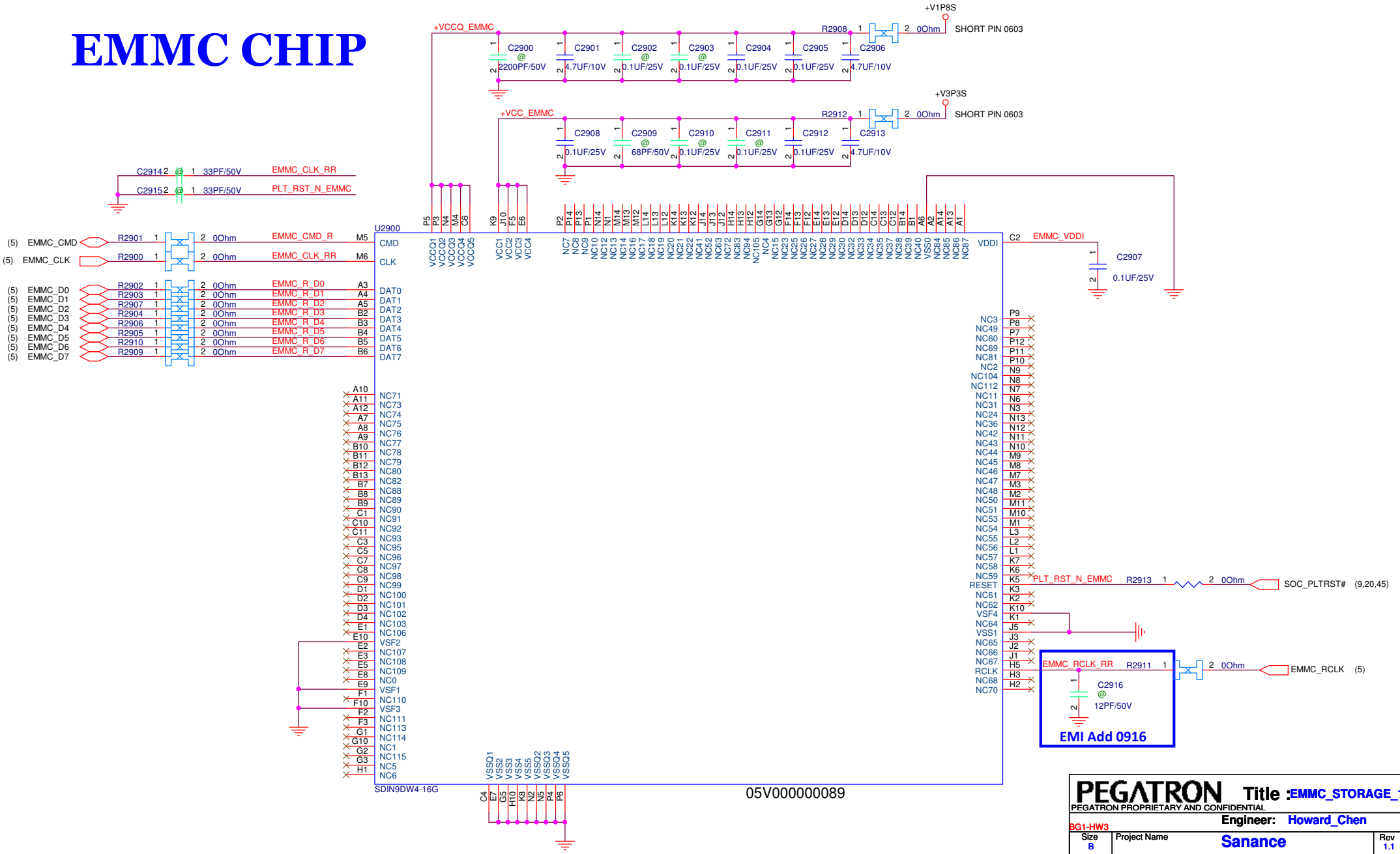
Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 28 of 68

EMMC CHIP



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

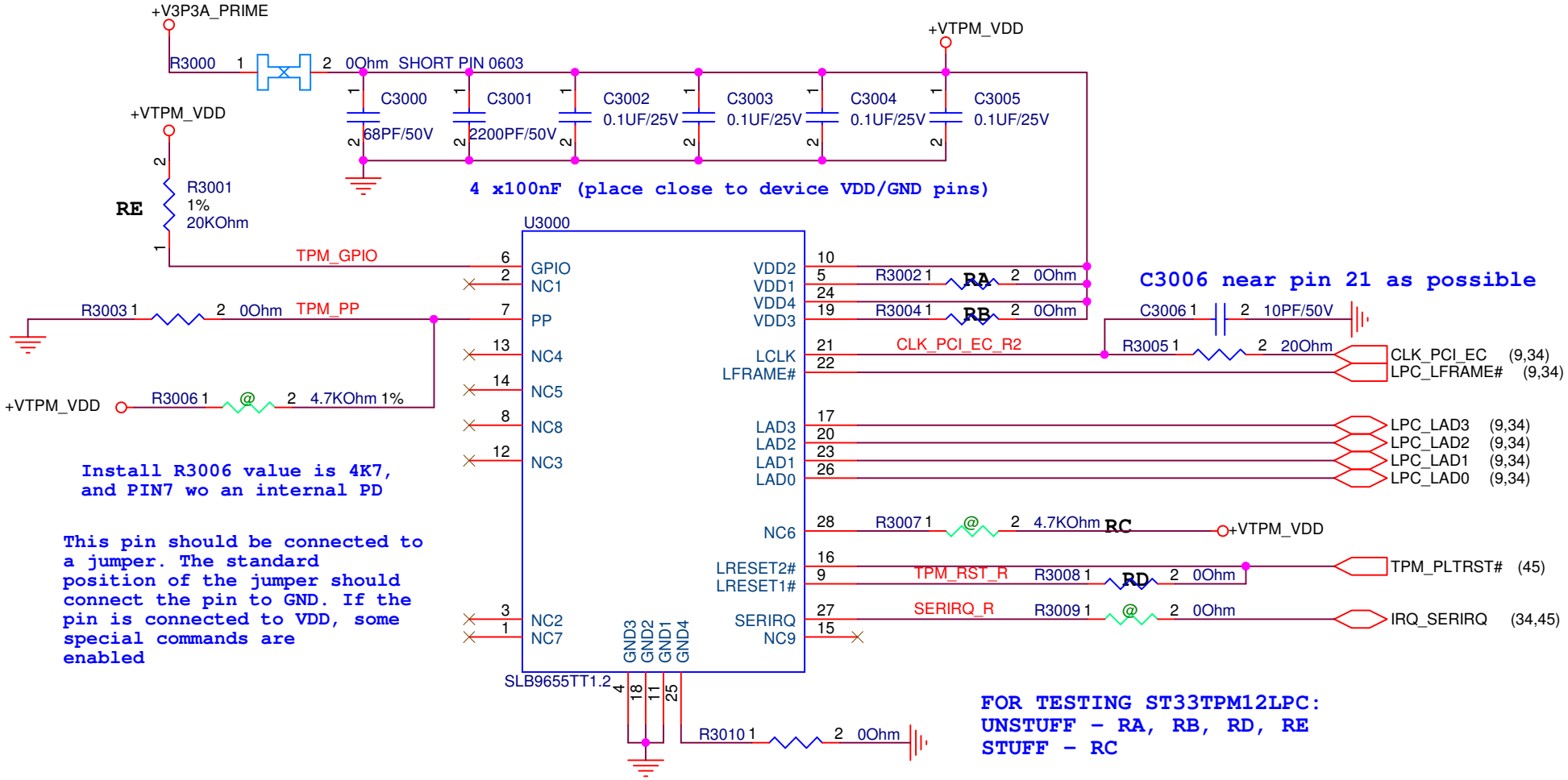
Title : EMMC_STORAGE_16G

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 29 of 68



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : INFINEON_TPM

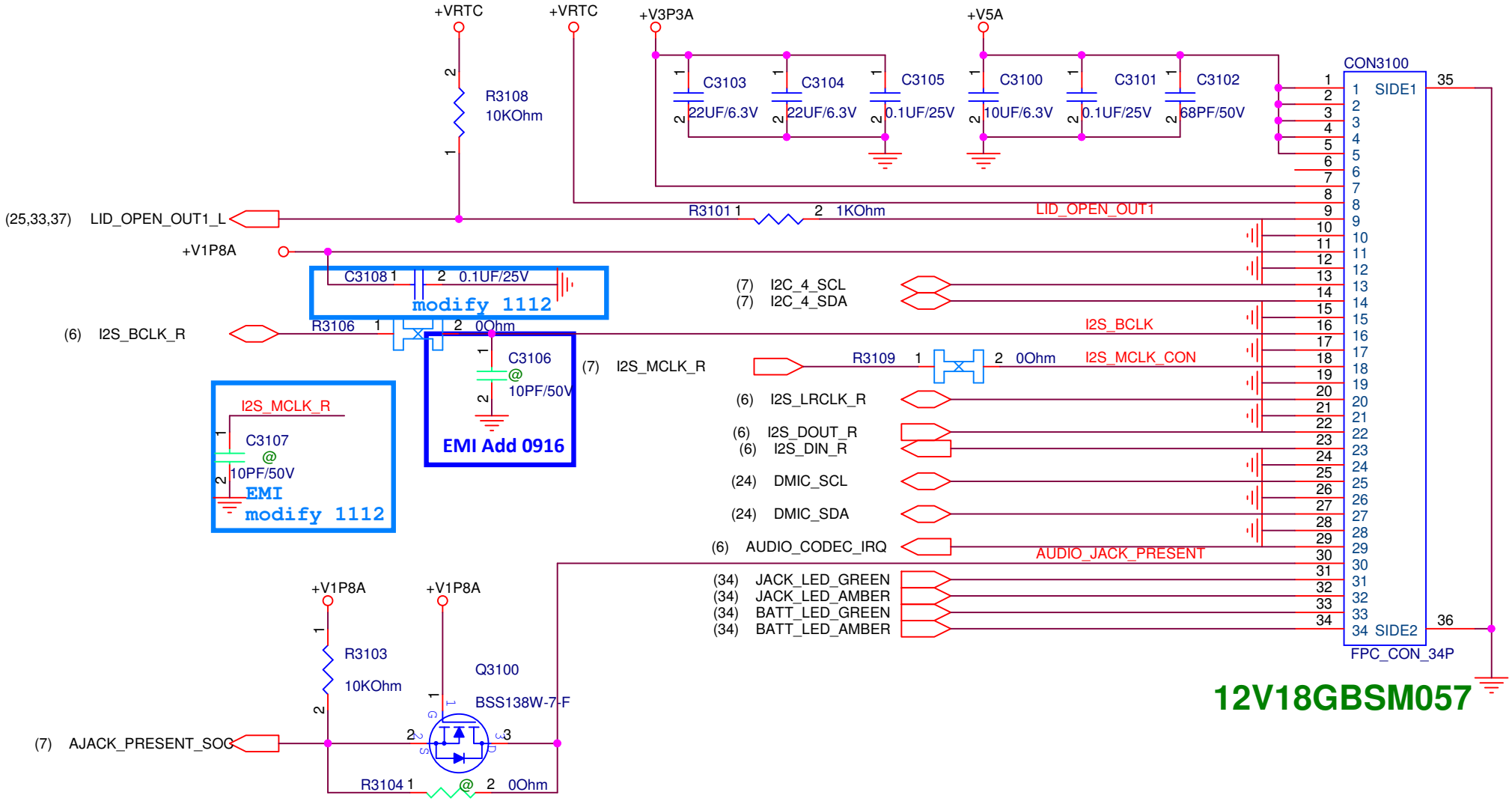
Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 30 of 68

IO_BOARD_CONN



12V18GBSM057

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : IO_DB_CONN_(MB)

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

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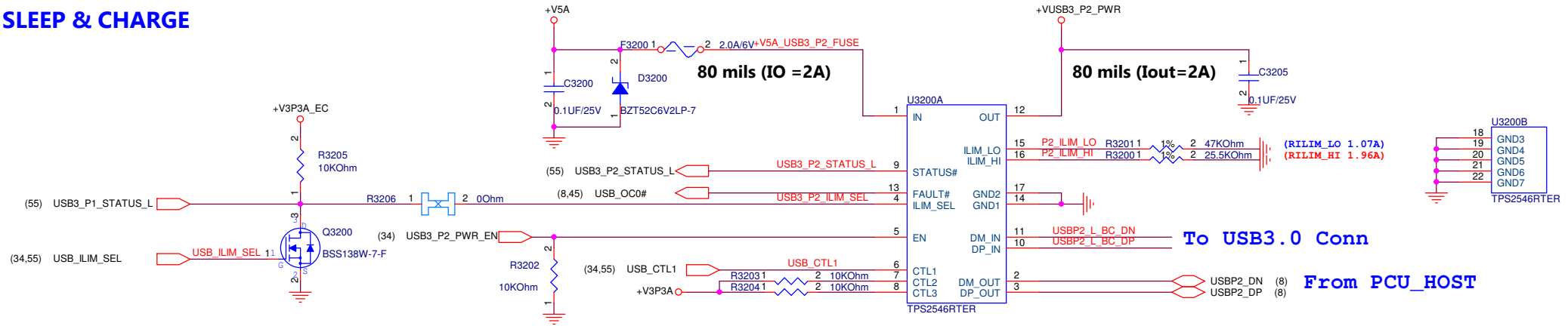
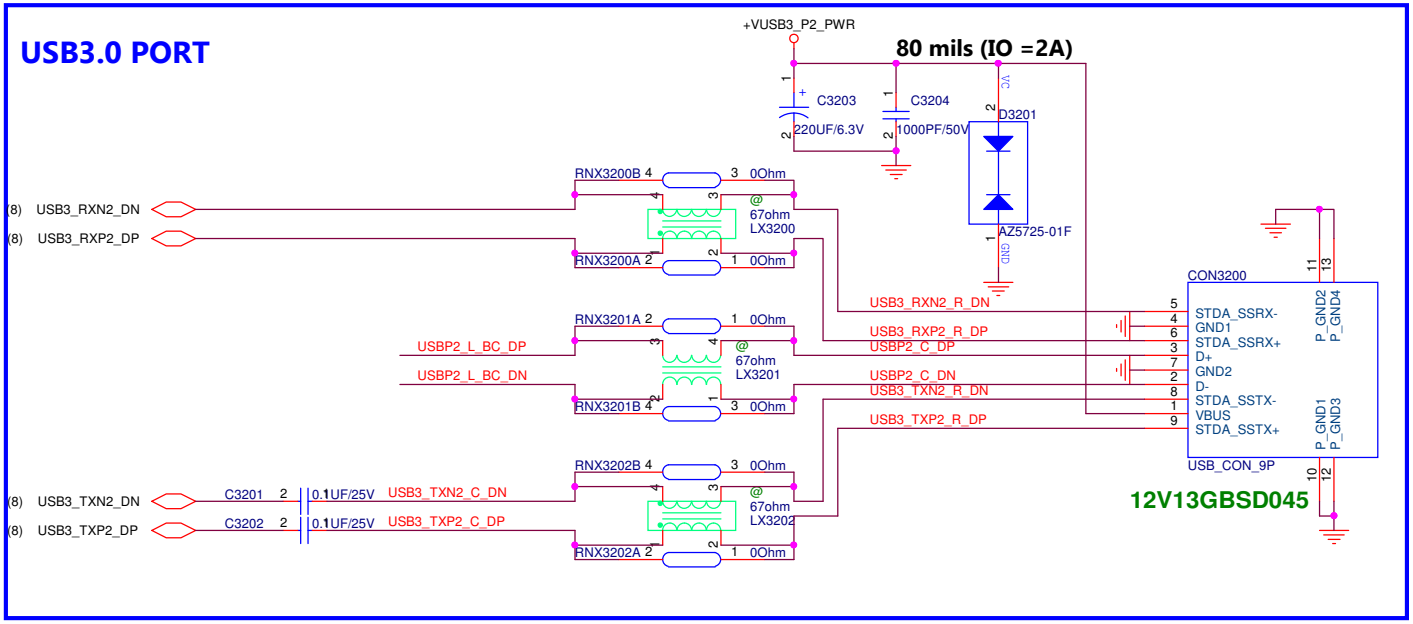
USB 3.0 PORT2 and CHARGER(MB)

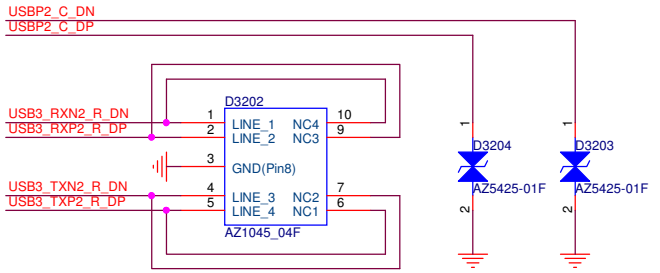
SLEEP & CHARGE



USB3.0 PORT



ESD CHIP



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB30 PORT & CHARG

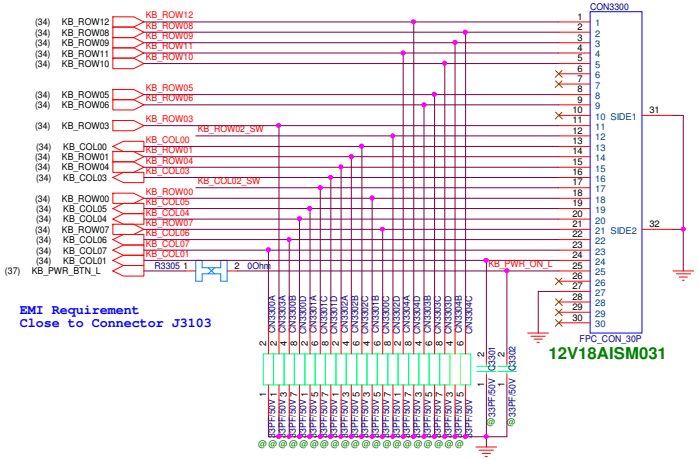
Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

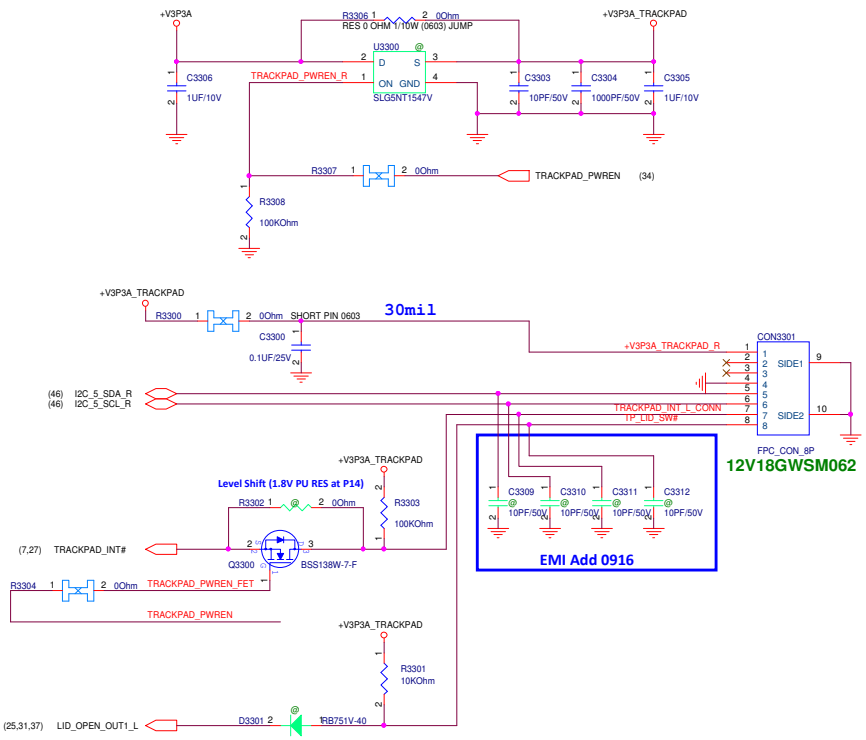
Date: Friday, February 19, 2016 Sheet 32 of 68

Keyboard Conn

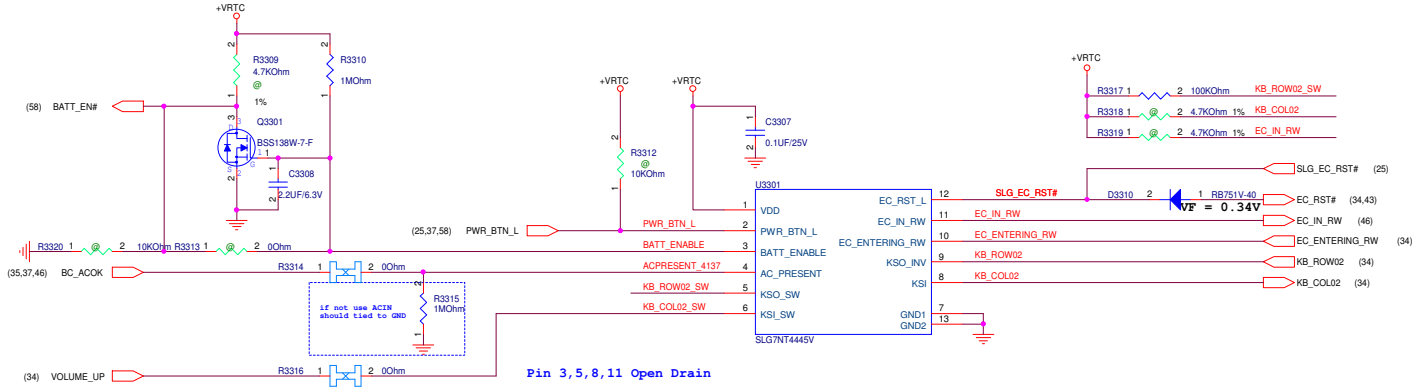


EMI Remove 0916

Track PAD BOARD CONN (TPD)



HOLELESS RESET 2-CHIP(KBC)



Connect to EC reset pin
Connect to GPIO on CPU with PU to GPIO power well
Connect to EC pin C5 (must be low when EC IN RESET)

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_TP_KB_CONN

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
C	Sanance	1.1

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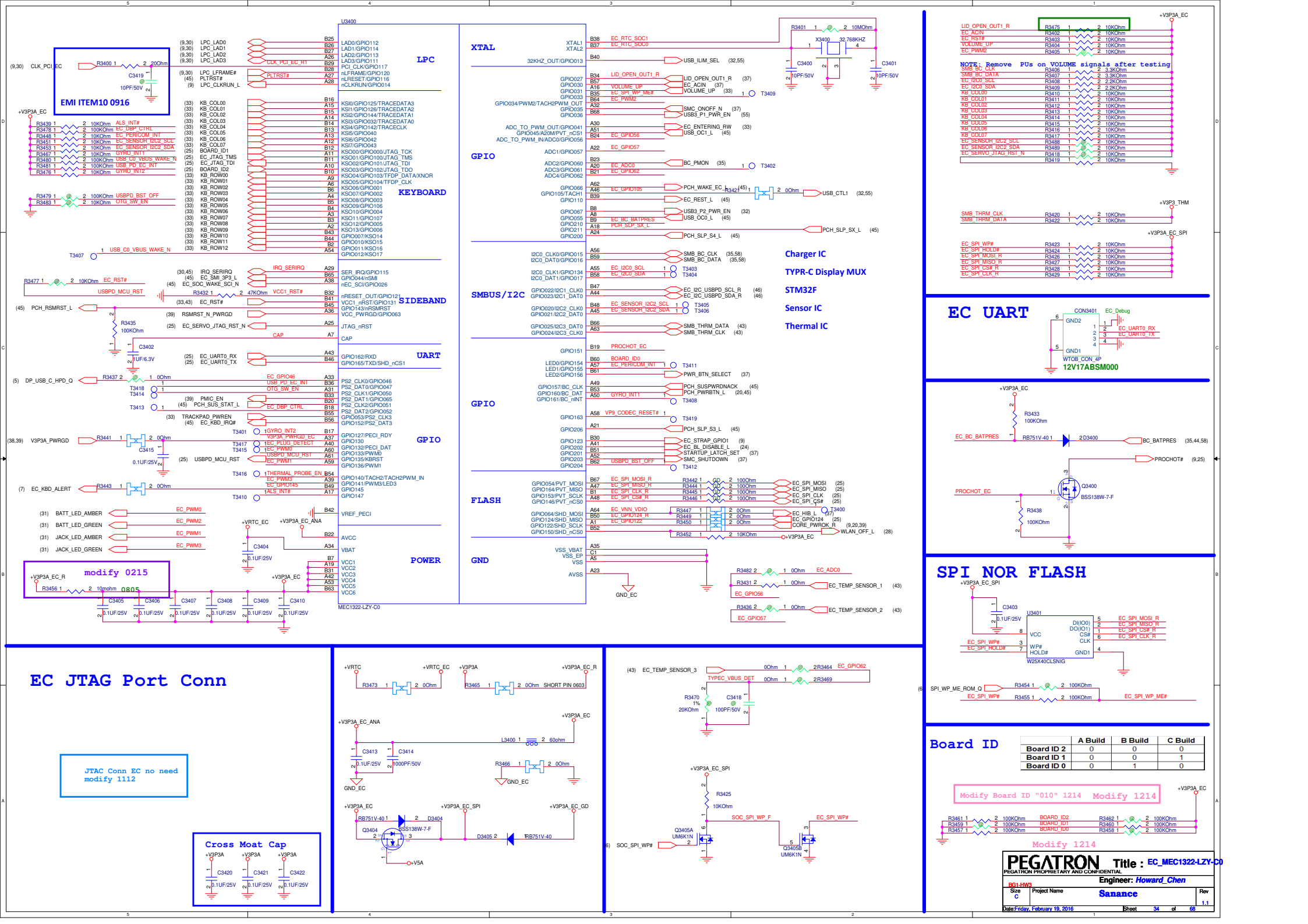
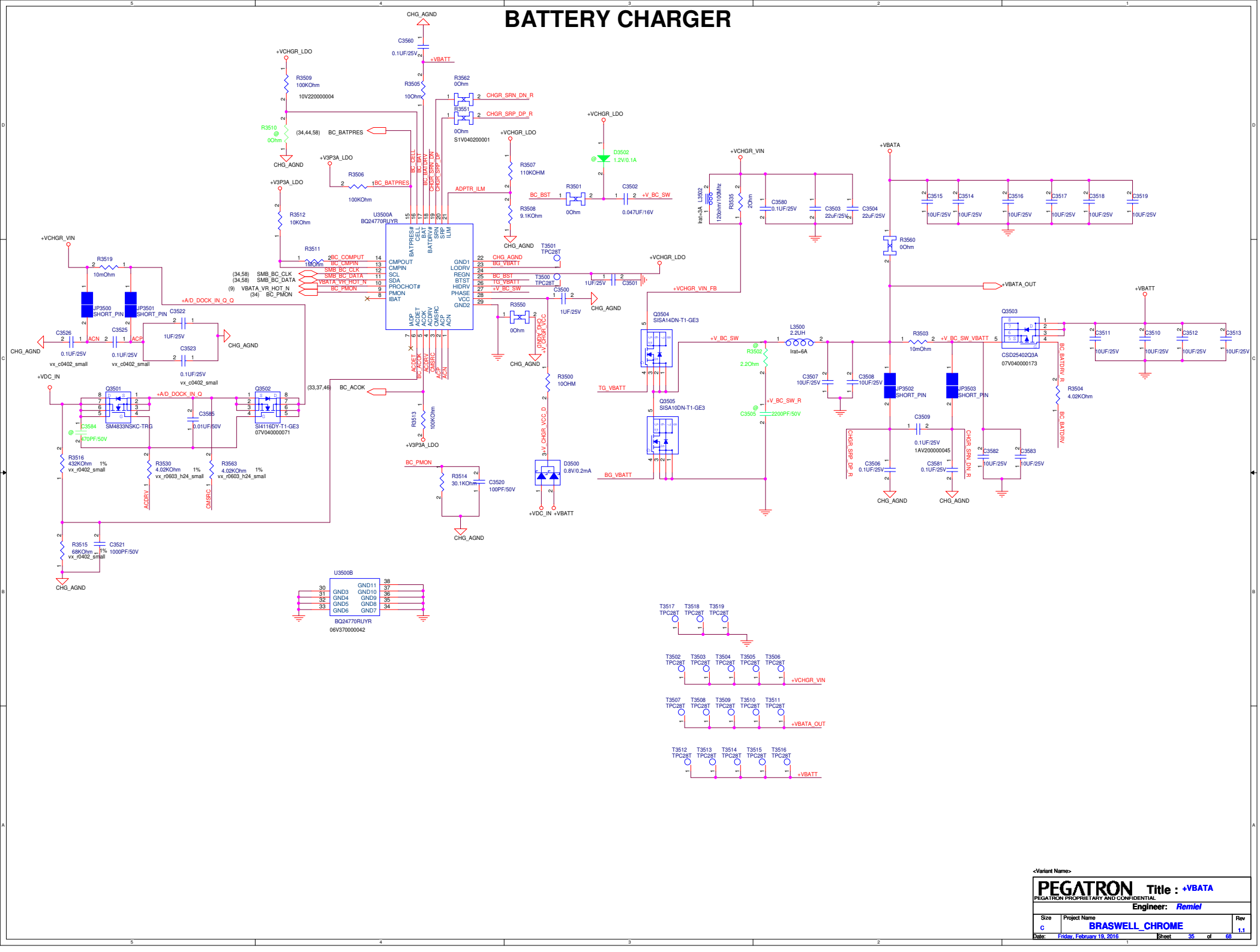

EMI ITEM10 0916
modify 0215
0805
JTAC Conn EC no need modify 1112
Cross Moat Cap
EC JTAG Port Conn
EC UART
SPI NOR FLASH
Board ID
Modify Board ID "010" 1214 Modify 1214
Modify 1214
Charger IC
TYPR-C Display MUX
STM32F
Sensor IC
Thermal IC
12V17ABSM000
NOTE: Remove PUs on VOLUME signals after testing
MEC1322-LZY-C0
LPC
KEYBOARD
SIDEBAND
UART
GPIO
SMBUS/I2C
FLASH
POWER
GND
XTAL
PEGATRON
Title : EC_MEC1322-LZY-C0
Engineer: Howard_Chen
Sanance
Date: Friday, February 19, 2016

BATTERY CHARGER



<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : +VBATA

Engineer: Remiel

Size	Project Name	Rev
C	BRASWELL_CHROME	1.1

Date: Friday, February 19, 2016 Sheet 35 of 68

PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: *Howard_Chen*

BG1-HW3

Size	Project Name	Rev
B	**Sanance**	1.1

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POWERON and WAKE SEQUENCING

Remove DB_PWRBTN_L
0910

+V3P3A_LDO
R3701
100KOhm
PWR_BTN_L
(25,33,58) PWR_BTN_L
C3700
0.1UF/25V
U3700
74AHC1G04GW
06V030000071
PWR_BTN_L
PWR_BTN
+V3P3A_EC
R3700
10KOhm
SMC_ONOFF_N (34)
Q3700
BSS138W-7-F
+V3P3A_LDO
C3701
0.1UF/25V
U3701
NC7SZ175L6X
STARTUP_FF_CLEAR_N
V5A_EN_OR
+V3P3A_LDO
R3707
100KOhm
Q3702
BSS138W-7-F
SMC_SHUTDOWN (34)
R3710
100KOhm
R3704
10KOhm
(34) STARTUP_LATCH_SET
R3705
10KOhm
+V3P3A_LDO
R3706
100KOhm
Q3701
@
BSS138W-7-F
R3709
0Ohm
(34) PWR_BTN_SELECT
(33) KB_PWR_BTN_L
R3711
@
1MOhm
U3702
NC7SZ332P6X
R3708
0Ohm
OR_INPUT_PD
BC_ACOK
STARTUP_LATCH_SET
+V3P3A_LDO
C3702
0.1UF/25V
R3703
@
0Ohm
D3700
0.8V/0.2mA
V5A_EN (38)
C3703
0.1UF/25V
WAKE_V5A_EN
D3701
@
RB751V-40
+V3P3A_LDO
R3712
100KOhm
C3704
0.1UF/25V
U3703
TC7SZ14FU
EC_WAKE
(34) EC_HIB_L
R3717
10KOhm
C3705
0.1UF/25V
U3704
SN74LVC2G02DCUR
NL27_B1_Y2
WAKE_V5A_EN_R
+V3P3A_LDO
R3713
100KOhm
R3714
0Ohm
C3706
0.1UF/25V
(34) EC_ACIN
D37021
RB751V-40
(33,35,46) BC_ACOK
C37071
@
0.1UF/25V
Q3703
@
BSS138W-7-F
C3709
0.1UF/25V
R3715
@
47KOhm
Q3704
BSS138W-7-F
(31,33) LID_OPEN_OUT1_L
C37082
0.01UF/25V
LID_OPEN_OUT1_L_FET
D3703
RB751V-40
R3716
47KOhm
LID_OPEN_OUT1_R (34)

EC HIB WAKE SOURCES

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWERON and

BG1-HW3

Engineer: Howard Chen

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 37 of 68

+5VO & +3VO POWER SUPPLY

+V5A

IC SPEC 6A

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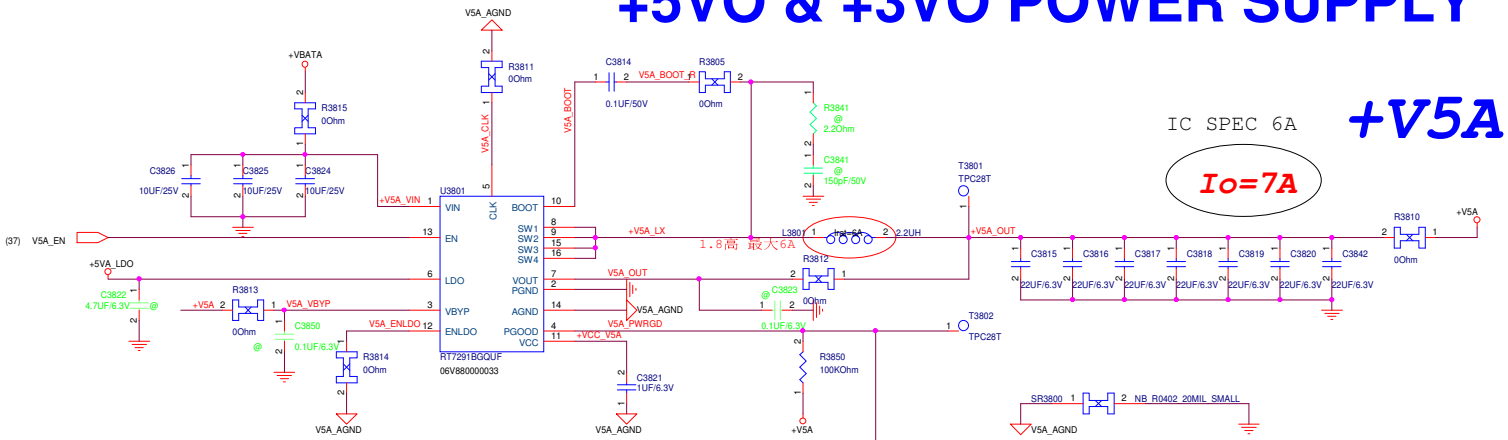
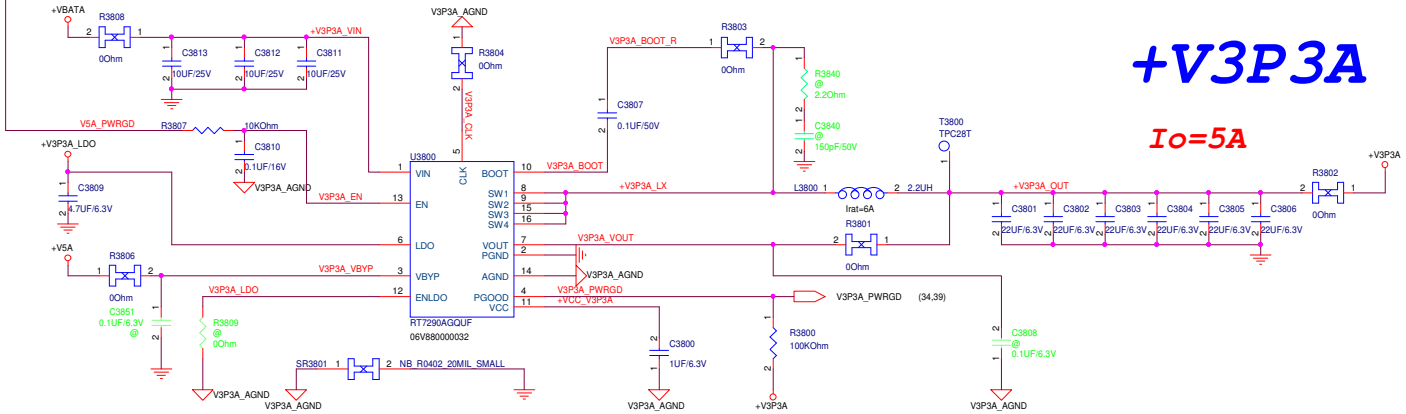
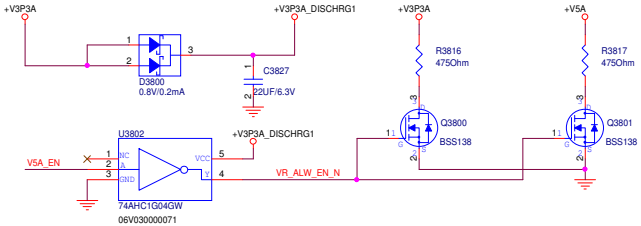


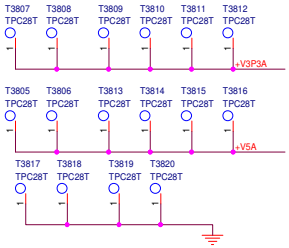
+V3P3A

Io=5A



DISCHARGE CKT





<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL

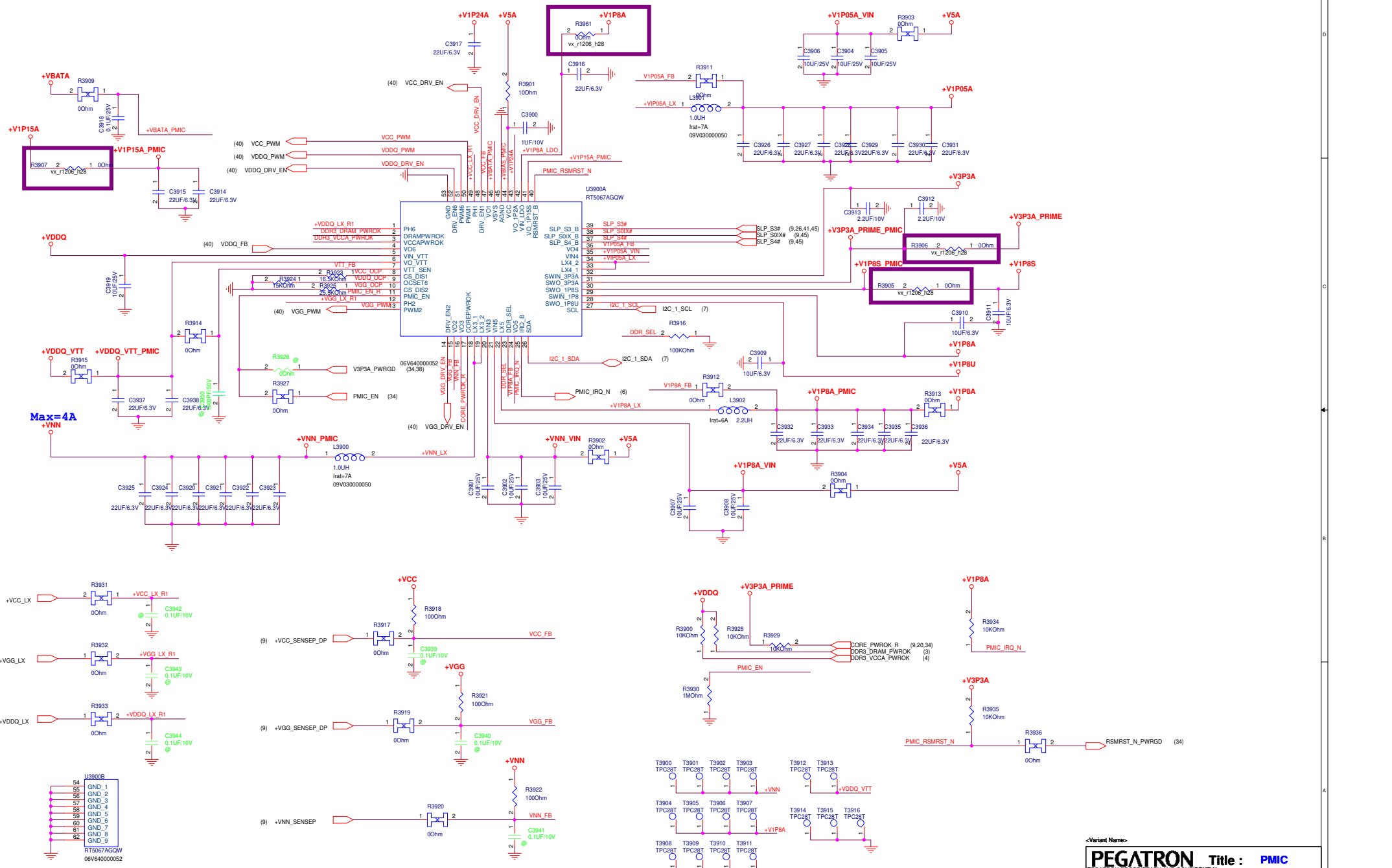
Title : +V3P3A +V5A

Engineer: Remiel

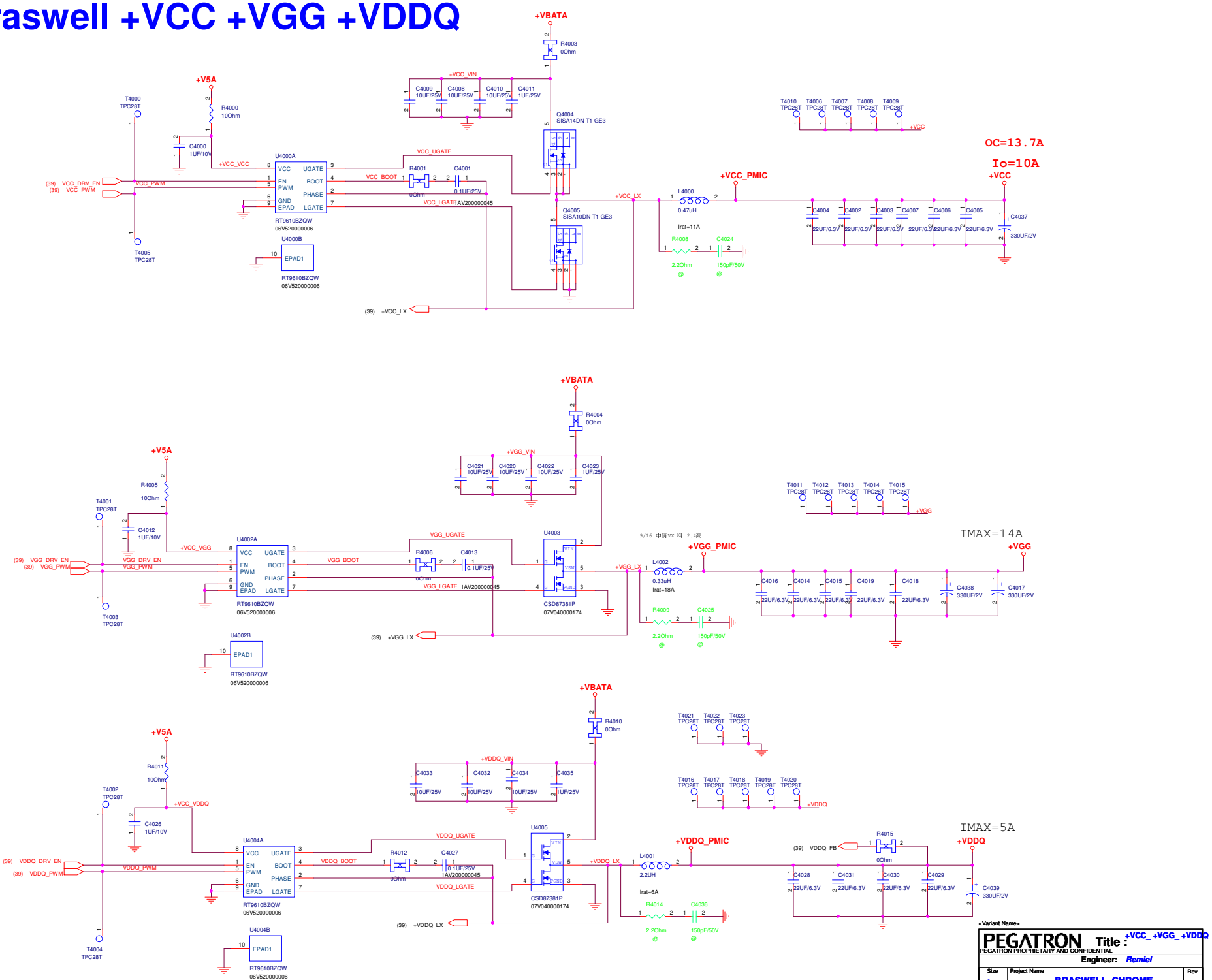
Size	Project Name	Rev
C	BRASWELL_CHROME	1.1

Date: Friday, February 19, 2016 Sheet 38 of 68

PMIC


+VBATA
+V1P15A
+V1P15A_PMIC
+VDDQ
+VDDQ_VTT
+VDDQ_VTT_PMIC
Max=4A
+VNN
+VNN_PMIC
+V1P24A
+V5A
+V1P8A
+V1P05A_VIN
+V1P05A
+V3P3A
+V3P3A_PRIME
+V3P3A_PRIME_PMIC
+V1P8S_PMIC
+V1P8S
+V1P8A_PMIC
+V1P8A_VIN
+V5A
U3900A
RT5067AGQW
U3900B
RT5067AGQW
06V640000052
+VCC
+VGG
+VNN
+VDDQ
+V3P3A_PRIME
+V1P8A
+V3P3A
+VNN
+VDDQ_VTT
+V1P8A
+V1P05A

Braswell +VCC +VGG +VDDQ



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Remiel

Title : +VCC_ +VGG_ +VDDQ

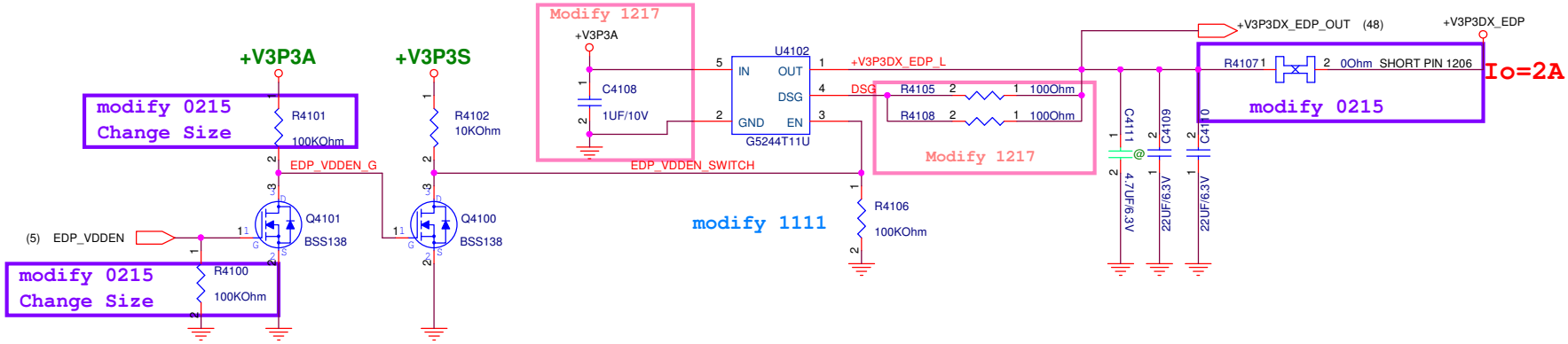
Size	Project Name	Rev
Custom	BRASWELL_CHROME	1.1

Date: Friday, February 19, 2016 Sheet 40 of 68

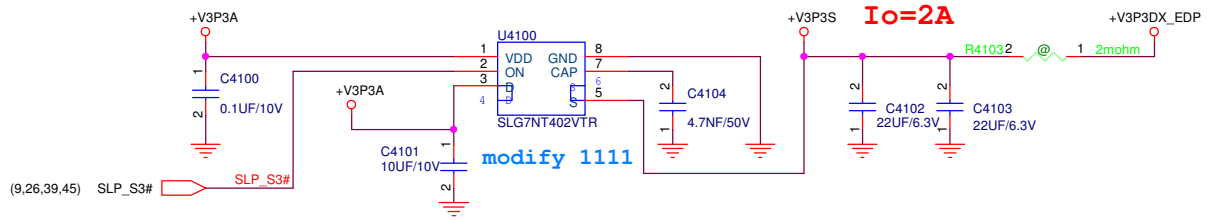
<Variant Name>

POWER GATE

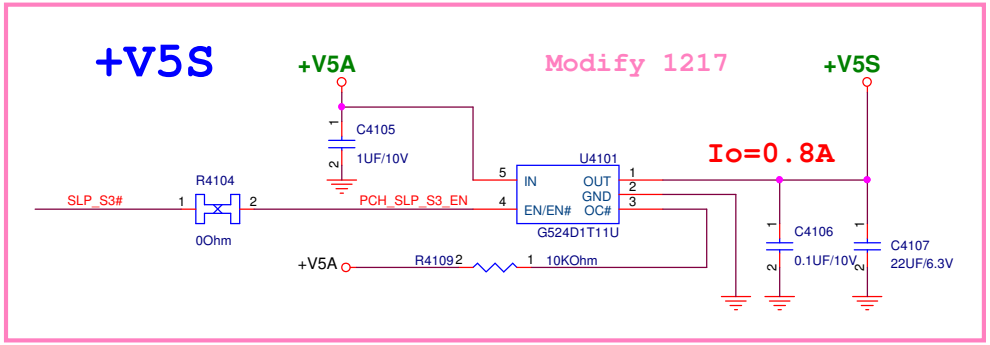
+V3P3DX_EDP



+V3P3S



+V5S



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER GATE

BG1-HW3

Engineer: Remiel

Size	Project Name	Rev
B	BRASWELL_CHROME	1.1

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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : **********

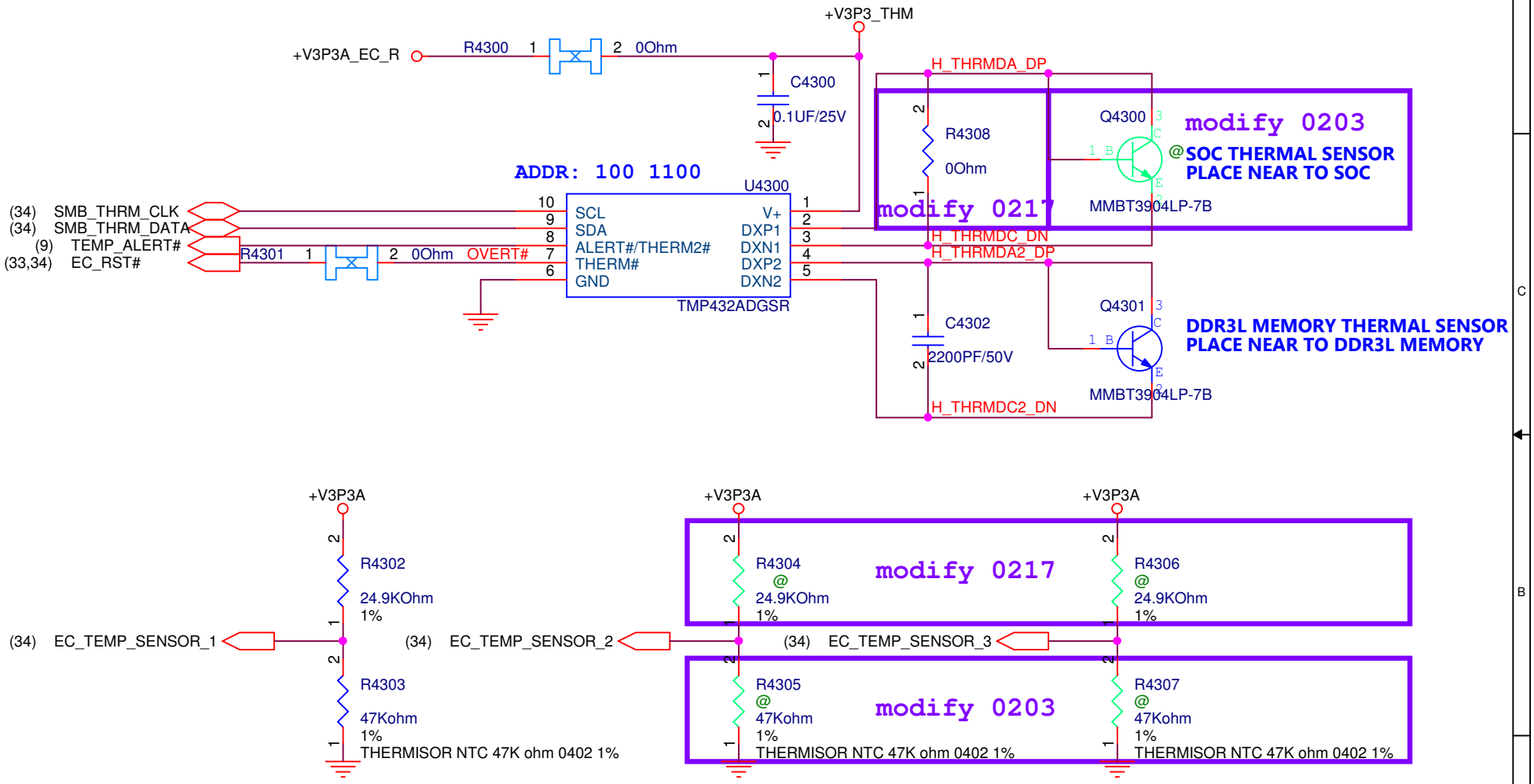
Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 42 of 68

Thermal Sensor(THM)



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : THERMAL_SENSOR

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

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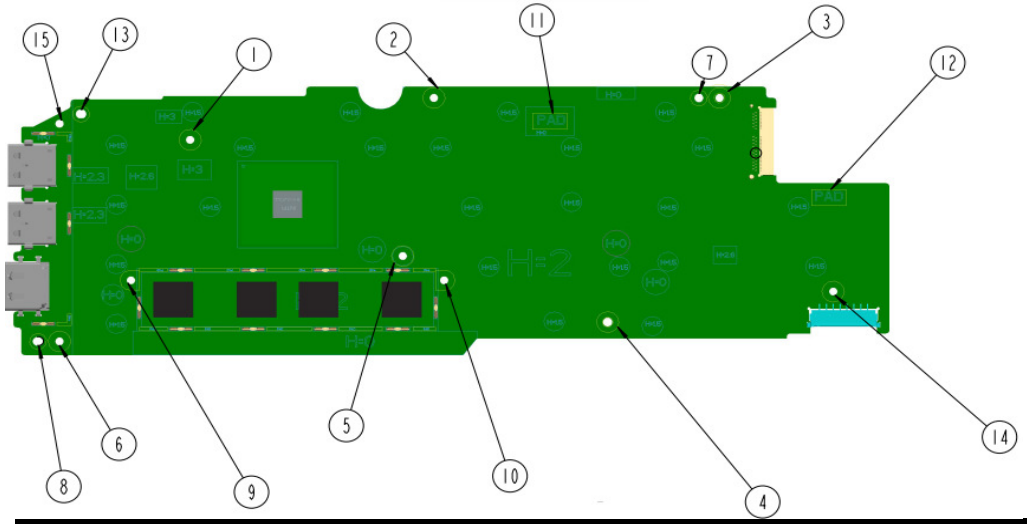
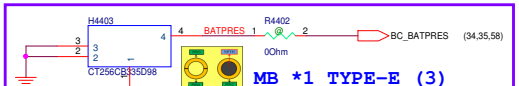
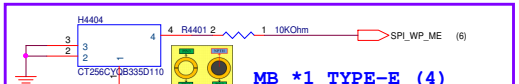


	PTH/NPTH	Ø	TOP PAD	BTM_PAD	
1	PTH	2.5	6.5	6.5	
2	PTH	2.5	6.5	6.5	
3	PTH	2.5	3.2/6.5	See No.3	
4	PTH	2.8	3.2/6.5	See No.4	
5	PTH	2.5	6.5	6.5	
6	PTH	2.5	6.5	6.5	
7	PTH	2.5	5.0	3.0	
8	PTH	2.7 L3.2	5.0	N/A	
9	PTH	2.5	See No.9	N/A	
10	PTH	2.5	See No.10	N/A	
11			See No.11		
12			See No.11		
13	PTH	2.7 L3.2	5.0	N/A	
14	PTH	2.5	6.5	6.5	
15	NPTH	2.5	N/A	N/A	

MB *4pcs TYPE-A (1,2,5,6,14)

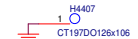


MB *1 TYPE-E (3)



MB *1 TYPE-E (4)

MB *1pcs TYPE-D (7)

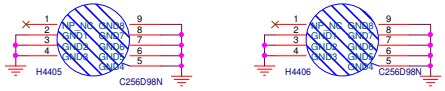


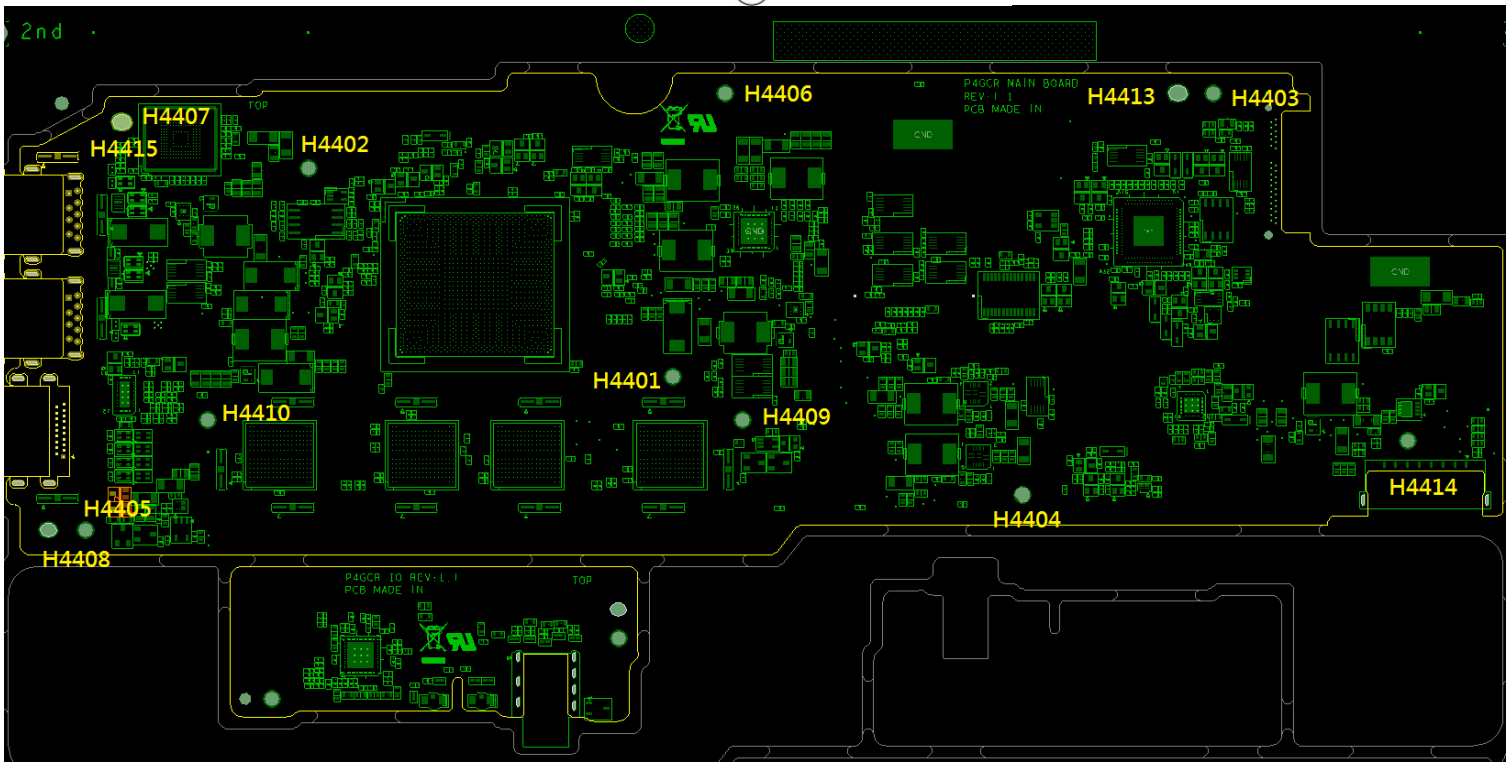
MB *2pcs TYPE-G (11,12)

MB *2pcs TYPE-C (8,13)

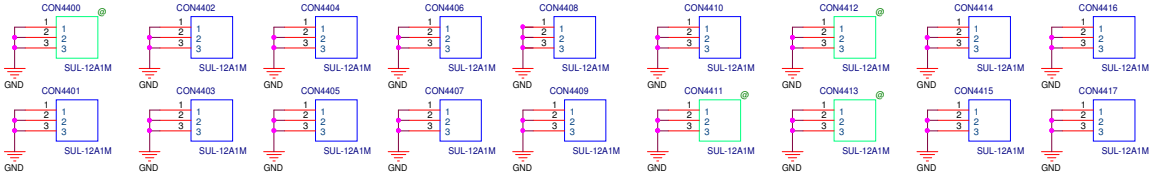
MB *2pcs TYPE-B (9,10)

New Part **modify 1116**

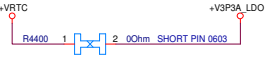




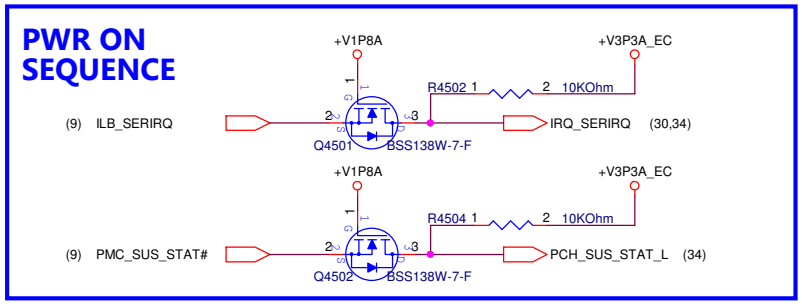
Shelding Case PAD ME Change material modify 1113

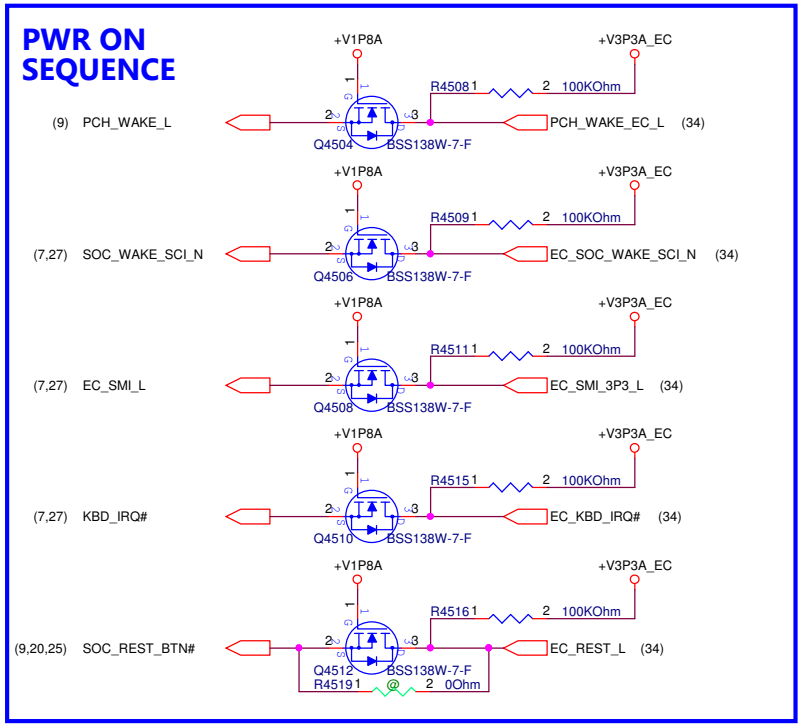


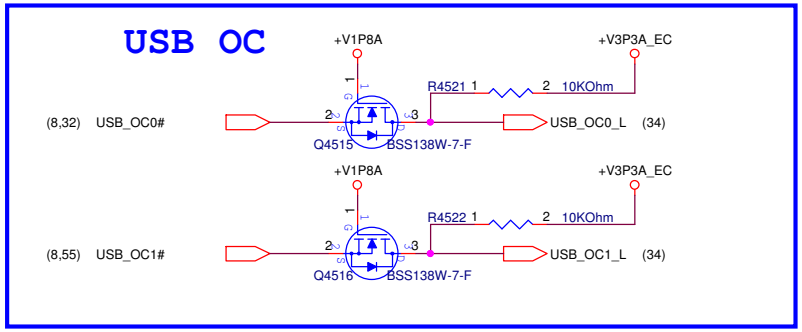
RTC CIRCUIT

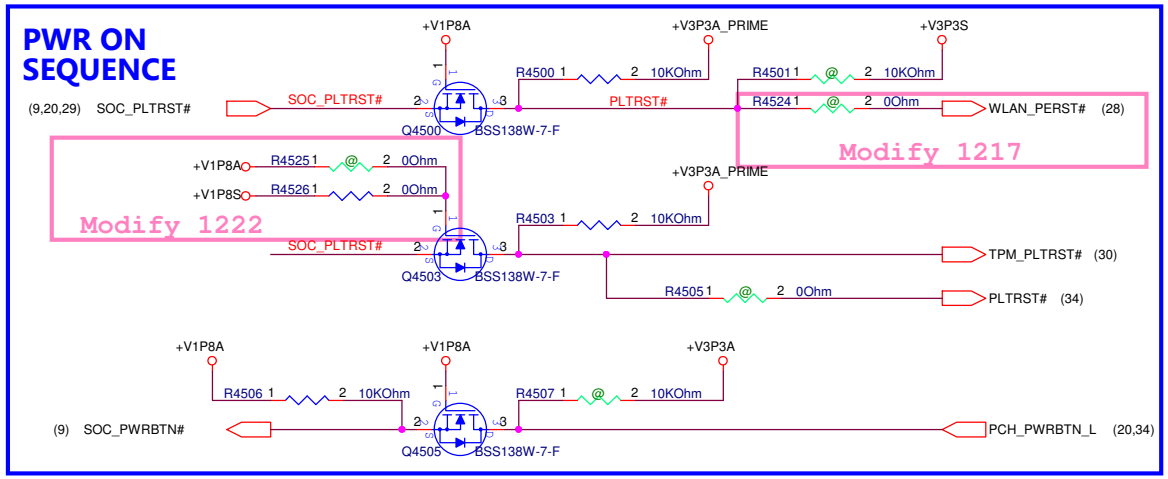


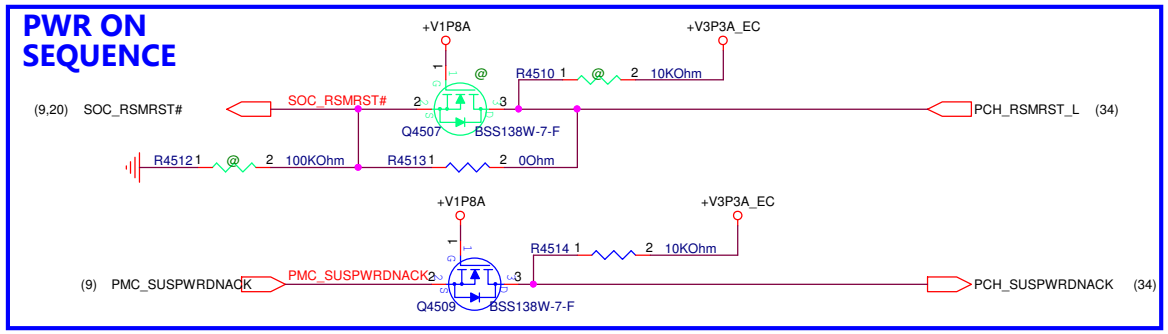
PEGATRON Title : MB_ME_SCREW_RTC
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Howard_Chen
BG1-HW3
Size C | Project Name Sanance | Rev 1.1
Date: Friday, February 19, 2016 | Sheet 44 of 68

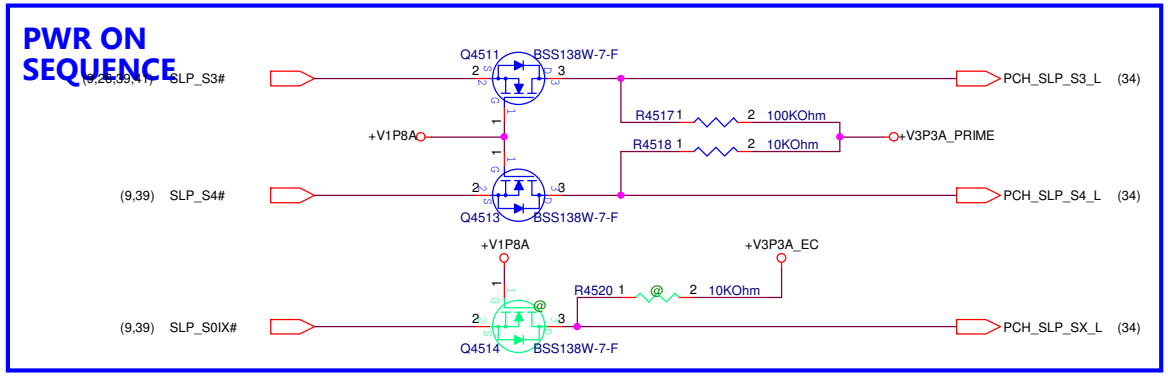


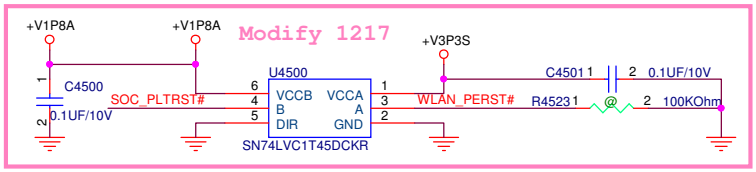












PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LEVEL SHIFT (1)

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

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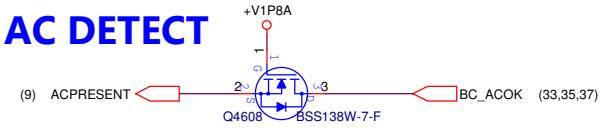
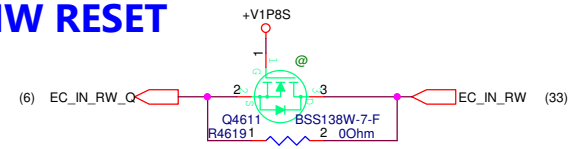
LTE

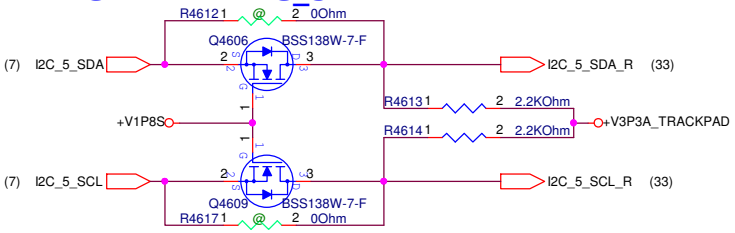
AC DETECT



HW RESET

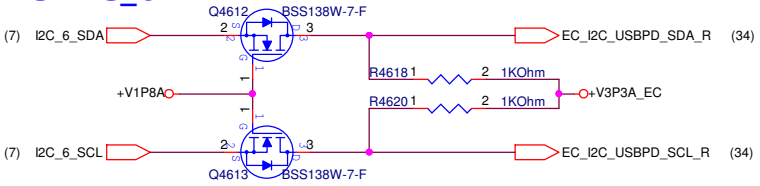


TRACK PAD I2C_5

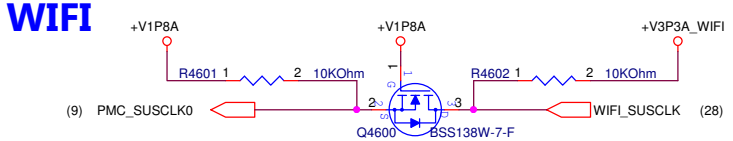


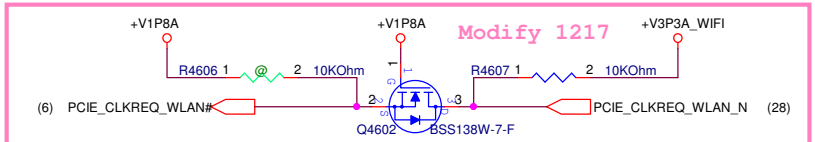
EC I2C_6

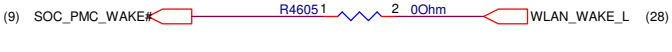
Check

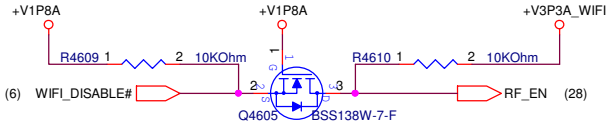


WIFI

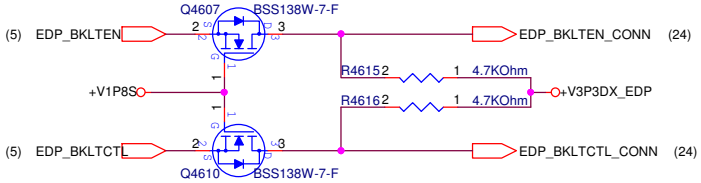








eDP CONTROL PIN



TOUCH SCREEN I2C_0

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LEVEL SHIFT (2)

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

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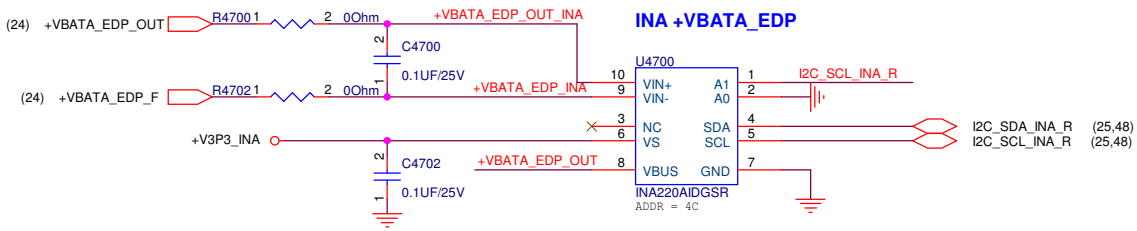
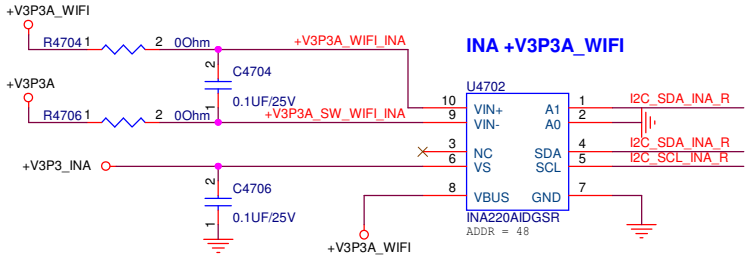
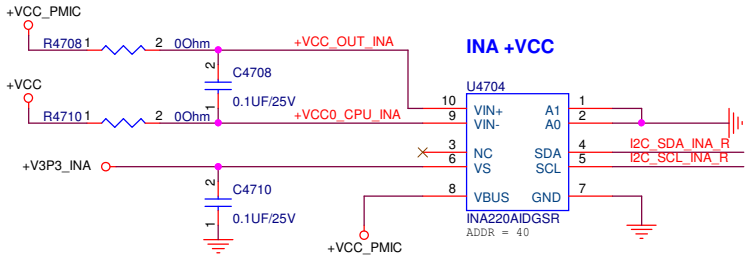
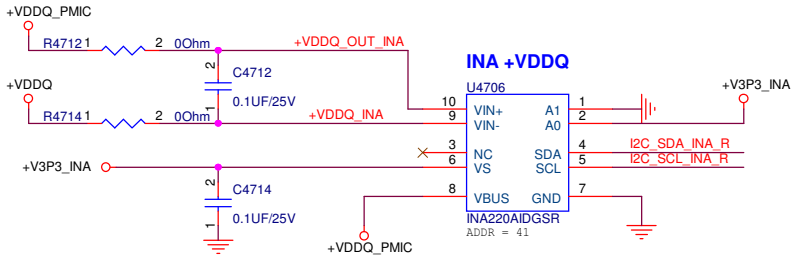
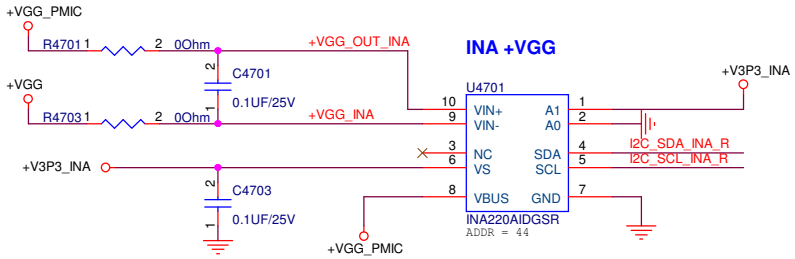
INA DEVICES 1

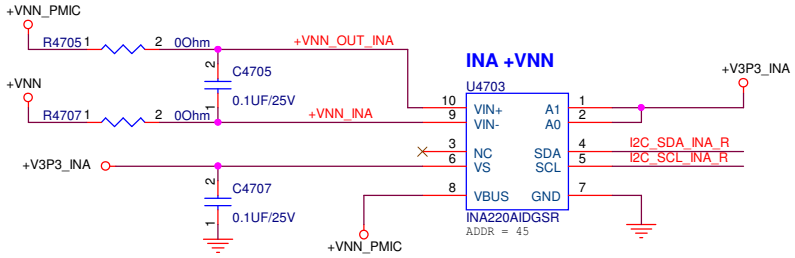


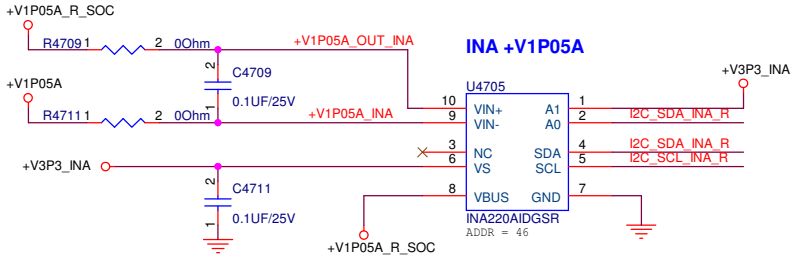


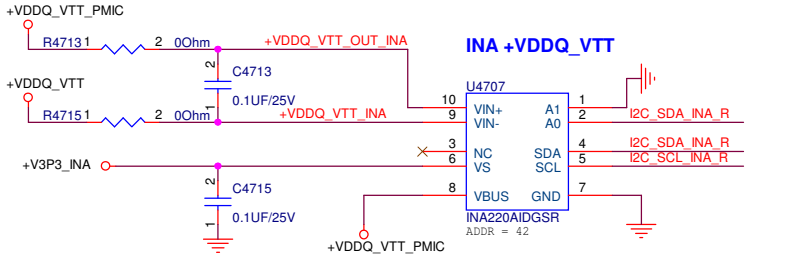












PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : INA DEVICES 1

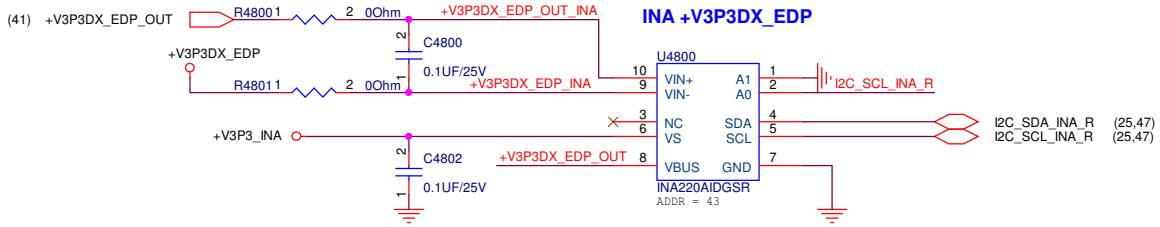
Engineer: Howard_Chen

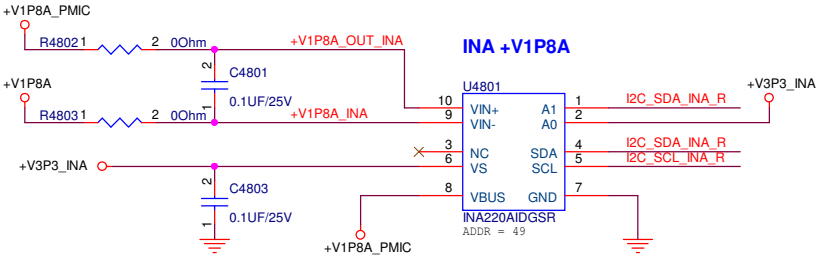
BG1-HW3

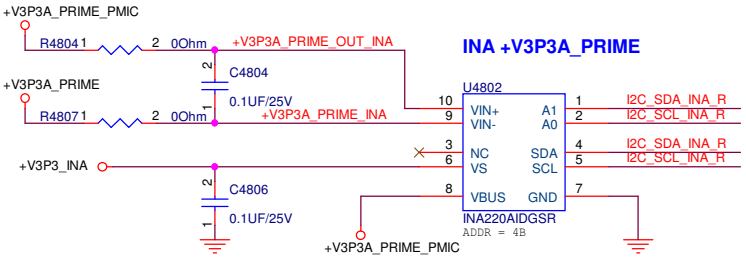
Size	Project Name	Rev
B	Sanance	1.1

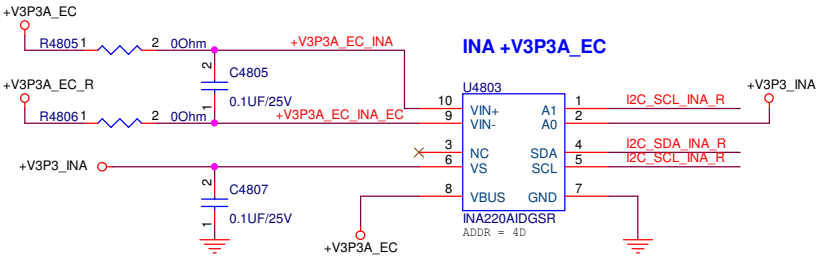
Date: Friday, February 19, 2016 Sheet 47 of 68

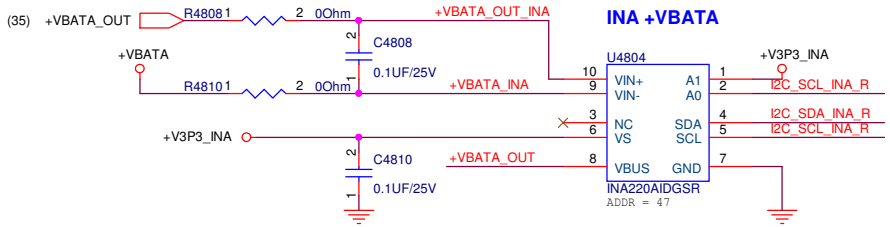
INA DEVICES 2

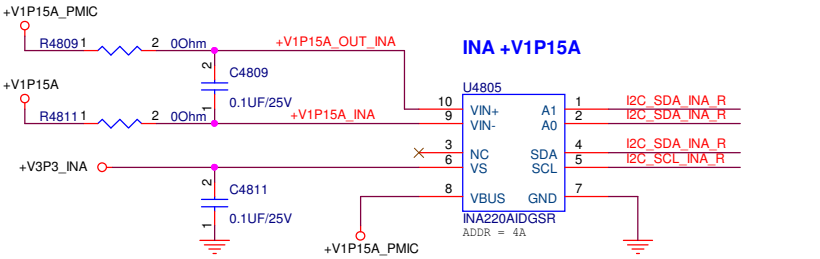












Howard_Chen

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : INA DEVICES 2

Engineer:

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

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PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

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PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

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PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : **********

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 51 of 68

KEPLER

PEGATRON

Title : KEPLER

Engineer: *Howard_Chen*

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 52 of 68

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : VIDEO CODEC

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

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R2.0 modify List

update dsn 0203 1000 modify Page20,remove CON2000 (Joe Lo)[2016/02/03 上午 09:56:24]

update dsn 0203 1130 Q4300,4301換Symbol page20 測點 (Joe Lo)[2016/02/03 上午 11:46:03]

update dsn 0203 1300 update dsn 0203 1300 (Joe Lo)[2016/02/03 下午 01:14:32]

PEGATRON Title : LIST

BG1-HW3

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1

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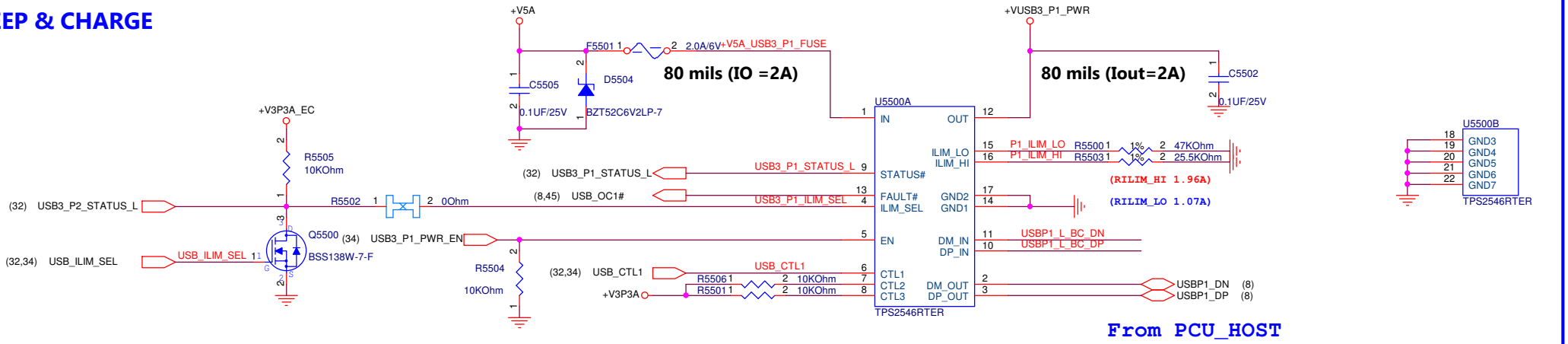
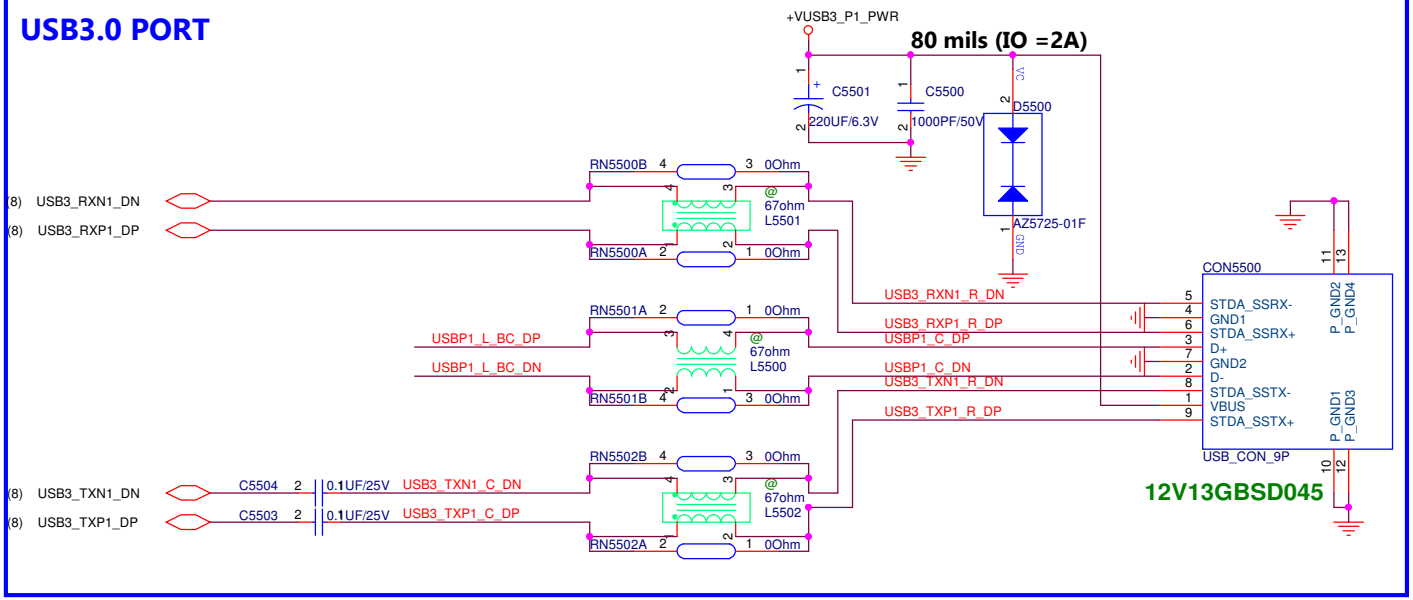
USB 3.0 PORT1 and CHARGER(MB)

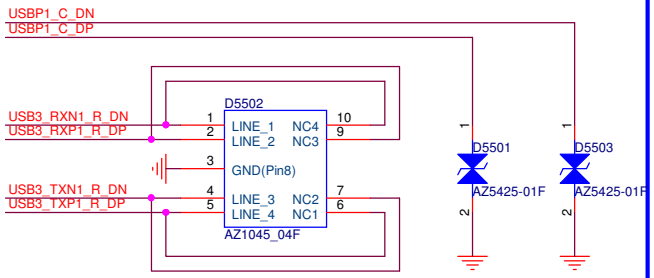
SLEEP & CHARGE



USB3.0 PORT



ESD CHIP



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : USB30 PORT & CHARG

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
B	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 55 of 68

PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer:

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

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PEGATRON

Title : **********

PEGATRON PROPRIETARY AND CONFIDENTIAL

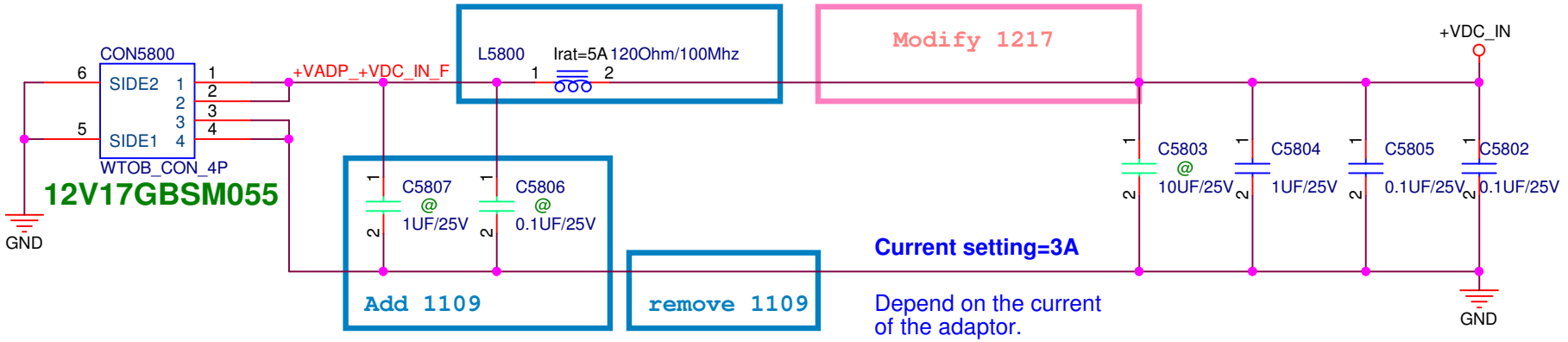
Engineer:

BG1-HW3

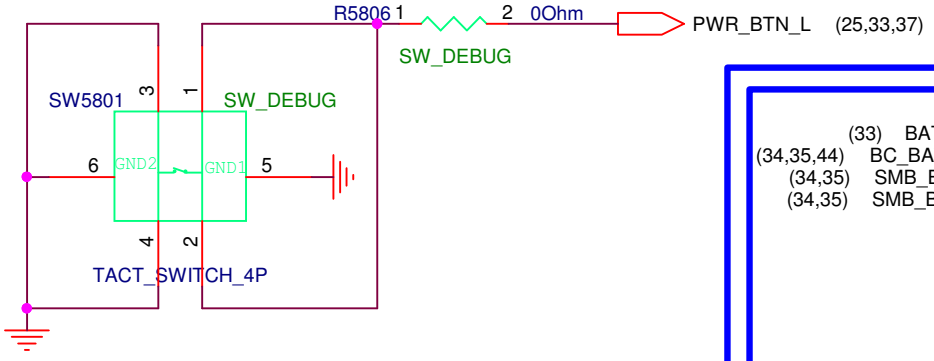
Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 57 of 68

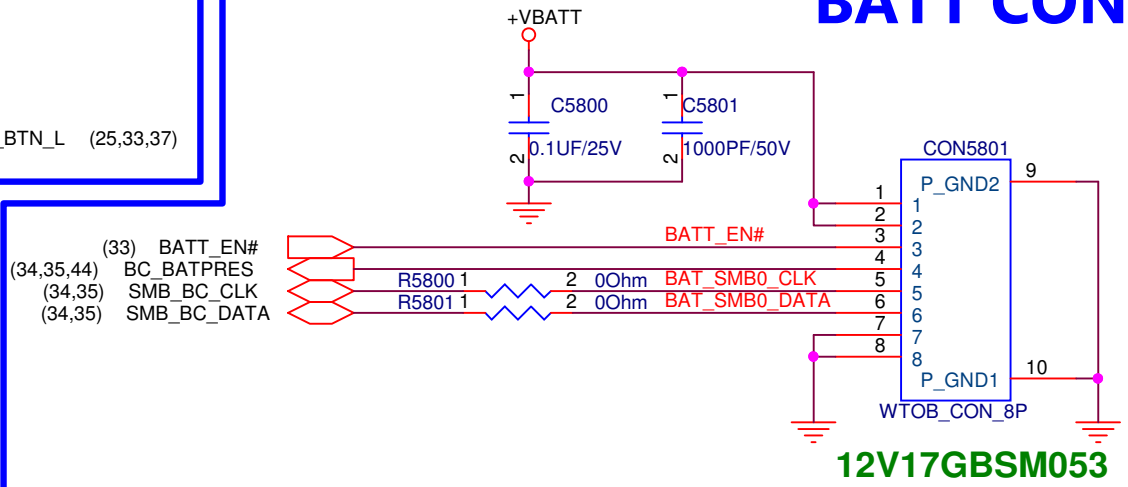
DC Jack CONN



PWR BTM (Without KB)



BATT CONN



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DC & BAT_CONN

Engineer: Howard_Chen

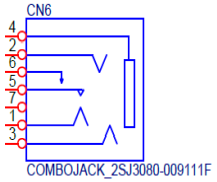
BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 58 of 68

HEADPHONE/Mic combo (ADO)

combo jack
Normal open
P/N: DFTJ06FR652
PIN1 --> L?
PIN2 --> R?
PIN3 --> GND/MIC?
PIN4 --> MIC/GND?
PIN5 --> JD?
PIN6 --> GND?
PIN7 --> Shielding?



(64) MICBIAS1
(64) CODEC_IN1_P_RING2
(64) HP_OUT_L_FB
(64) HP_OUT_R_FB
(64) CODEC_IN1_N_SLEEVE
(64) MICBIAS2

DR1051 2 2.2KOhm
DR1041 2 33Ohm
DR1021 2 33Ohm
DR1061 2 2.2KOhm
DL100 1 2 100ohm
DL103 1 2 100ohm
DL102 1 2 100ohm
DL101 1 2 100ohm
A_GND DR1001 @ 2 0Ohm

DC105 100PF/50V
DC106 100PF/50V
DC100 @ 10PF/50V
DC101 @ 10PF/50V
DC102 100PF/50V
DC103 100PF/50V

CONN_RING
HP_OUT_L
JACK_PLUG_DETECT
HP_OUT_R
CONN_SLEEVE

DCON100
PHONE_JACK_7P
12V14GBSD098

2AUDIO_JACK_JD
DR101 1KOhm

SOC DET (ADO)

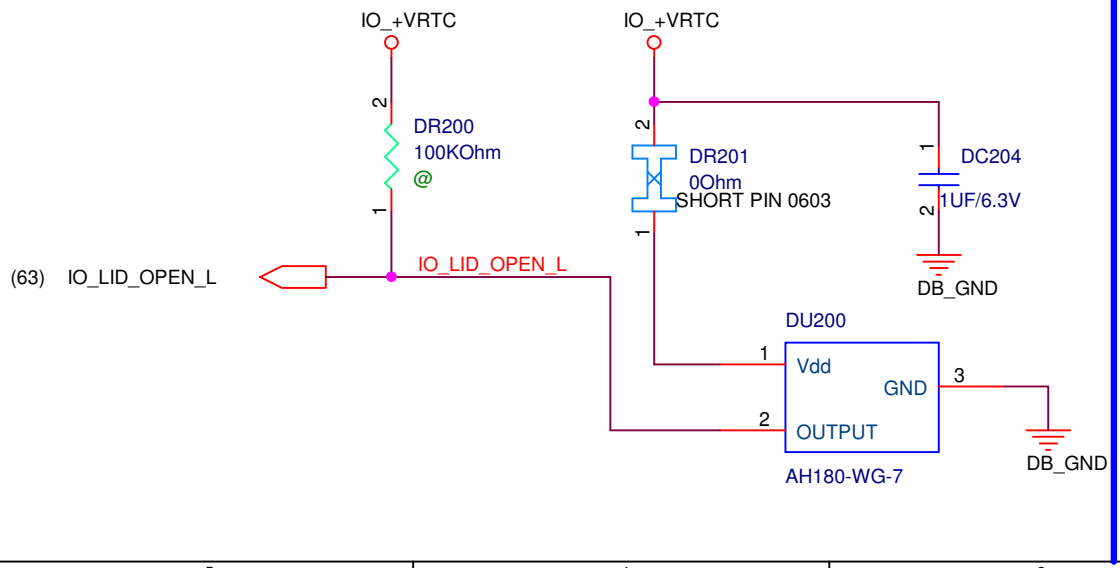
+V1P8_JD
DR1071 2 220KOhm
(63) IO_AUDIO_JACK_PRESENT
DR1031 @ 2 0Ohm
modify 1217
JACK_PLUG_DETECT
DC104 0.1UF/25V
(64) CODEC_JD
DR1081 2 0Ohm

DD100 GND 1 2 VC
DD101 GND 1 2 VC
DD102 GND 1 2 VC
DD103 GND 1 2 VC
DD104 GND 1 2 VC
AZ5725-01F

EMI ITEM1 0917

PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : AUDIO JACK		
BG1-HW3	Engineer: Howard_Chen		
Size A	Project Name Sanance		Rev 1.1
Date: Friday, February 19, 2016	Sheet 59 of 68		

LID Switch



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LID

Engineer: Howard_Chen

BG1-HW3

Size	Project Name	Rev
A	Sanance	1.1
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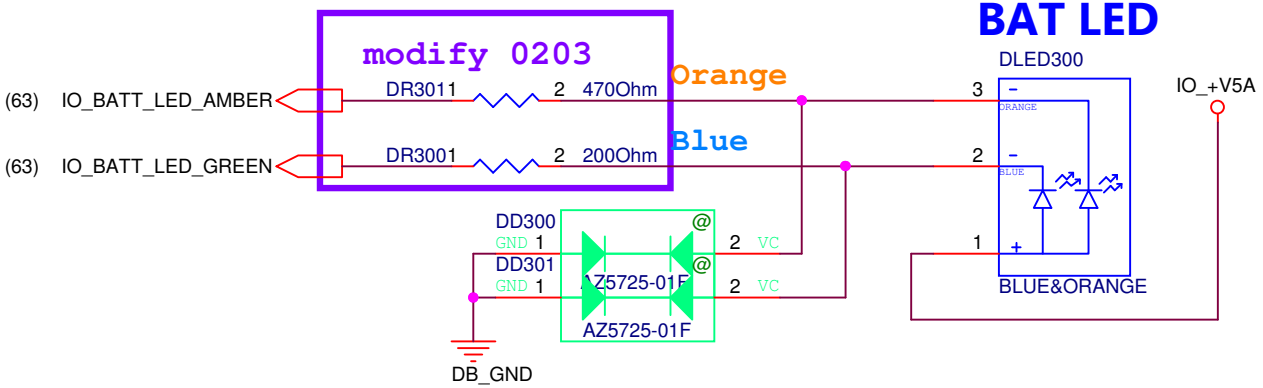
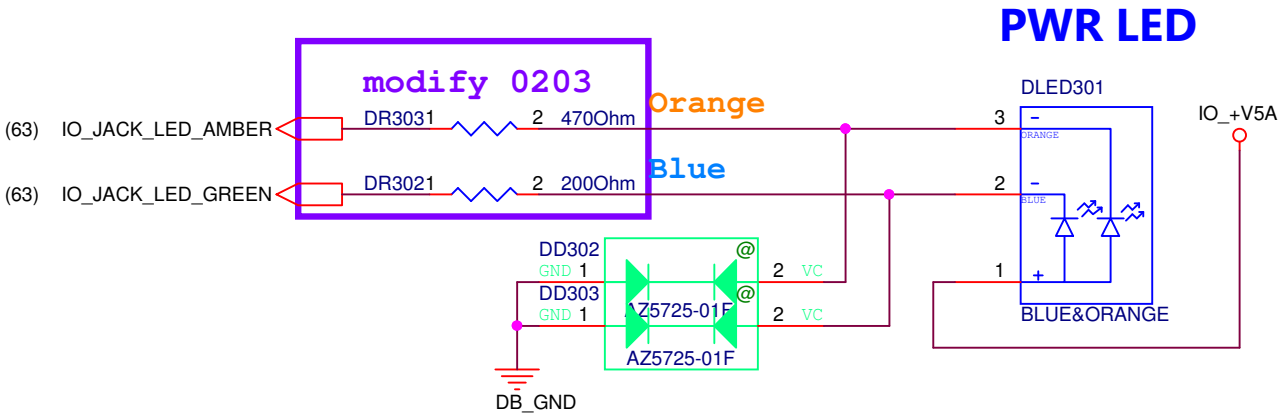
LED Display

BAT LED



PWR LED



PEGATRON

Title : LED

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1
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PEGATRON

Title : *****

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1
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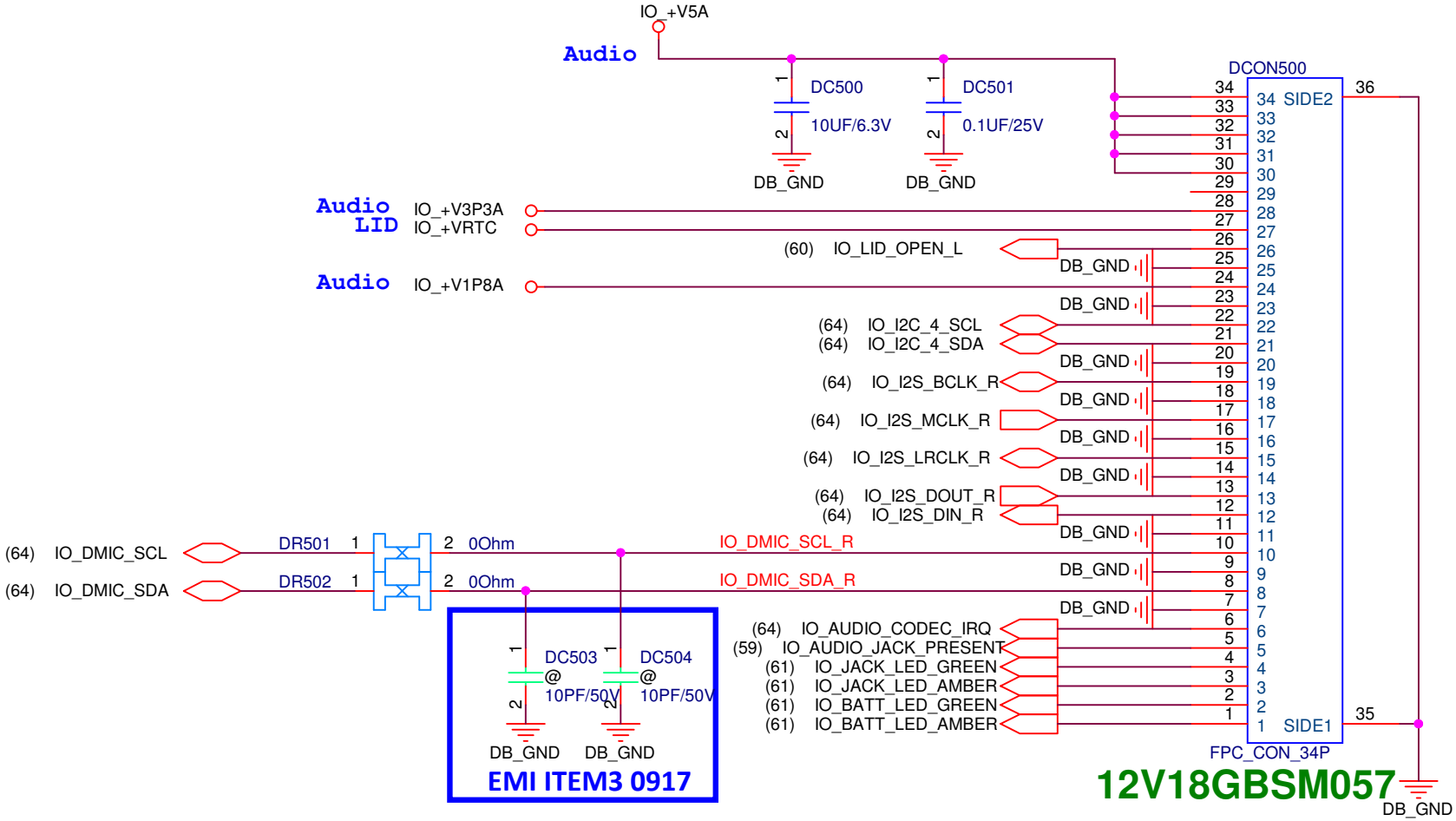
IO CONN (DB)



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3

Title : IO BD CONN

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1
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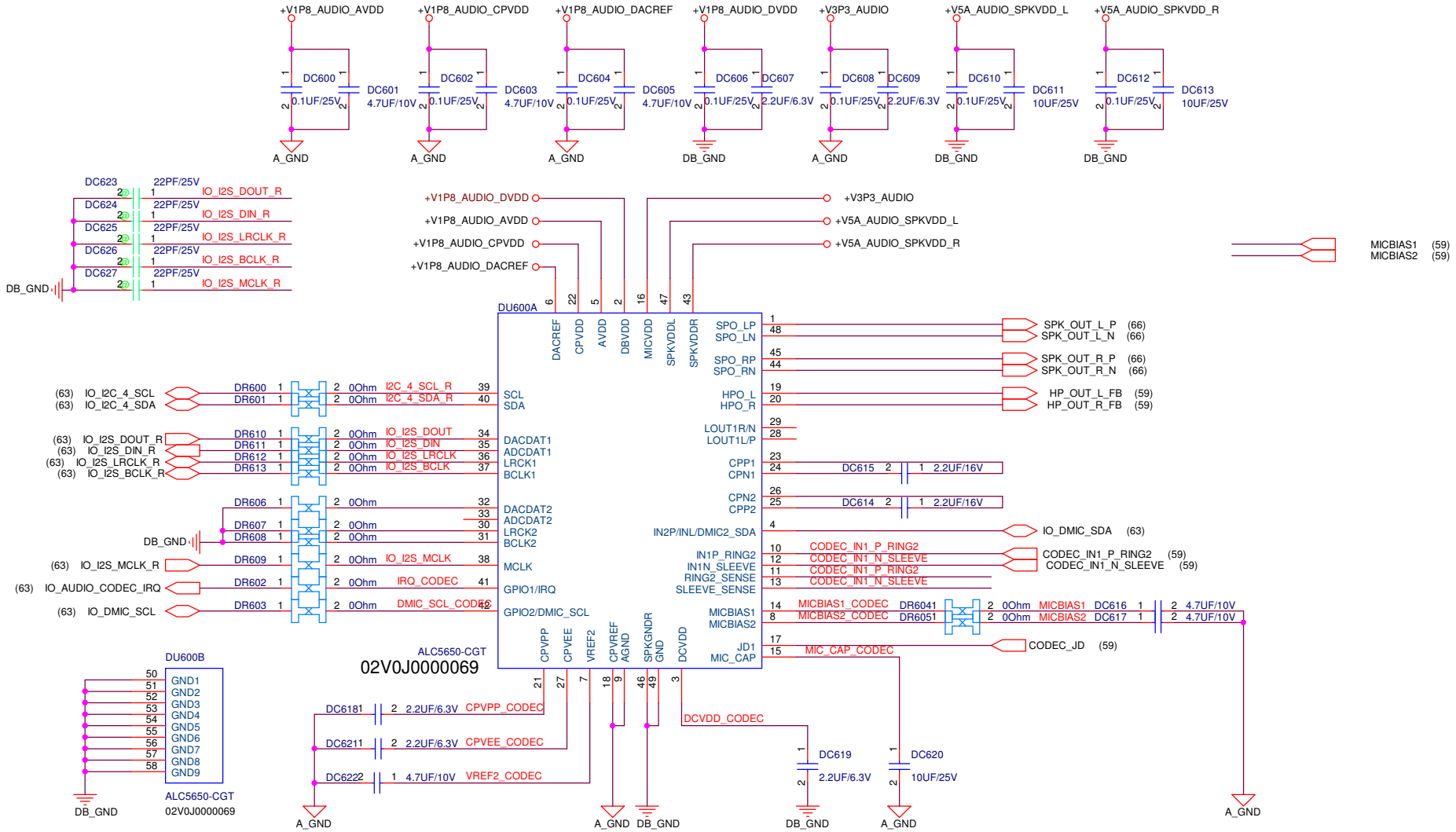

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3

Title : AUDIO CODEC

Engineer: Howard_Chen

Size	Project Name	Rev
B	Sanance	1.1

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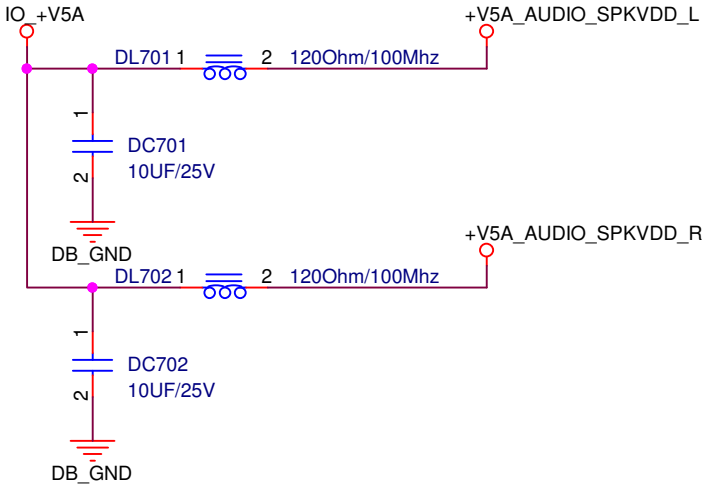
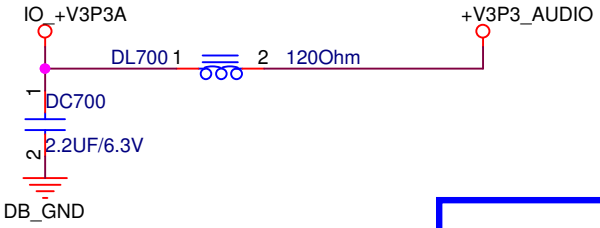
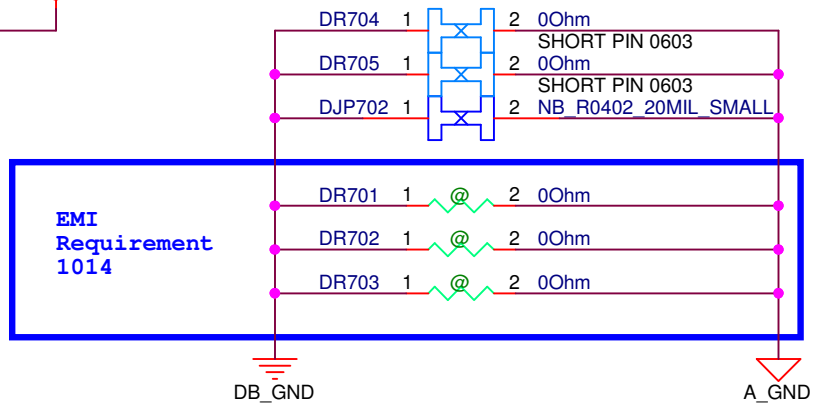
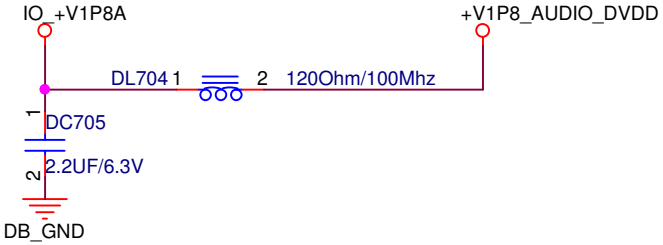
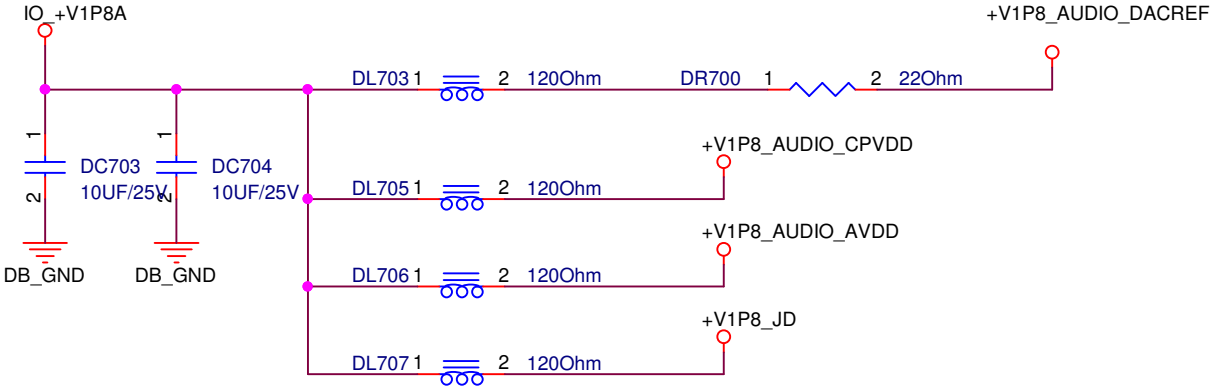
Codec PWR











PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3

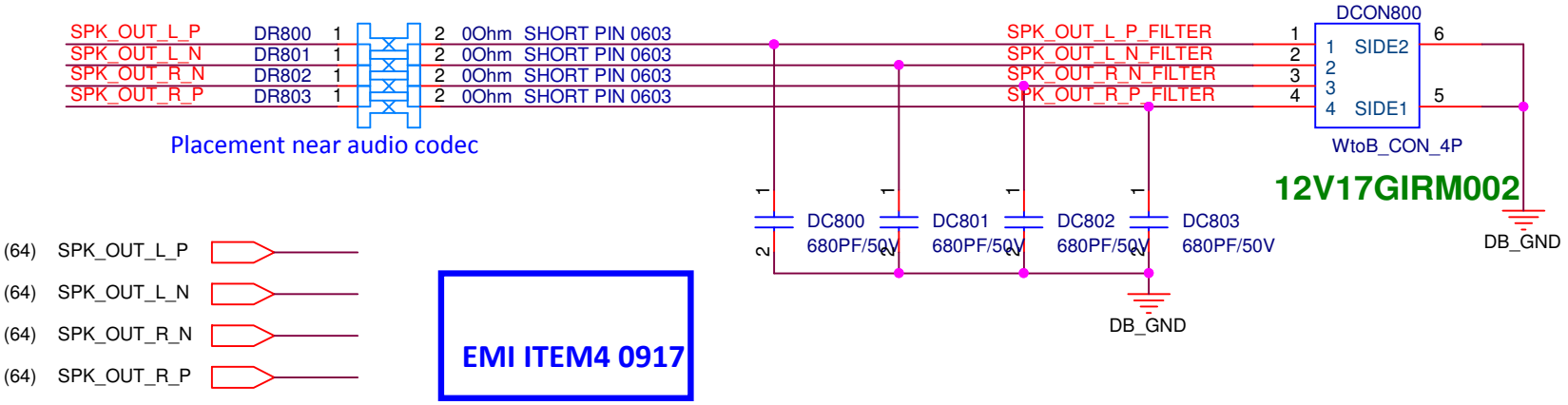
Title : AUDIO POWER

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1

Date: Friday, February 19, 2016 Sheet 65 of 68

Internal Speaker(ADO) -- > (2W)



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : SPEAKER

~~BG1-HW3~~

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1
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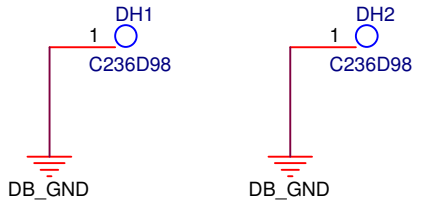
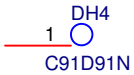
SB *2pcs TYPE-A (1,2)

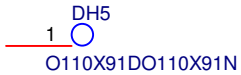


SB *2pcs TYPE-B (3,4)

modify 1116



SB *1pcs TYPE-C (5)



PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : SCREW HOLE

~~BG1-HW3~~

Engineer: Howard_Chen

Size	Project Name	Rev
A	Sanance	1.1
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A --> B Build

11/09.
(1) Change Symbol Q3405 to dual MOS symbol to do Level for SPI write protect.
(2) Change net name from SLP_S3# to PCH_SLP_S3_L .
(3) Modify DC-IN Circuit , remove L5801 ; add C5806 ,C5807 ; Change 5800 Bead material current to 5 Amp ; Set C5803 un-staff.
(4) Update Board ID for B Build stage (001)

PEGATRON Title :

History

Engineer:

Size	Project Name	Rev
C	Sanance	1.1

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