1. Schematic Page Description :

Origins Schematic Ver :

01

SoC I2C table

Function	Channel	Read	Write
NA	I2C0	0x?	
PMIC	I2C1	0x?	0x?
Audio codec	I2C4		
Track Pad	I2C5		
EC	I2C6		

EC SMBus/I2C table

Function	Channel	Address
Battery/charger	SMB0	
NA	SMB1	
PCH	I2C1	
NA	I2C2	
Thermal	I2C3	

Current sensor address

Function	Channel	Function	Channel
+VBATA	0x47	+VCC_OUT	0x40
+V5A	0x43	+VGG	0x44
+V3P3A	0x4B	+VNN	0x45
+V1P05A	0x46	+VDDQ_OUT	0x41
+V1P8A	0x49		

USB3/2 port mapping

USB3 Port No#	Usage	USB2 Port No#	Usage
USB3P0	NA	USB2P0	NA
USB3P1	I/O	USB2P1	I/O(3.0)
USB3P2	I/O	USB2P2	I/O(3.0)
USB3P3	NA	USB2P3	CCD
		USB2P4	BT

PCIe port mapping

PCIe port No#	Usage	PCIe CLK#	Usage
PCIe_0	NA	PCIe_CLK0	NA
PCIe_1	NA	PCIe_CLK1	NA
PCIe_2	WLAN	PCIe_CLK2	WLAN
PCIe_3	NA	PCIe_CLK3	NA

PROJECT : NL6D
Quanta Computer Inc.

Size	Document Number	Rev
	Sch Page description	1A

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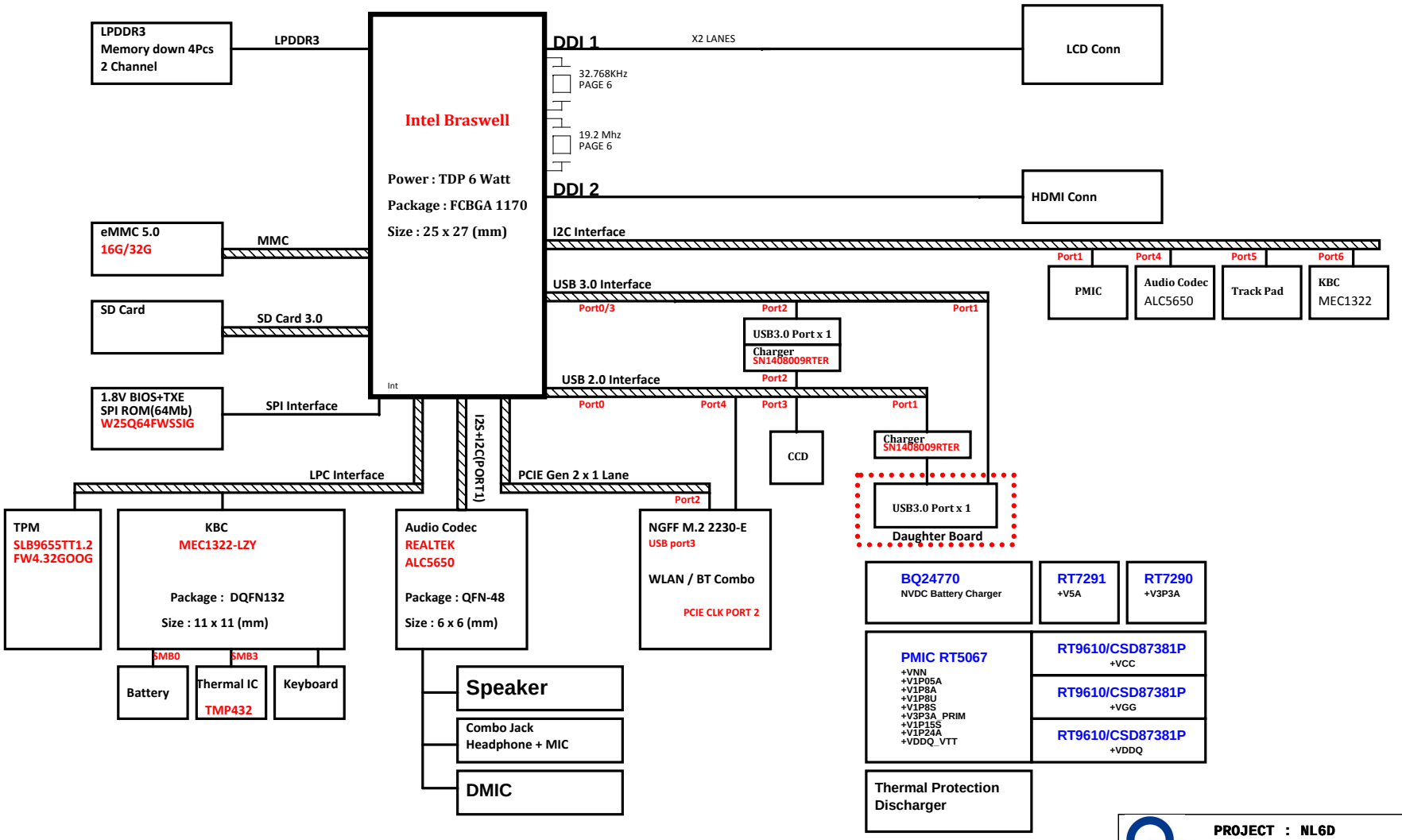
NL6D Chromebook
Intel Braswell Platform Block Diagram



PROJECT : NL6D
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Size	Document Number	Rev
	Block Diagram	1A

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PROJECT : NL6D

Quanta Computer Inc.

Size	Document Number	Rev
	Power Sequence	1A

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PROJECT : NL6D
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Size	Document Number	Rev
	SMBUS_I2C	1A
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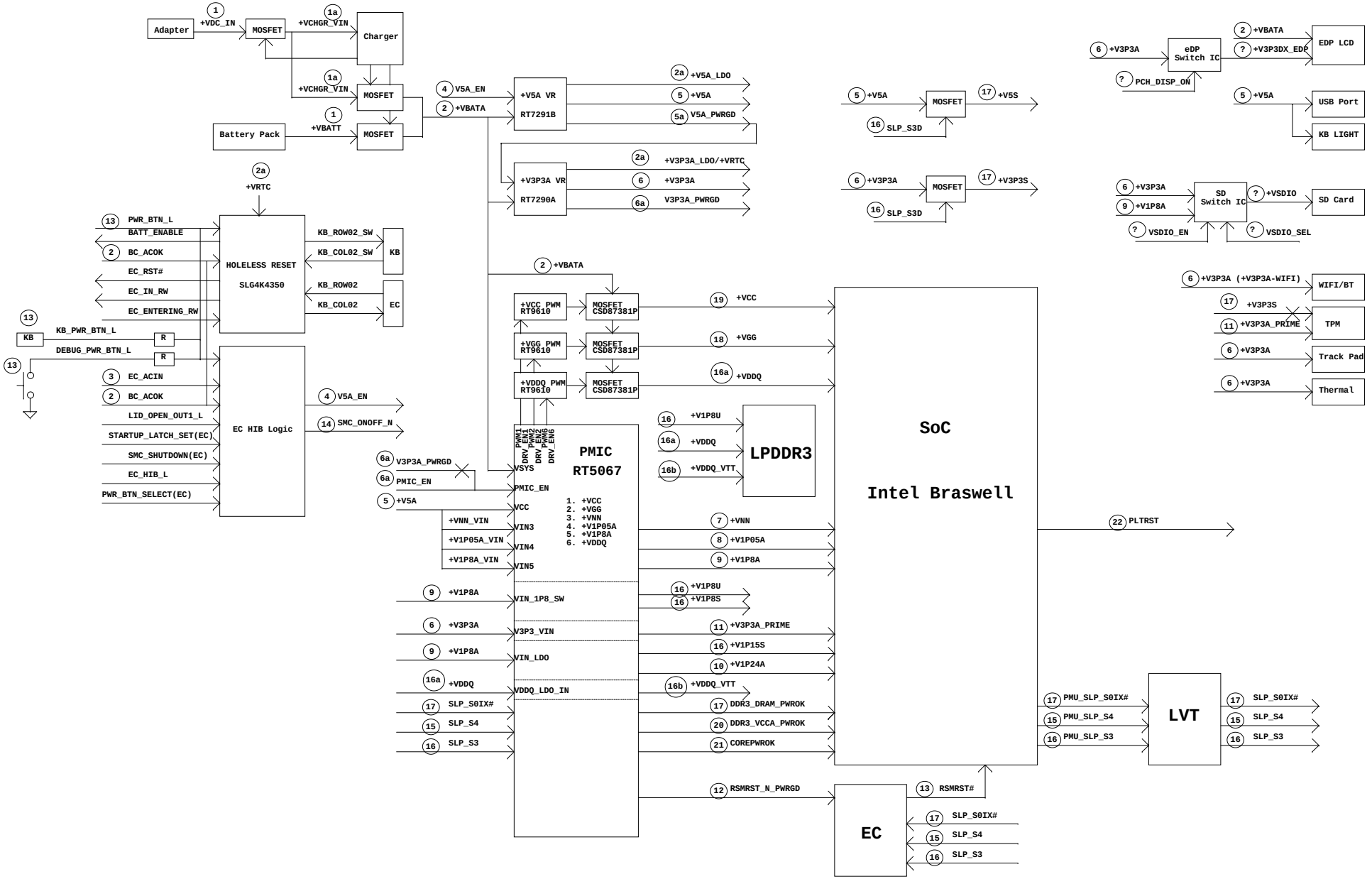

PROJECT : NL6D
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Size	Document Number	Rev
	BSW PWR TREE	1A

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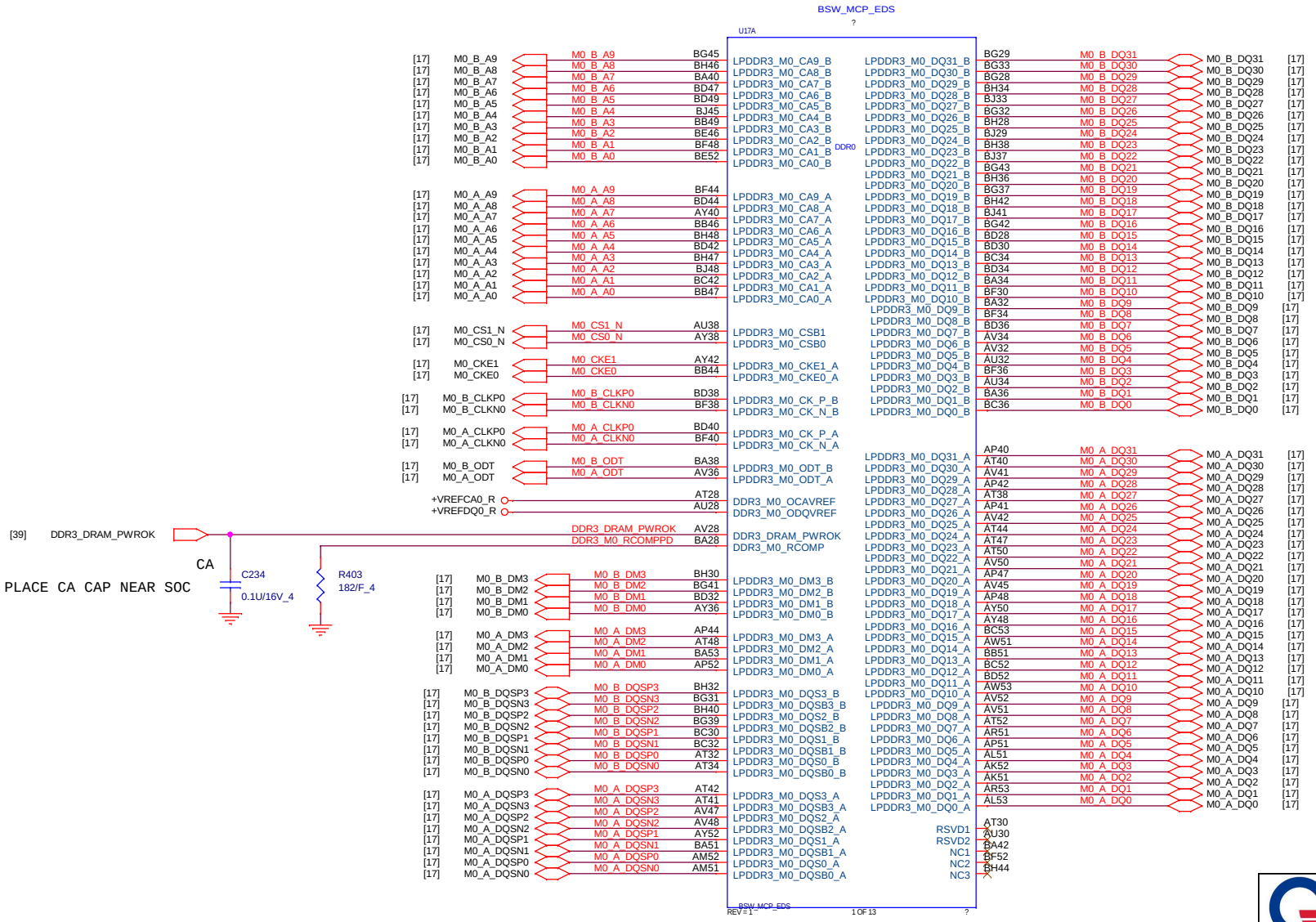
SoC (CPU)

BRASWELL SOC - MEMORY LPDDR3 CHANNEL A

06



PROJECT : NL6D

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Size	Document Number	Rev
	BSW 1/10 (DDRA)	1A
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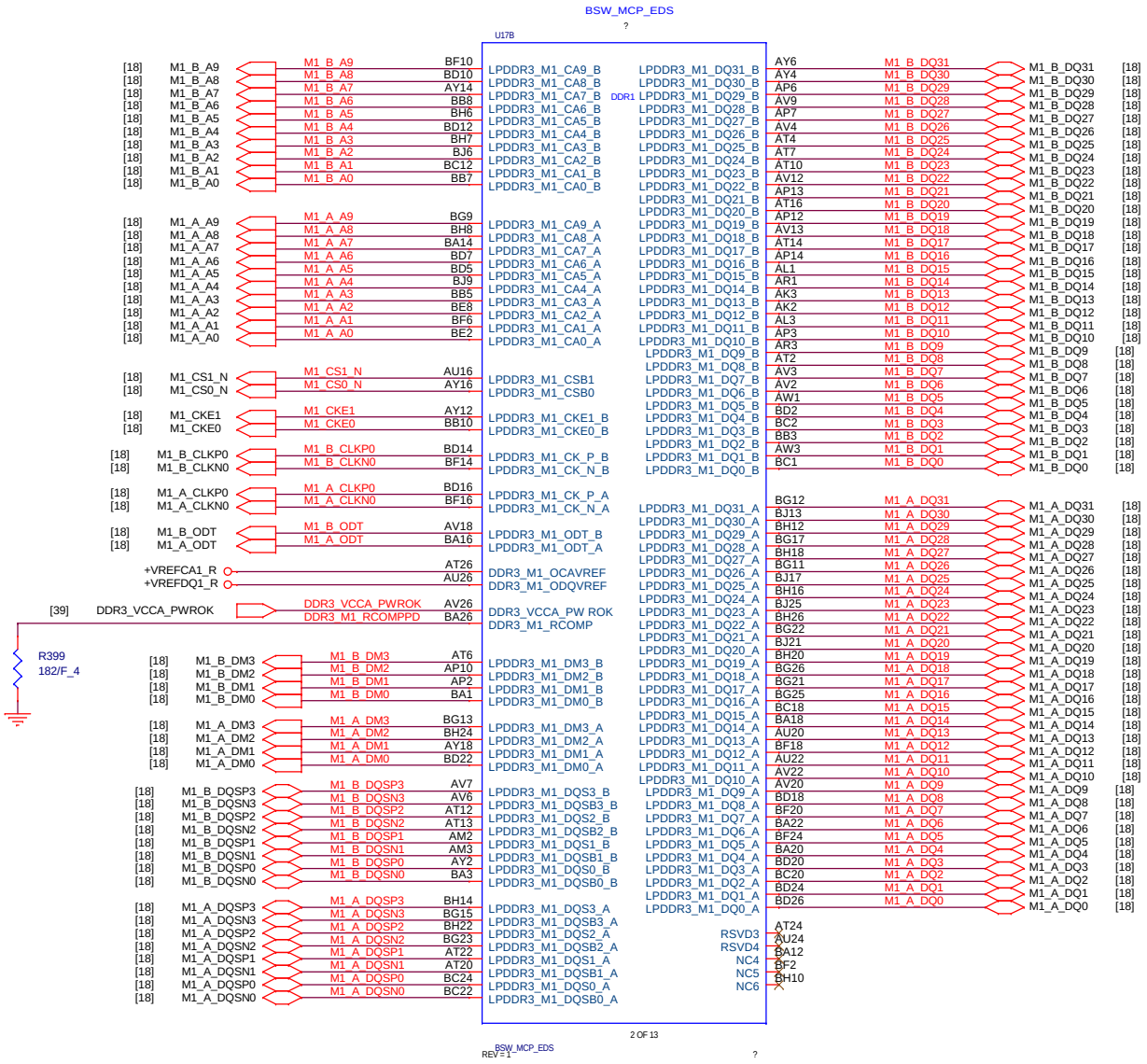
BRASWELL - MEMORY LPDDR3 CHANNEL B

SoC (CPU)

07



PROJECT : NL6D		
Quanta Computer Inc.		
Size	Document Number: BSW 2/10 (DDRB)	Rev: 1A
Date: Tuesday, April 12, 2016	Sheet 7 of 41	

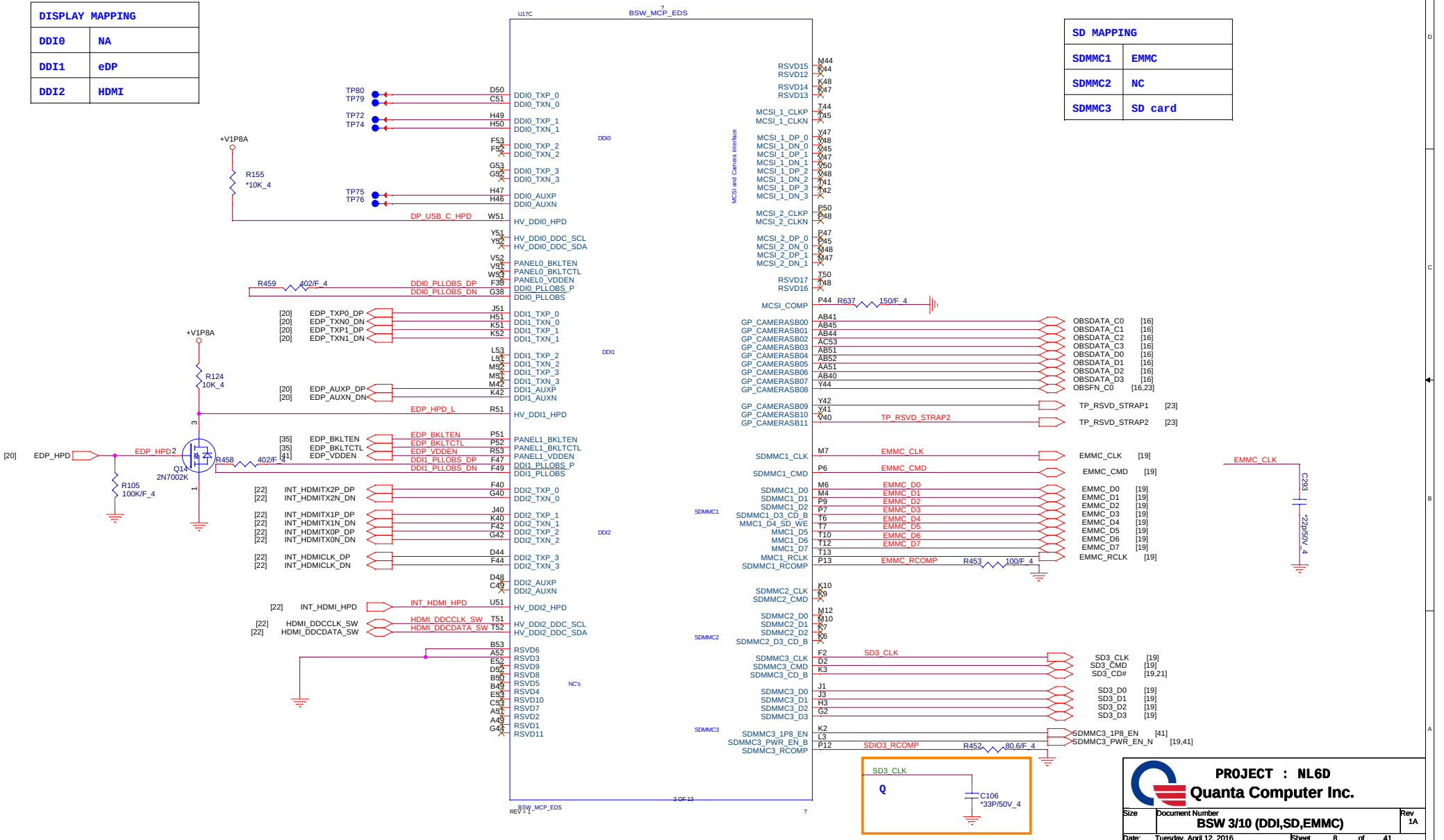
BRASWELL SOC - DISPLAY, XDP, EMMC, SD

SoC (CPU)

08

DISPLAY MAPPING	
DDI0	NA
DDI1	eDP
DDI2	HDMI

SD MAPPING	
SDMMC1	EMMC
SDMMC2	NC
SDMMC3	SD card



PROJECT : NL6D			
Quanta Computer Inc.			
Size	Document Number		Rev
	BSW 3/10 (DDI,SD,EMMC)		1A
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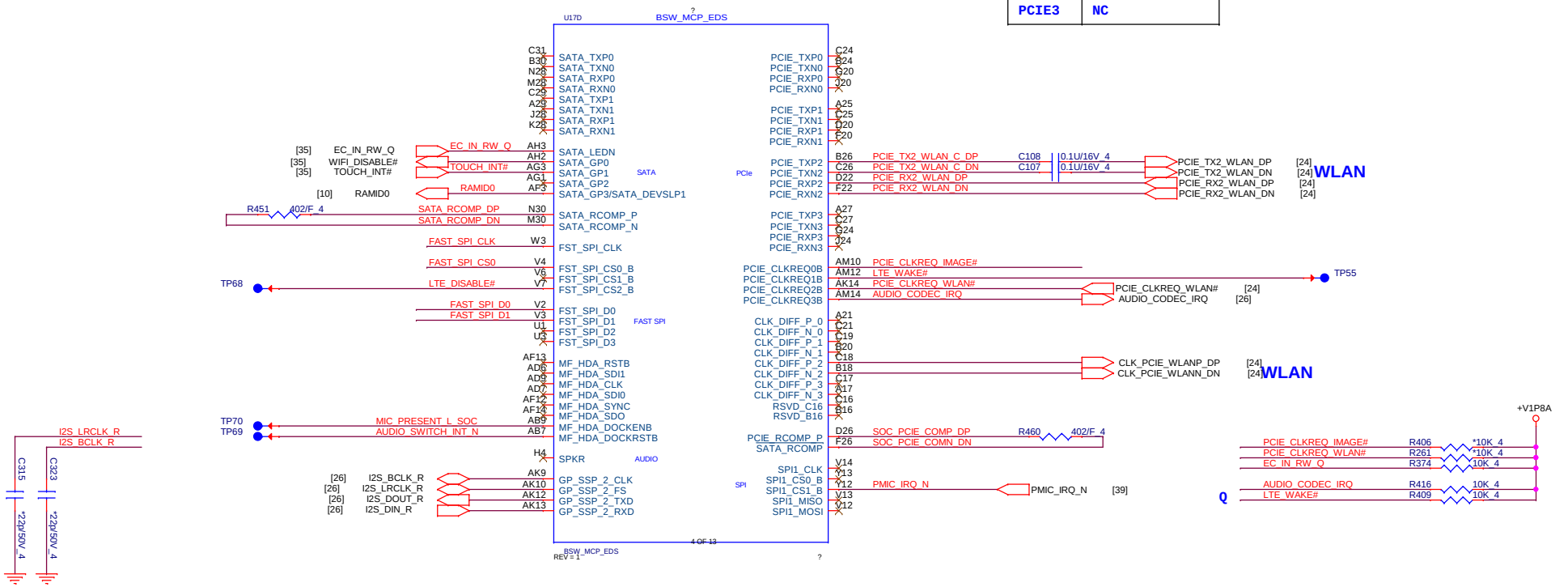
BSW SOC - SATA, PCIe, SPI, I2S

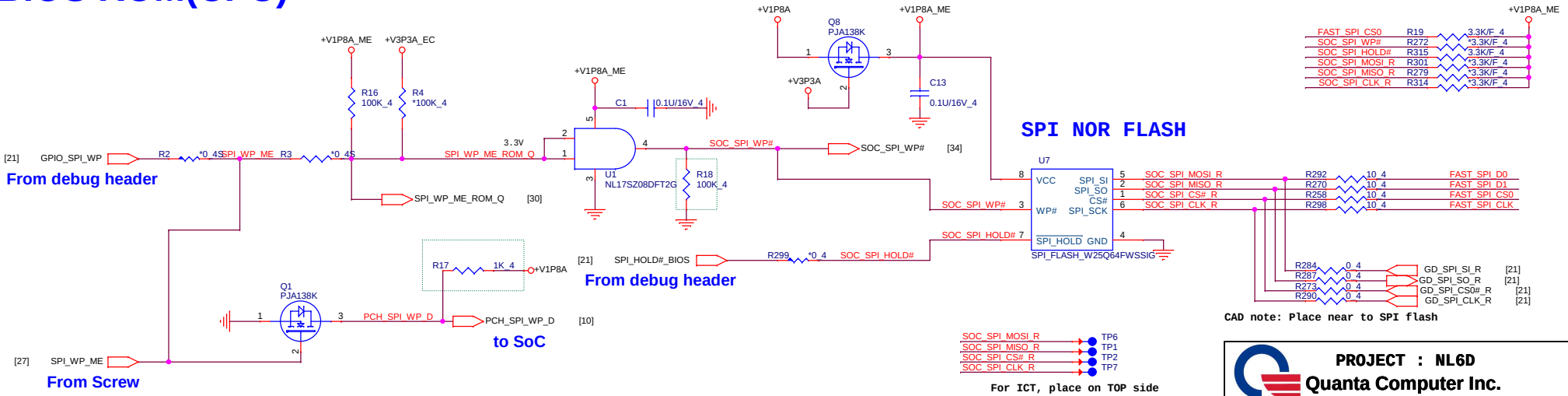
09

PCIe MAPPING	
PCIE0	NC
PCIE1	NC
PCIE2	WIFI (StP)
PCIE3	NC

SoC (CPU)



BIOS ROM(CPU)



PROJECT : NL6D

Quanta Computer Inc.

Size	Document Number	Rev
	BSW 4/10 (PCIE/SATA/SPI)	1A
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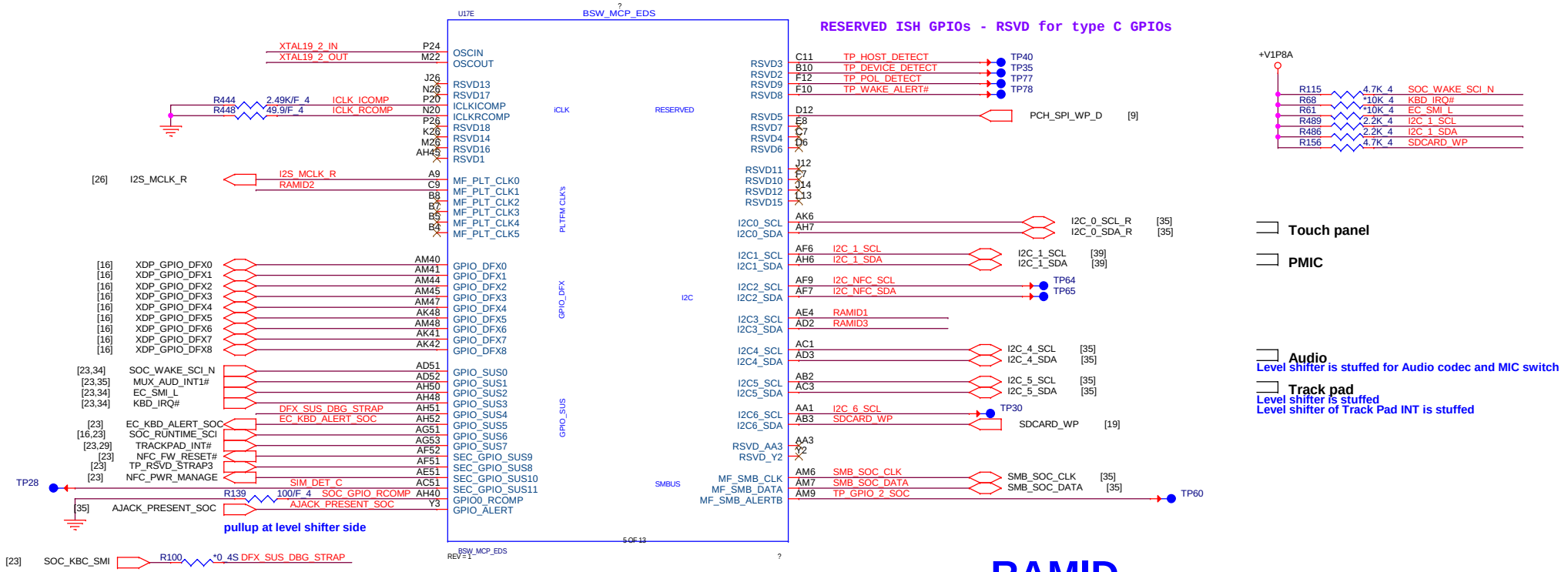
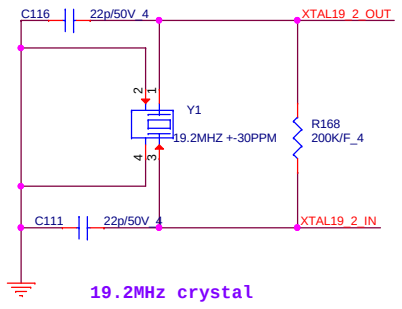
SoC (CPU)

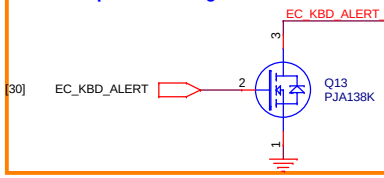
BRASWELL - I2C, XDP, SM BUS



19.2MHz X'tal

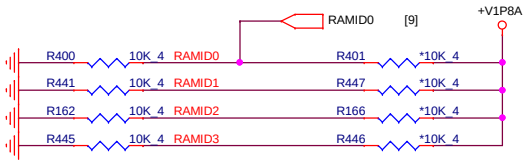


0312 added KBD_ALERT pin to notify SoC to lock ME FW
Keep reserving this feature in DVT build



Vender	RAM_ID3	RAM_ID[2..0]	Q PN	Mfr. PN	Freq.	Size	Total Size
Samsung	0 (1-CH)	000	AKD5QWST508	K4E8E304EE-EGCF	1866MHz	4Gb	2GB
Hynix	0 (1-CH)	001	AKD5RW0TW53	H9CCNNN8GTMLAR-NUD	1866MHz	4Gb	2GB
Micron	0 (1-CH)	010	AKD5QWSTL01	MT52L256M32D1PF-107 WT:B	1866MHz	4Gb	2GB
Samsung	0 (1-CH)	011	AKD5QWST521	K4E8E324EB-EGCF	1866MHz	4Gb	2GB
Micron	0 (1-CH)	100	AKD5QWWT401	EDF8132A3MA-JD-F-R	1866MHz	4Gb	2GB
Samsung	1 (2-CH)	000	AKD5QWST508	K4E8E304EE-EGCF	1866MHz	4Gb	4GB
Hynix	1 (2-CH)	001	AKD5RW0TW53	H9CCNNN8GTMLAR-NUD	1866MHz	4Gb	4GB
Micron	1 (2-CH)	010	AKD5QWSTL01	MT52L256M32D1PF-107 WT:B	1866MHz	4Gb	4GB
Samsung	1 (2-CH)	011	AKD5QWST521	K4E8E324EB-EGCF	1866MHz	4Gb	4GB
Micron	1 (2-CH)	100	AKD5QWWT401	EDF8132A3MA-JD-F-R	1866MHz	4Gb	4GB

RAMID



Samsung Hynix

R527 *10K_4 R526 *10K_4
R534 *10K_4 R533 *10K_4

Micron

For BOM, place BOT side

PROJECT : NL6D
Quanta Computer Inc.

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	BSW 5/10 (I2C/DFX/GPIO)	1A

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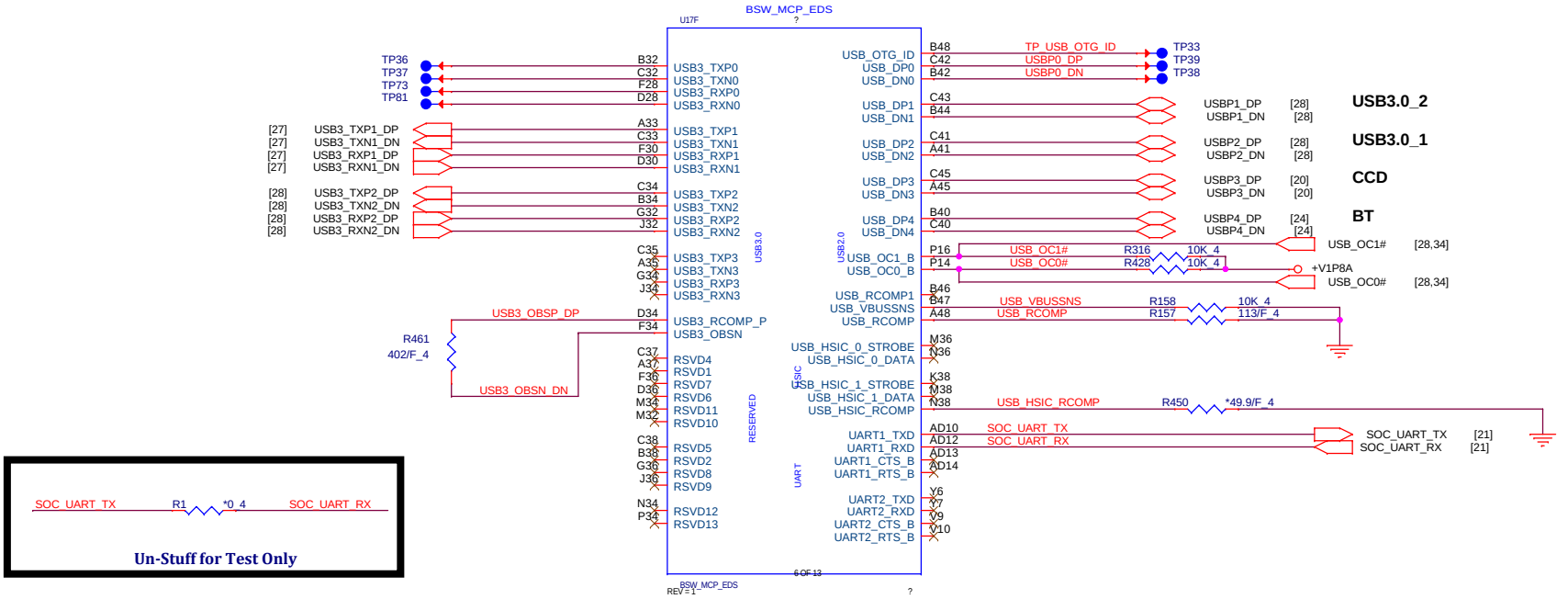
BRASWELL - USB INTERFACE

11

SoC (CPU)



PROJECT : NL6D		
Quanta Computer Inc.		
Size	Document Number: BSW 6/10 (USB)	Rev: 1A
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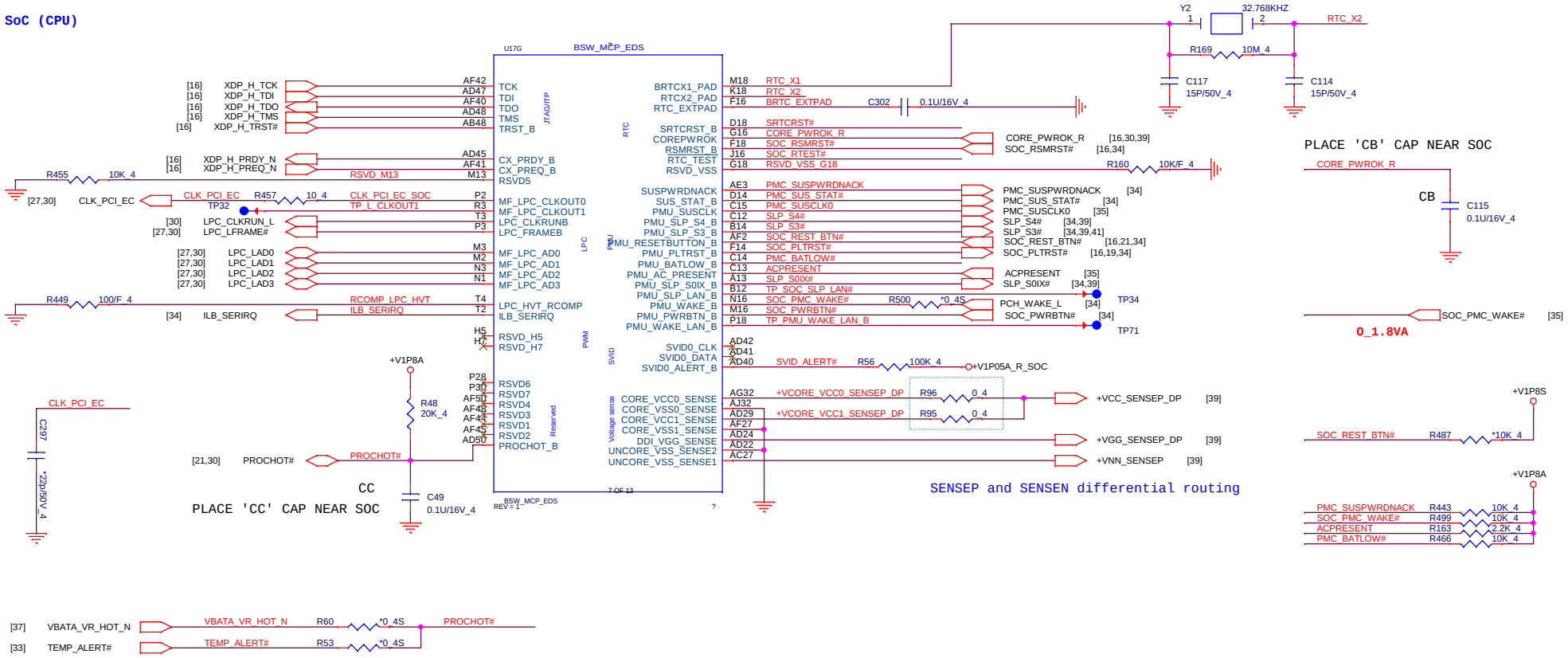
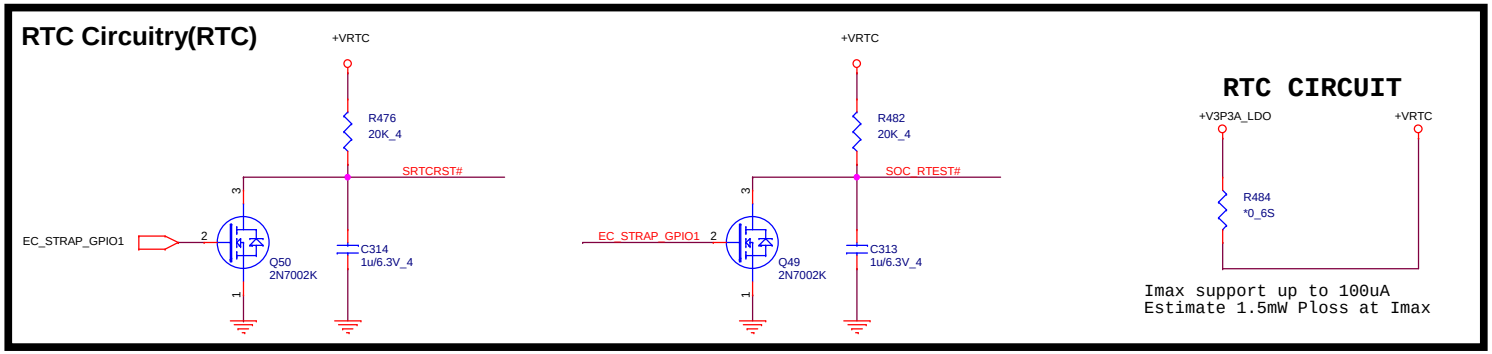
BRASWELL - JTAG, LPC, THERMAL, PMU

SoC (CPU)

RTC 32.768KHz X'tal





PROJECT : NL6D

Quanta Computer Inc.

Size	Document Number	Rev
	BSW 7/10 (JTAG/LPC//PMU)	1A

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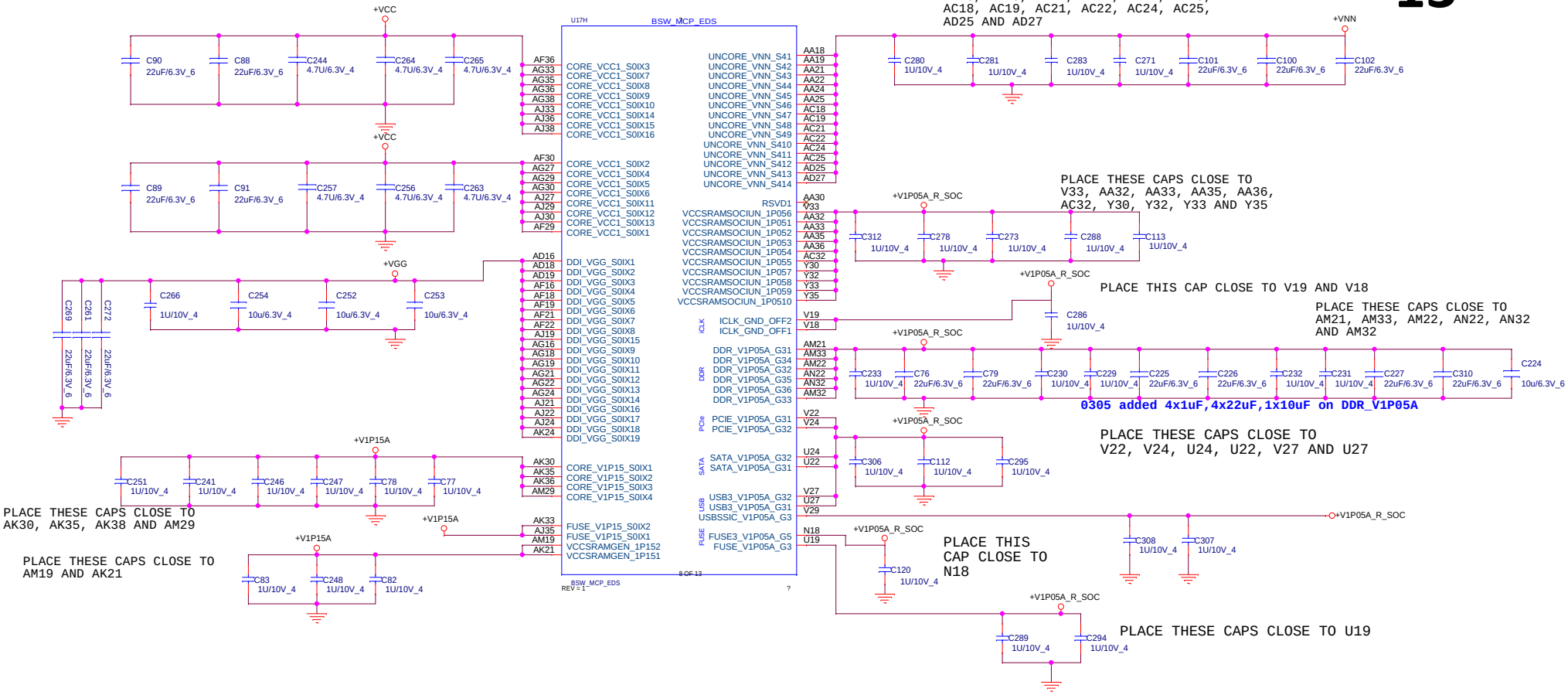
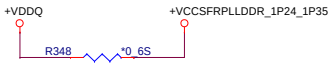
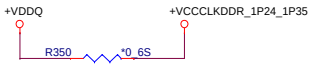
BRASWELL - POWER 1

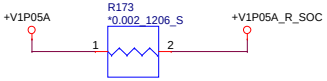
SoC (CPU)

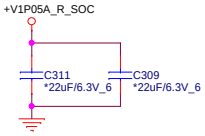
13



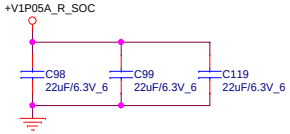








DUMMY CAPS. TO BE DELETED IN NEXT REVISION



CAD NOTE: PLACE CLOSE TO PIN AM21,
AM33, AM22, AN22, AN32 AND AM32 POWER PLANE

PROJECT : NL6D

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	BSW 8/10 (Power 1)	1A
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SoC (CPU)

BRASWELL - POWER 2

14

PLACE THESE CAPS CLOSE TO AM25

PLACE THESE CAPS CLOSE TO AN27

PLACE THESE CAPS CLOSE TO V36 & Y36

PLACE THESE CAPS CLOSE TO Y27 & Y25

PLACE THESE CAPS CLOSE TO P38, V30 & AC30

PLACE THESE CAPS CLOSE TO AF35, AD35, AD38 & AC36

PLACE THESE CAPS CLOSE TO THE DDR_VDDQ_G_ PINS

PLACE THESE CAPS CLOSE TO E1 AND E2

PLACE THESE CAPS CLOSE TO G1

PLACE THESE CAPS CLOSE TO AH4 AND AF4

PLACE THESE CAPS CLOSE TO Y18

PLACE THESE CAPS CLOSE TO AD33, AK18, AF33 AND AK19

PLACE THESE CAPS CLOSE TO THEIR PINS

U17I BSW_MCP_EDS 9 OF 13 REV = 1

PLACE CAPS NEAR SOC

PLACE THIS CAP CLOSE TO U16

PLACE THIS CAP CLOSE TO G10 & H10

SD3 IO SUPPLY

LPC IO SUPPLY

AUDIO IO SUPPLY

Size	Document Number: BSW 9/10 (Power 2)	Rev: 1A
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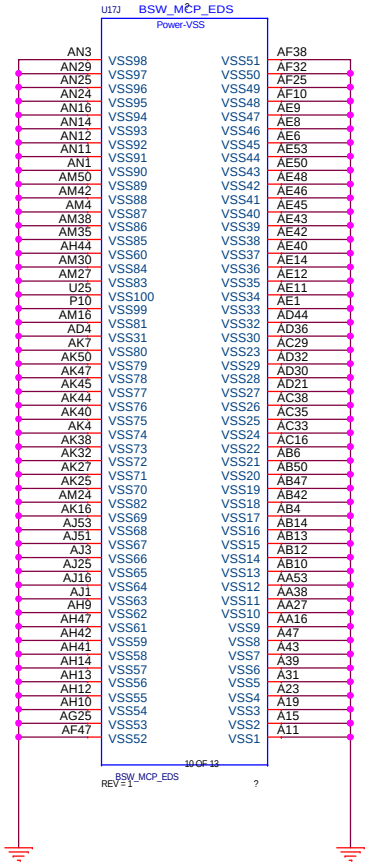
PROJECT : NL6D

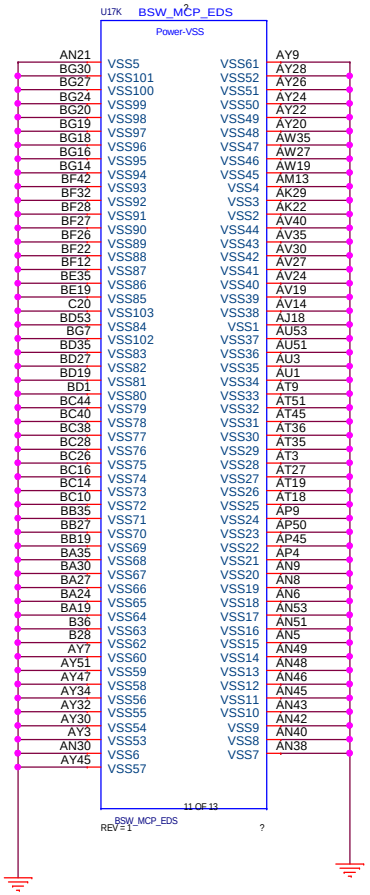
Quanta Computer Inc.

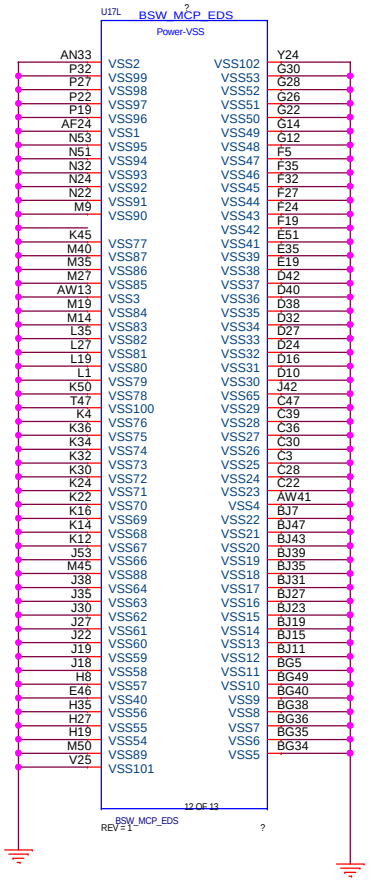
SoC (CPU)

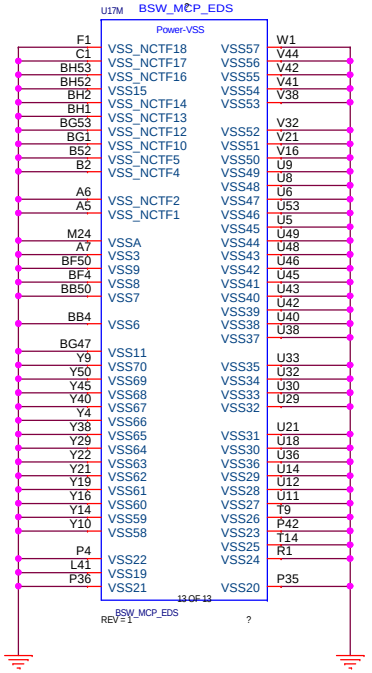
BRASWELL - GND

15









PROJECT : NL6D

Quanta Computer Inc.

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	BSW 10/10 (GND)	1A
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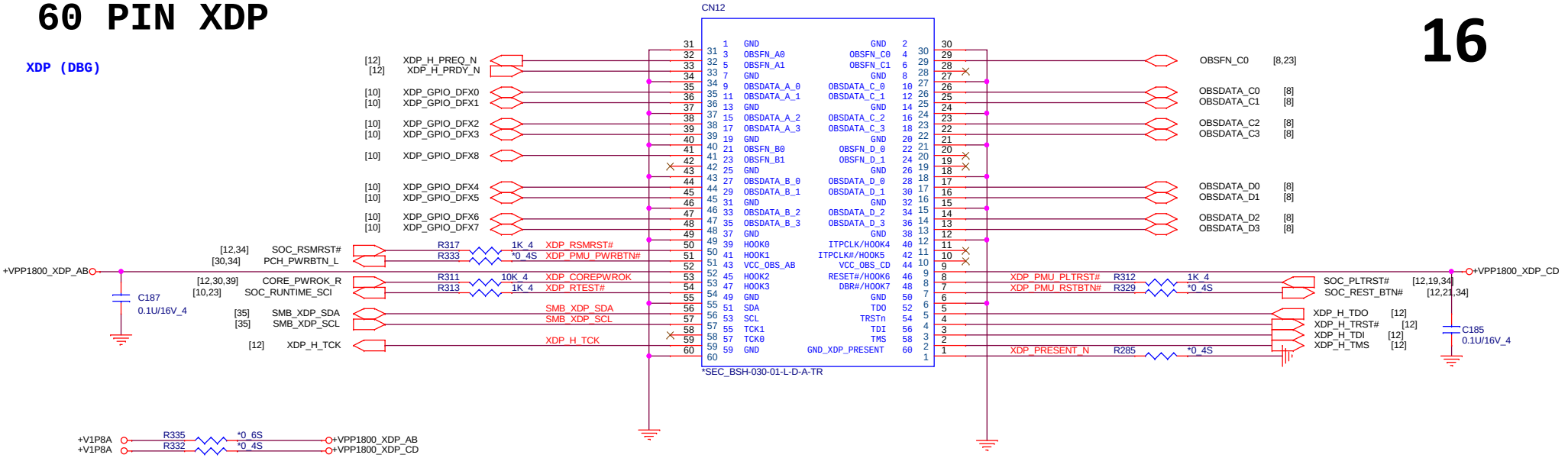
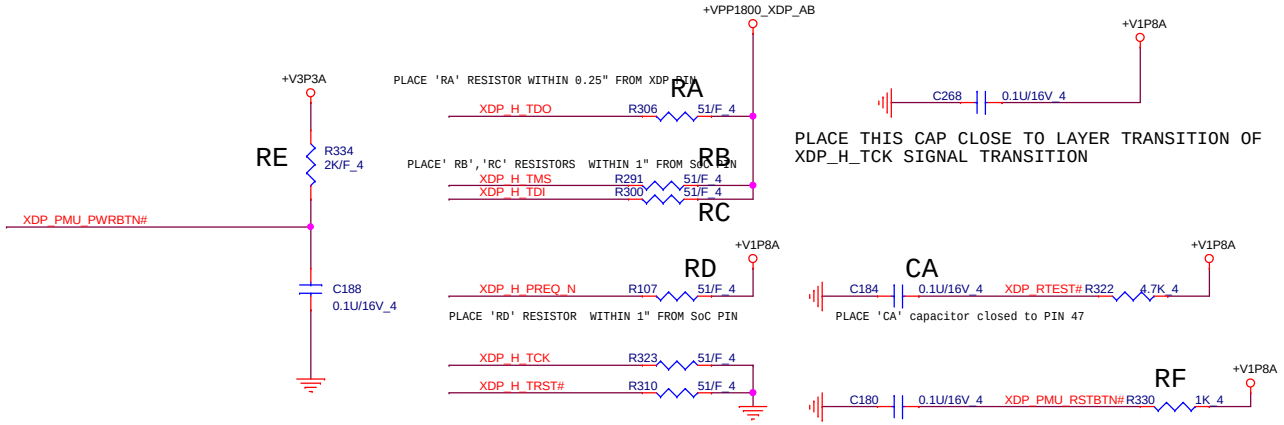
60 PIN XDP

XDP (DBG)



16

PULL-UPS AND DOWNS FOR XDP SIGNALS



In reference board,RE is 2K and RF is stuffed

APS

PROJECT : NL6D

Quanta Computer Inc.

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	XDP	1A
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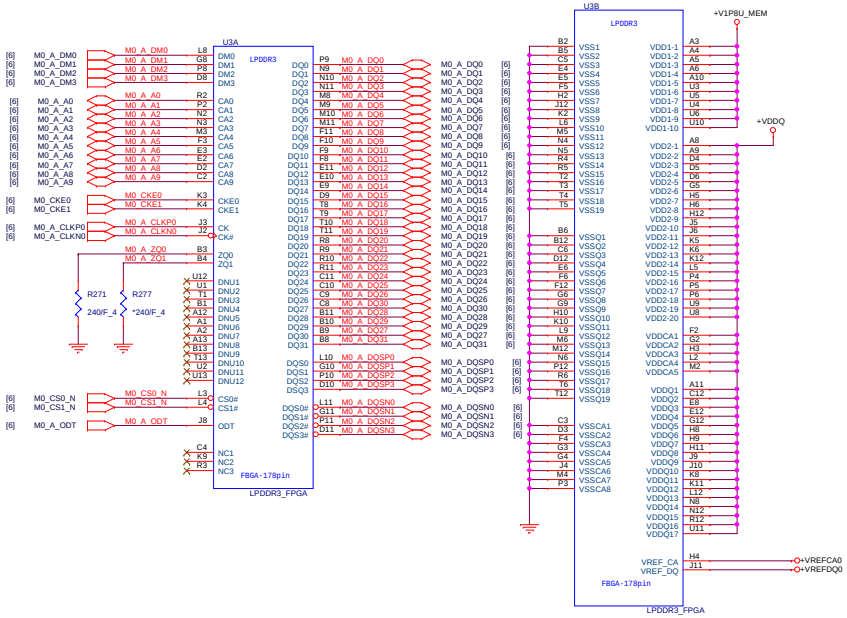
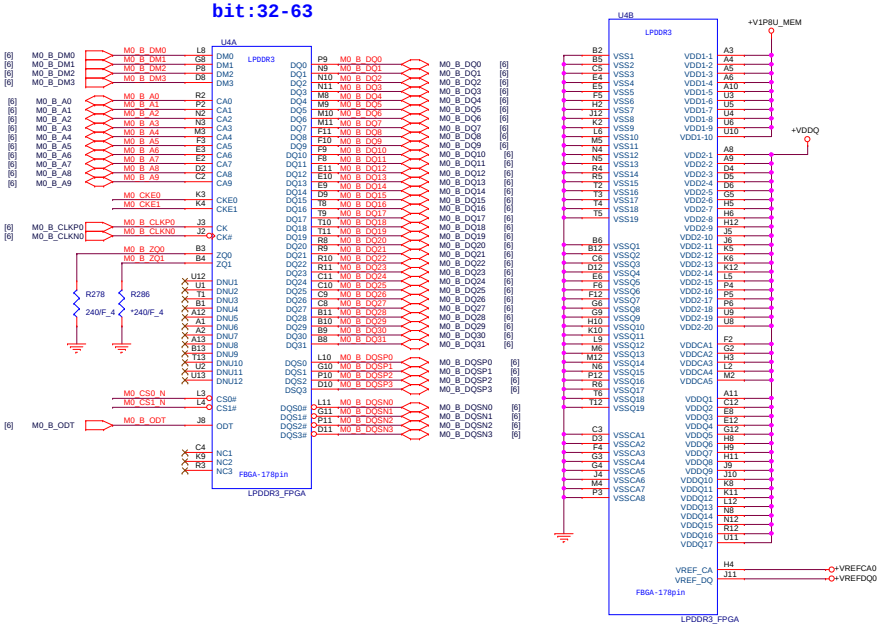
LPDDR3 MEMORY CHANNEL A

CHANNEL A:8Gb*2 LPDDR3

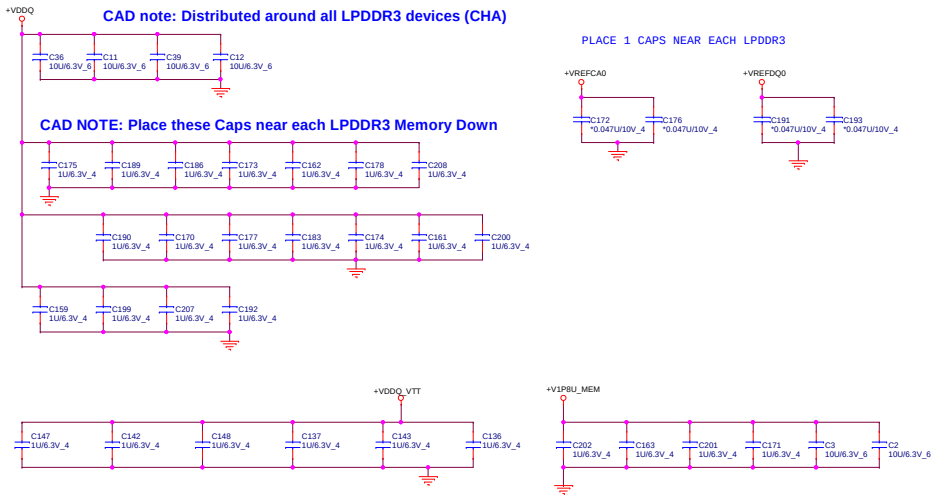
bit:0-31



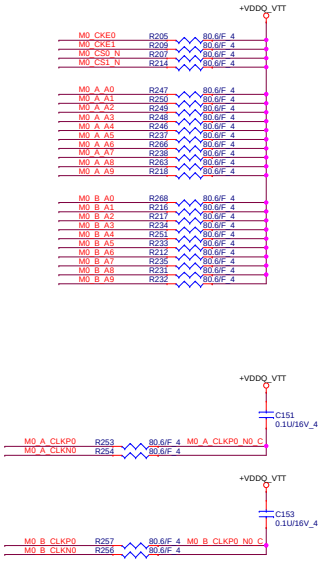
bit:32-63



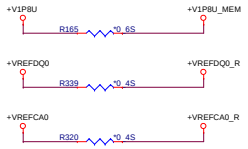
DE-CAPS FOR MEMORY CHANNEL A



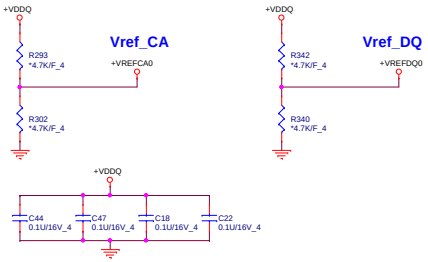
VTT TERMINATIONS



VOLTAGE MERGE



VREF_CA AND DQ CIRCUITS



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Quanta Computer Inc.		
Size	Document Number: ON BOARD_LPDDR3_A	Rev: 1A
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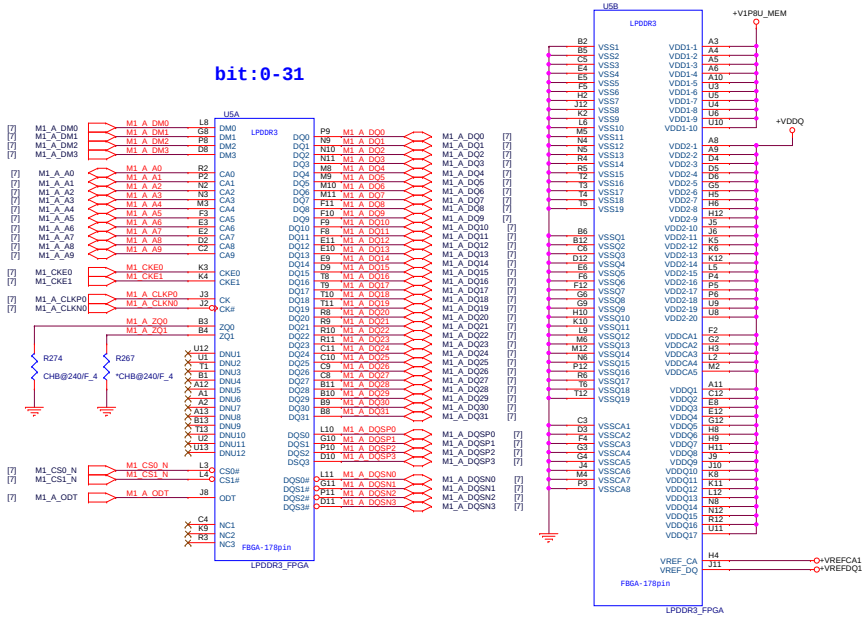
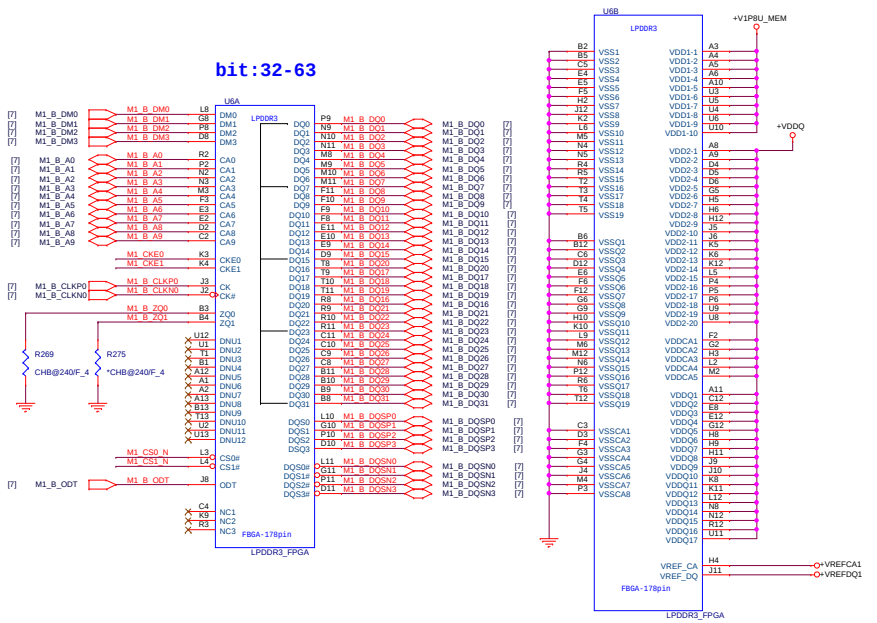
LPDDR3 MEMORY CHANNEL B

CHANNEL B:8Gb*2 LPDDR3

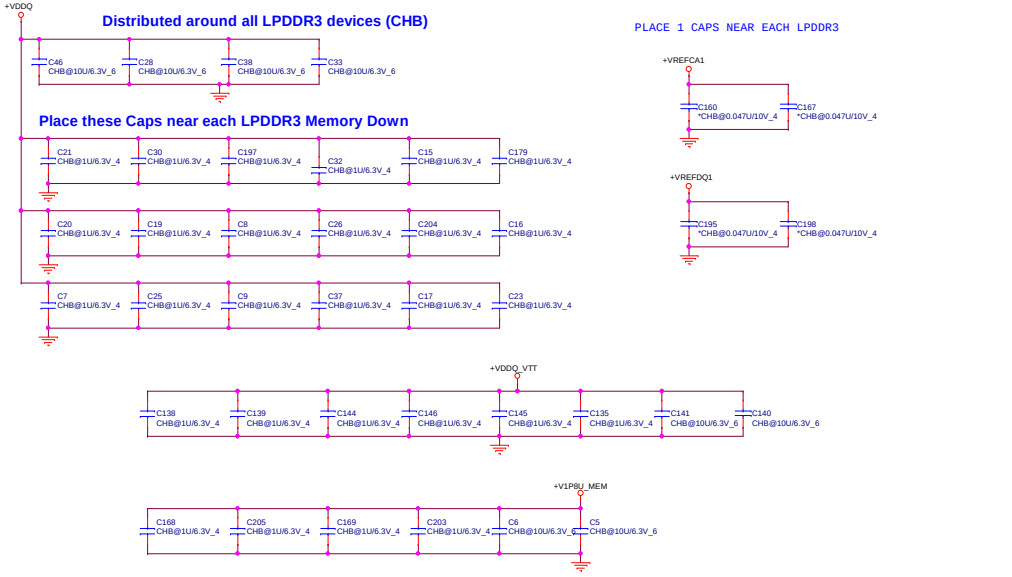
bit:0-31



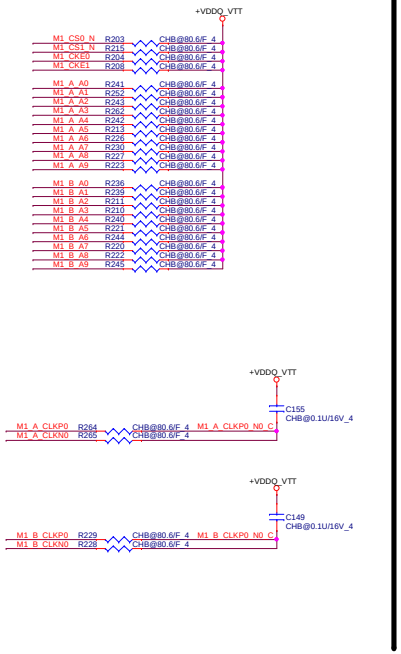
bit:32-63



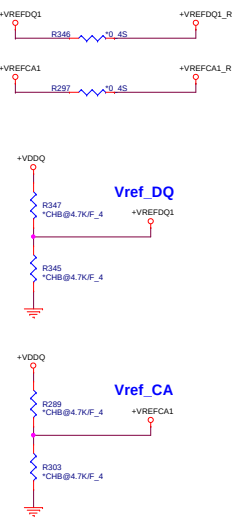
DE-CAPS FOR MEMORY CHANNEL B



VTT TERMINATIONS



VREF_DQ CIRCUIT



PROJECT : NL6D
Quanta Computer Inc.

Size	Document Number	Rev
	ON BOARD_LPDDR3_B	1A
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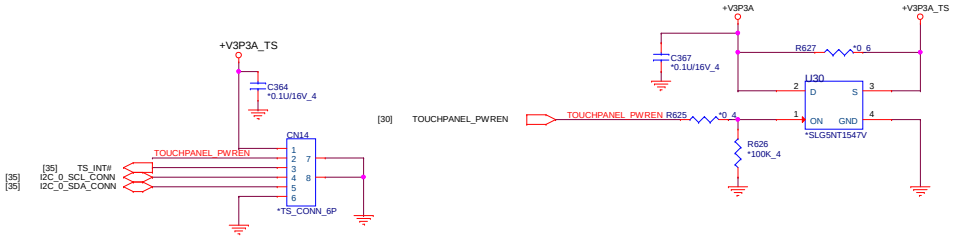
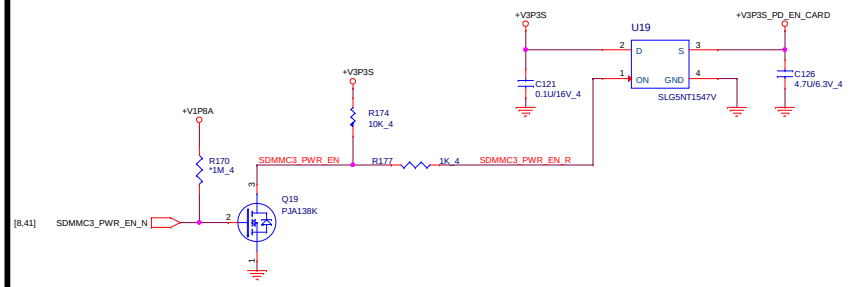
SD/MMC CARD READER CONNECTOR

Touch panel connector



SD SLOT POWER SUPPLY

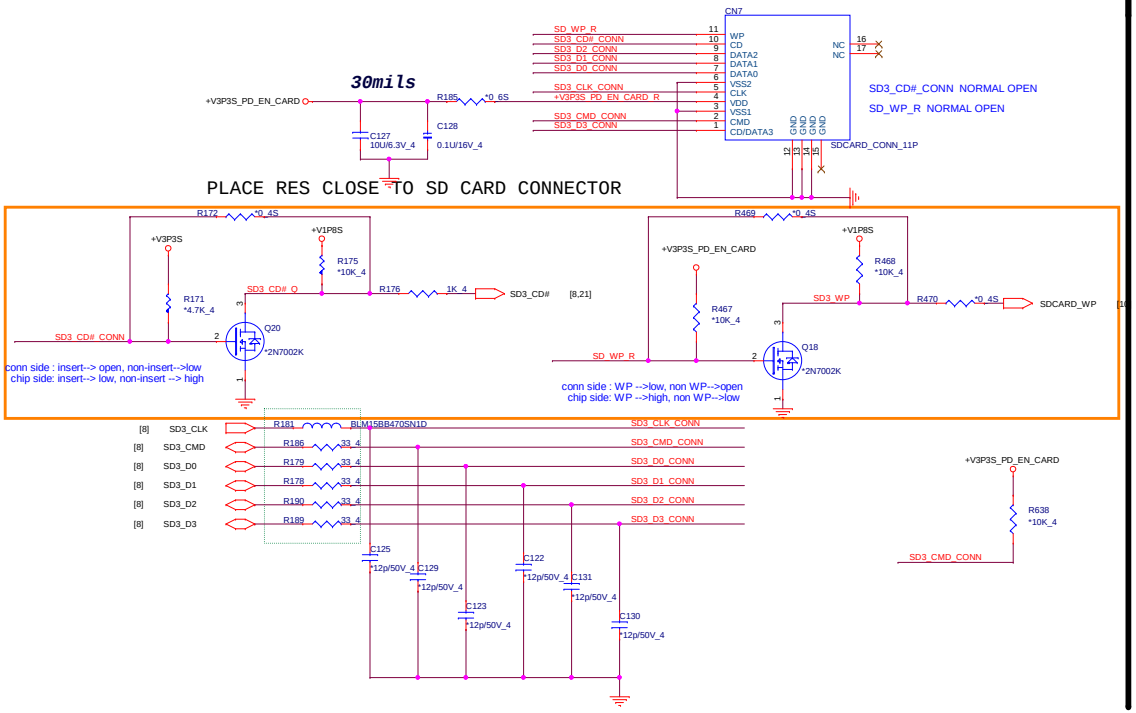
Card Reader(CRD)



SD SLOT/EMI

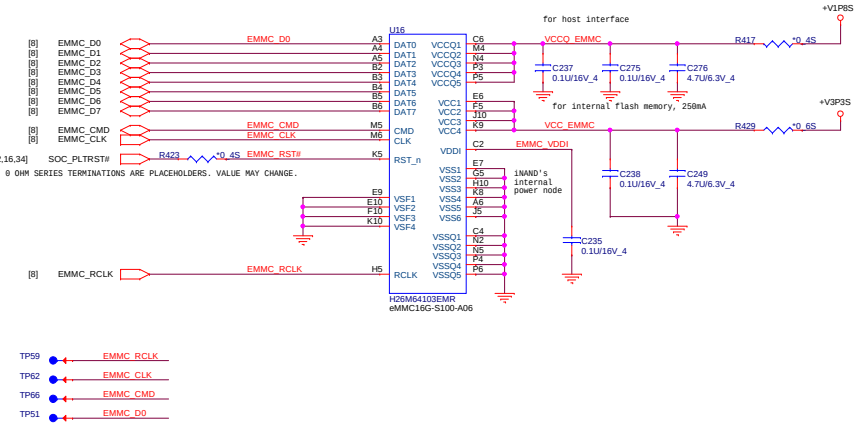
Card Reader(CRD)

This is full size SD card (push-push type)



eMMC (MMC)

eMMC



16G
Samsung-->KLMAG2WEMB-B031-AKE2RF-T505-- IC FLASH(153)KLMAG2WEMB-B031(FBGA)STNBSQ
Hynix--> H26M52103FMR (0x03)--AR0ZHQR1000--PROG IC FLASH(153P)H26M52103FMR STNBSQ

32G
Samsung-->KLMBG4WEBC-B031--AKE3SZ-T500--IC FLASH(153)KLMBG4WEBC-B031(FBGA)STNBSQ
Hynix--> H26M64103EMR (0x03)--AR0ZHQR1001--PROG IC FLASH(153P)H26M64103EMR STNBSQ

PROJECT : NL6D
Quanta Computer Inc.

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	SDIO/eMMC/TS	1A

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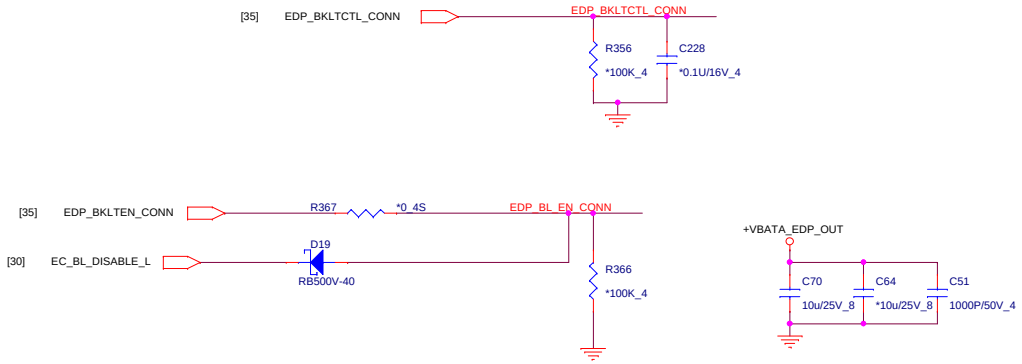
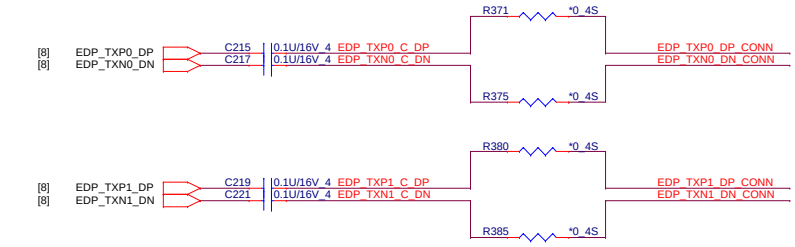
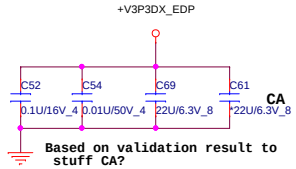
eDP PANEL CONTROL

LCD(LDS)



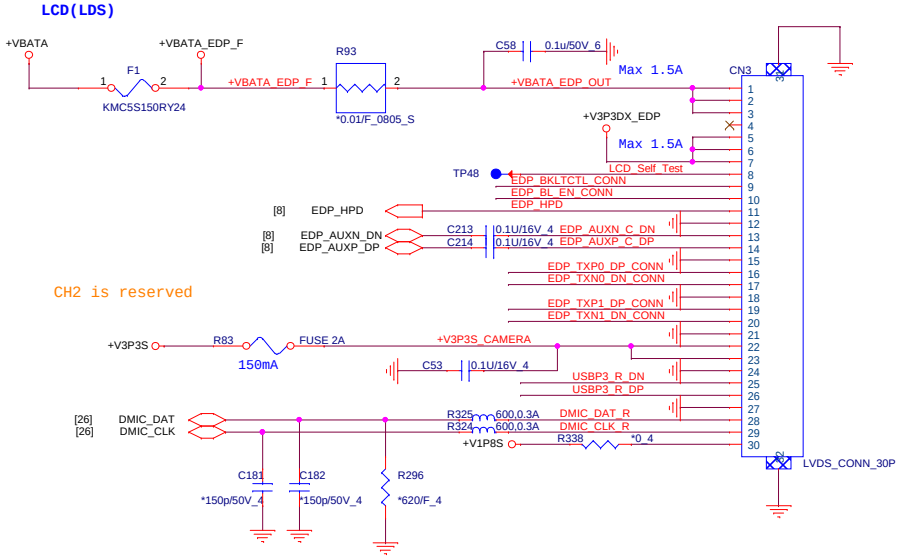


eDP Power



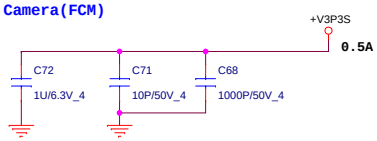
eDP CONNECTOR

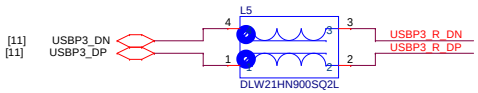
LCD(LDS)



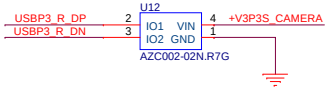
CAMERA - POWER AND USB CMC

Front Camera(FCM)





ESD



Layout note:Place close to CN9

PROJECT : NL6D Quanta Computer Inc.		
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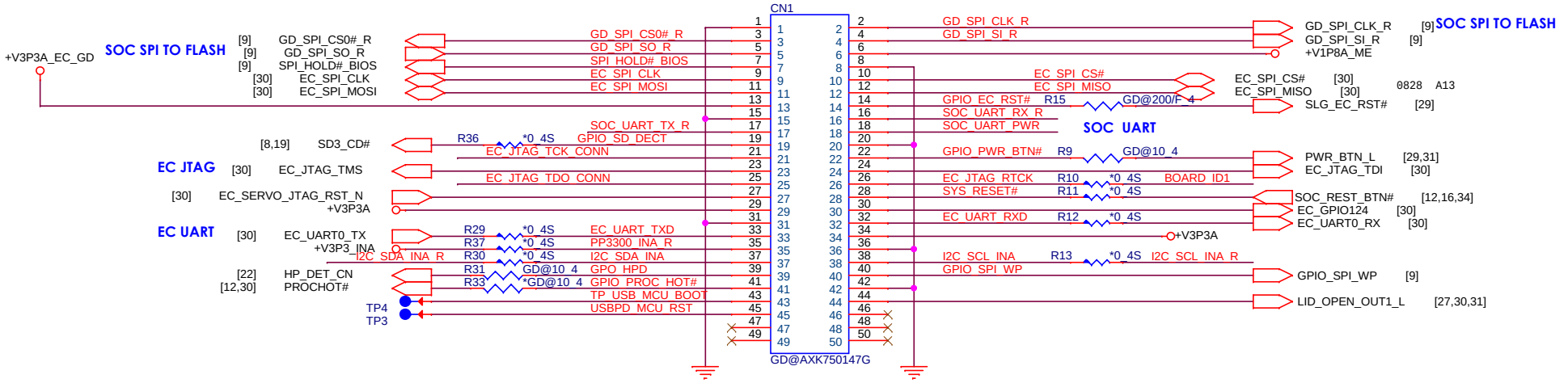
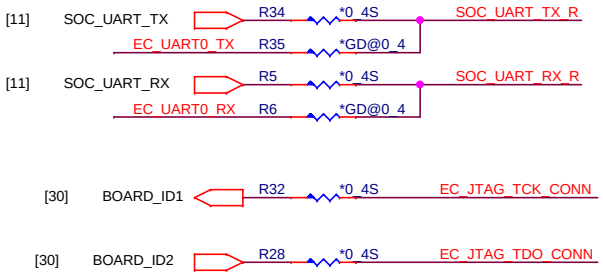
Google debug(DBG)

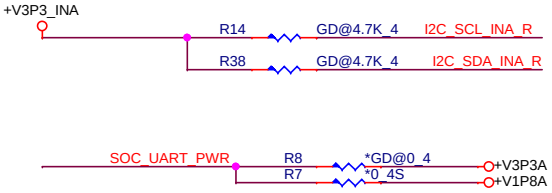
GOOGLE DEBUG PORT

21

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD







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Quanta Computer Inc.

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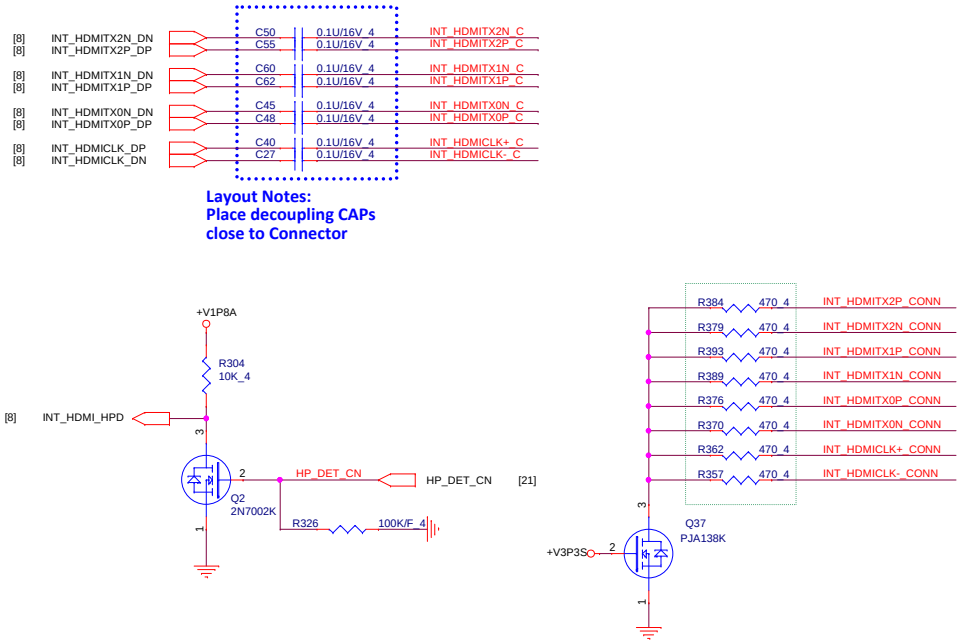
HDMI INTERFACE

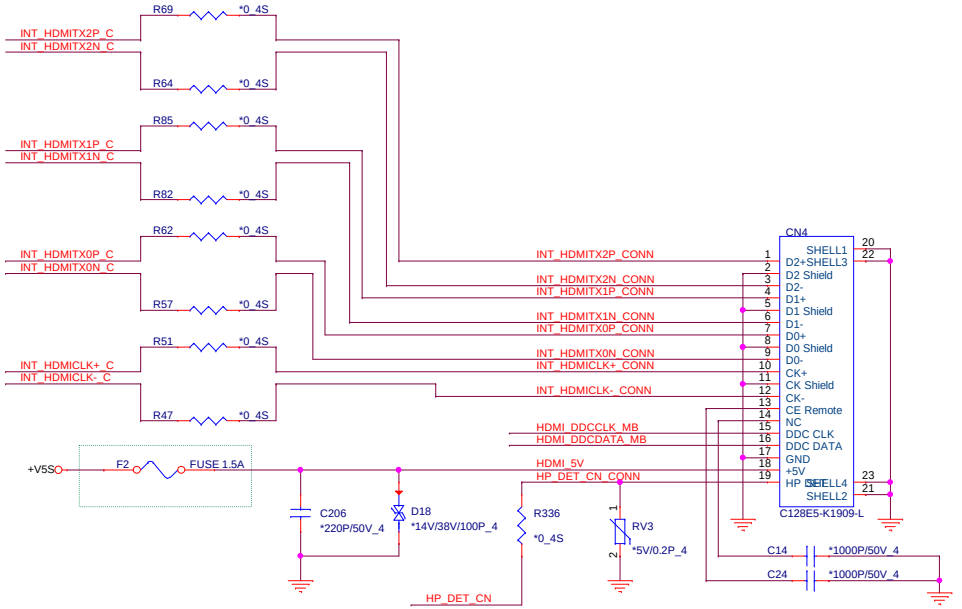
HDMI(HDM)

22

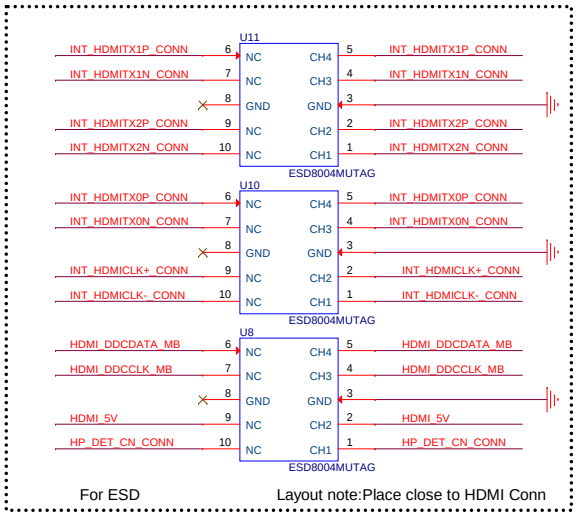
HDMI LEVEL SHIFTER



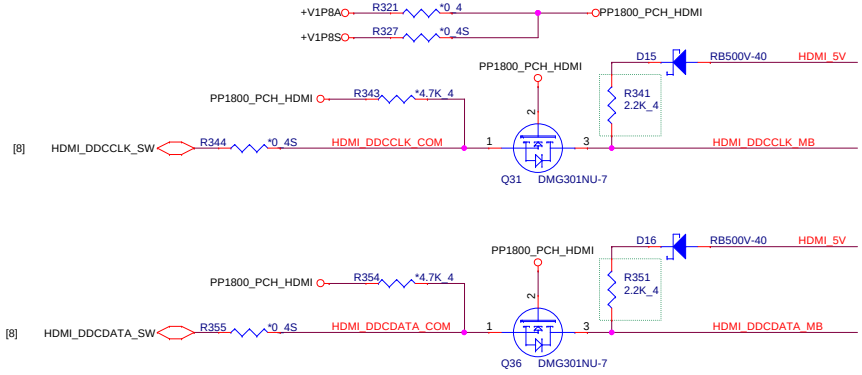
HDMI CONNECTOR



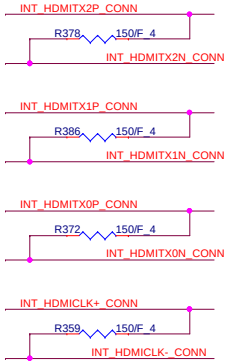
ESD 靠近HDMI CONNECTOR(CN2)



LEVEL TRANSLATOR/ EMI



EMI



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Quanta Computer Inc.

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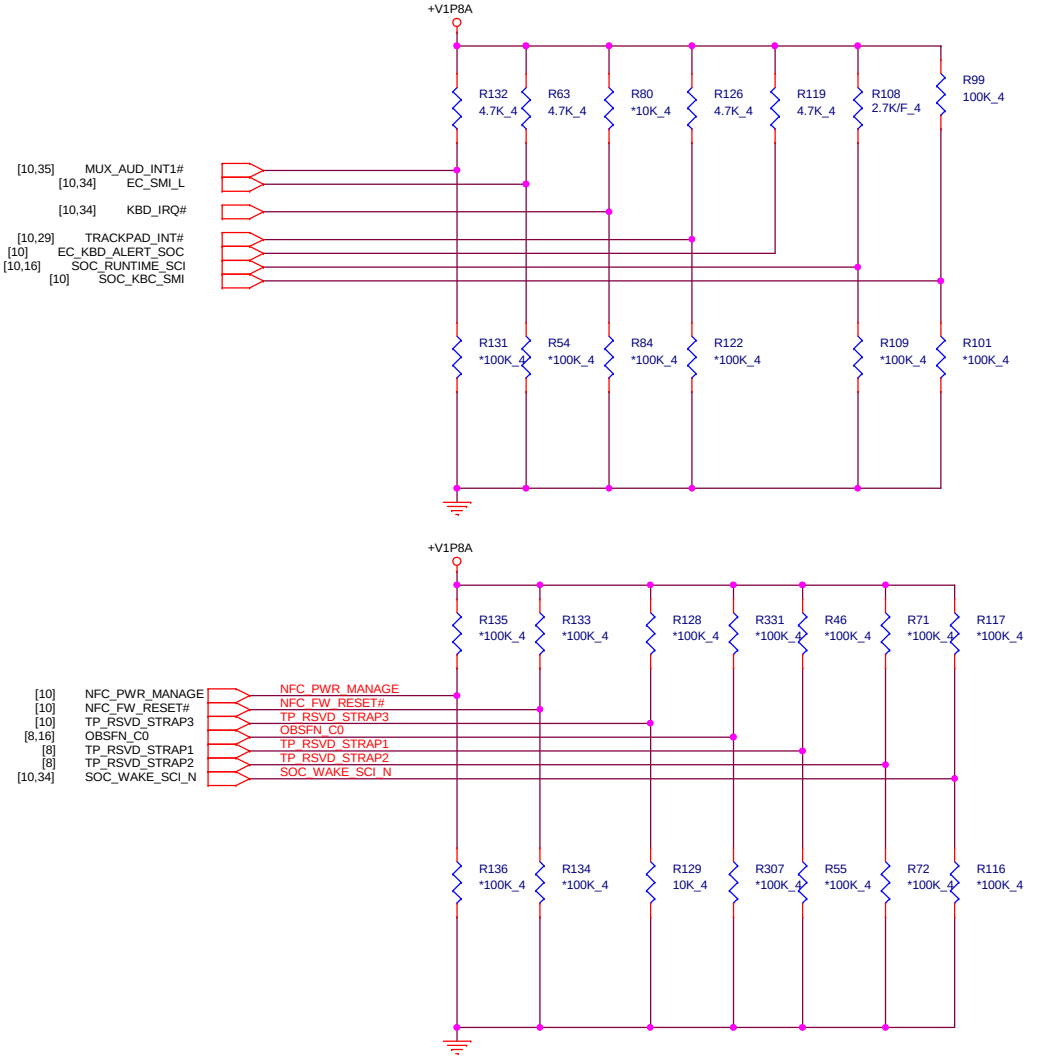
STRAPS SETTINGS

SoC (CPU)

BSW Strapping Table (based on EDS V1.0), sampled on the rising edge of PMU_RSMRST_N

Pin Name	Strap description	Configuration
GPIO_SUS0	DDI0 Detect	0 = DDI0 not detected **1 = DDI0 detected**
GPIO_SUS1	DDI1 Detect	0 = DDI1 not detected **1 = DDI1 detected**
GPIO_SUS2	Top Swap (A16 Override)	0 = change boot loader address **1 = Normal operation**
GPIO_SUS3	DSI Display Detect (Leave floating if GPIO functionality is not used, it is not POR)	**0 = DSI not detected** 1 = DSI detected
GPIO_SUS4	BIOS Boot Selection	0 = No SPI **1 = SPI**
GPIO_SUS5	Security Flash Descriptors	0 = Not support **1 = Normal operation**
GPIO_SUS6	Halt Boot strap	**1 = Normal operation** (MUST be high at RSMRST# de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS7	DFX SUS DEBUG strap	0 = SUSDUG **1 = No SUSDUG**
GPIO_SUS8	PLLs.ICLK.USB2,DDI ,SFR,supply select	**0 = Supply is 1.25V** 1 = Supply is 1.35V
GPIO_SUS9	ICLK.USB2,DDI,SFR Bypass	**0 = No Bypass(Default)** 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	**0 = No Bypass(Default)** 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	**0 = No Bypass(Default)** 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	**0 = No Bypass(Default)** 1 = Bypass



PROJECT : NL6D

Quanta Computer Inc.

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	STRAPS	1A
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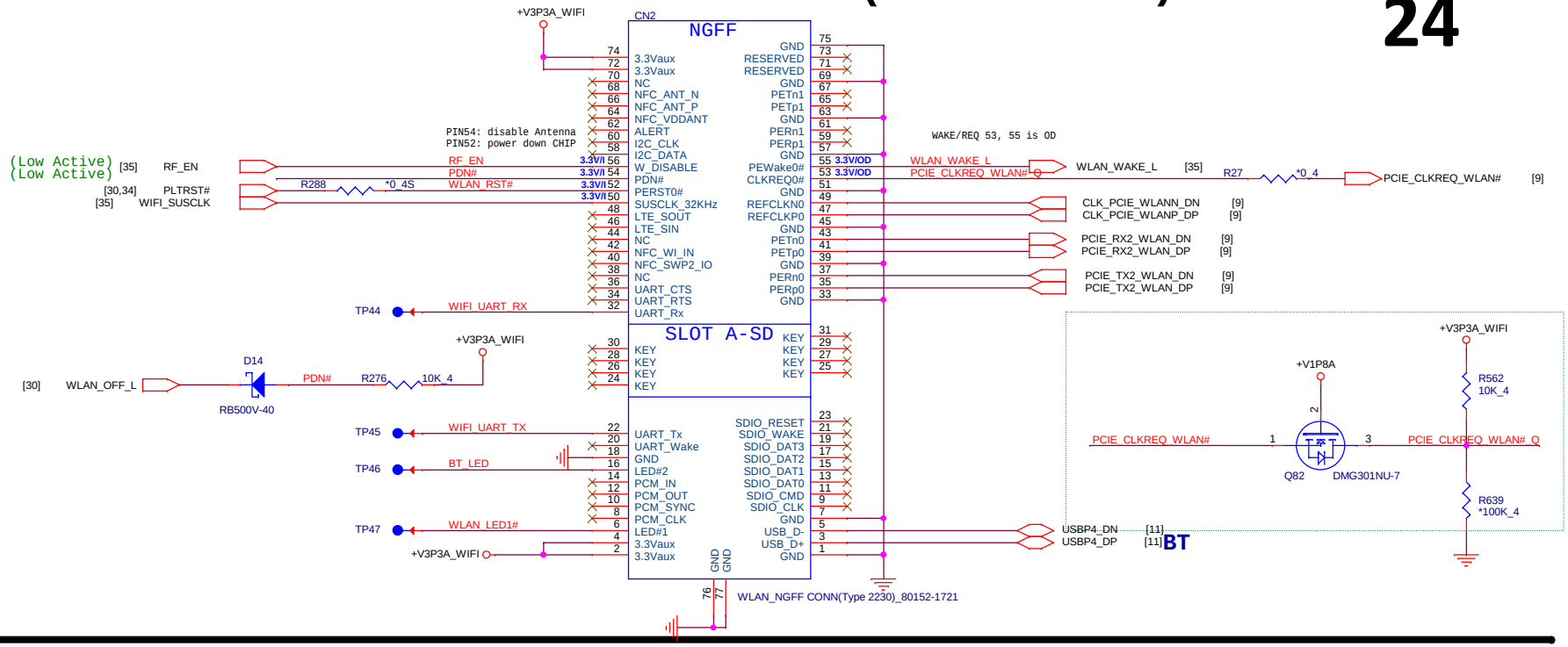
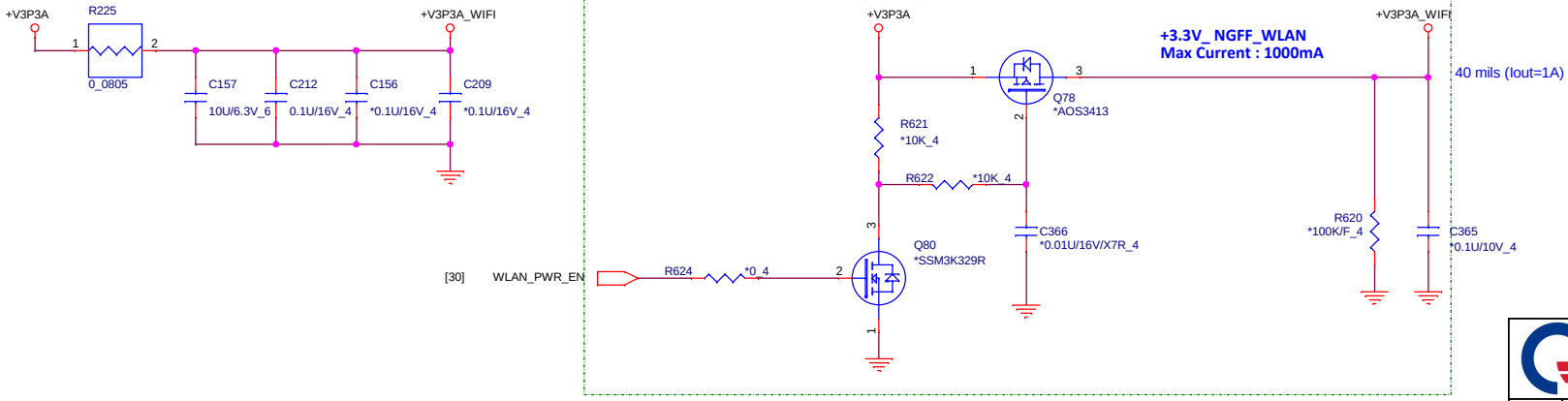
WIFI/BT COMBO NGFF E KEY(NGF)

WIFI/BT COMBO (NGFF E KEY)

24





PROJECT : NL6D

Quanta Computer Inc.

Size	Document Number	Rev
	WIFI/BT(NGFF)	1A

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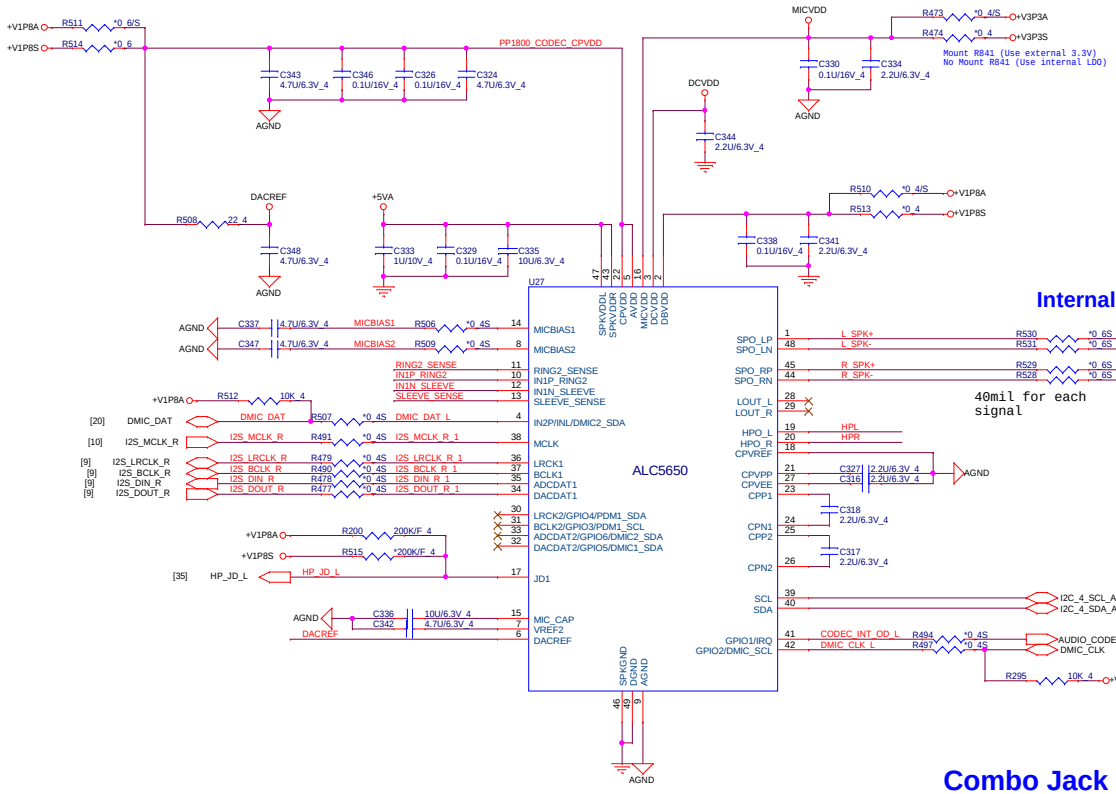
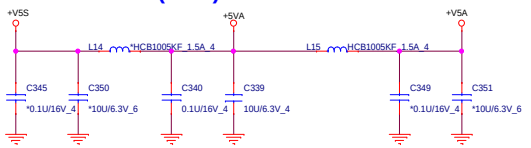
Removed (2015/03/27)

LTE NGFF (LTE)

Codec (ADO)

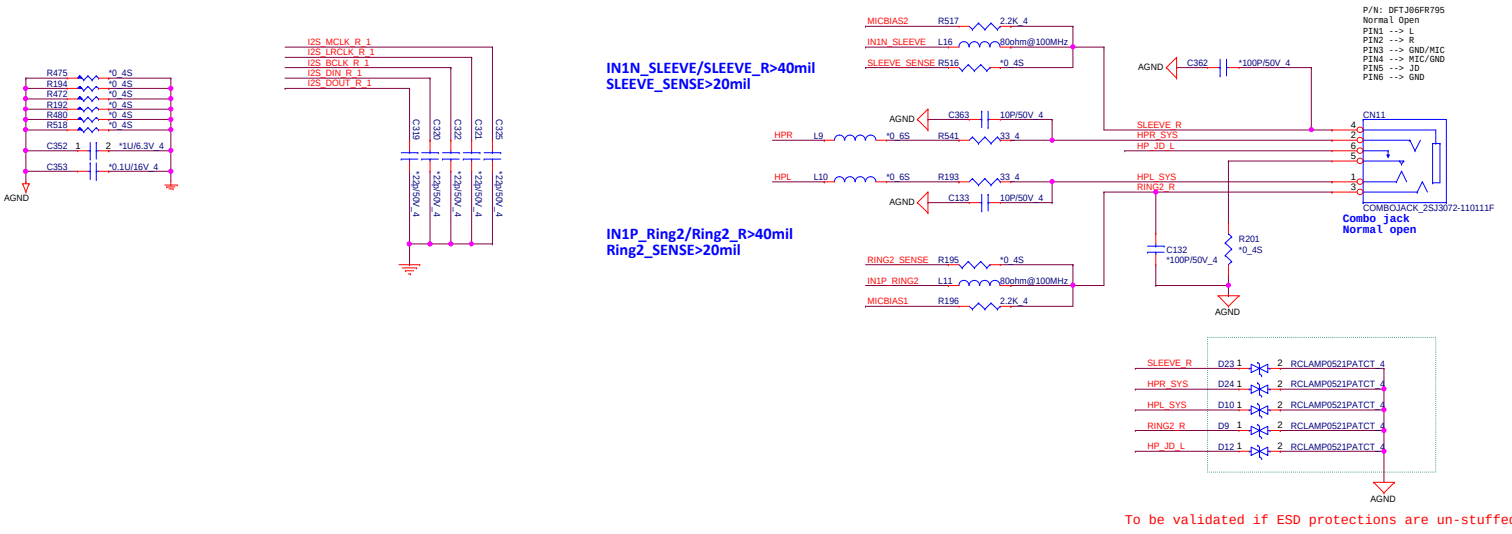


Codec PWR 5V (ADO)



Internal Speaker (ADO)

Combo Jack (ADO)



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Quanta Computer Inc.		
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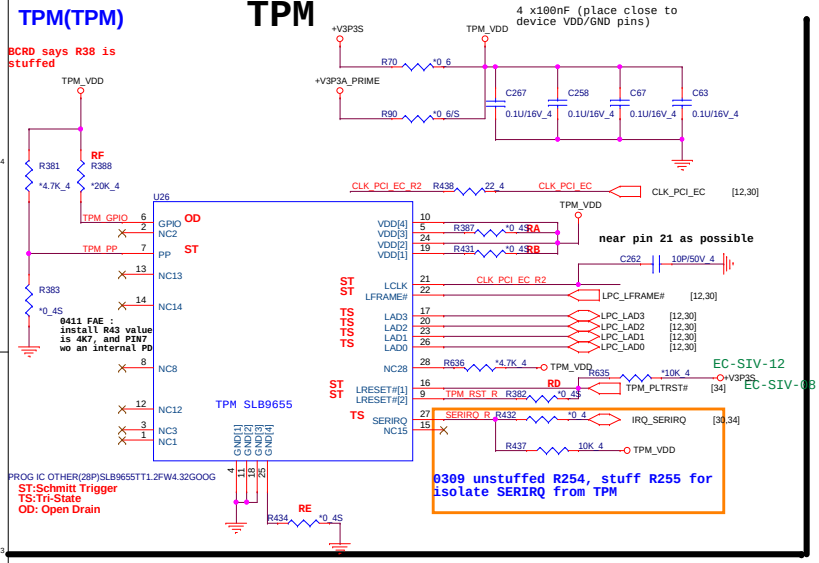
TPM/DAUGHTER BOARD CONNECTOR

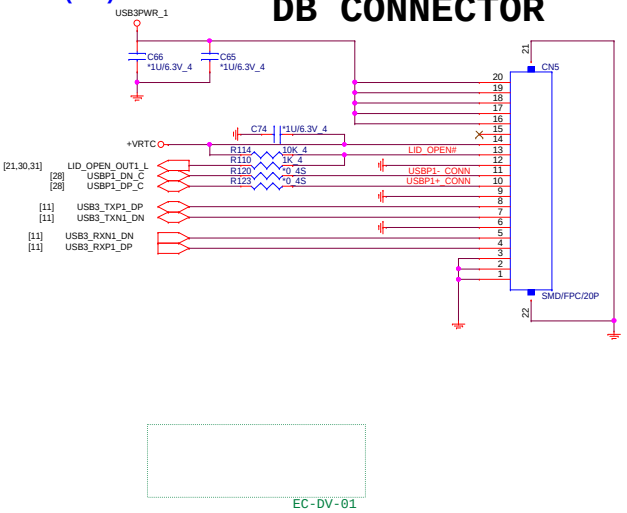
TPM(TPM)

TPM



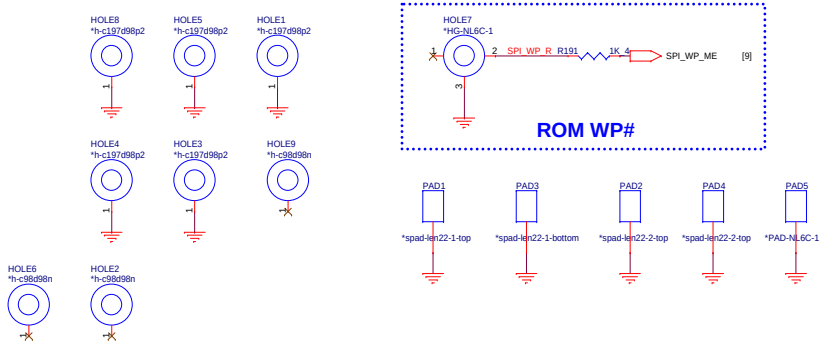
DB(UIF)

DB CONNECTOR

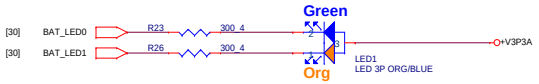


Holes(OTH)

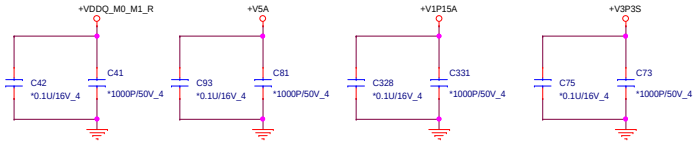
MOUNTING HOLES



Battery LED



EMI caps



RF caps

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Quanta Computer Inc.			
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	DB /TPM/Hole		1A
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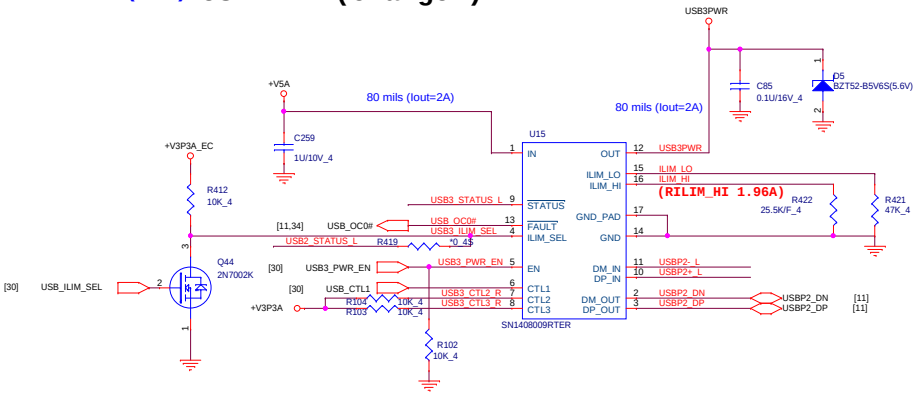
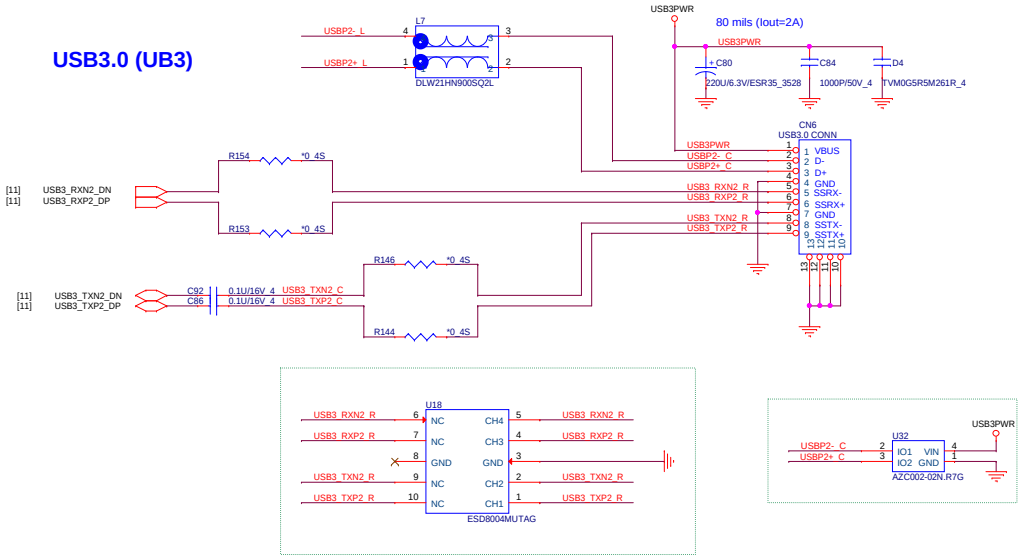
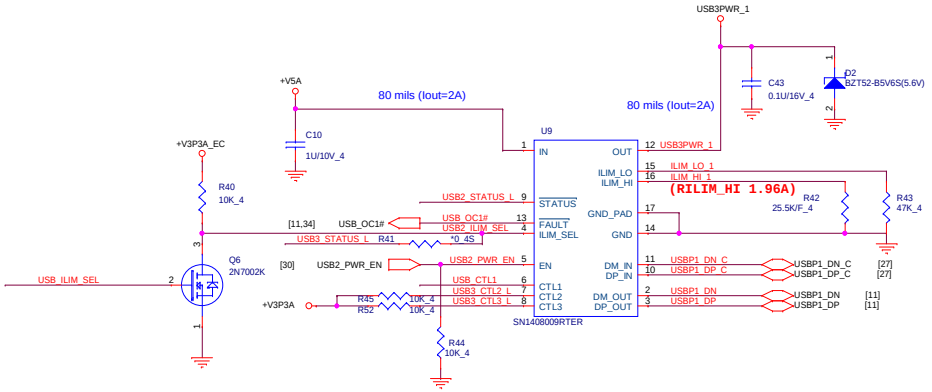
USB3.0 (UB3) USB PWR (Charger)



USB3.0 (UB3)



USB PWR(Charger)



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Quanta Computer Inc.		
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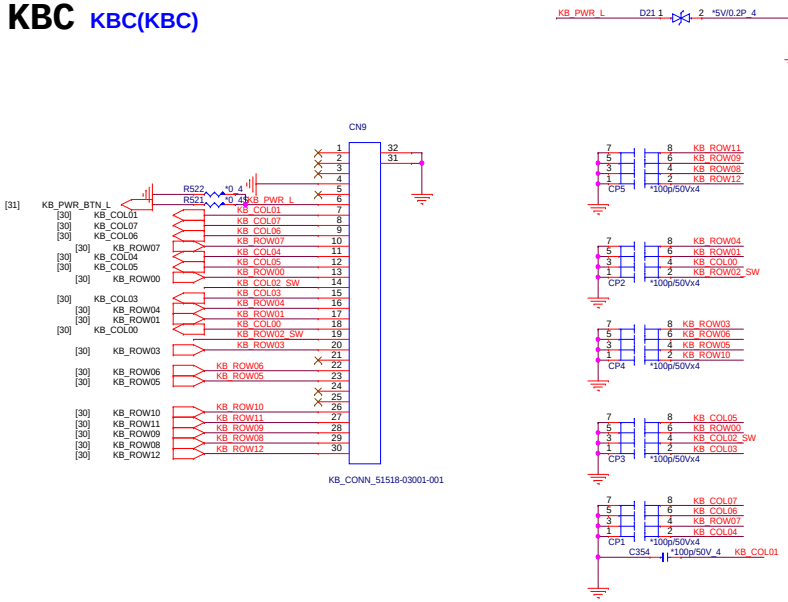
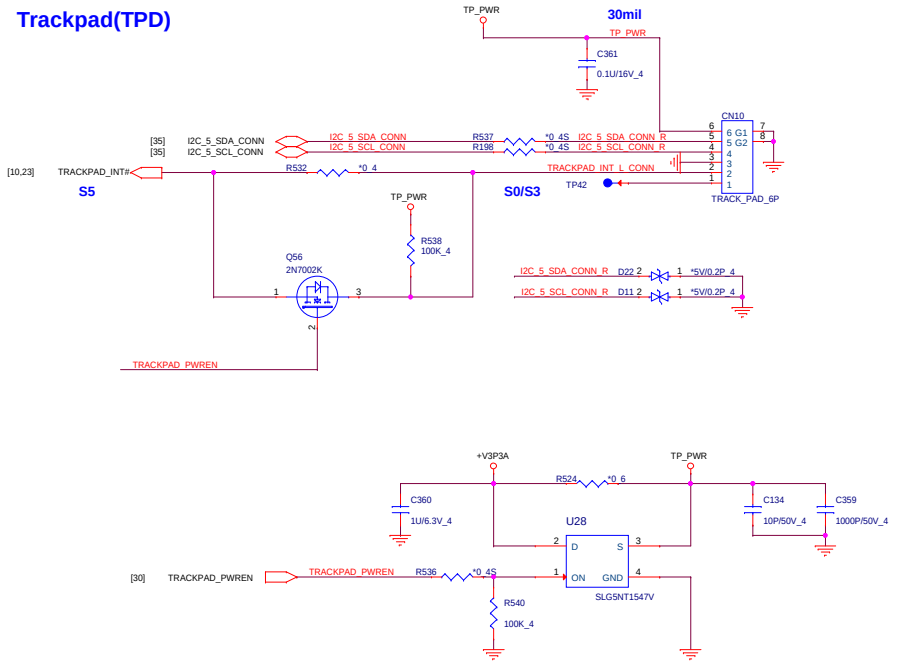
KBC KBC(KBC)



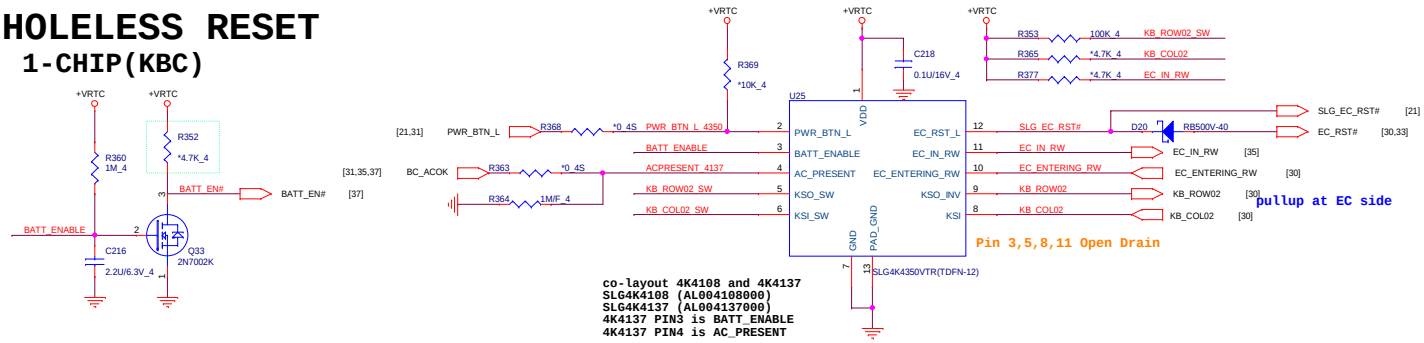
TRACK PAD BOARD CONN

Trackpad(TPD)



HOLELESS RESET

1-CHIP(KBC)



co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

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Quanta Computer Inc.		
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the C load need check

EMBEDDED CONTROLLER

EC-SIV-18

U14

XTAL
LPC
GPIO
KEYBOARD
SMBUS/I2C
SIDEBAND
UART
GPIO
GPIO
FLASH
POWER
GND

MEC1322-LZY DQFN132

SPI NOR FLASH

U13 W25X40CLSSIG

RAM ID - USE FOR BOARD ID

	EVT1.6	EVT1.5	EVT1.7	DVT	BCRD2 FAB1	BCRD2 FAB1.1
BOARD_ID0	0	0	1	1	0	1
BOARD_ID1	1	NA	0	1	0	0
BOARD_ID2	0	NA	0	0	1	1

For ICT, place on TOP side

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Quanta Computer Inc.

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	KBC	1A

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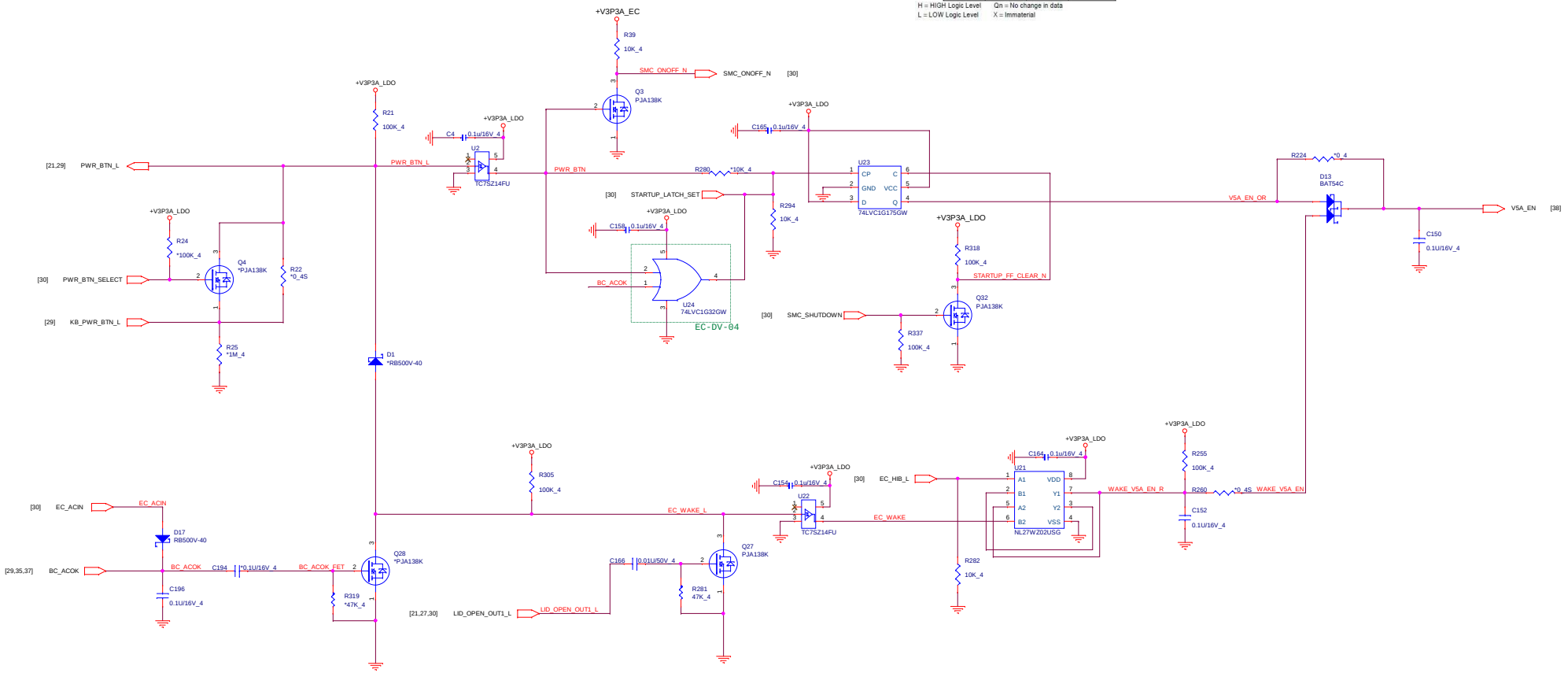
Function Table

Inputs			Output
CP	D	$\overline{C}$	Q
↓	L	H	L
↓	H	H	H
↘	X	H	Qn
X	X	L	L

H = HIGH Logic Level Qn = No change in data
L = LOW Logic Level X = Immaterial



EC HIB WAKE SOURCES

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Quanta Computer Inc.

Size	Document Number	Rev
	PWRBTN/PS/SVID	1A

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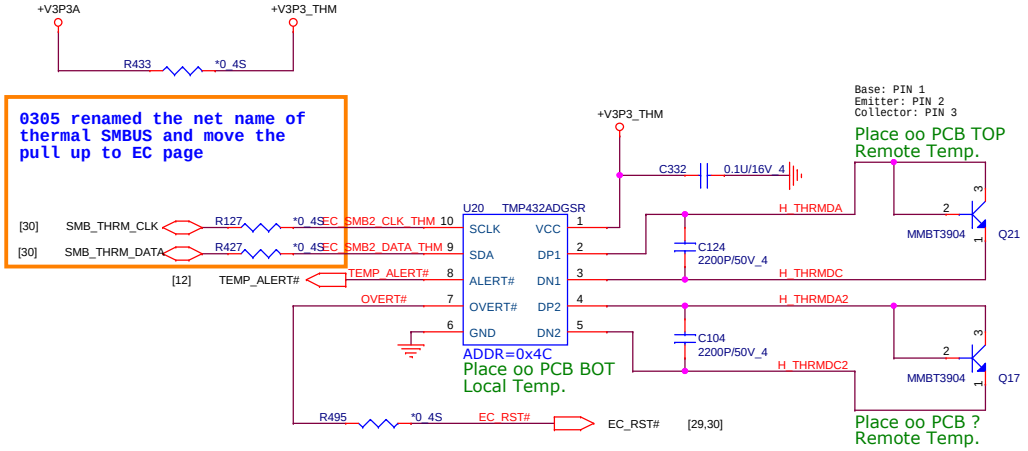
Removed (2015/03/30)

Thermal (THM)

THERMAL SENSOR



ACCELEROMETER

G-Sensor (ACS)

Removed (2015/03/27)

Touch screen(TSN)

Removed (2015/03/27)

Touch screen(TSN)

Removed (2015/03/27)

LED board(UIF)

Removed (2015/03/27)

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Quanta Computer Inc.

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	SENSORS	1A
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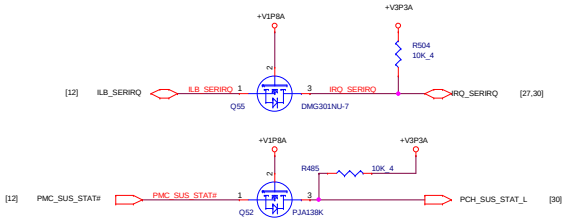
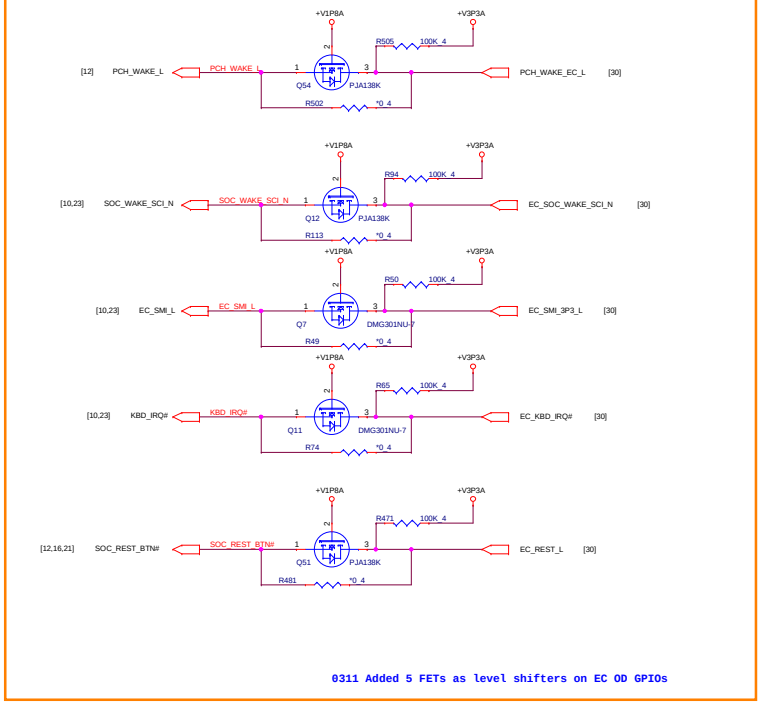
LEVEL TRANSLATOR 1

SoC(CPU)

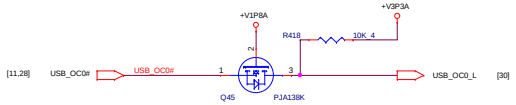
PWRON SEQUENCE



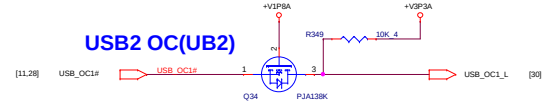


USB OC

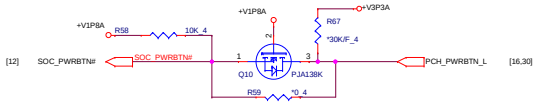
USB3 OC(UB3)

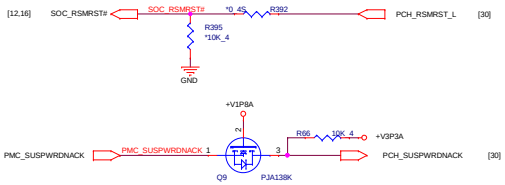


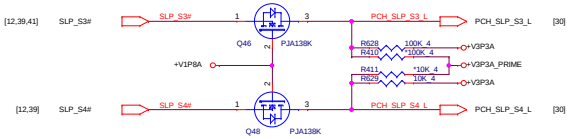
USB2 OC(UB2)



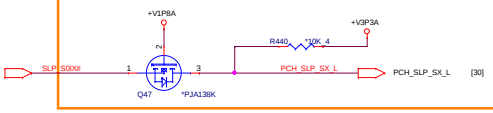
PWRON SEQUENCE

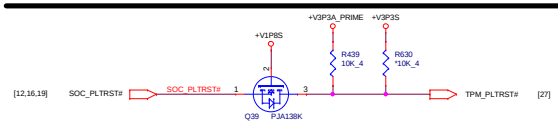


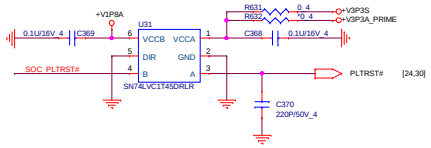




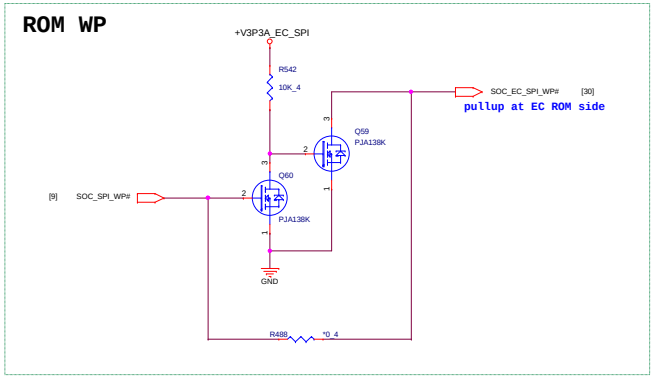
0305 SLP_SX related components are stuffed

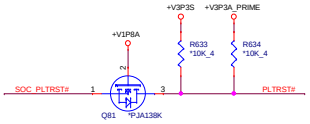






ROM WP





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NOTE:USE 4 BIT LEVEL TRANSLATORS

LEVEL TRANSLATOR 2

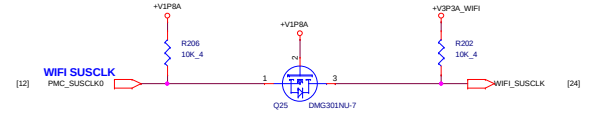
35

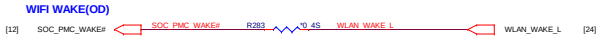
LTE(LTE)

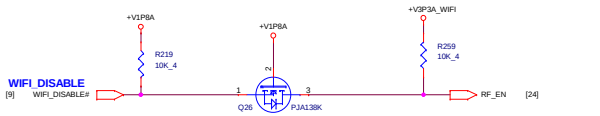
Removed (2015/03/27)

WiFi(NGF)

WIFI SIGNALS

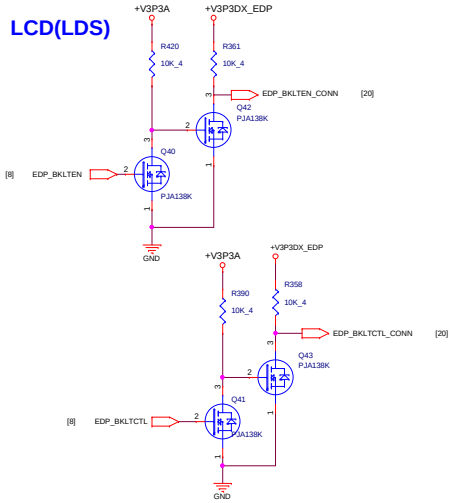






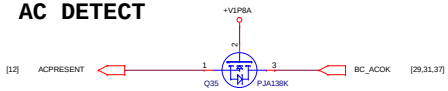
eDP CONTROL PIN

LCD(LDS)



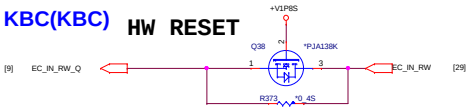
KBC(KBC)

AC DETECT

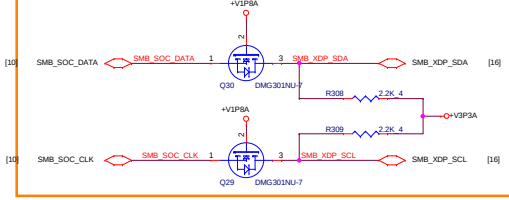


KBC(KBC)

HW RESET



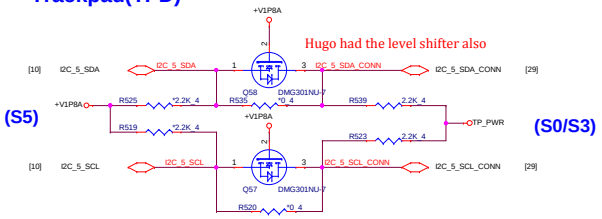
0310 Added level shifter on SMBUS from SoC to XDP, it will be un-stuffed in MP



TRACK PAD I2C_5 SIGNALS

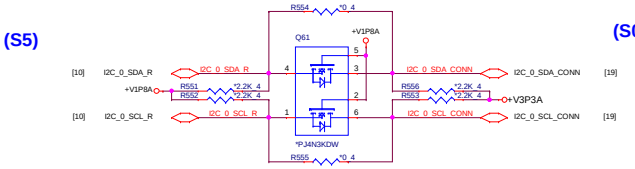
Trackpad(TPD)

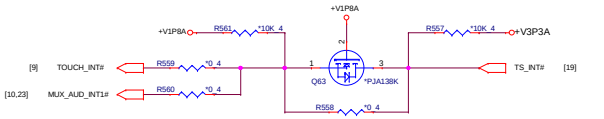
Hugo had the level shifter also



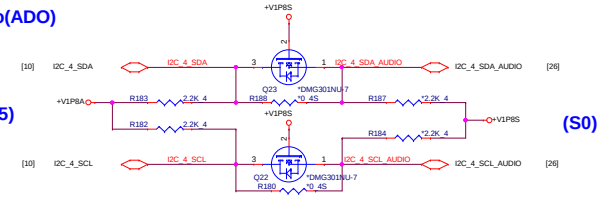
Touch Screen(TSN)

TOUCH SCREEN I2C_0 SIGNALS

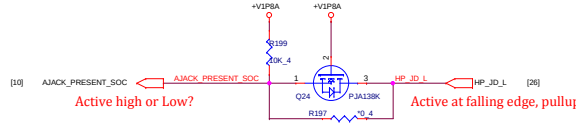




Audio(ADO)



Removed (2015/04/09)



Active high or Low?

Active at falling edge, pullup at 227 side

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NL6D

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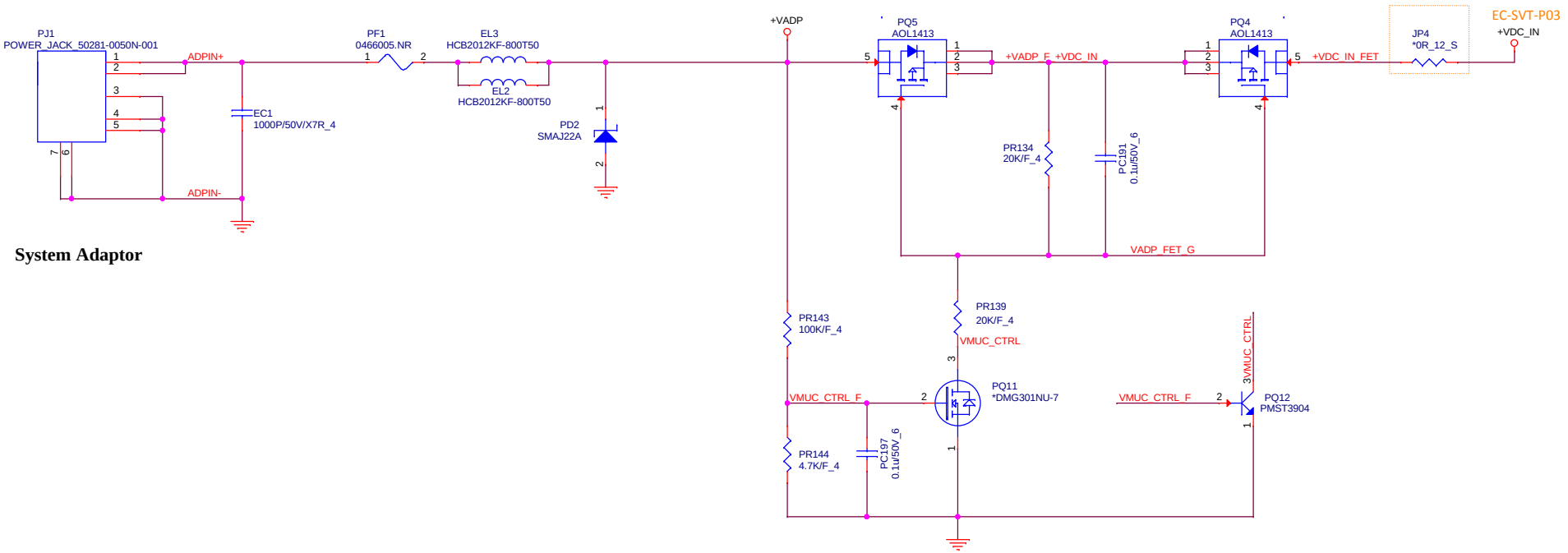
DC JACK



System Adaptor

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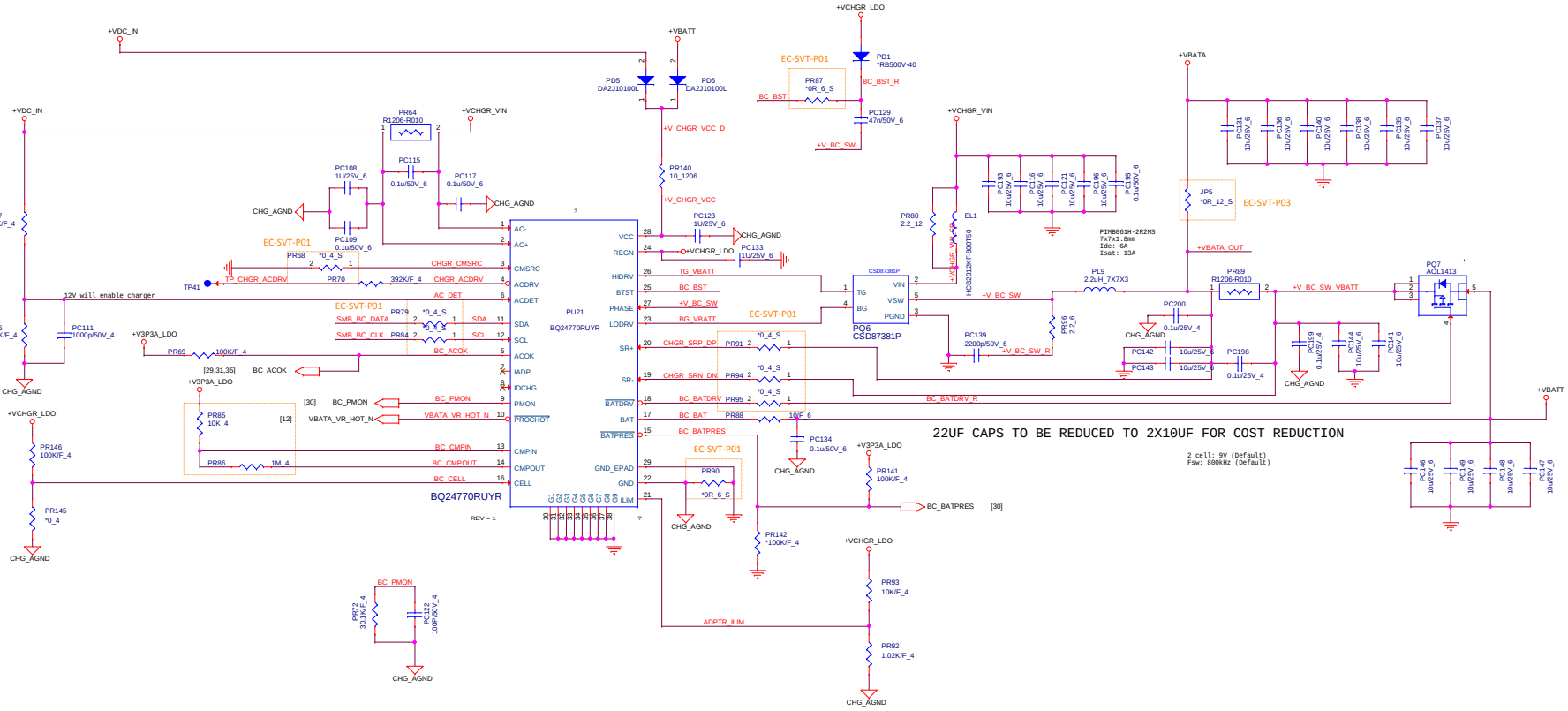
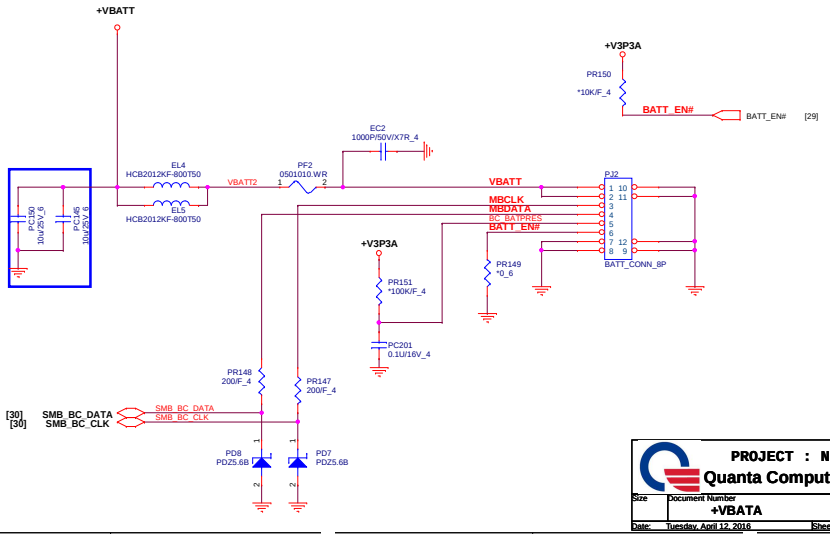


Removed (2015/09/21)

BATTERY CONNECTOR



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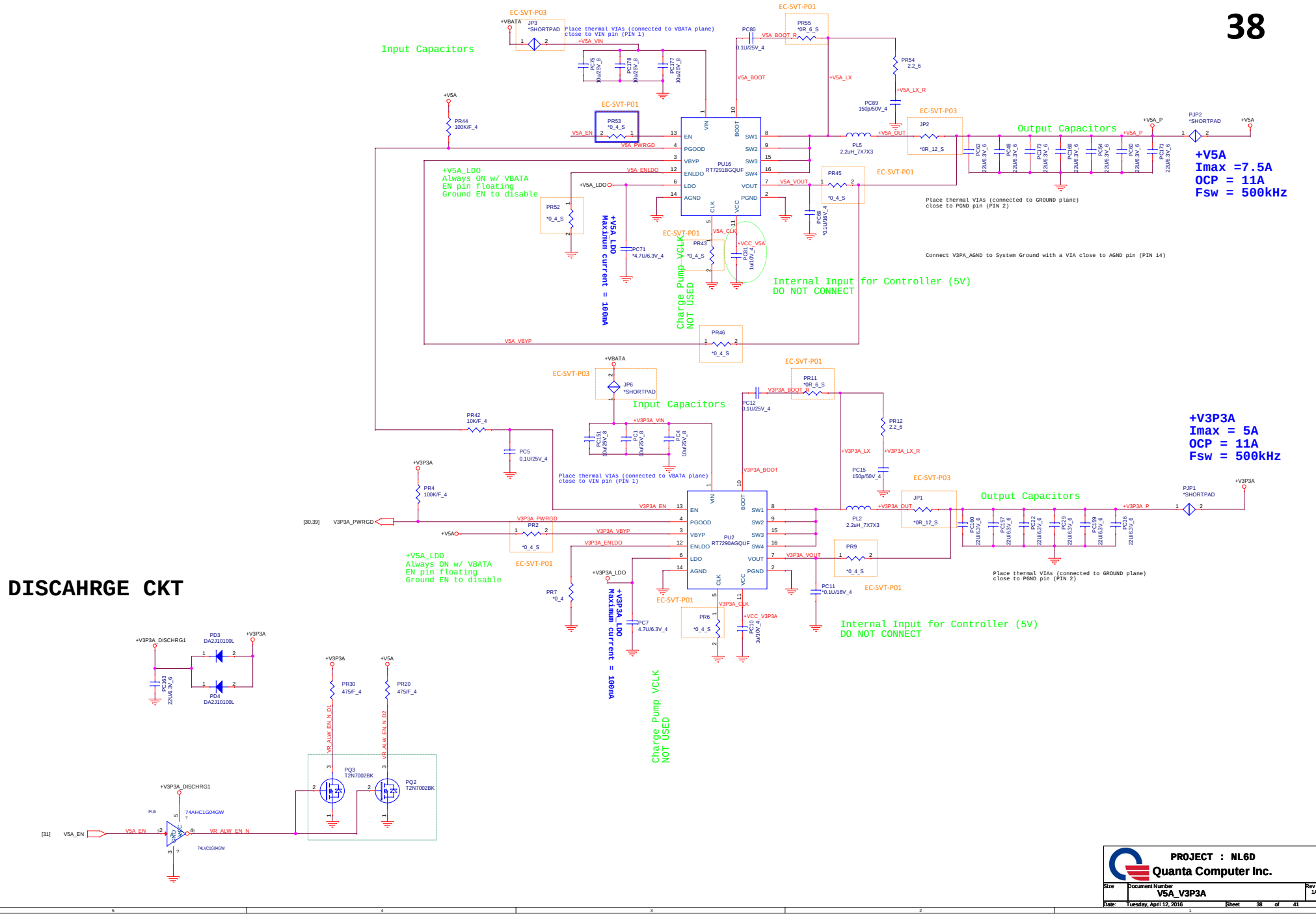
Input Capacitors
+V5A_LDO
Always ON w/ VBATA
EN pin floating
Ground EN to disable
+V5A_LDO Maximum current = 100mA
Charge Pump VCLK NOT USED
Internal Input for Controller (5V)
DO NOT CONNECT
Output Capacitors
+V5A
Imax =7.5A
OCP = 11A
Fsw = 500kHz
Place thermal VIAs (connected to GROUND plane) close to PGND pin (PIN 2)
Connect V3PA_AGND to System Ground with a VIA close to AGND pin (PIN 14)
+V3P3A
Imax = 5A
OCP = 11A
Fsw = 500kHz
+V3P3A_LDO Maximum current = 100mA
DISCAHRGE CKT
+V3P3A_DISCHRG1
74AHC1G04GW
74LVC1G04GW
VR_ALW_EN_N_D1
VR_ALW_EN_N_D2
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V5A_V3P3A
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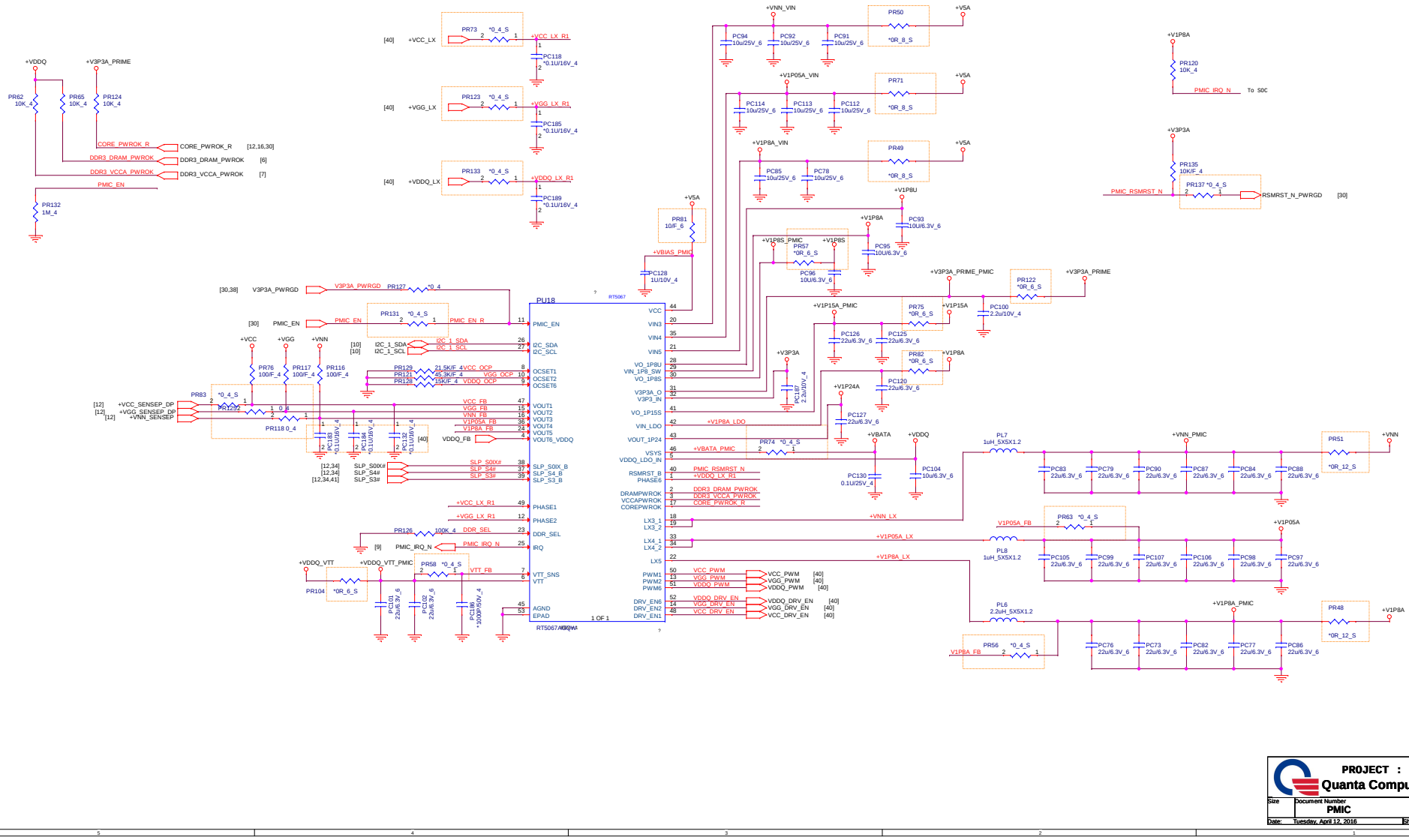
PMIC



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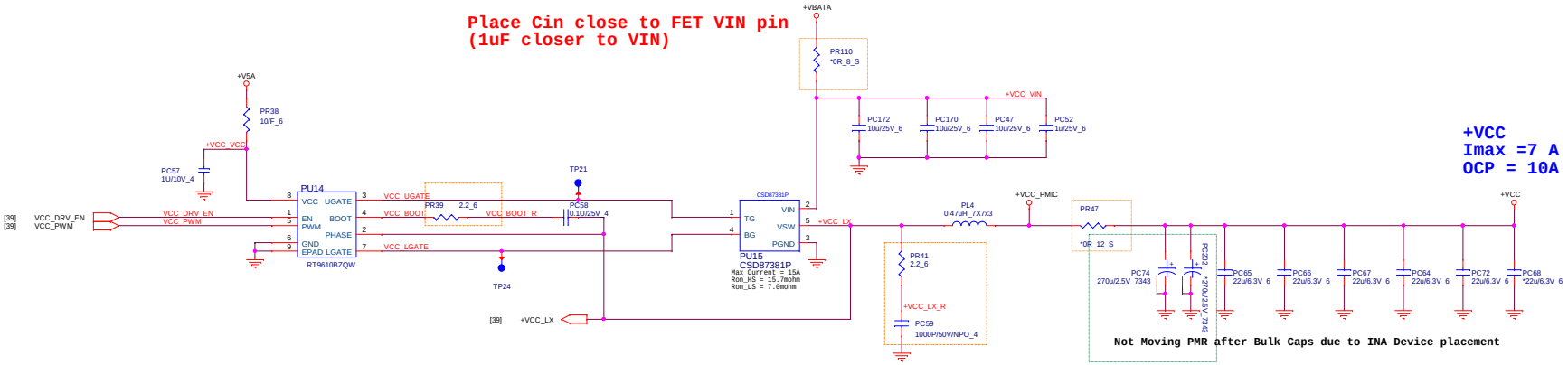
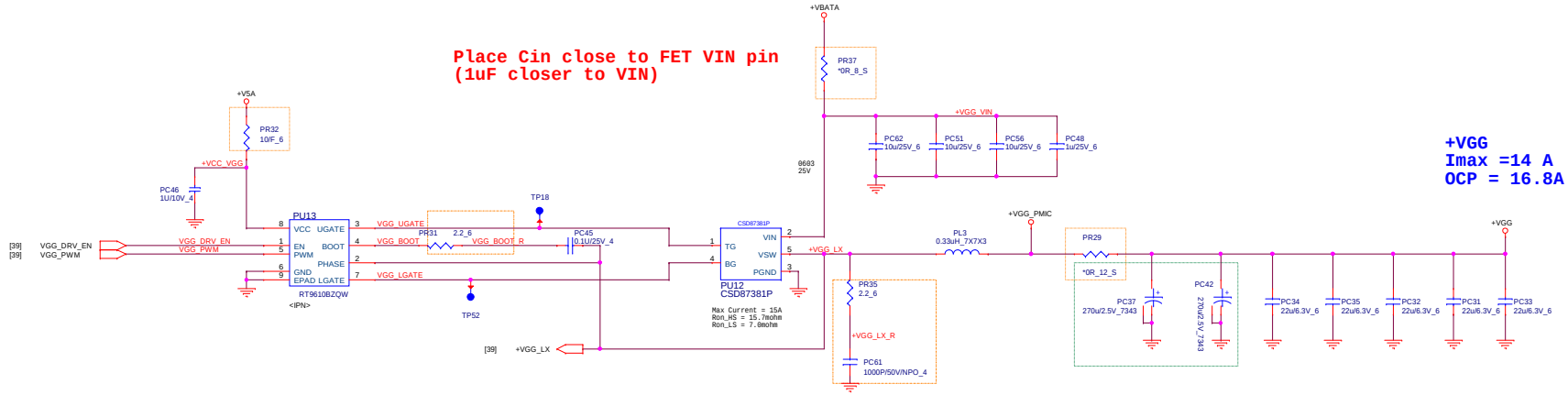
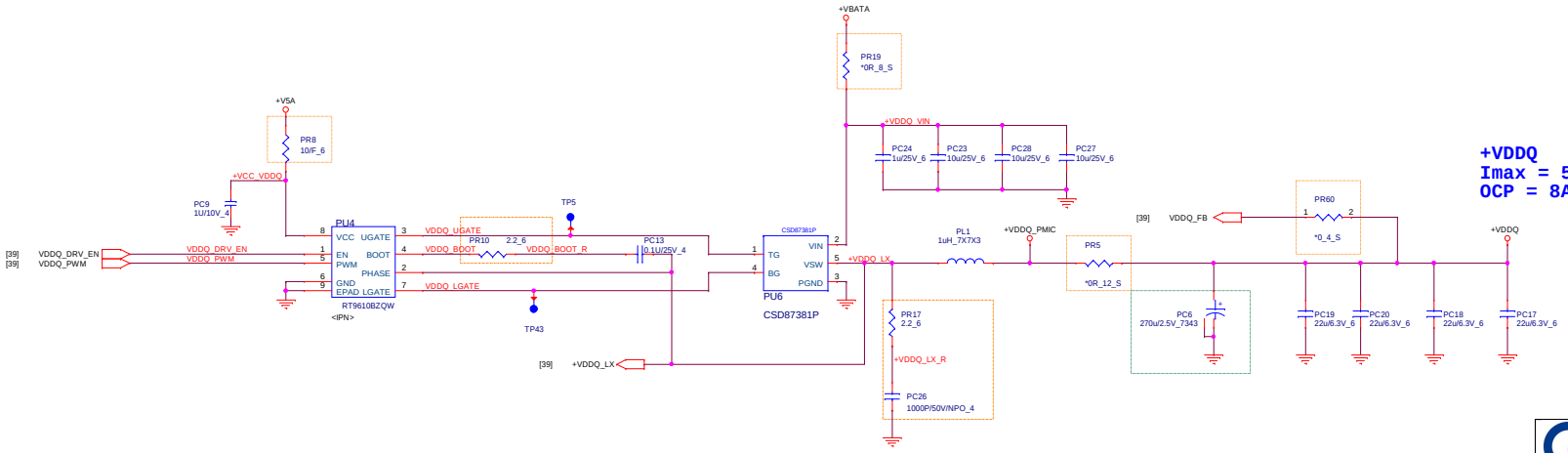
VR PAGE : +VCC, +VGG, +VDDQ



+VCC
Imax =7 A
OCP = 10A



+VGG
Imax =14 A
OCP = 16.8A



+VDDQ
Imax = 5A
OCP = 8A

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	VCC, VGG, VDDQ	1A
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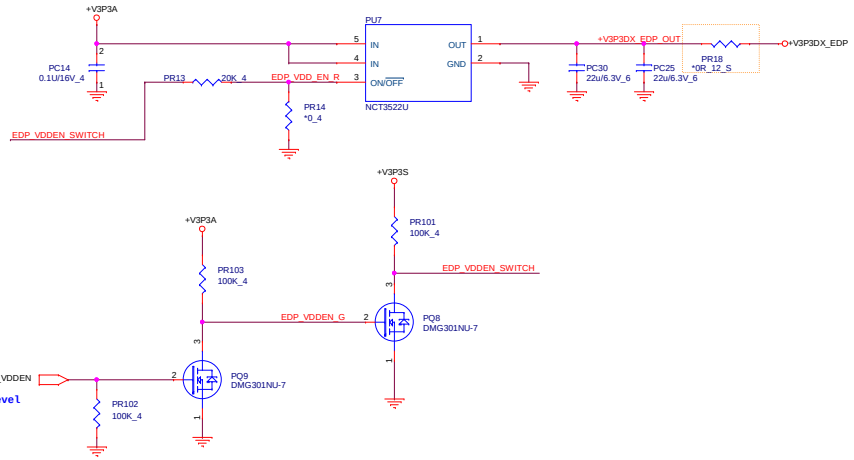
VR PAGE: POWER GATES

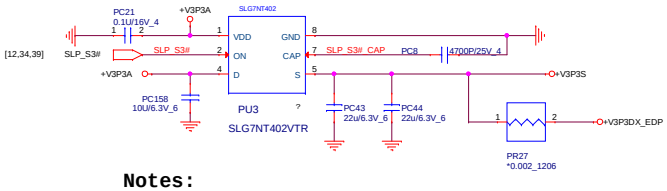
+V3P3DX_EDP: VCC_EDP

CHECK SLEW RATE



DEFAULT OPTION FOR PANEL POWER SEQUENCING

+V3P3S



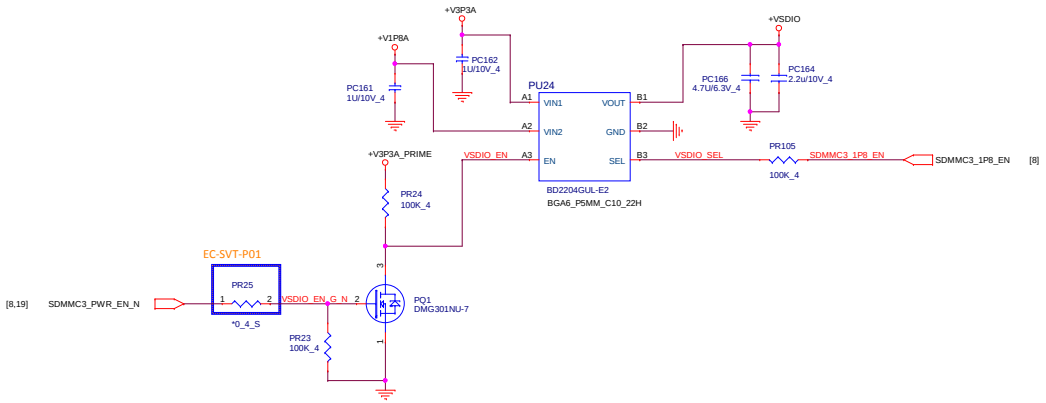
Notes:
Imax: 4A
Rise time: 1ms

+VSDIO

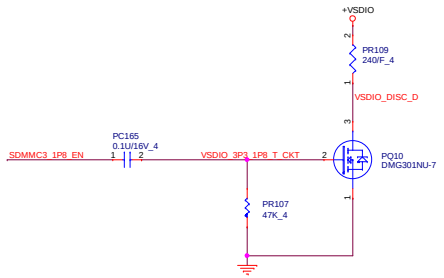
SDMMC3_PWR_EN_N	SDMMC3_1P8_EN	VSDIO (V)
1	0	0V
1	1	0V
0	0	3.3V
0	1	1.8V

Notes:
Imax: 100 mA
Rise time: 150 uSec

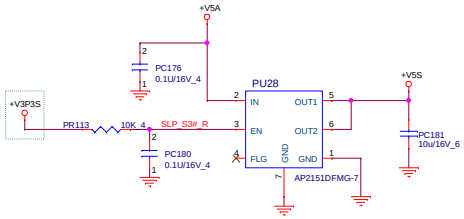
CAD Note : place the caps close to IC
NEW FOOT PRINT IS REQUIRED



Design Note :
controls the time when VSDIO changes from 3.3V to 1.8V



+V5S



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