1. Schematic Page Description :

Origins Schematic Ver :

01

SoC I2C table

Function	Channel	Read	Write
Touch Screen	I2C0	0x?	
Audio Codec	I2C1	0x?	0x?
VNN (reserve)	I2C4		
Track Pad	I2C5		
EC	I2C6		

EC SMBus/I2C table

Function	Channel	Address
Battery/Thermal	SMB0	
NA	SMB1	
G-Sensor	I2C1	
PCH	I2C2	
VNN	I2C3	

Current sensor address

Function	Channel	Function	Channel
+VBATA	0x47	+VCC_OUT	0x40
+V5A	0x43	+VGG	0x44
+V3P3A	0x4B	+VNN	0x45
+V1P05A	0x46	+VDDQ_OUT	0x41
+V1P8A	0x49		

USB3/2 port mapping

USB3 Port No#	Usage	USB2 Port No#	Usage
USB3P0	NA	USB2P0	I/O(2.0)
USB3P1	NA	USB2P1	LTE
USB3P2	I/O	USB2P2	I/O(3.0)
USB3P3	NA	USB2P3	CCD
		USB2P4	BT

PCIe port mapping

PCIe port No#	Usage	PCIe CLK#	Usage
PCIe_0	Video Codec	PCIe_CLK0	Video Codec
PCIe_1	Video Codec	PCIe_CLK1	NA
PCIe_2	WLAN	PCIe_CLK2	WLAN
PCIe_3	NA	PCIe_CLK3	NA

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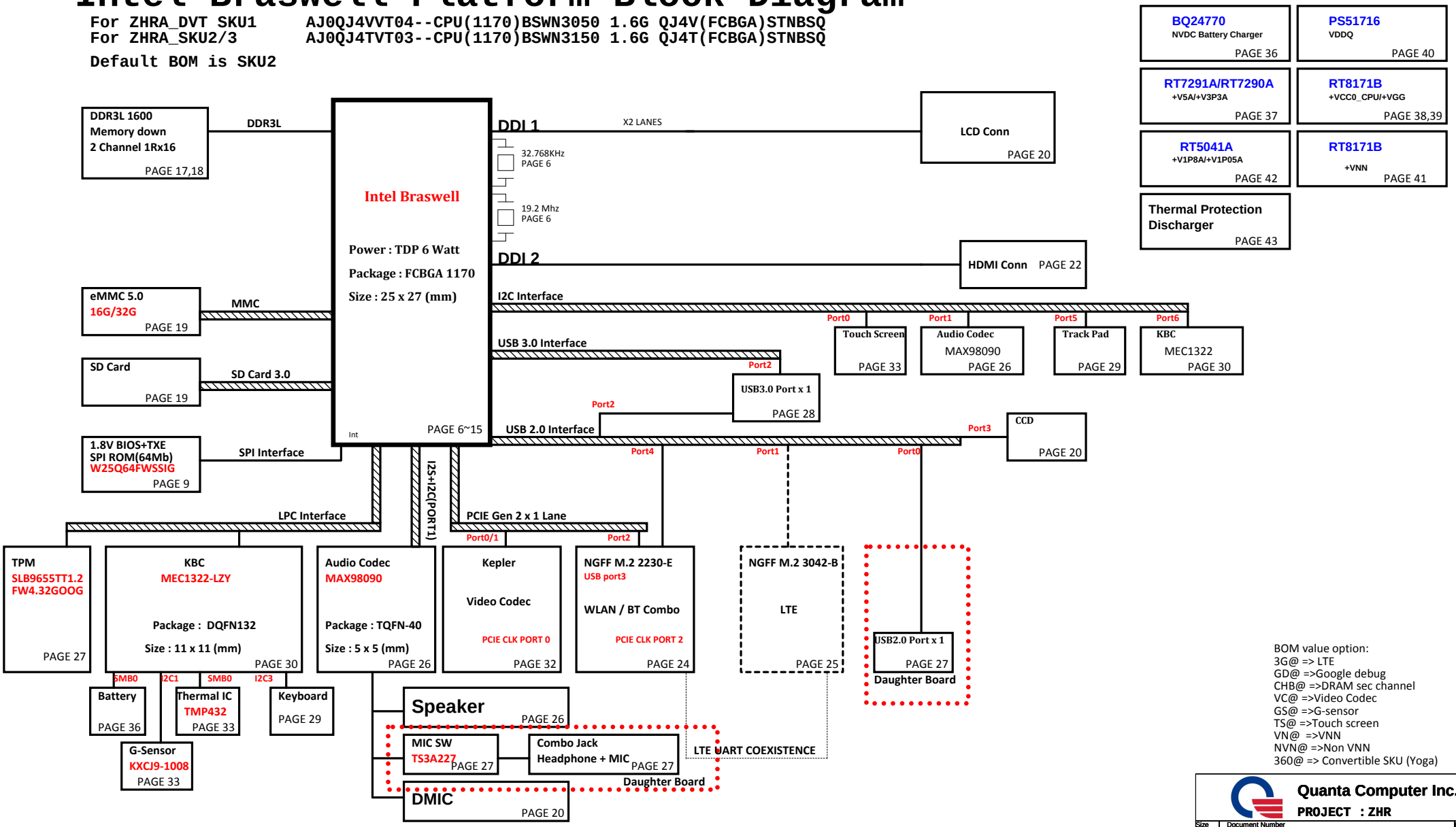
ZHRA/Origins_T

02

Intel Braswell Platform Block Diagram

For ZHRA_DVT SKU1 AJ0QJ4VVT04--CPU(1170)BSWN3050 1.6G QJ4V(FCBGA)STNBSQ
For ZHRA_SKU2/3 AJ0QJ4TVT03--CPU(1170)BSWN3150 1.6G QJ4T(FCBGA)STNBSQ

Default BOM is SKU2



BQ24770
NVDC Battery Charger
PAGE 36

PS51716
VDDQ
PAGE 40

RT7291A/RT7290A
+V5A/+V3P3A
PAGE 37

RT8171B
+VCC0_CPU/+VGG
PAGE 38,39

RT5041A
+V1P8A/+V1P05A
PAGE 42

RT8171B
+VNN
PAGE 41

Thermal Protection
Discharger
PAGE 43

BOM value option:
3G@ => LTE
GD@ =>Google debug
CHB@ =>DRAM sec channel
VC@ =>Video Codec
GS@ =>G-sensor
TS@ =>Touch screen
VN@ =>VNN
NVN@ =>Non VNN
360@ => Convertible SKU (Yoga)

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	Block Diagram	1A

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Size	Document Number	Rev
	SMBUS_I2C	1A

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Size	Document Number	Rev
	BSW PWR TREE	1A

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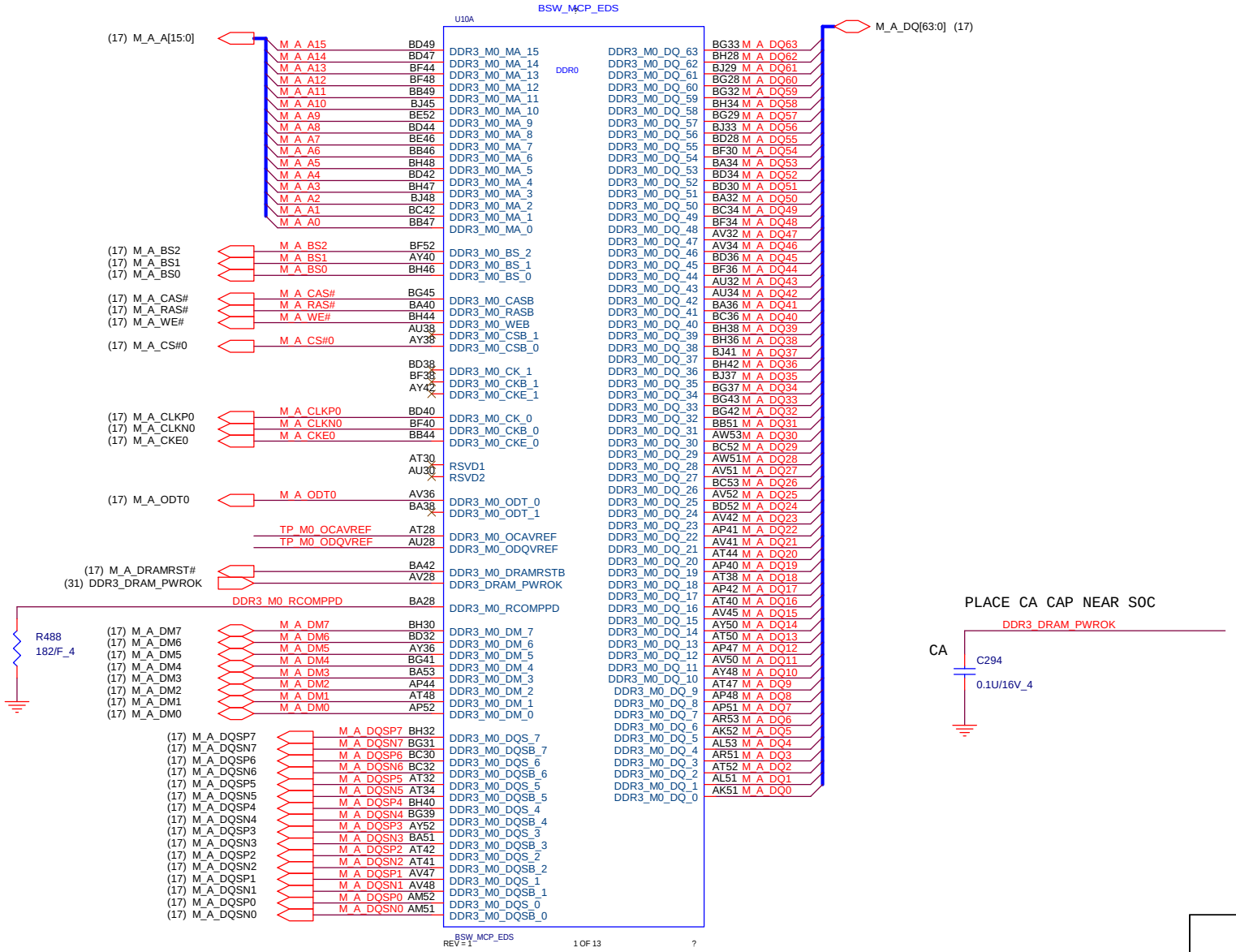
SoC (CPU)

BRASWELL SOC - MEMORY DDR3L CHANNEL A

06



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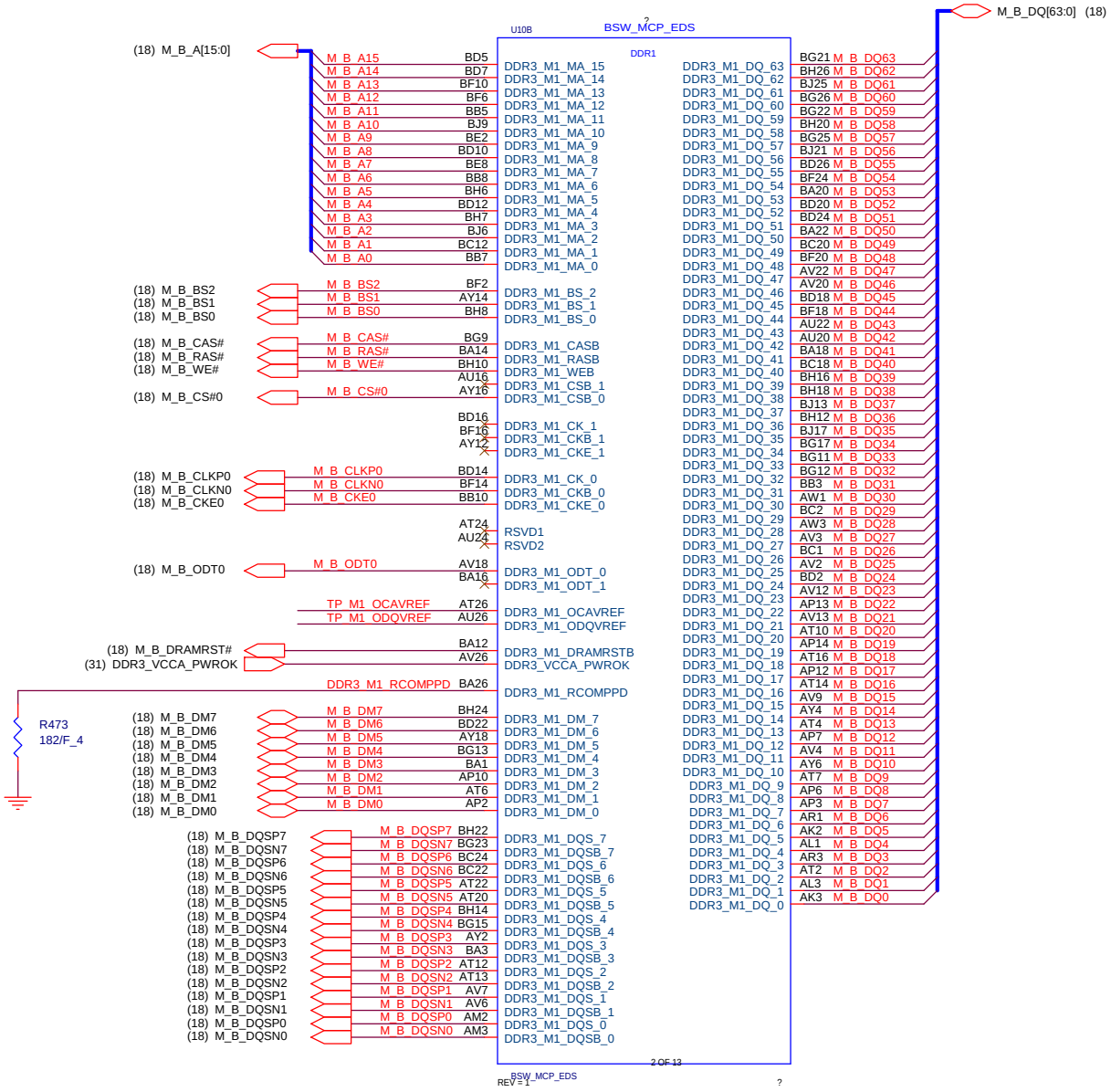
BRASWELL - MEMORY DDR3L CHANNEL B

SoC (CPU)

07



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Size	Document Number BSW 2/10 (DDRB)	Rev 1A
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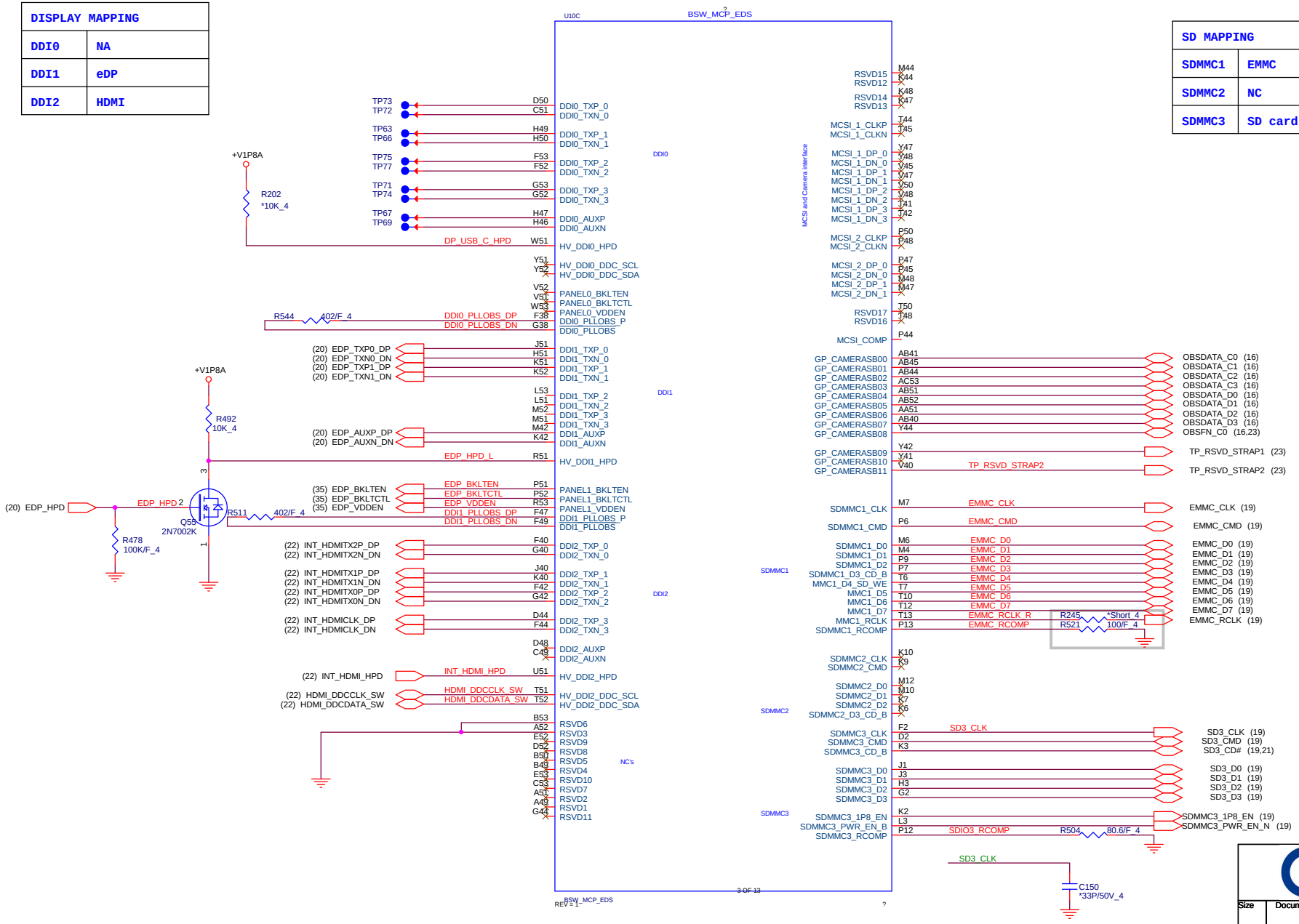
BRASWELL SOC - DISPLAY, XDP, EMMC, SD

SoC (CPU)

08

DISPLAY MAPPING	
DDI0	NA
DDI1	eDP
DDI2	HDMI

SD MAPPING	
SDMMC1	EMMC
SDMMC2	NC
SDMMC3	SD card



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PROJECT : ZHR			
Size	Document Number		Rev
	BSW 3/10 (DDI,SD,EMMC)		1A
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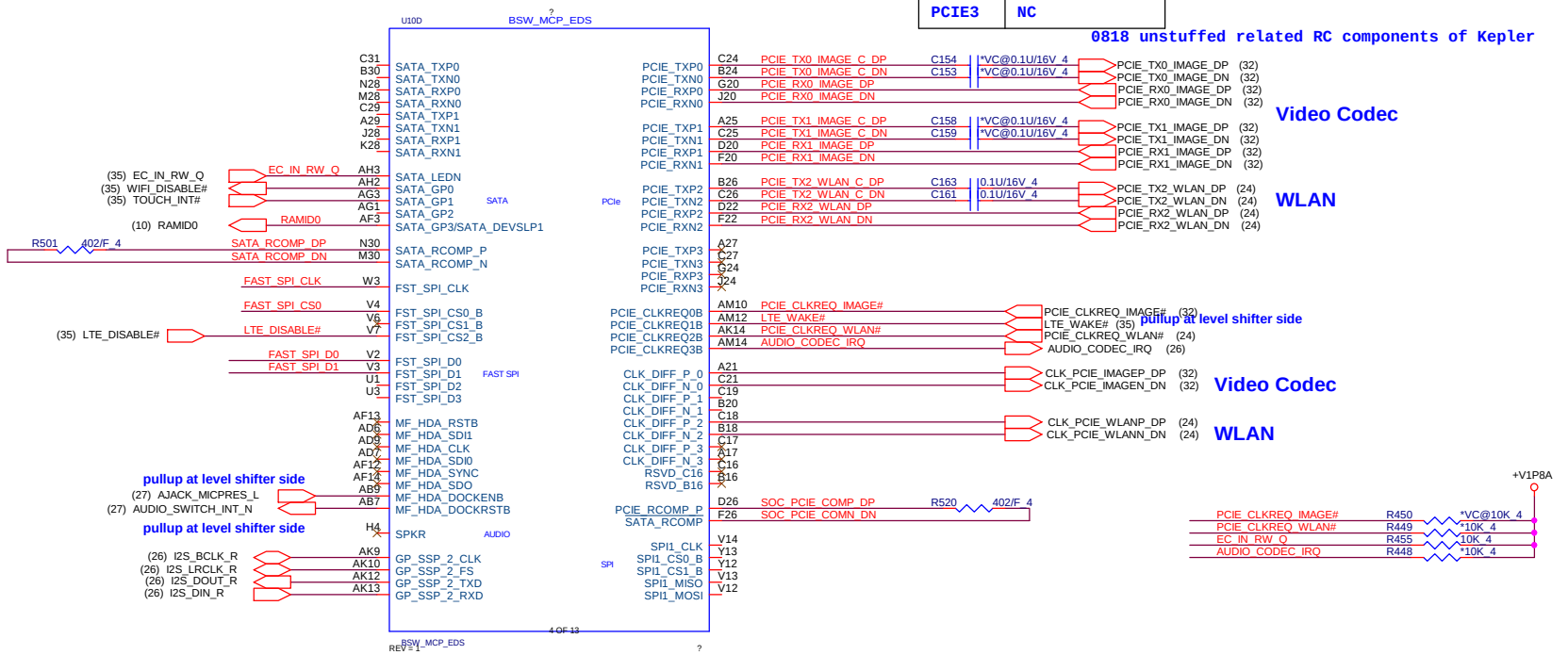
BSW SOC - SATA, PCIe, SPI, I2S

09

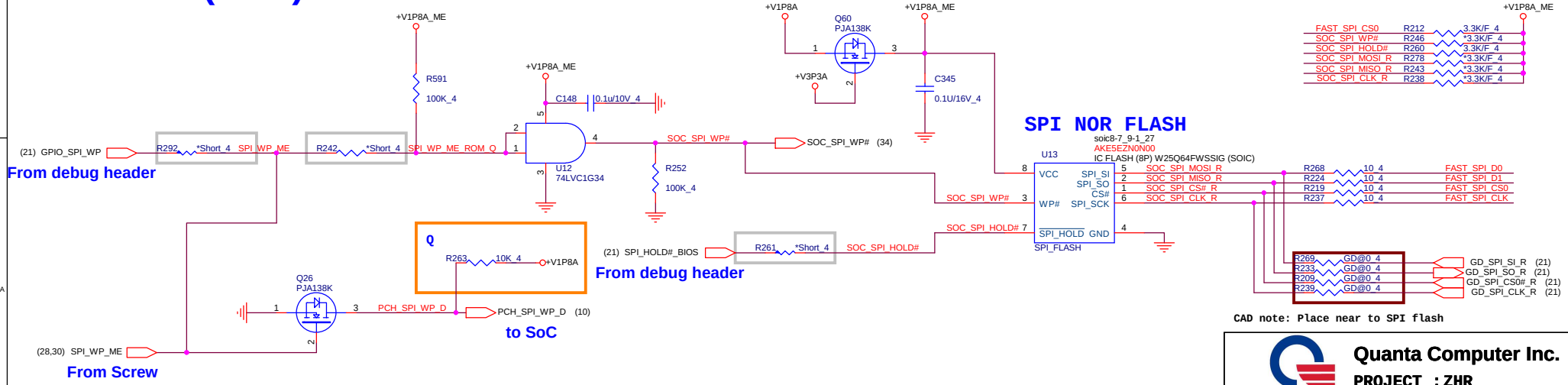
SoC (CPU)

PCIe MAPPING	
PCIE0	Video Codec
PCIE1	Video Codec
PCIE2	WIFI (StP)
PCIE3	NC

0818 unstuffed related RC components of Kepler



BIOS ROM(CPU)



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PROJECT : ZHR

Size	Document Number	Rev
	BSW 4/10 (PCIE/SATA/SPI)	1A
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SoC (CPU)

BRASWELL - I2C, XDP, SM BUS

10

U10E BSW_MCP_EDS

RESERVED ISH GPIOs - RSVD for type C GPIOs

XTAL19_2_IN P24 OSCIN
XTAL19_2_OUT M22 OSCOUT
J26 RSVD13
N26 RSVD17
R293 2.49K/F_4 ICLK_ICOMP P20 ICLKICOMP
R295 49.9/F_4 ICLK_RCOMP N20 ICLKRCOMP
P26 RSVD18
K26 RSVD14
M26 RSVD16
AH45 RSVD1

(26) I2S_MCLK_R I2S_MCLK_R A9 MF_PLT_CLK0
RAMID2 C9 MF_PLT_CLK1
B8 MF_PLT_CLK2
B7 MF_PLT_CLK3
B5 MF_PLT_CLK4
B4 MF_PLT_CLK5

(16) XDP_GPIO_DFX0 AM40 GPIO_DFX0
(16) XDP_GPIO_DFX1 AM41 GPIO_DFX1
(16) XDP_GPIO_DFX2 AM44 GPIO_DFX2
(16) XDP_GPIO_DFX3 AM45 GPIO_DFX3
(16) XDP_GPIO_DFX4 AM47 GPIO_DFX4
(16) XDP_GPIO_DFX5 AK48 GPIO_DFX5
(16) XDP_GPIO_DFX6 AM48 GPIO_DFX6
(16) XDP_GPIO_DFX7 AK41 GPIO_DFX7
(16) XDP_GPIO_DFX8 AK42 GPIO_DFX8

(23,34) SOC_WAKE_SCI_N AD51 GPIO_SUS0
(23,35) MUX_AUD_INT1# AD52 GPIO_SUS1
(23,34) EC_SMI_L AH50 GPIO_SUS2
(23,34) KBD_IRQ# AH48 GPIO_SUS3
DFX_SUS_DBG_STRAP AH51 GPIO_SUS4
EC_KBD_ALERT_SOC AH52 GPIO_SUS5
(16,23) SOC_RUNTIME_SCI AG51 GPIO_SUS6
(23) TRACKPAD_INT# TRACKPAD_INT# AG53 GPIO_SUS7
(23) NFC_FW_RESET# AF52 SEC_GPIO_SUS9
(23) TP_RSVD_STRAP3 AF51 SEC_GPIO_SUS8
(23) NFC_PWR_MANAGE AE51 SEC_GPIO_SUS10
(35) SIM_DET_C AC51 SEC_GPIO_SUS11
R193 100/F_4 SOC_GPIO_RCOMP AH40 GPIO0_RCOMP
(35) DET_TRIGGER DET_TRIGGER Y3 GPIO_ALERT

pullup at level shifter side

(23) SOC_KBC_SMI R173 *Short_4 DFX_SUS_DBG_STRAP

5 OF 13 BSW_MCP_EDS REV = 1

RSVD3 C11 TP_HOST_DETECT TP34
RSVD2 B10 TP_DEVICE_DETECT TP29
RSVD9 F12 TP_POL_DETECT TP70
RSVD8 F10 TP_WAKE_ALERT# TP68
RSVD5 D12 PCH_SPI_WP_D (9)
RSVD7 E8
RSVD4 C7
RSVD6 D6
RSVD11 J12
RSVD10 F7
RSVD12 J14
RSVD15 L13
I2C0_SCL AK6 I2C_0_SCL R471 *Short_4 I2C_0_SCL_R I2C_0_SCL_R (35)
I2C0_SDA AH7 I2C_0_SDA R464 *Short_4 I2C_0_SDA_R I2C_0_SDA_R (35)
I2C1_SCL AF6 I2C_1_SCL (35)
I2C1_SDA AH6 I2C_1_SDA (35)
I2C2_SCL AF9 I2C_NFC_SCL TP7
I2C2_SDA AF7 I2C_NFC_SDA TP6
I2C3_SCL AE4 RAMID1
I2C3_SDA AD2 RAMID3
I2C4_SCL AC1 I2C_4_SCL_C TP9
I2C4_SDA AD3 I2C_4_SDA_C TP8
I2C5_SCL AB2 I2C_5_SCL (35)
I2C5_SDA AC3 I2C_5_SDA (35)
TP38
I2C6_SCL AA1 I2C_6_SCL_C
I2C6_SDA AB3 SDCARD_WP SDCARD_WP (19)
RSVD_AA3 AA3
RSVD_Y2 Y2
SMBUS AM6 SMB_SOC_CLK SMB_SOC_CLK (16,35)
MF_SMB_CLK AM7 SMB_SOC_DATA SMB_SOC_DATA (16,35)
MF_SMB_DATA AM9 TP_GPIO_2_SOC TP55
MF_SMB_ALERTB

Touch panel
Level shifter is un-stuffed
Level shifter of Touch screen INT is un-stuffed

Audio
Level shifter is stuffed for Audio codec and MIC switch

Level shifter of Track Pad INT is stuffed
Track pad Level shifter is stuffed

+V1P8A
R166 4.7K_4 SOC_WAKE_SCI_N
R153 *10K_4 KBD_IRQ#
R157 *10K_4 EC_SMI_L

RAMID

RAMID0 (9)
+V1P8A
R460 *10K_4 RAMID0 R454 10K_4
R178 *10K_4 RAMID1 R184 10K_4
R271 10K_4 RAMID2 R281 *10K_4
R195 10K_4 RAMID3 R192 *10K_4

0819 Changed the PU of RAMID back to 10K

19.2MHz X'tal

C164 15P/50V_4 XTAL19_2_OUT
Y2 19.2MHZ +-20PPM
R310 200K/F_4
C171 15P/50V_4 XTAL19_2_IN

2nd source:BG619200014 (TXC)

EC_KBD_ALERT_SOC EC_KBD_ALERT_SOC (23)
(30) EC_KBD_ALERT Q95 PJA138K

TRACKPAD_INT# R827 33_4 TRACKPAD_INT#_R (29)
C423 180p/50V_4

Vender	RAM_ID	Q PN	Mfr. PN	Freq.	Size	Total Size	
Samsung	0000	AKD5PGST514	K4B4G1646Q-HYK0	1600MHz	4Gb	4GB	
Hynix	0001	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4Gb	4GB	ZHRA DVT SKU2/3
Samsung	0010	AKD5PGST514	K4B4G1646Q-HYK0	1600MHz	4Gb	2GB	ZHRA DVT SKU1
Hynix	0011	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4Gb	2GB	

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	BSW 5/10 (I2C/DFX/GPIO)	1A
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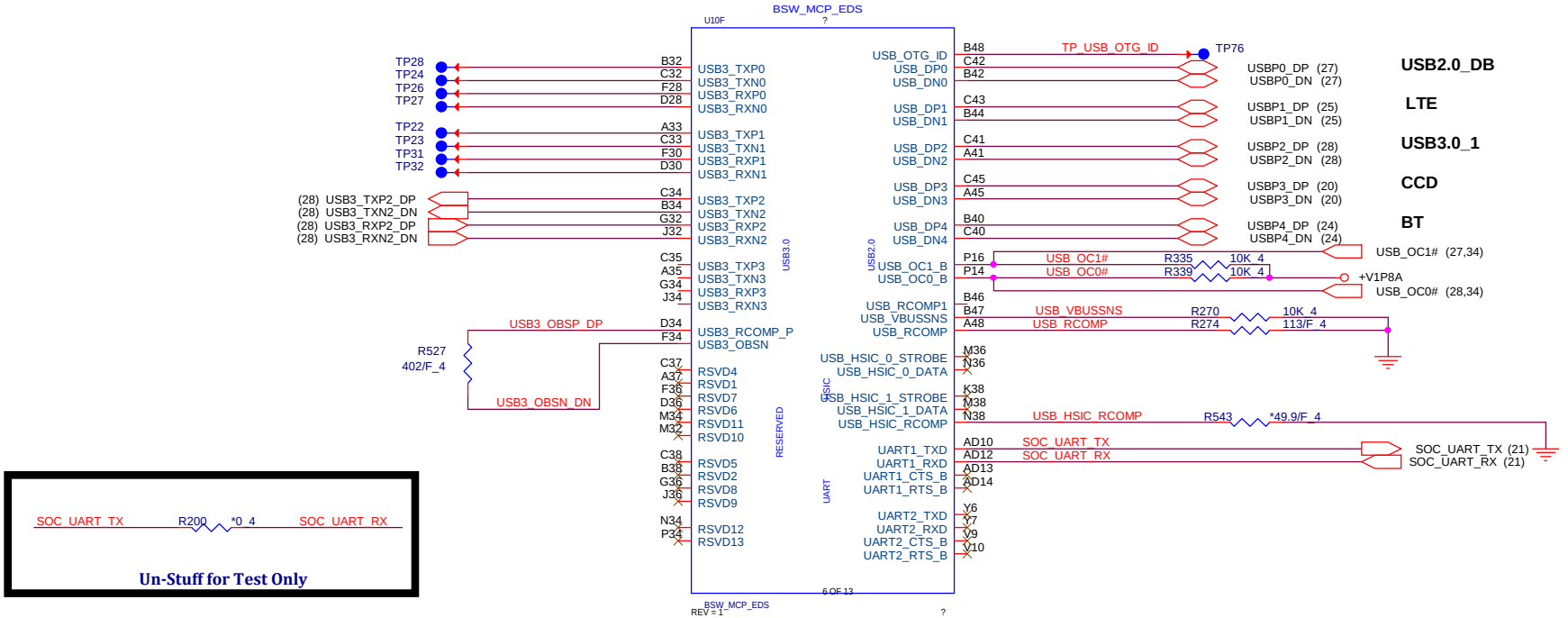
BRASWELL - USB INTERFACE

11

SoC (CPU)



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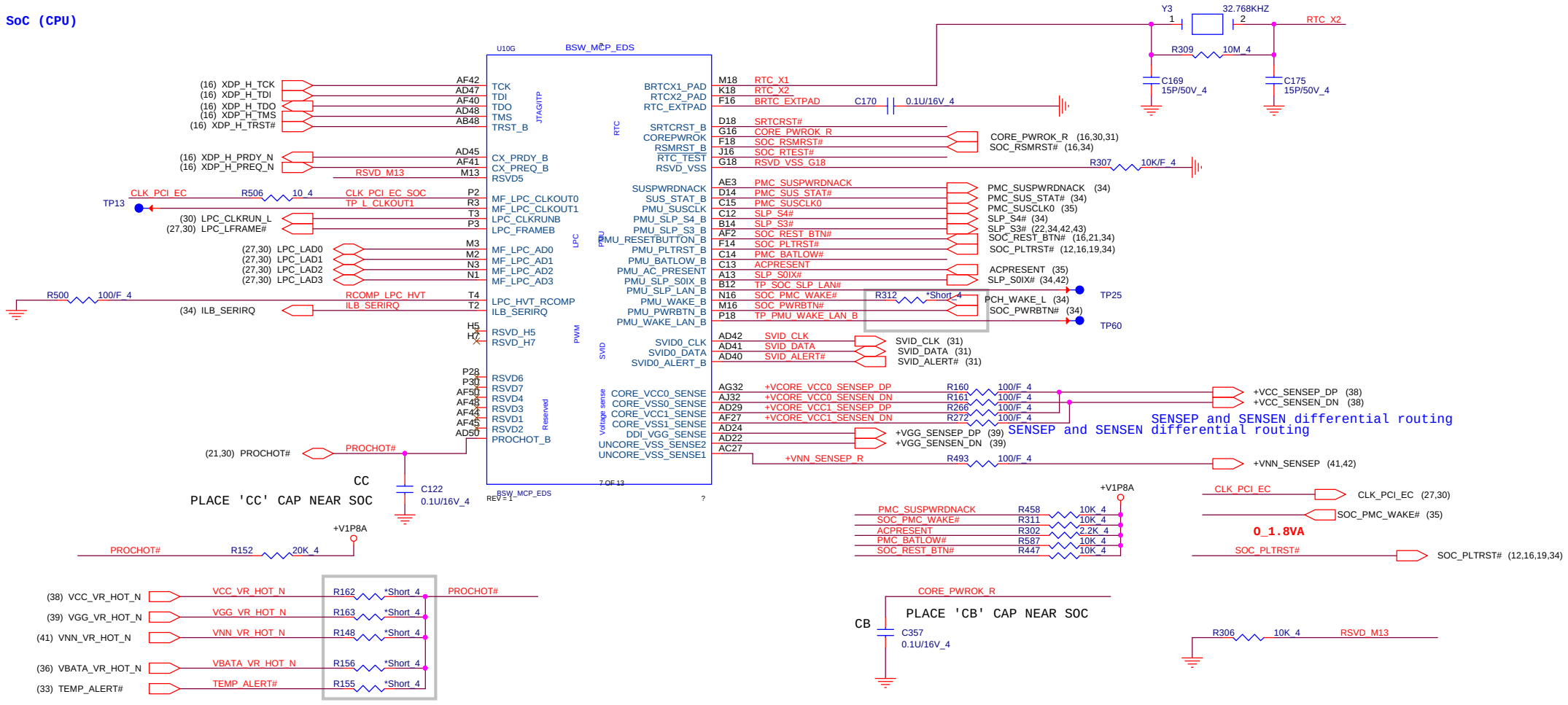
Size	Document Number	Rev
	BSW 6/10 (USB)	1A

Date: Monday, September 14, 2015 Sheet 11 of 47

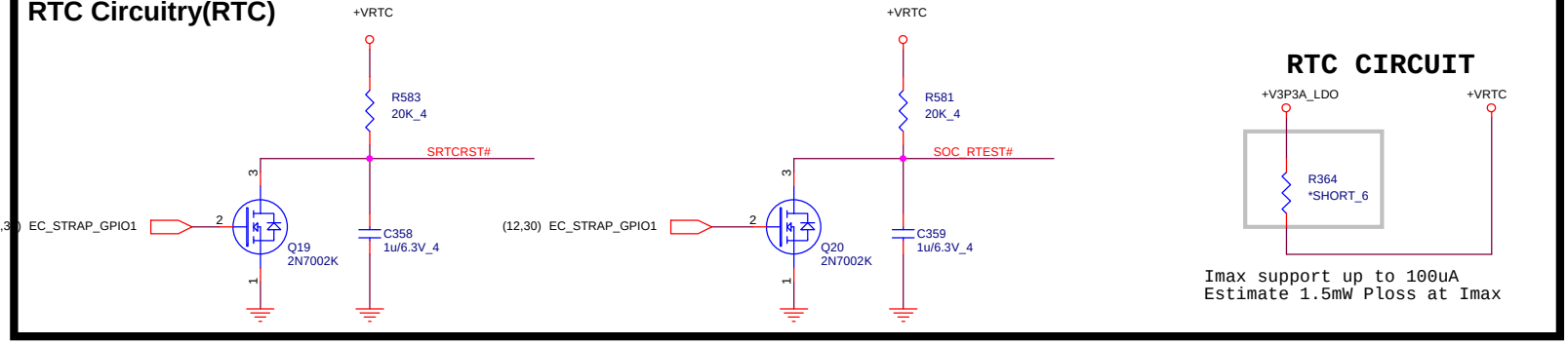
BRASWELL - JTAG, LPC, THERMAL, PMU

SoC (CPU)

RTC 32.768KHz X'tal



RTC Circuitry(RTC)



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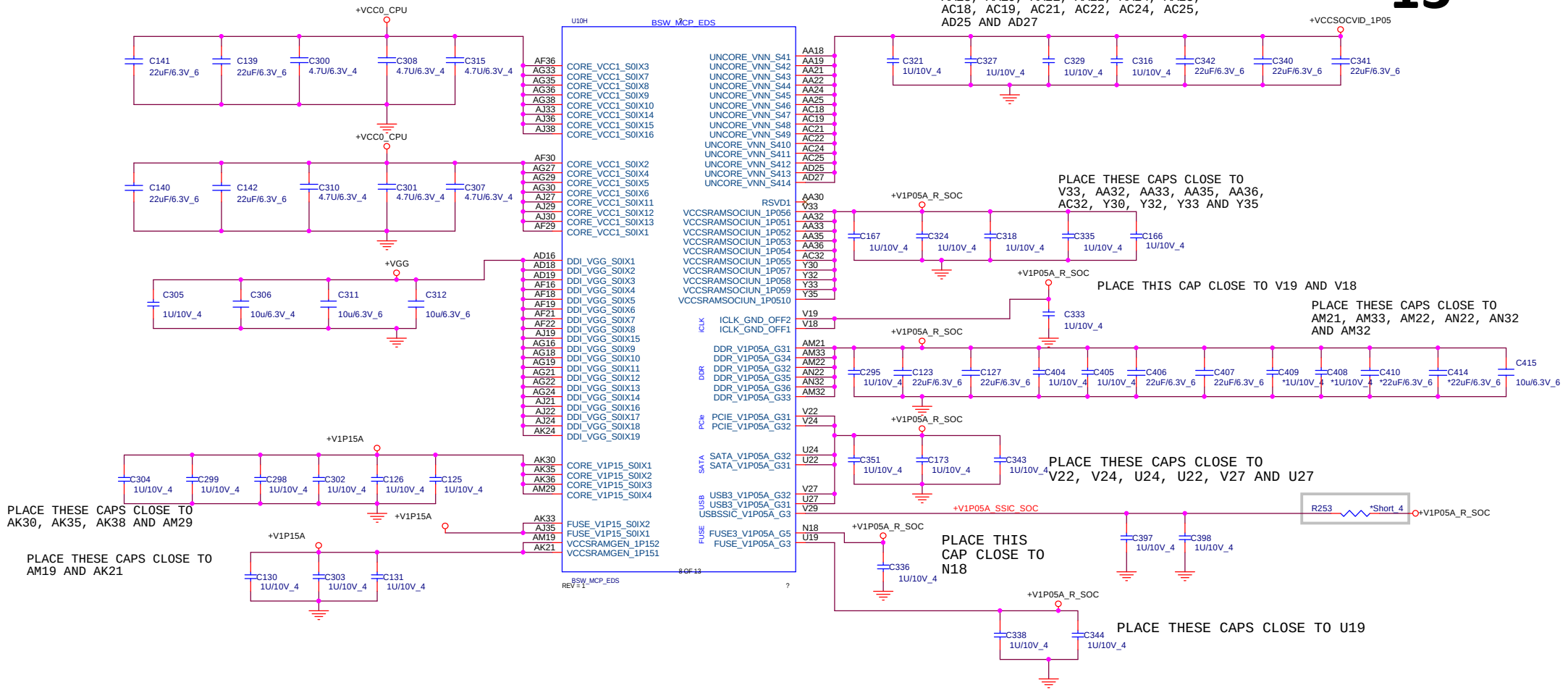
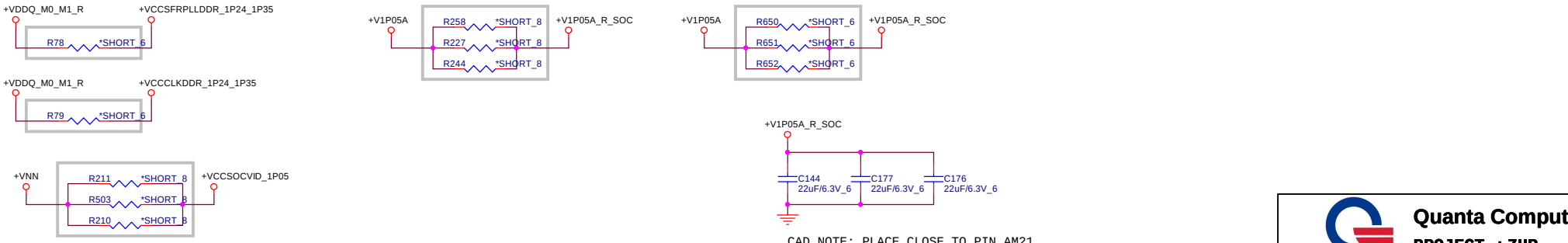
Size	Document Number	Rev
	BSW 7/10 (JTAG/LPC//PMU)	1A
Date: Monday, September 14, 2015	Sheet 12 of 47	

BRASWELL - POWER 1

SoC (CPU)

13





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PROJECT : ZHR

Size	Document Number	Rev
	BSW 8/10 (Power 1)	1A
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SoC (CPU)

BRASWELL - POWER 2

14

PLACE THESE CAPS CLOSE TO AM25

PLACE THESE CAPS CLOSE TO AN27

PLACE THESE CAPS CLOSE TO V36 & Y36

PLACE THESE CAPS CLOSE TO Y27 & Y25

PLACE THESE CAPS CLOSE TO P38, V30 & AC30

PLACE THESE CAPS CLOSE TO AF35, AD35, AD38 & AC36

PLACE THESE CAPS CLOSE TO THE DDR_VDDQ_G_ PINS

PLACE THESE CAPS CLOSE TO E1 AND E2

PLACE THESE CAPS CLOSE TO G1

PLACE THESE CAPS CLOSE TO AH4 AND AF4

PLACE THESE CAPS CLOSE TO Y18

PLACE THESE CAPS CLOSE TO AD33, AK18, AF33 AND AK19

PLACE THESE CAPS CLOSE TO THEIR PINS

U10I BSW_MCP_EDS

BSW_MCP_EDS REV = 1

9 OF 13

PLACE CAPS NEAR SOC

PLACE THIS CAP CLOSE TO U16

PLACE THIS CAP CLOSE TO G10 & H10

SD3 IO SUPPLY

LPC IO SUPPLY

AUDIO IO SUPPLY

Quanta Computer Inc. PROJECT : ZHR			
Size	Document Number: BSW 9/10 (Power 2)		Rev: 1A
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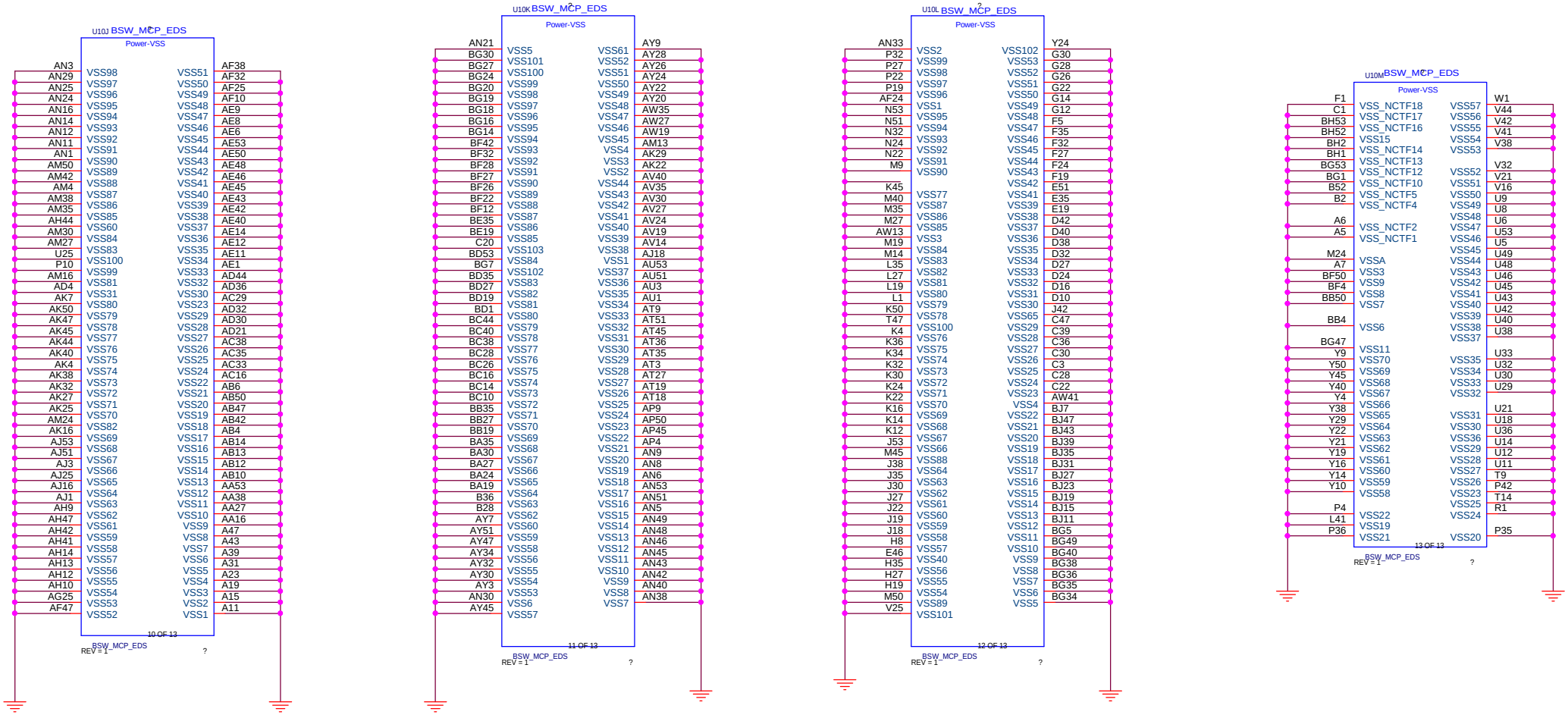
SoC (CPU)

BRASWELL - GND

15



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PROJECT : ZHR		
Size	Document Number: BSW 10/10 (GND)	Rev: 1A
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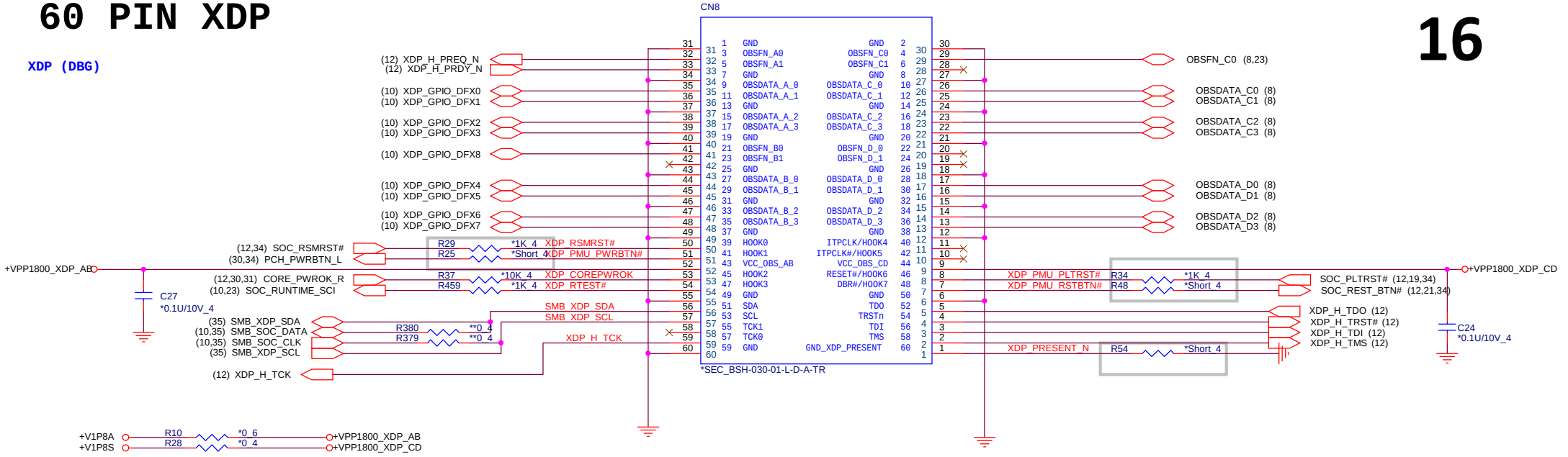
60 PIN XDP

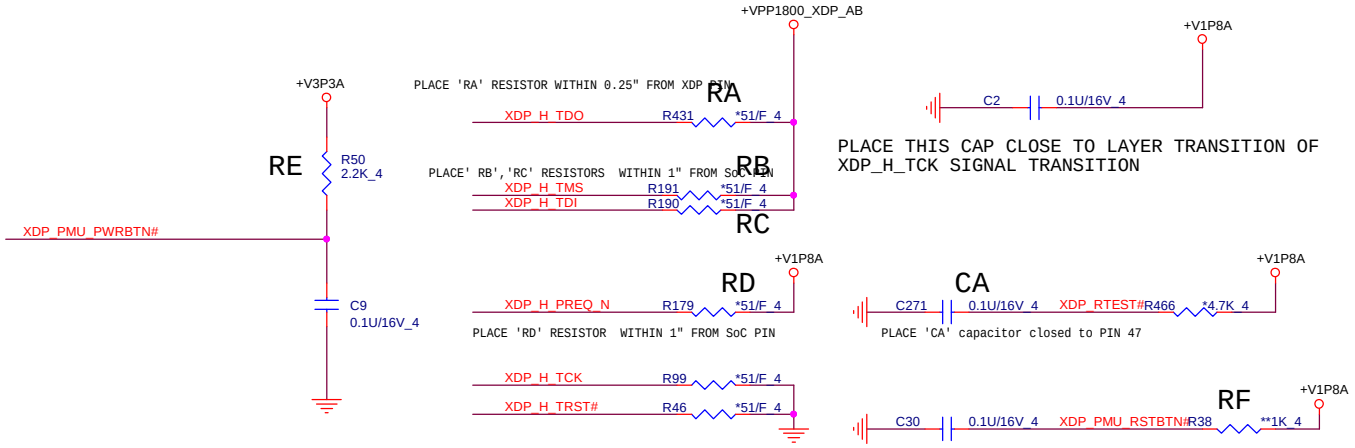
XDP (DBG)

16



0818 unstuffed related RC components of ITP header

PULL-UPS AND DOWNS FOR XDP SIGNALS



APS

Quanta Computer Inc.

PROJECT : ZHR

Size	Document Number	Rev
	XDP	1A

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On board memory(OBM)

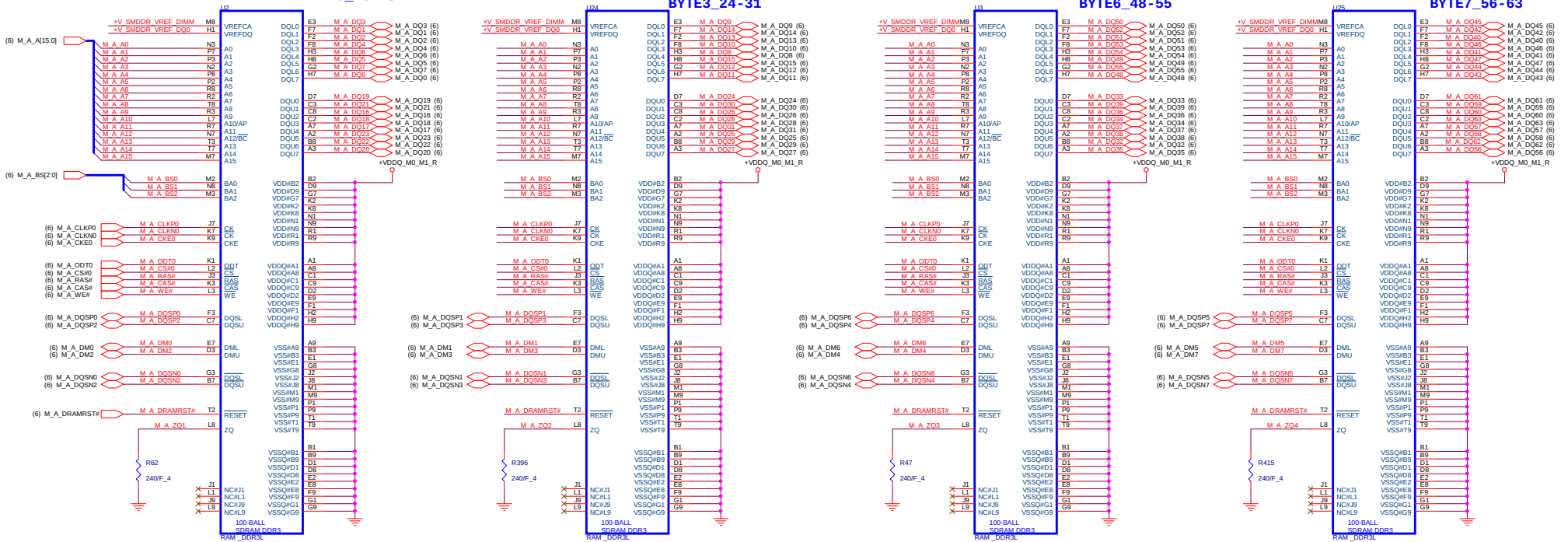
DDR3L MEMORY CHANNEL A

BYTE3_0-7
BYTE0_16-23

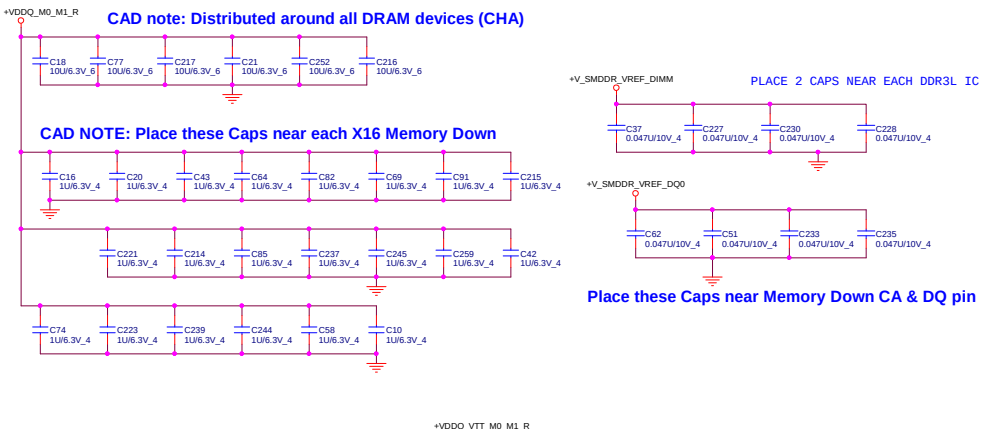
BYTE0_8-15
BYTE3_24-31

BYTE4_32-39
BYTE6_48-55

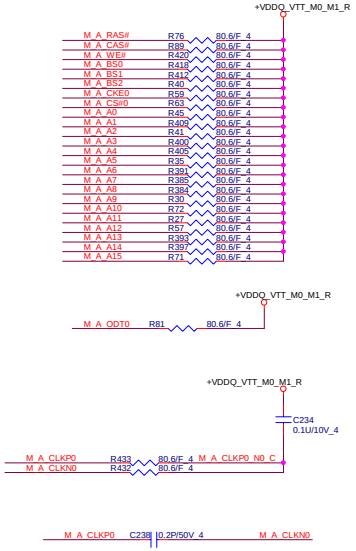
BYTE5_40-47
BYTE7_56-63



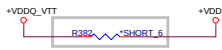
DE-CAPS FOR MEMORY CHANNEL A



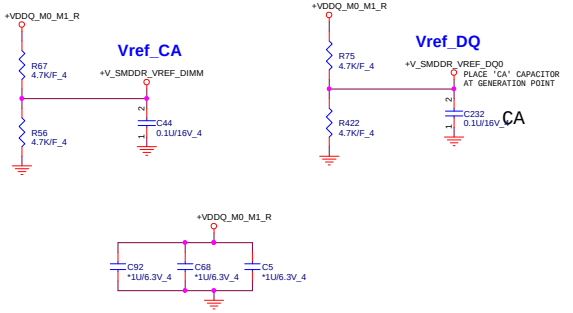
VTT TERMINATIONS



VOLTAGE MERGE



VREF_CA AND DQ CIRCUITS



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PROJECT : ZHR

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 CHA	1A
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On board memory(OBM)

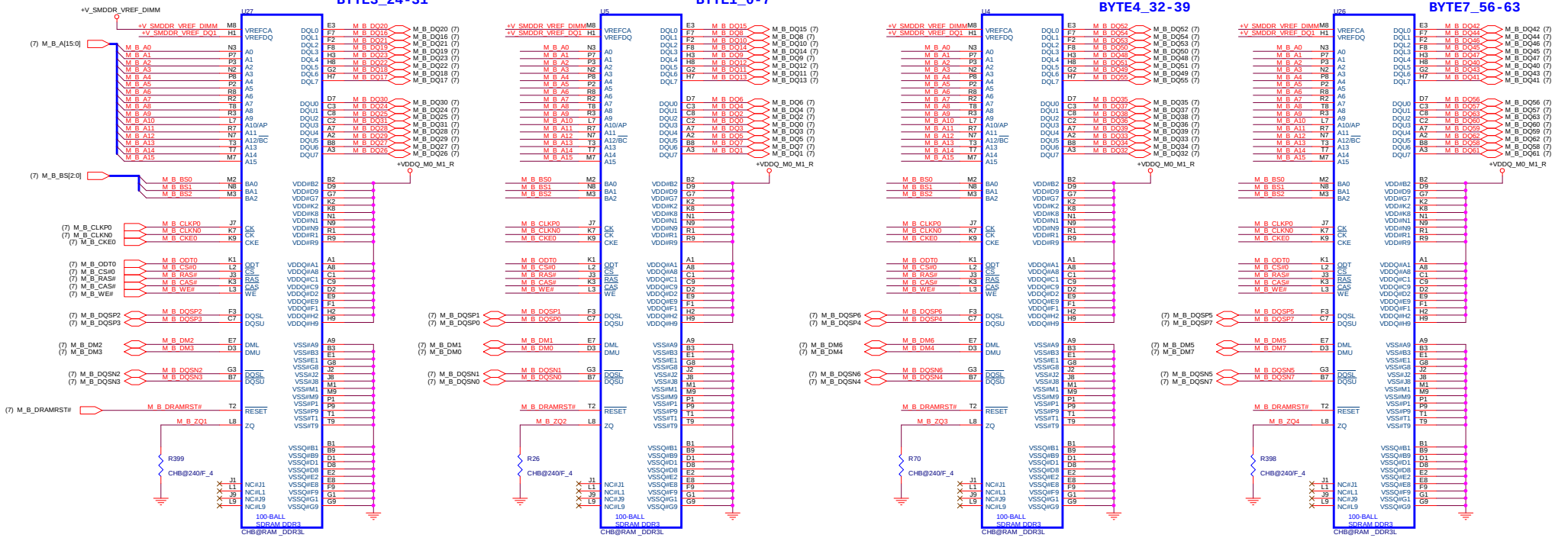
DDR3L MEMORY CHANNEL B

BYTE2_16-23
BYTE3_24-31

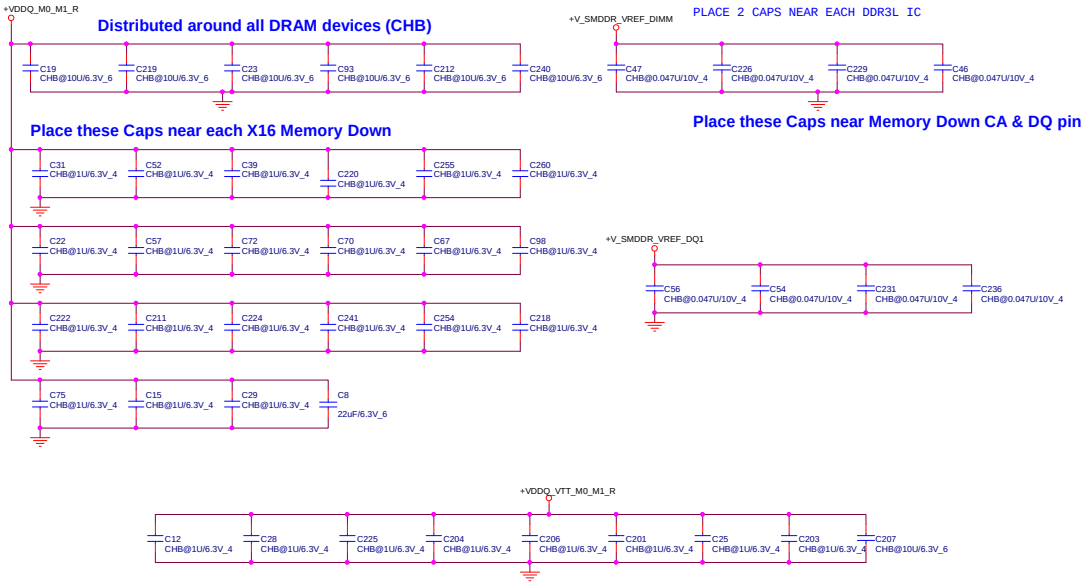
BYTE0_8-15
BYTE1_0-7

BYTE6_48-55
BYTE4_32-39

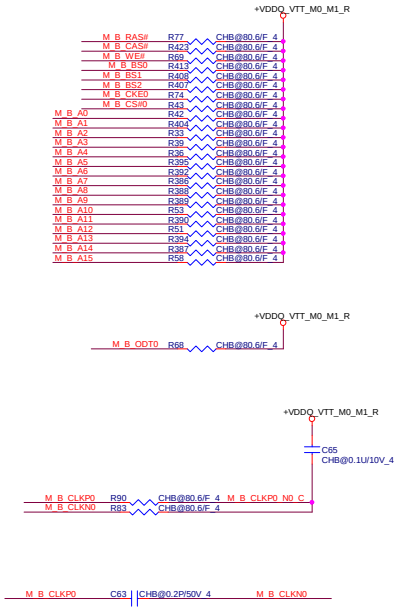
BYTE5_40-47
BYTE7_56-63



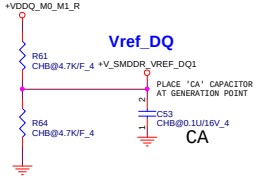
DE-CAPS FOR MEMORY CHANNEL B



VTT TERMINATIONS



VREF_DQ CIRCUIT



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PROJECT : ZHR

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 CHB	1A
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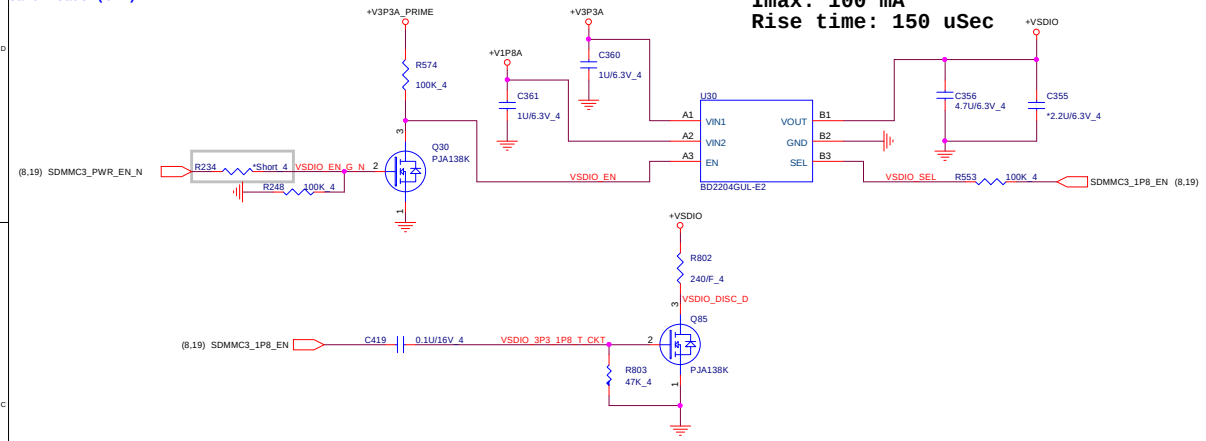
+VSDIO

SDMMC3_PWR_EN_N	SDMMC3_1P8_EN	VSDIO (V)
1	0	0V
1	1	0V
0	0	3.3V
0	1	1.8V

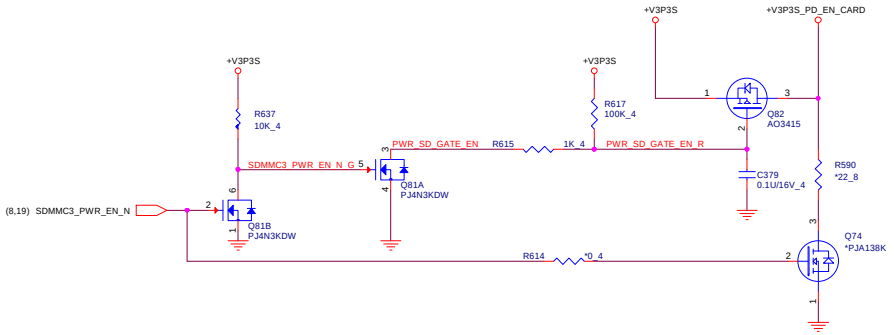
SD/MMC CARD READER CONNECTOR

Card Reader(CRD)



SD SLOT POWER SUPPLY

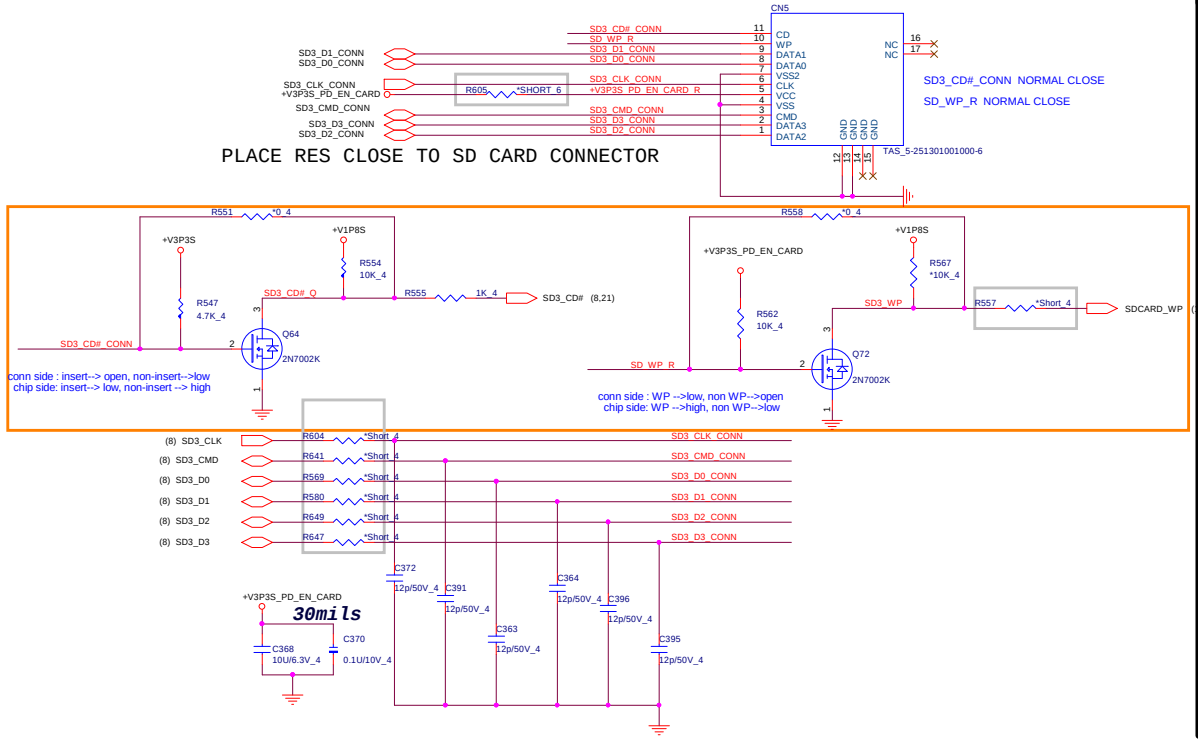
Card Reader(CRD)



SD SLOT/EMI

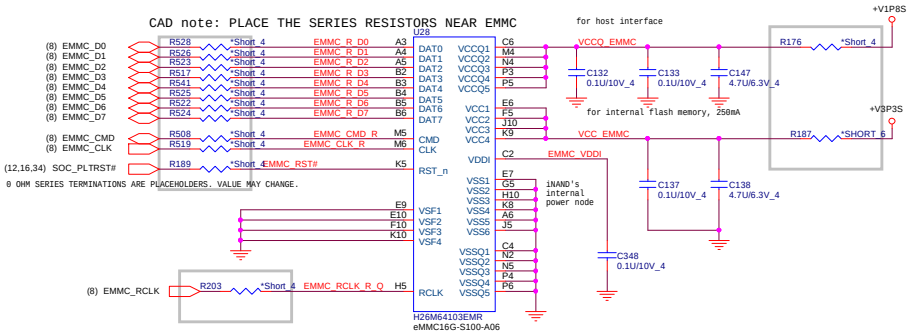
This is full size SD card (push-push type)

Card Reader(CRD)



eMMC (MMC)

eMMC



16G
Samsung-->KLMAG2WEMB-B031-AKE2RF-T505-- IC FLASH(153)KLMAG2WEMB-B031(FBGA)STNBSQ
Hynix--> H26M52103FMR (0x03)--AR0ZHQR1000--PROG IC FLASH(153P)H26M52103FMR STNBSQ

32G
Samsung-->KLMBG4WEBC-B031--AKE3SZ-T500--IC FLASH(153)KLMBG4WEBC-B031(FBGA)STNBSQ
Hynix--> H26M64103EMR (0x03)--AR0ZHQR1001--PROG IC FLASH(153P)H26M64103EMR STNBSQ

Quanta Computer Inc.
PROJECT : ZHR

Size	Document Number	Rev
	SDIO/eMMC	1A

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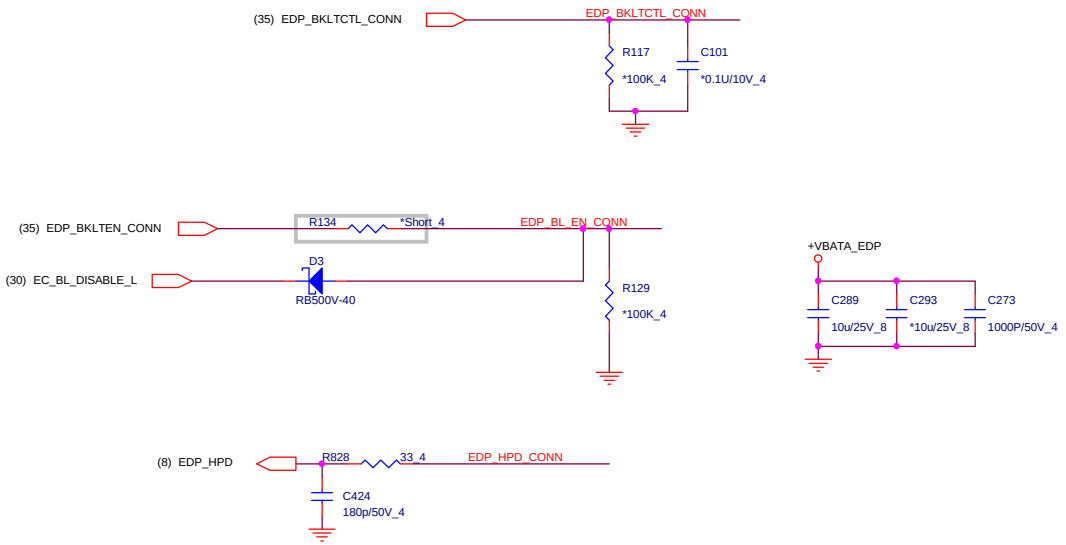
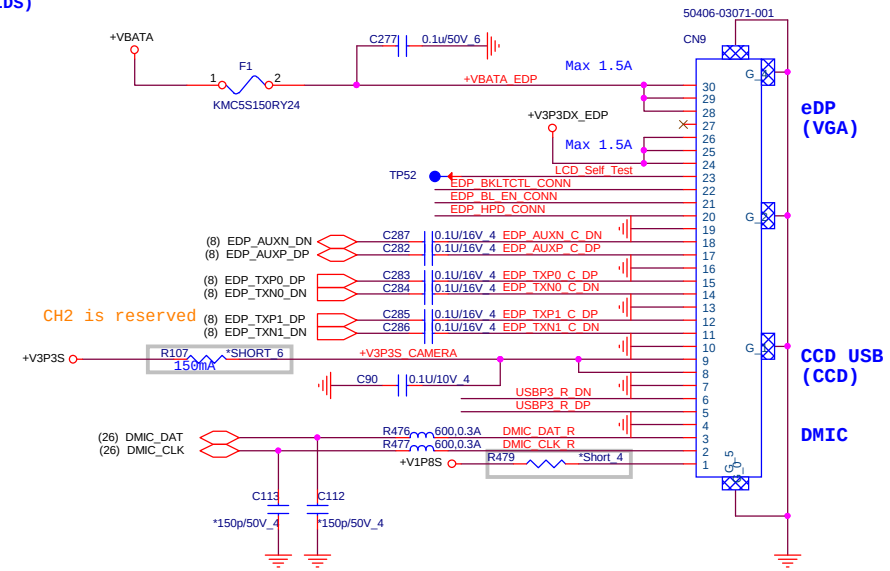
eDP PANEL CONTROL

LCD(LDS)



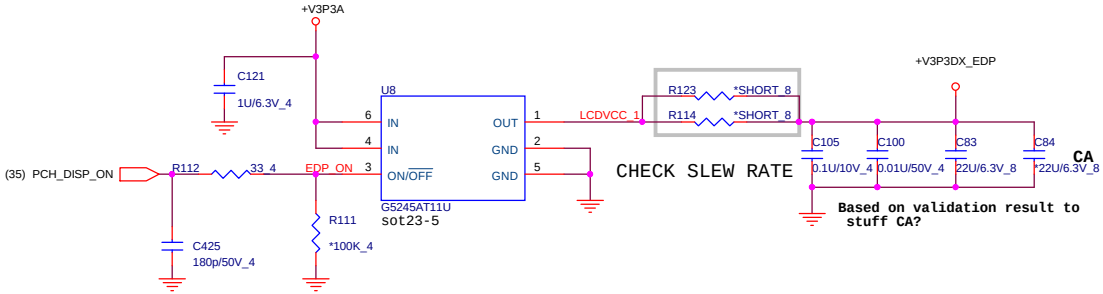
eDP CONNECTOR

LCD(LDS)



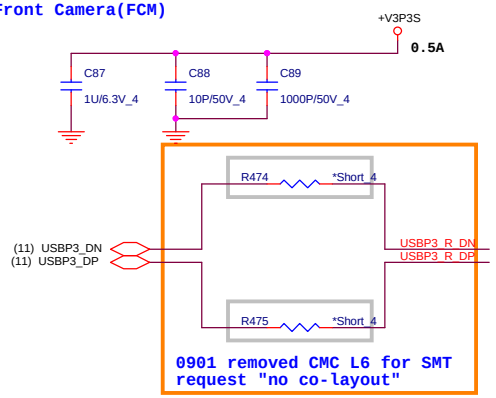
LCD(LDS)

eDP Power



CAMERA - POWER AND USB CMC

Front Camera(FCM)



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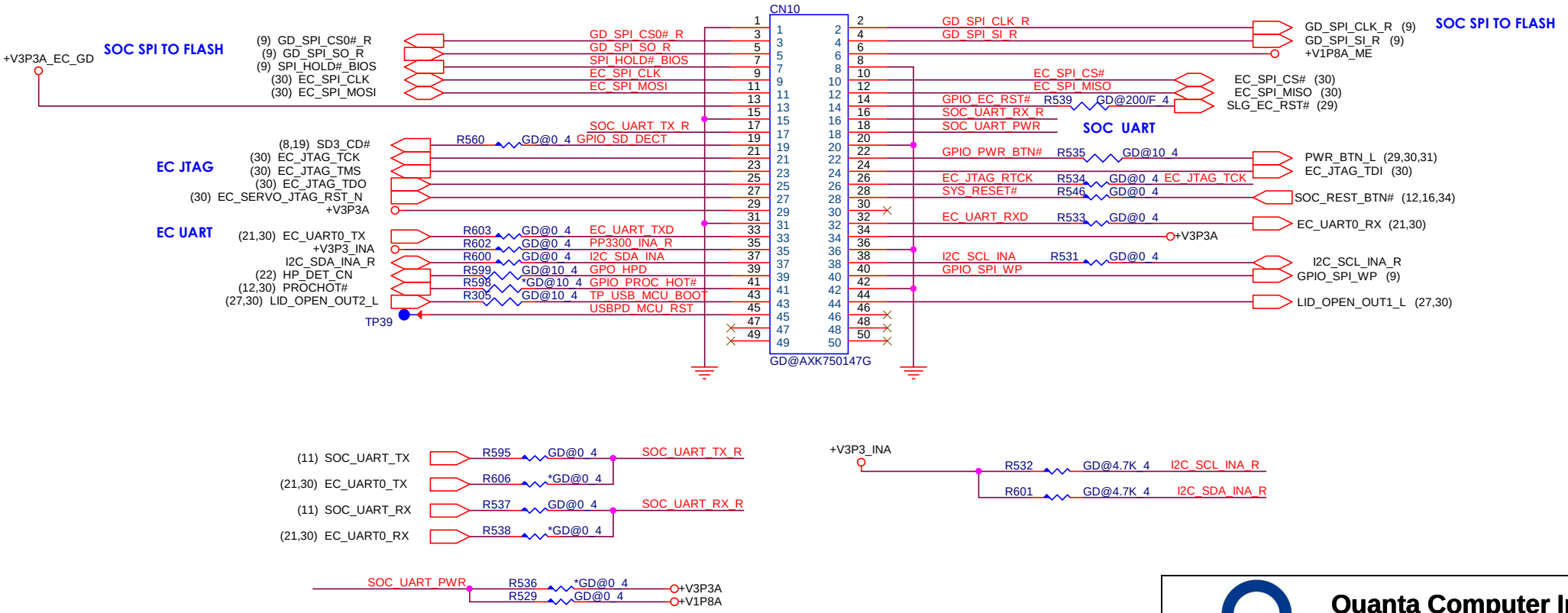
Size	Document Number	Rev
	eDP/CCD/DMIC/Touch-panel	1A
Date: Monday, September 14, 2015	Sheet 20 of 47	

Google debug(DBG)

GOOGLE DEBUG PORT

21

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD



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Size	Document Number	Rev
	Google Debug & FP header	1A
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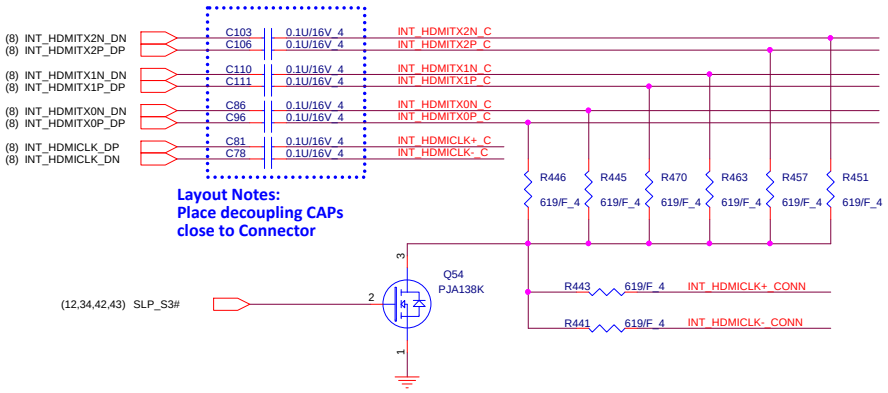
HDMI(HDM)

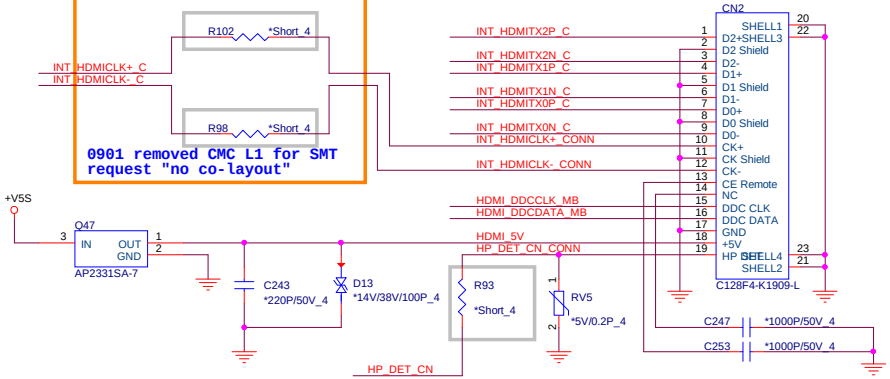
HDMI INTERFACE

22

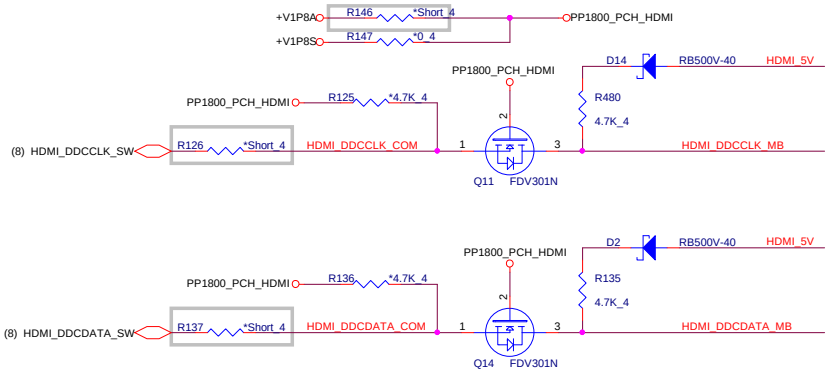
HDMI LEVEL SHIFTER



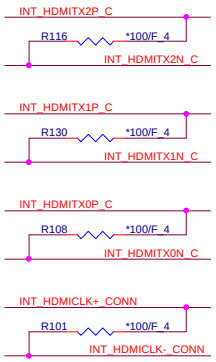
HDMI CONNECTOR

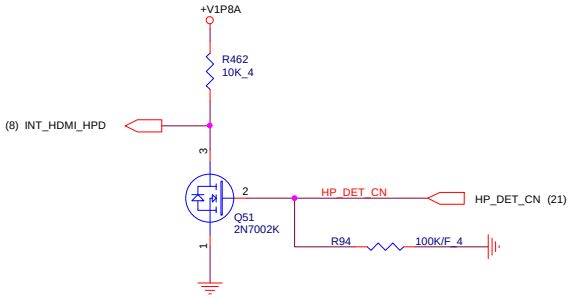


LEVEL TRANSLATOR/ EMI



EMI





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	HDMI	1A
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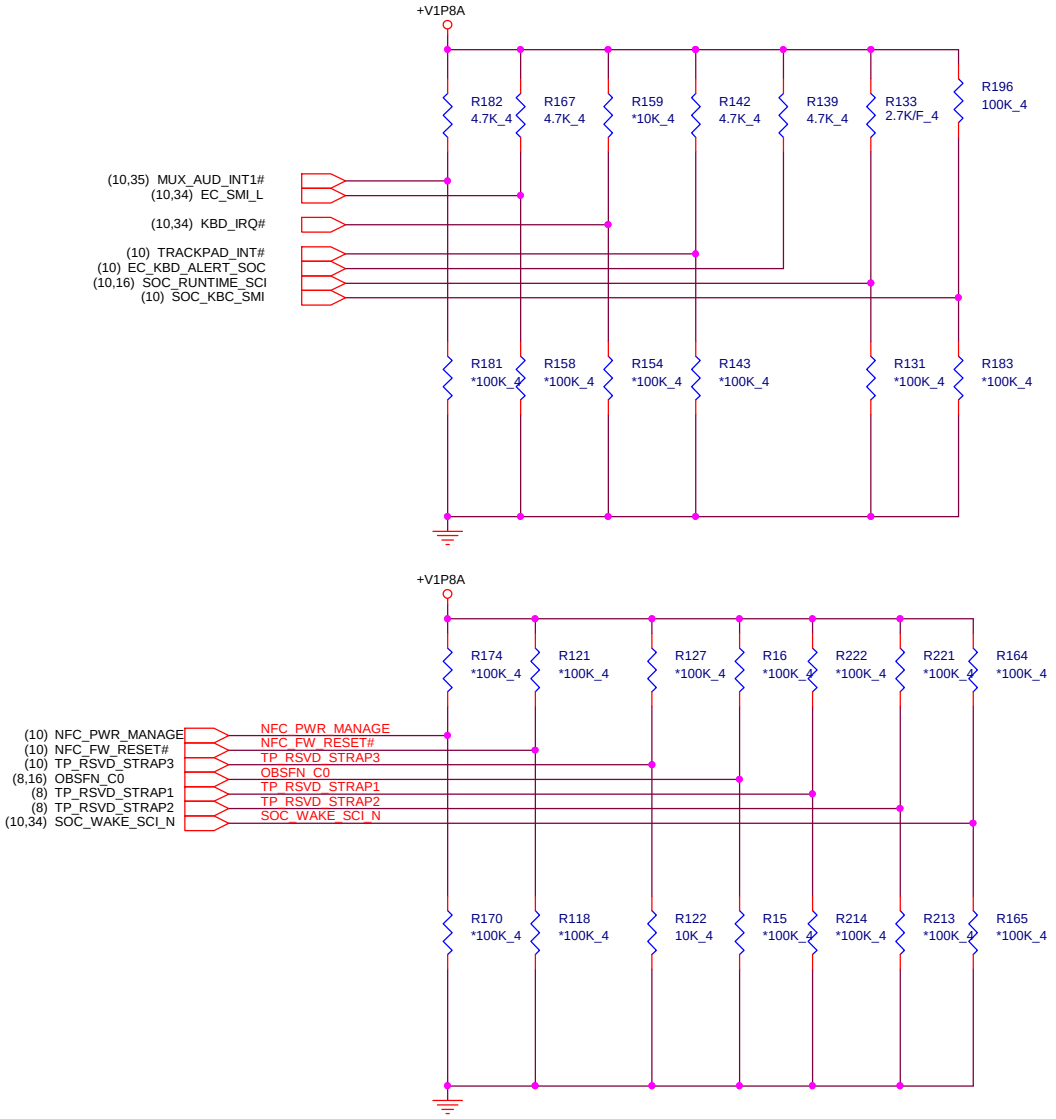
STRAPS SETTINGS

SoC (CPU)

BSW Strapping Table (based on EDS V1.0), sampled on the rising edge of PMU_RSMRST_N

Pin Name	Strap description	Configuration
GPIO_SUS0	DDI0 Detect	0 = DDI0 not detected **1 = DDI0 detected**
GPIO_SUS1	DDI1 Detect	0 = DDI1 not detected **1 = DDI1 detected**
GPIO_SUS2	Top Swap (A16 Override)	0 = change boot loader address **1 = Normal operation**
GPIO_SUS3	DSI Display Detect (Leave floating if GPIO functionality is not used, it is not POR)	**0 = DSI not detected** 1 = DSI detected
GPIO_SUS4	BIOS Boot Selection	0 = No SPI **1 = SPI**
GPIO_SUS5	Security Flash Descriptors	0 = Not support **1 = Normal operation**
GPIO_SUS6	Halt Boot strap	**1 = Normal operation** (MUST be high at RSMRST# de-asser to ensure proper platform operation and use of GPIO_DFX[8:0]
GPIO_SUS7	DFX SUS DEBUG strap	0 = SUSDUG **1 = No SUSDUG**
GPIO_SUS8	PLLs.ICLK.USB2,DDI ,SFR,supply select	**0 = Supply is 1.25V** 1 = Supply is 1.35V
GPIO_SUS9	ICLK.USB2,DDI,SFR Bypass	**0 = No Bypass(Default)** 1 = Bypass with 1.05V
GPIO_CAMERASB08	ICLK Xtal OSC Bypass	**0 = No Bypass(Default)** 1 = Bypass
GPIO_CAMERASB09	CCU SUS RO Bypass	**0 = No Bypass(Default)** 1 = Bypass
GPIO_CAMERASB11	RTC OSC Bypass	**0 = No Bypass(Default)** 1 = Bypass



Quanta Computer Inc.

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	STRAPS	1A
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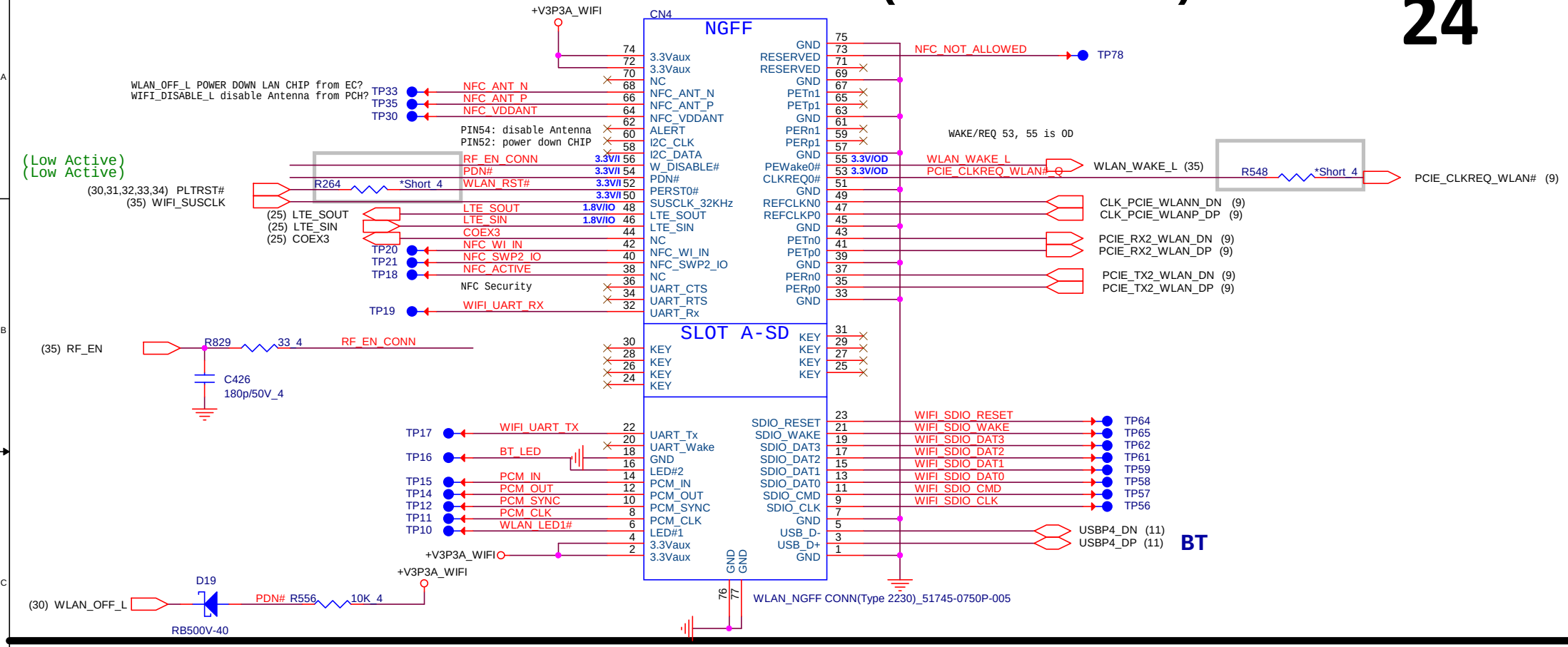
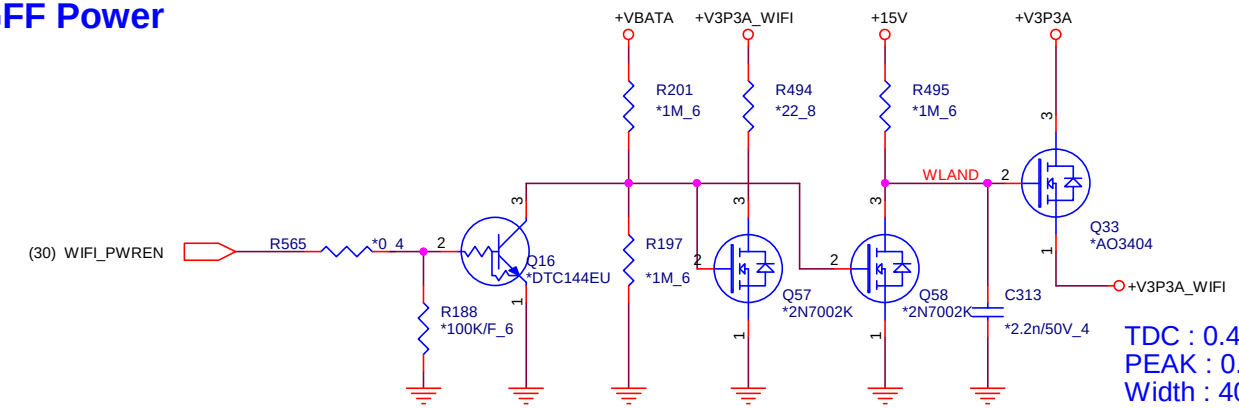
WIFI/BT COMBO NGFF E KEY(NGF)

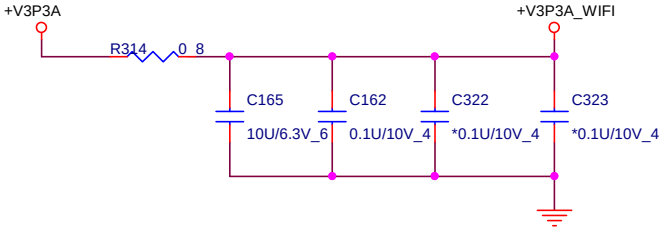
WIFI/BT COMBO (NGFF E KEY)

24



WL/BT NGFF Power





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	WIFI/BT(NGFF)	1A
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LTE

LTE NGFF Power(LTE)

Peak:2.75A
Normal:1.1A

+V3P3A
+3V_LTE
R486 *3G@SHORT_8
R490 *3G@SHORT_8

+VBATA +3V_LTE +15V +V3P3A
R207 *3G@1M_6
R172 *3G@22_8
R498 *3G@1M_6
LTED
Q15 *3G@MDV1528Q
(30) LTE_PWREN
Q18 *3G@DTC144EU
R185 *100K/F_6
R199 *3G@1M_6
Q17 *3G@2N7002K
Q59 *3G@2N7002K
C332 *3G@2.2n/50V_4
+3V_LTE

TDC : 1.875A
PEAK : 2.5A
Width : 80mil

MultiMedia SIM (LTE)

25

SIM_DET D1 *3G@5V/0.2P_4
UIM_RST RV3 *3G@EGA-0402
UIM_VPP RV4 *3G@EGA-0402
UIM_CLK RV2 *3G@EGA-0402
UIM_DATA RV1 *3G@EGA-0402
H=0.9mm

SIM_DET C38 *3G@470P/50V_4
UIM_PWR C32 *3G@27P/50V_4
UIM_DATA C40 *3G@10P/50V_4
UIM_CLK C33 *3G@10P/50V_4
UIM_RST C34 *3G@27P/50V_4
UIM_VPP C49 *3G@0.1U/10V_4
UIM_VPP C50 *3G@33P/50V_4

UIM_VPP_C R66 *3G@0_4 UIM_VPP
UIM_PWR
C35 *3G@1U/6.3V_4
C41 *3G@0.1U/16V_4
Max: 7.5mA (Option)
R44 *3G@10K_4
JSIM1
UIM_VPP_C
UIM_DATA
SIM_DET
(35) SIM_DET
VPP
I/O Serial date I/O
Reserved
CD
VCC
RST
CLK
Reserved
GND
UIM_PWR
UIM_RST
UIM_CLK
*3G@SIM-CONN

<Layout Notes> Keep USIM signals max length within 8000mils.

LTE NGFF (LTE)

0901 removed CMC L5 for SMT request "no co-layout"

R414 *3G@0_4 LTE_CFG3
R421 *3G@0_4
R425 *3G@0_4
(11) USBP1_DP
(11) USBP1_DN
USBP1+_R
USBP1-_R

CN1
NGFF
CONFIG_3 GND GND USB_D+ USB_D- GND
3.3Vaux 3.3Vaux Power_On_Off W_DISABLE# LED#
KEY B
PLATFORM PIN OUT
CONFIG_0 Wake_On_WWAN# BODYSAR_N GND NC NC GND NC NC GND NC NC GND NC NC GND ANTCTL0 ANTCTL1 ANTCTL2 ANTCTL3 Reset# CONFIG_1 GND GND CONFIG_2
RESERVED RESERVED RESERVED RESERVED UIM-RESET UIM-CLK UIM-DATA UIM-PWR NC RESERVED RESERVED RESERVED RESERVED NC NC NC NC NC NC RESERVED UART_RX UART_TX SIM_DET NC 3.3Vaux 3.3Vaux 3.3Vaux
GND GND
*3G@BWE_80149-1721

+3V_LTE
C124 *3G@1U/6.3V_4
C291 *3G@10P/50V_4
C292 *3G@0.47U/6.3V_4
C115 *3G@10U/6.3V_6
C128 *3G@0.1U/10V_4
C45 *3G@0.1U/10V_4
C36 *3G@22U/6.3V_8
1.8V/I LTE_POWER_ON_OFF
3.3V/I LTE_DISABLE_L_R
LTE_LED#
TP1
R65 *3G@0_4 LTE_DISABLE_L (35)

NC at A stage, LTE card HW not implement yet
TP49 LTE_CFG0
(35) LTE_WAKE_L
R428 *3G@Short_4 LTE_WAKE_L_R
TP50 LTE_BODYSAR#
1.8V/O

GPS_DISABLE# TP2
UIM_VPP
UIM_RST
UIM_CLK
UIM_DATA
UIM_PWR
UART_MDM_RX TP3
MDM_WAKE_AP TP4
AP_WAKE_MDM TP5

TP51 UART_MDM_CTS

+3V_LTE
R484 *3G@100K/F_4
PLTRST#_3G
TP53 LTE_CFG1
1.8V/I
R468 *3G@124K/F_4
C274 *3G@33P/50V_4
TP54

+3V_LTE
R55 *3G@100K/F_4
LTE_POWER_ON_OFF
R60 *3G@124K/F_4

COEX3_R R453 *3G@0_4
UART_RX R110 *3G@0_4 LTE_SIN
UART_TX R120 *3G@0_4 LTE_SOUT
COEX3 (24)
LTE_SIN (24)
LTE_SOUT (24)
1.8V/IO
1.8V/IO
1.8V/I
3.3V/I
SIM_DET
SUSCLK R132 *3G@Short_4 LTE_SUSCLK
LTE_SUSCLK (35)

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	LTE(NGFF)	1A
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Codec (ADO)

26

+V1P8S

BOM Change to 0_4 due to material shortage

+5VA

L4 *Short_4 PP1800_CODEC_AVDD

R597 *SHORT_6 PP1800_CODEC_DVDDIO

C377 0.1U/10V_4 C185 1U/16V_4 C180 1U/16V_4

C387 1U/16V_4 C179 0.1U/10V_4 C191 10U/6.3V_4

Close to PIN26 Close to PIN38

C183 1U/16V_4 C190 0.1U/10V_4 C184 10U/6.3V_4

U31

MAX98090AETL+T

DVDDIO 28 DVDD 27 AVDD 26 HPVDD 38 SPKLVDD 14 SPKRVDD 13

(10) I2S_MCLK_R R629 *Short_4 CODEC_CLK_IN 35 MCLK

(9) I2S_BCLK_R 33 BCLK

(9) I2S_LRCLK_R 32 LRCLK

(9) I2S_DOUT_R 30 SDIN

(9) I2S_DIN_R 31 SDOUT

(35) I2C_1_SDA_AUDIO 37 SDA

(35) I2C_1_SCL_AUDIO 36 SCL

(9) AUDIO_CODEC_IRQ R622 *Short_4 CODEC_INT_OD_L 34 IRQ_L OD

(20) DMIC_DAT DMIC_DAT R619 *Short_4 DMIC_DAT_L 19 IN1/DMD

(20) DMIC_CLK DMIC_CLK R624 *Short_4 DMIC_CLK_L 18 IN2/DMC

20 IN3

21 IN4

(27) RCVP RCVP C373 1U/10V_4 CODEC_MIC_L_P

(27) RCVN RCVN C374 1U/10V_4 CODEC_MIC_L_N

CODEC_C1P 39 C1P

C389 1U/16V_4

CODEC_C1N 40 C1N

C392 1U/10V_4 3 CPVDD

C393 1U/10V_4 2 CPVSS

SPKLP 16 L_SPK+

SPKLN 15 L_SPK-

SPKRP 12 R_SPK+

SPKRN 11 R_SPK-

MICBIAS 22 MICBIAS_1 R320 *Short_4 MICBIAS

C178 1U/10V_4

R319 2.2K_4

RCVP/LOUTL 8

RCVN/LOUTR 9

HPSNS 5 RCVN

JACKSNS 7 MIC_DET R642 *0_4 RCVP

HPL 4 HPOUT-L R644 5.6_4 HPL HPL (27)

HPR 6 HPOUT-R R643 5.6_4 HPR HPR (27)

REF 23

BIAS 24

C376 1U/10V_4 C375 2.2U/6.3V_4 R373 *4.7K_4 R374 *4.7K_4

TGND 41 DGND 29 AGND 25 HPGND 1 SPKRGND 10 SPKLGND 17

R674 *Short_4

R645 *Short_4

Codec PWR 5V (ADO)

+V5S DIGITAL ANALOG AVDD1 +5VA

L8 HCB1005KF_1.5A_4

C386 *0.1U/10V_4 C388 *10U/6.3V_6 C188 0.1U/10V_4 C186 10U/6.3V_4

Internal Speaker (ADO)

L_SPK+ R367 *SHORT_6 L_SPK+_1

L_SPK- R366 *SHORT_6 L_SPK-_1

R_SPK- R368 *SHORT_6 R_SPK-_1

R_SPK+ R369 *SHORT_6 R_SPK+_1

CN14 SPK_CONN_4P

C194 10P/50V_4 C198 10P/50V_4 C195 10P/50V_4 C196 10P/50V_4

40mil for each signal

Quanta Computer Inc.

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	Audio Codec/SPK	1A

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TPM

TPM/DAUGHTER BOARD CONNECTOR

TPM(TPM)

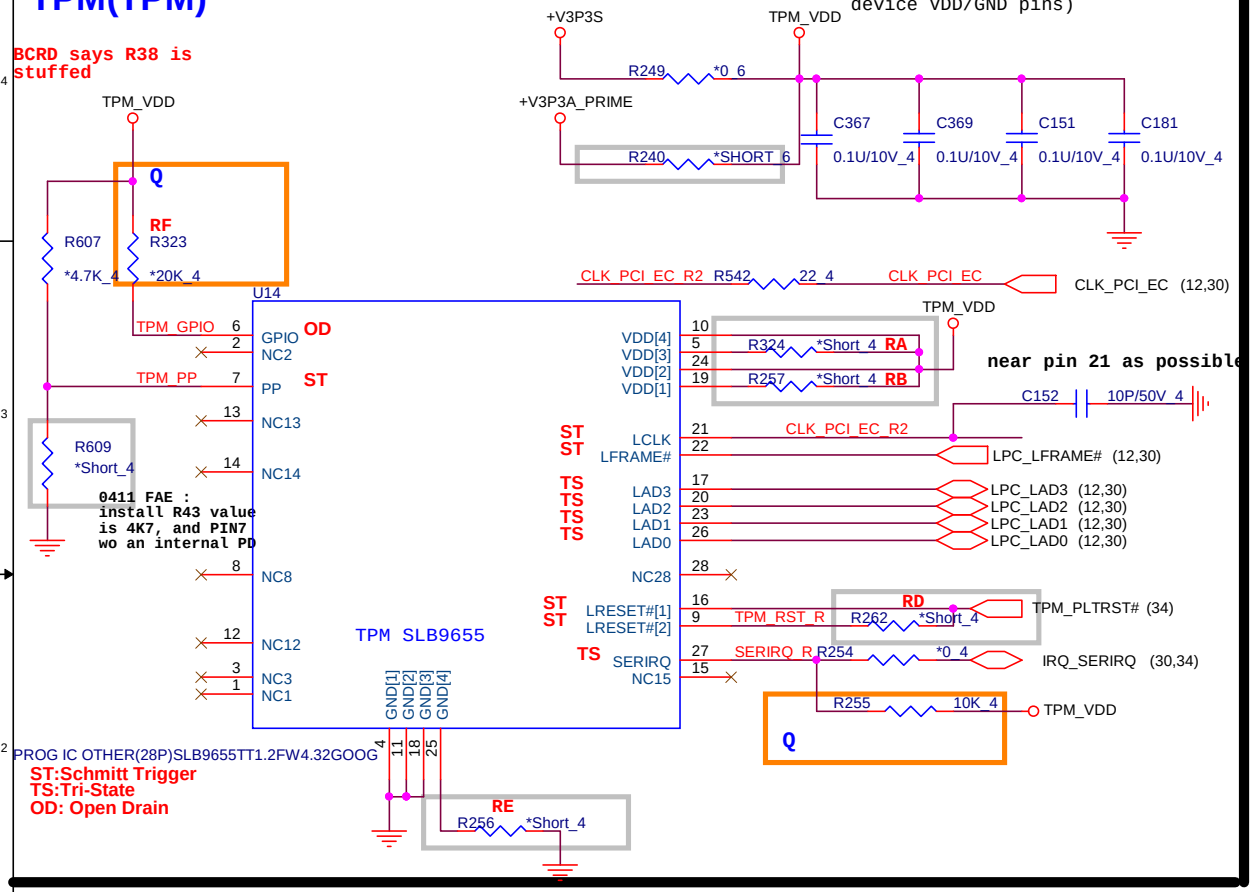
DB(UIF)

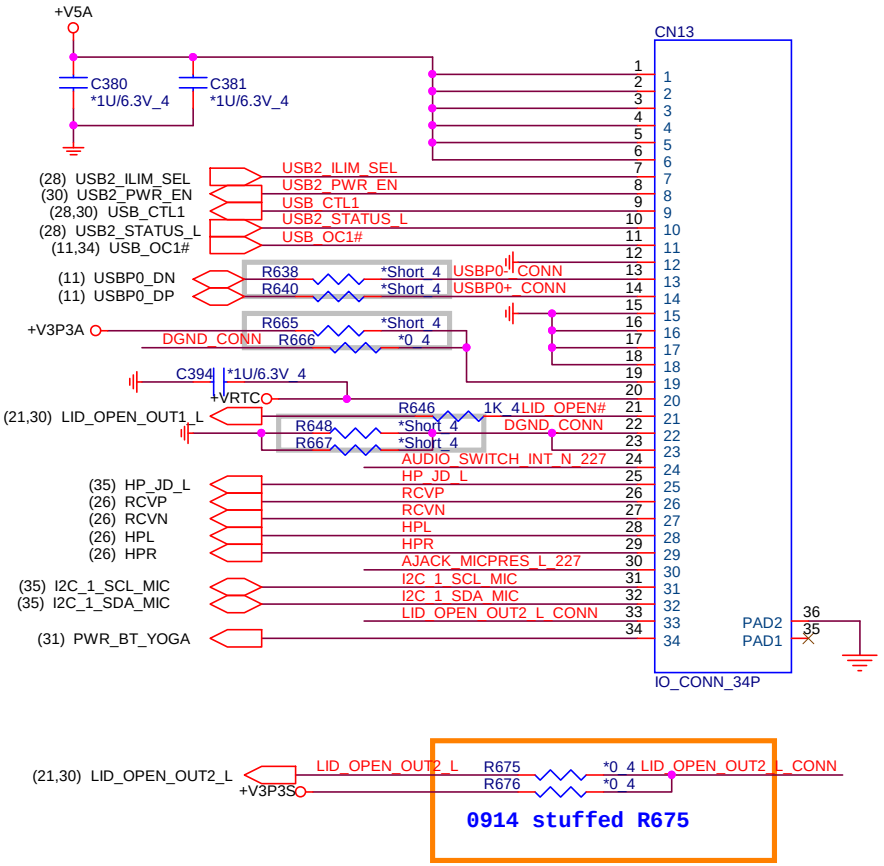
DB CONNECTOR

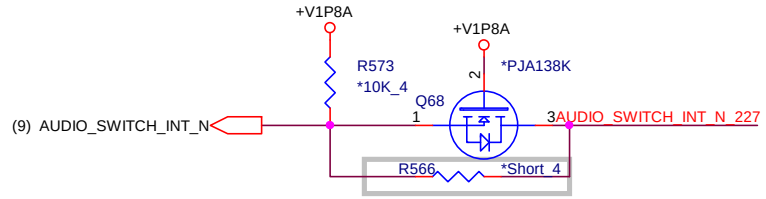
27

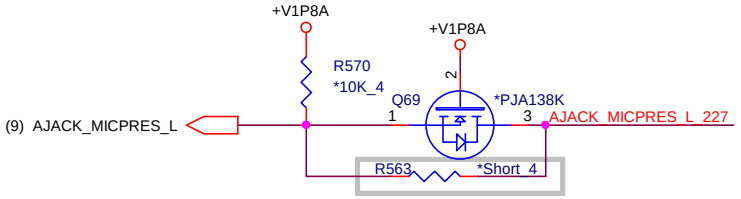
BCRD says R38 is stuffed

4 x100nF (place close to device VDD/GND pins)









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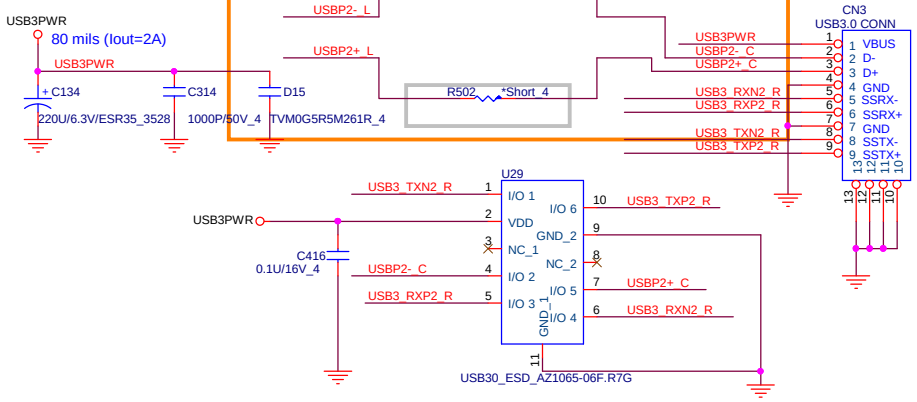
USB3 CONN

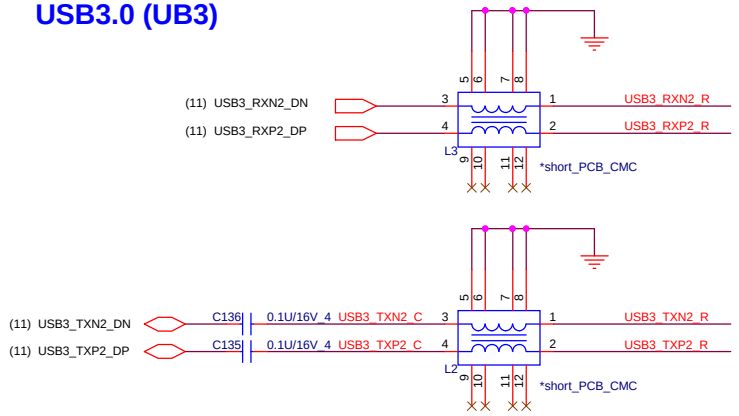
USB3.0 (UB3)

0901 removed CMC L7 for SMT request "no co-layout"



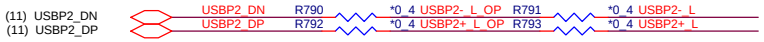
USB3.0 /HOLE

USB3.0 (UB3)

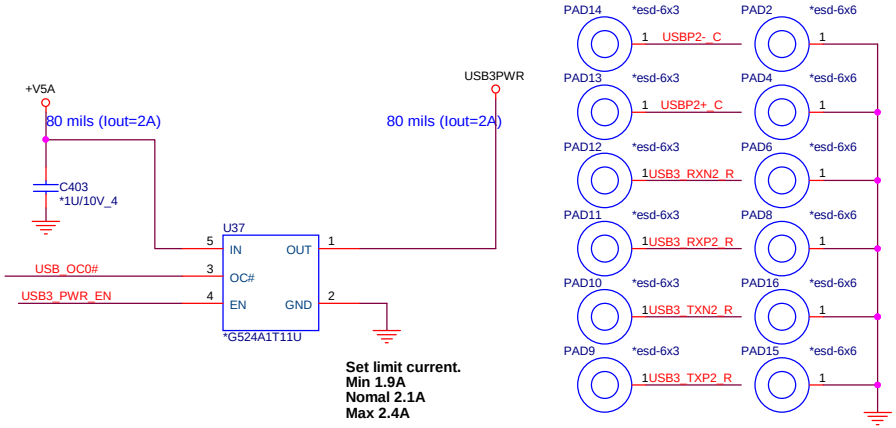


28

USB Colay BOM option

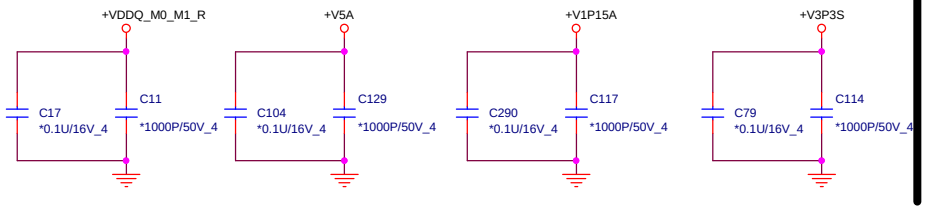


USB PWR(non-Charger)

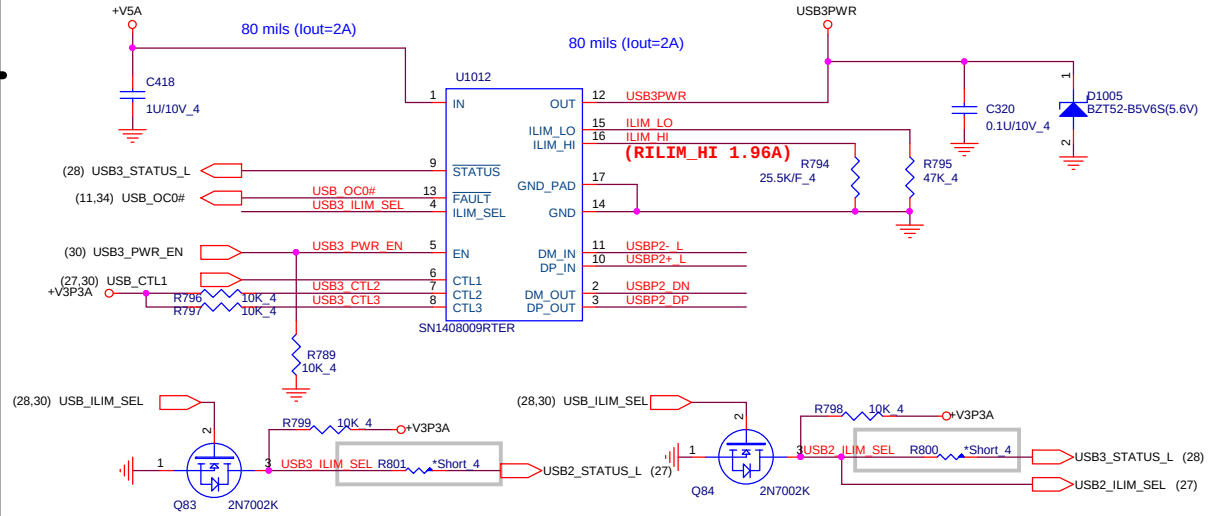


Set limit current.
Min 1.9A
Nomal 2.1A
Max 2.4A

EMI caps

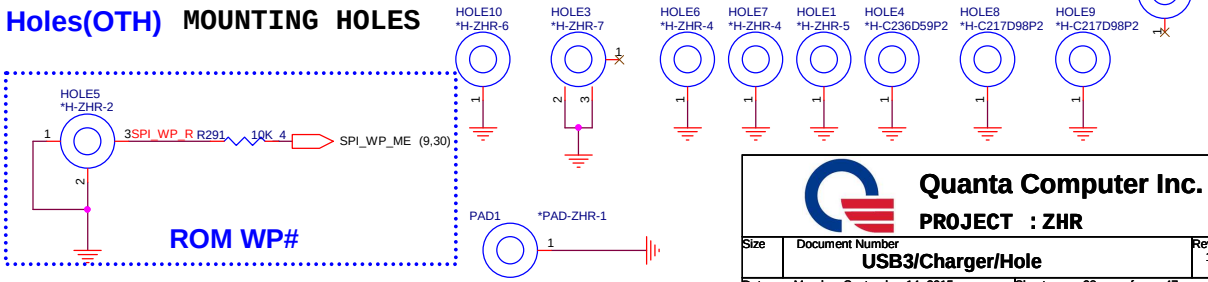


USB3.0 (UB3) USB PWR (Charger)



0910 changed Hole2/Hole3 Footprints
0911 changed Hole2 Footprints

Holes(OTH) MOUNTING HOLES



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	USB3/Charger/Hole	1A
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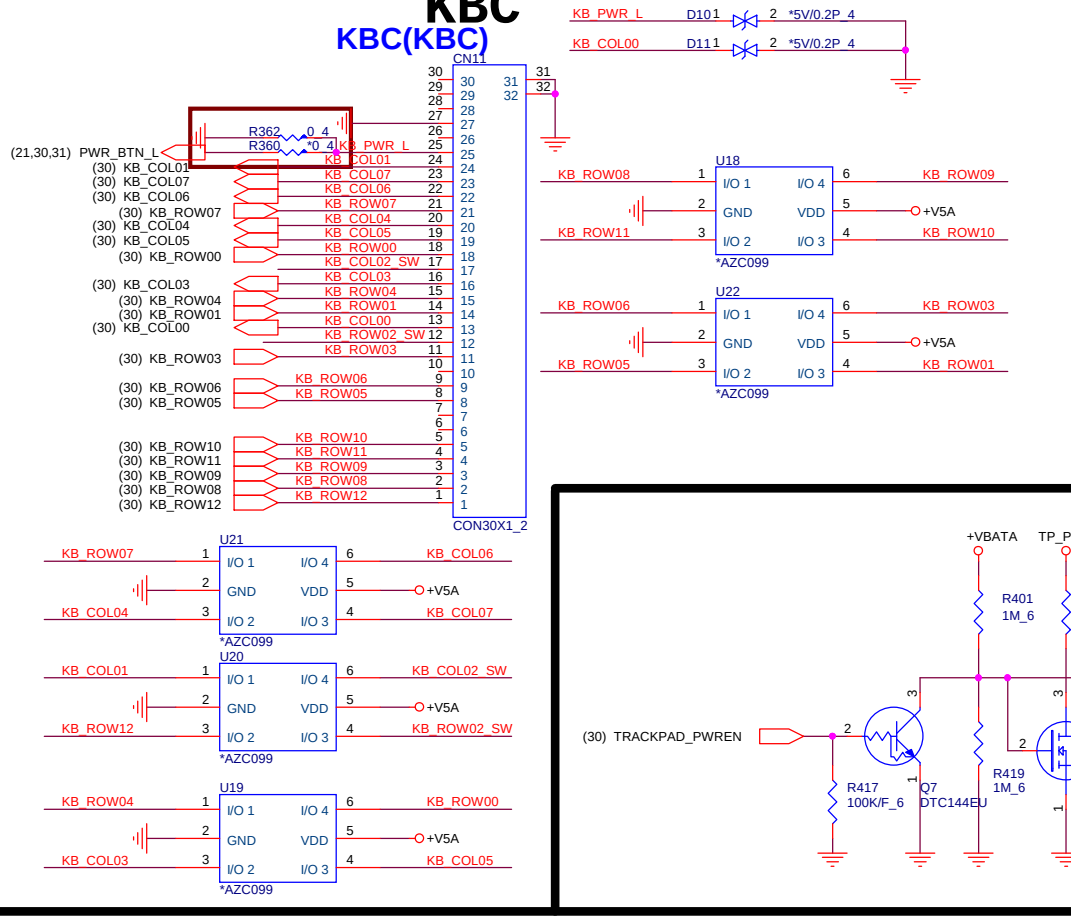
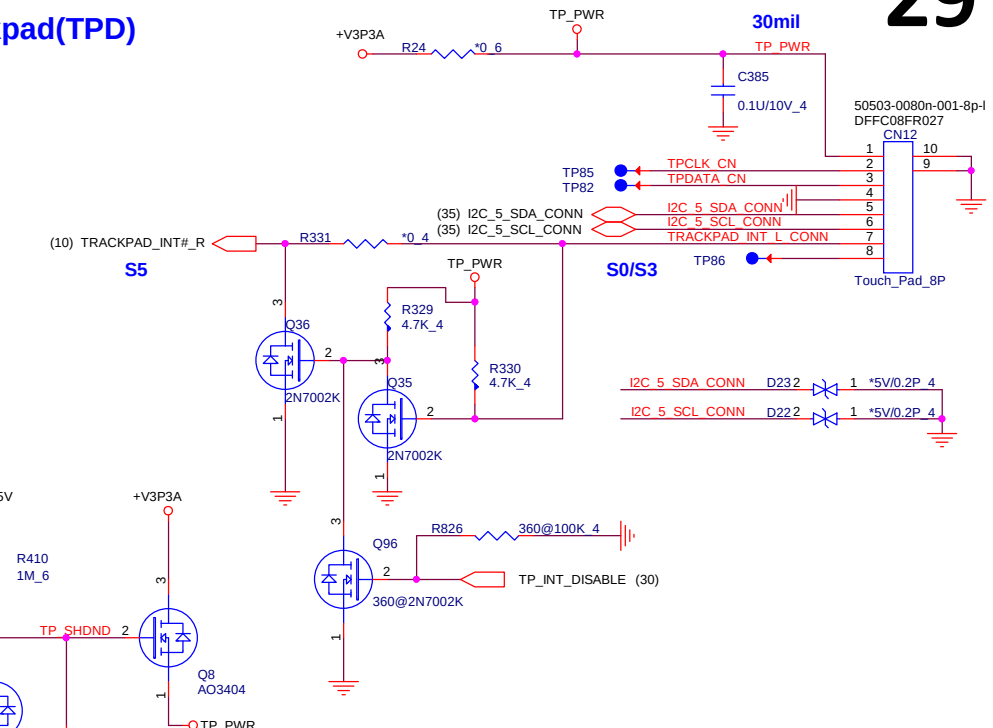
KBC

KBC(KBC)



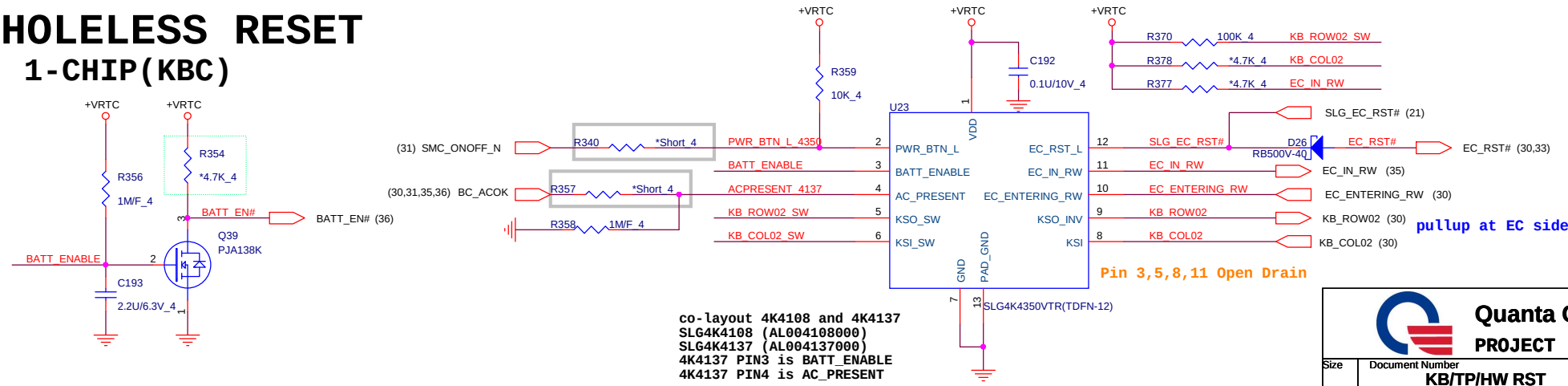
TRACK PAD BOARD CONN

Trackpad(TPD)



HOLELESS RESET

1-CHIP(KBC)



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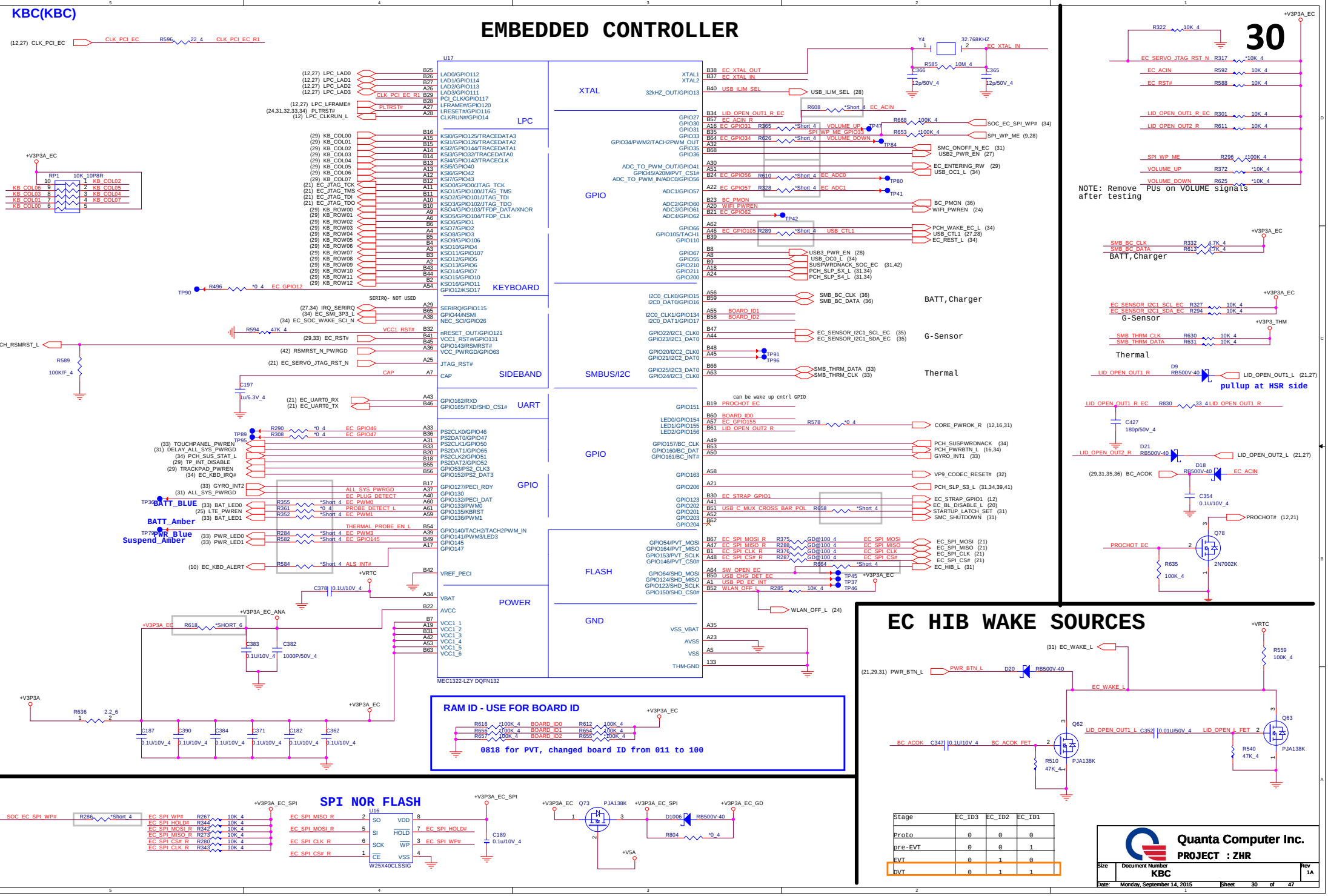
KBC(KBC)

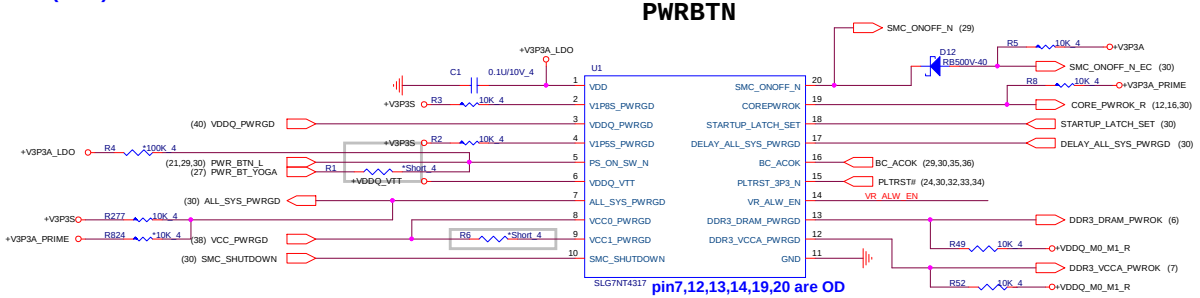
EMBEDDED CONTROLLER

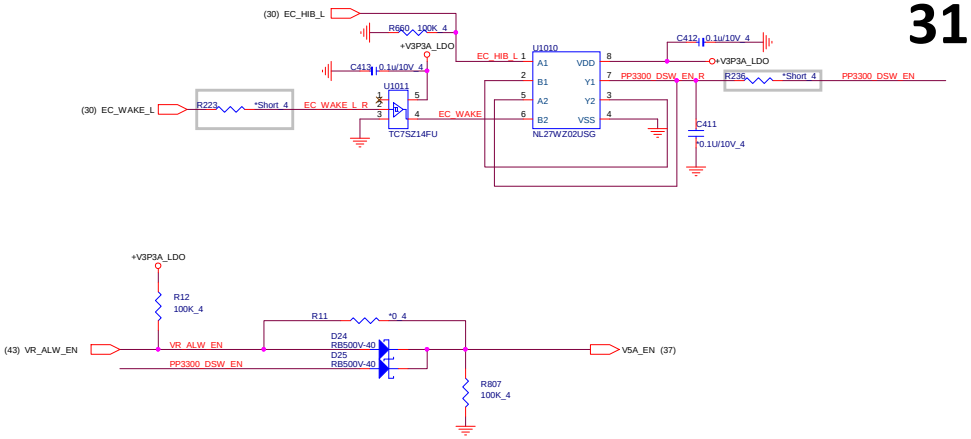


Stage	EC_ID3	EC_ID2	EC_ID1
Proto	0	0	0
pre-EVT	0	0	1
EVT	0	1	0
DVT	0	1	1

KBC(KBC)

PWRBTN



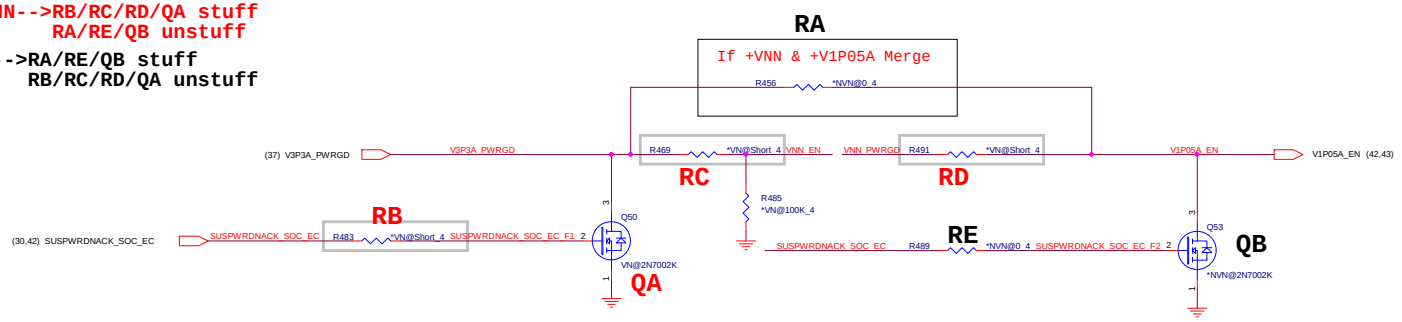


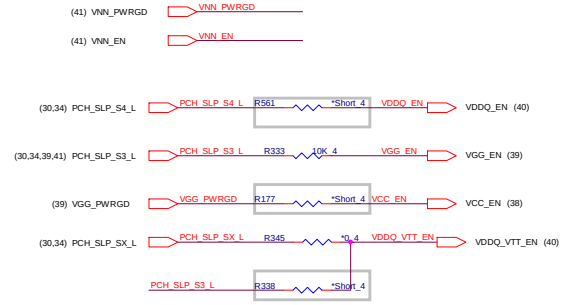
KBC(KBC)

POWER SEQUENCING

Dynamic VNN-->RB/RC/RD/QA stuff
RA/RE/QB unstuff

Fixed VNN-->RA/RE/QB stuff
RB/RC/RD/QA unstuff

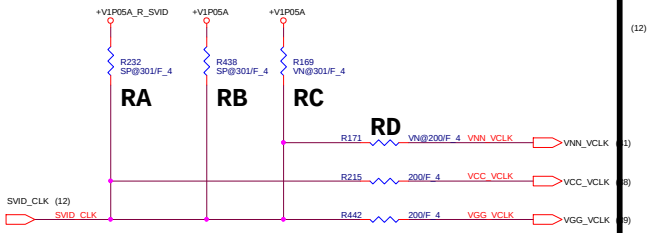




SVID(CPU) CLK

Dynamic VNN-->RA/RB/RC stuff 301 ohm
RD stuff 200 ohm

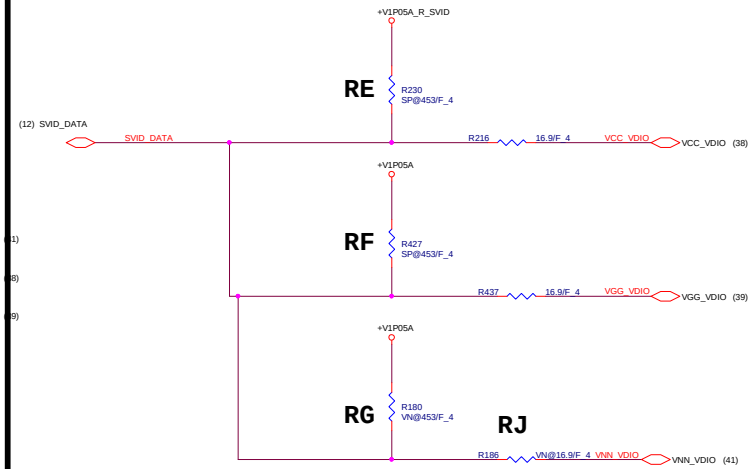
Fixed VNN-->RA/RB stuff 200 ohm,
RC/RD unstuffed



DATA

Dynamic VNN-->RE/RF/RG stuff 453 ohm
RJ stuff 16.9 ohm

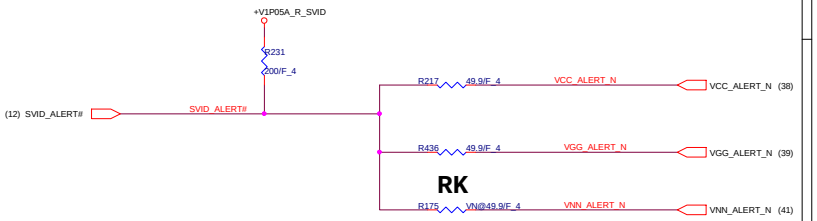
Fixed VNN-->RE/RF stuff 301 ohm,
RG/RJ unstuffed



ALERT

Dynamic VNN-->RK stuff 49.9 ohm

Fixed VNN-->RK unstuff



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	PWRBTN/PS/SVID	1A

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VIDEO CODEC

Video codec(VDC)

32

U7A **VC@VP9 VIDEO CODEC

U7B **VC@VP9 VIDEO CODEC

CAD NOTE:
MAKE +V1P24A_CODEC A POWER SHAPE
NEAR THE CODEC

BCRD says RA/RB/RC/RD are EMI bead 75ohm at 100MHz

0909 changed Footprint of video codec

0818 unstuffed related RC components of Kepler

RD

RA

RA

RC

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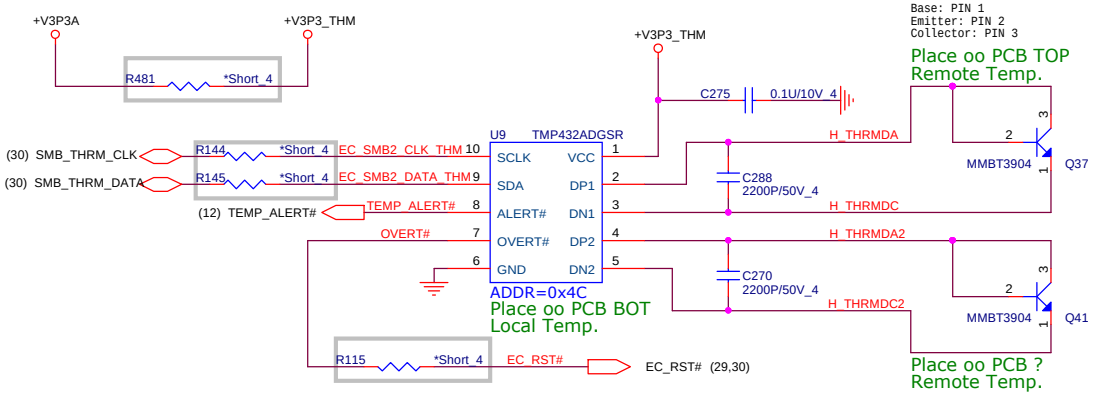
Thermal (THM)

THERMAL SENSOR

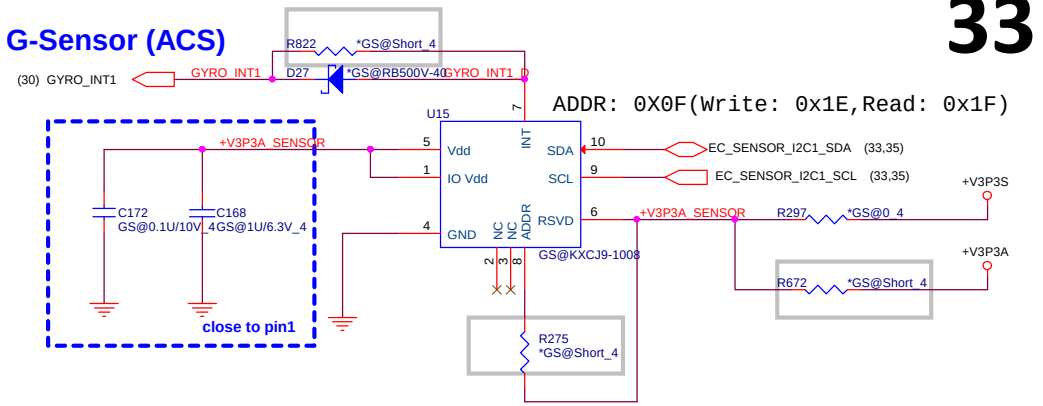
SENSORS/Touch screen Board/LED Board

33

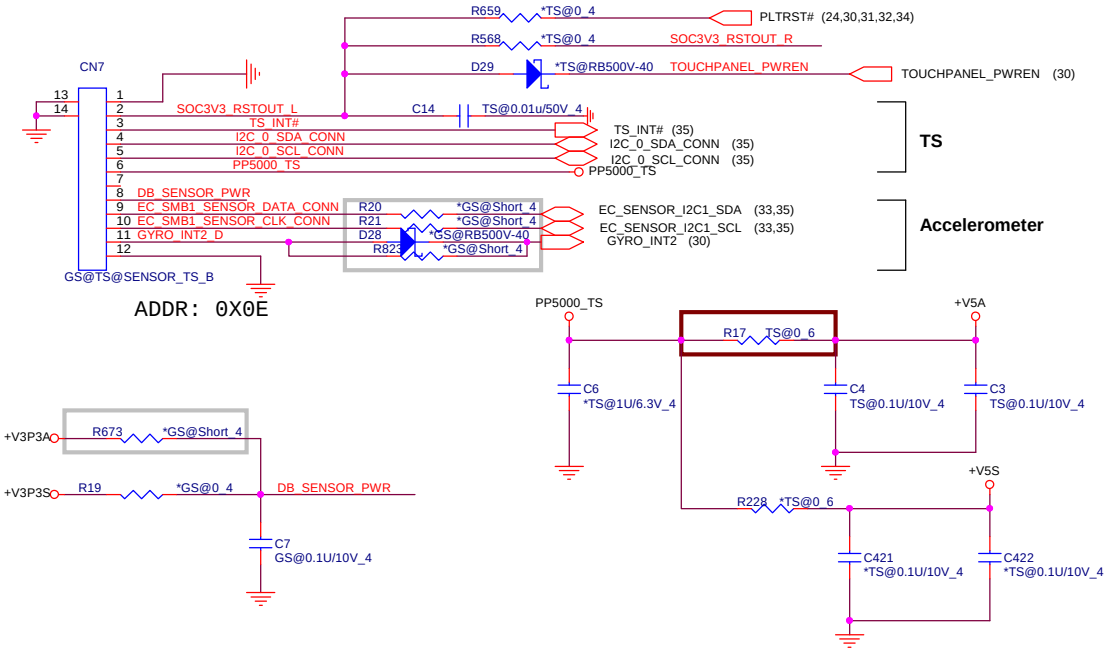


ACCELEROMETER

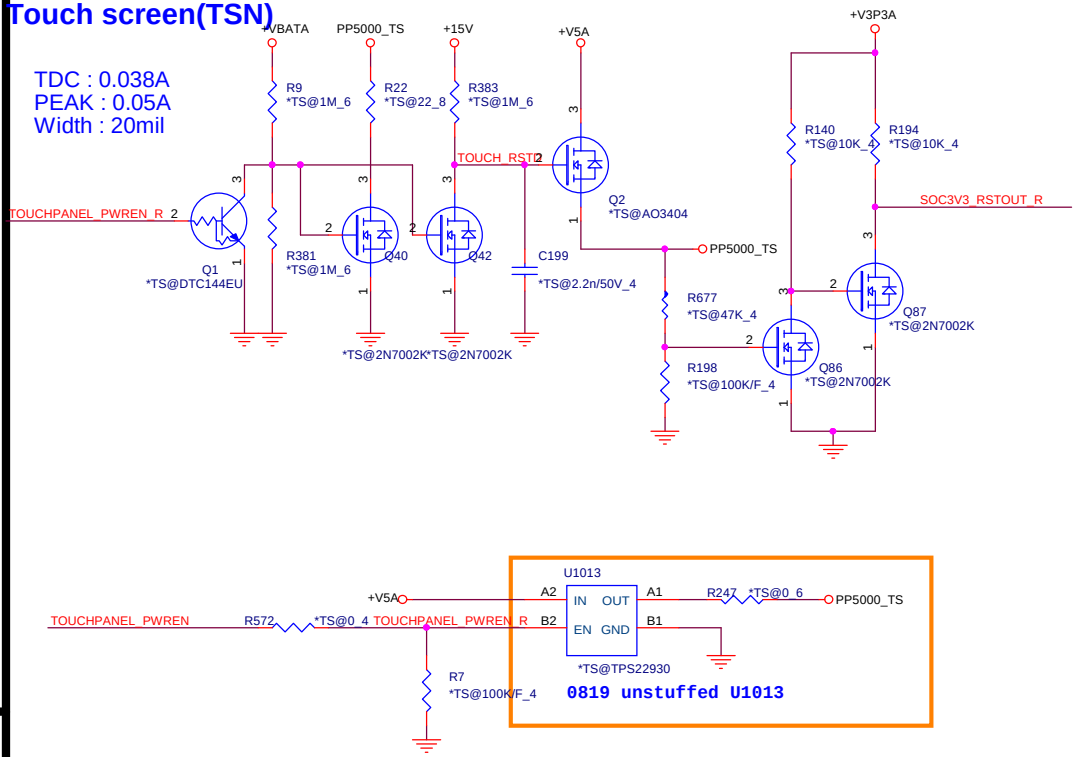
G-Sensor (ACS)



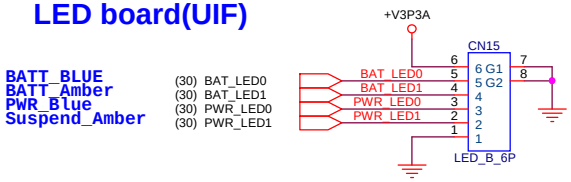
Touch screen(TSN)



Touch screen(TSN)



LED board(UIF)



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	SENSORS/LEDB	1A
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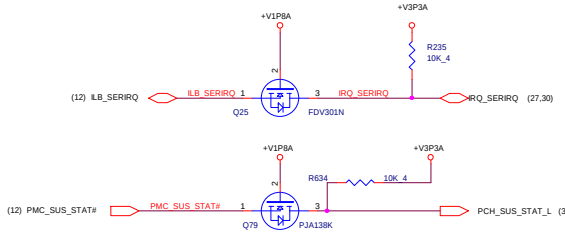
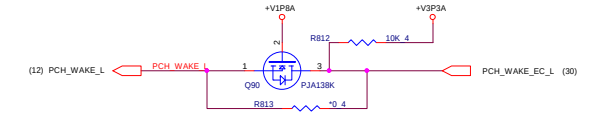
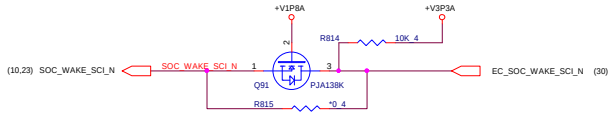
LEVEL TRANSLATOR 1

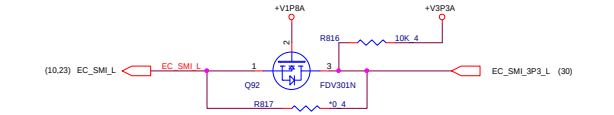
SoC(CPU)

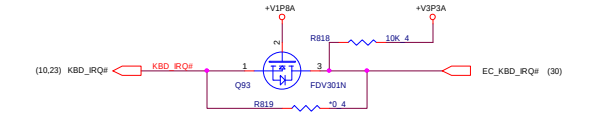
PWRON SEQUENCE

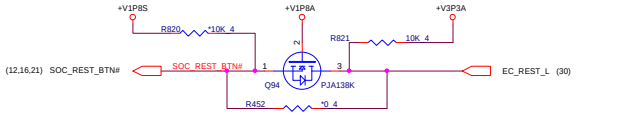




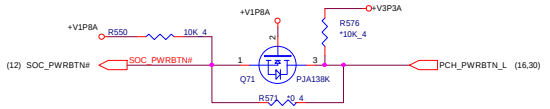


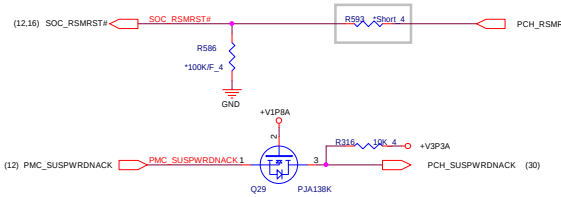


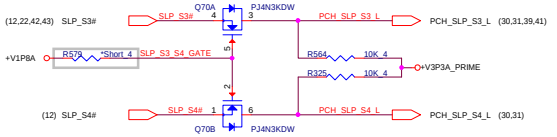


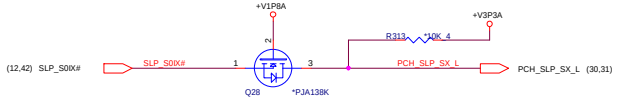


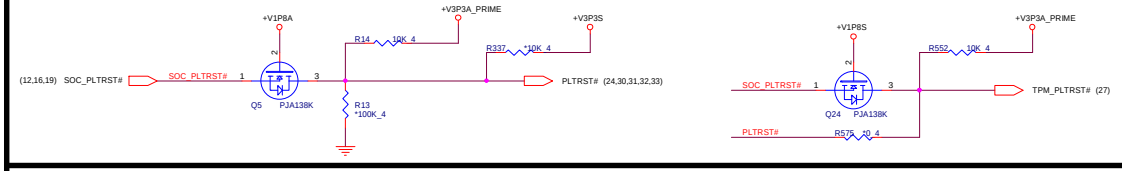
PWRON SEQUENCE



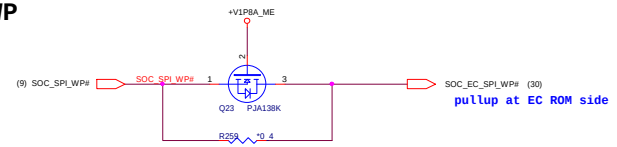








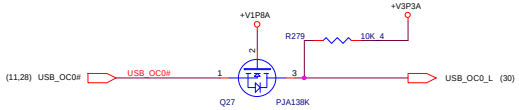
ROM WP



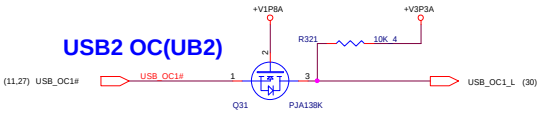
pullup at EC ROM side

USB OC

USB3 OC(UB3)



USB2 OC(UB2)



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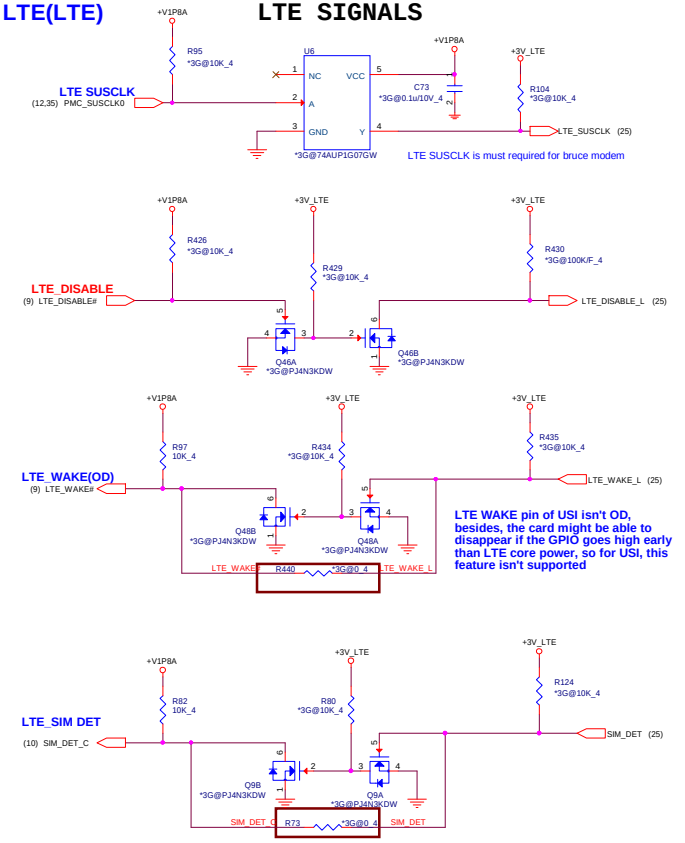
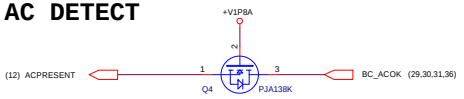
NOTE:USE 4 BIT LEVEL TRANSLATORS

LEVEL TRANSLATOR 2

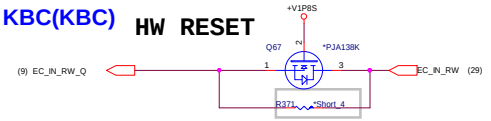
LTE(LTE) LTE SIGNALS



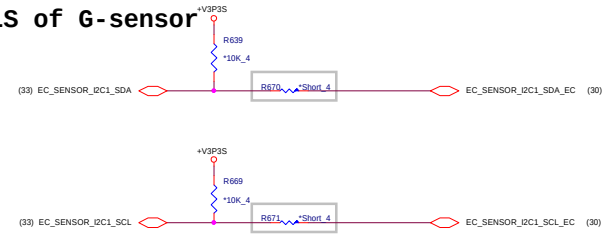
KBC(KBC) AC DETECT



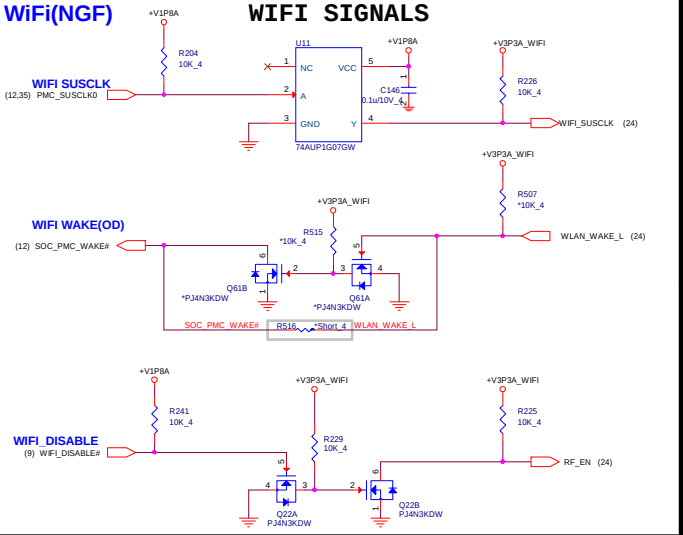
KBC(KBC) HW RESET



LS of G-sensor

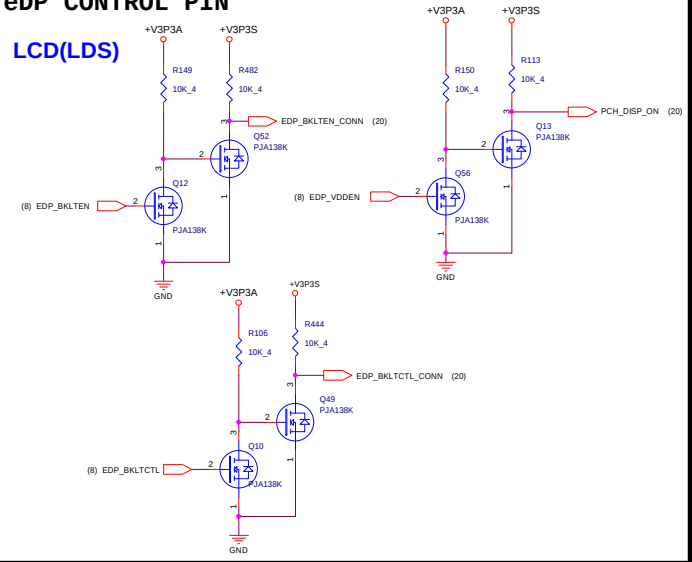


WiFi(NGF) WIFI SIGNALS

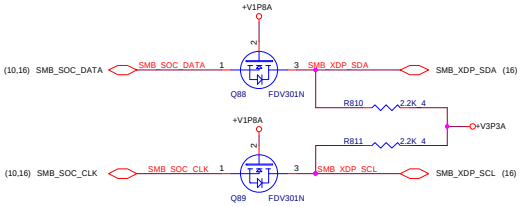


eDP CONTROL PIN

LCD(LDS)



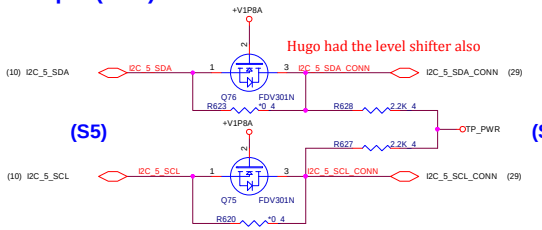
LS of XDP SMBUS



TRACK PAD I2C_5 SIGNALS

Trackpad(TPD)

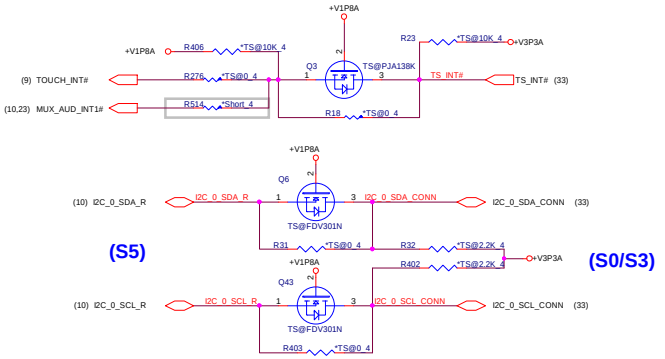
Hugo had the level shifter also



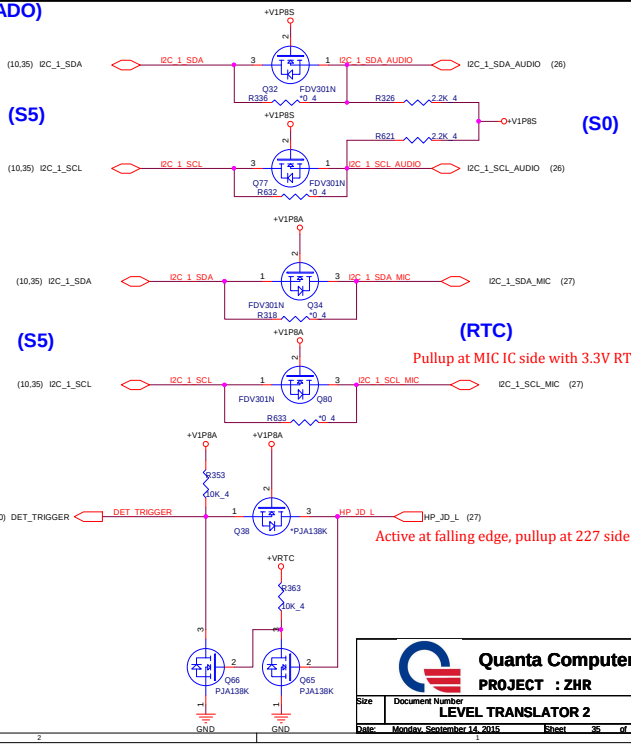
Touch Screen(TSN)

Note that there have pull up resistors on I2C/INT on touch controller board
Hugo had the level shifter also

TOUCH SCREEN I2C_0 SIGNALS



Audio(ADO)



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VR PAGE: +VBATA

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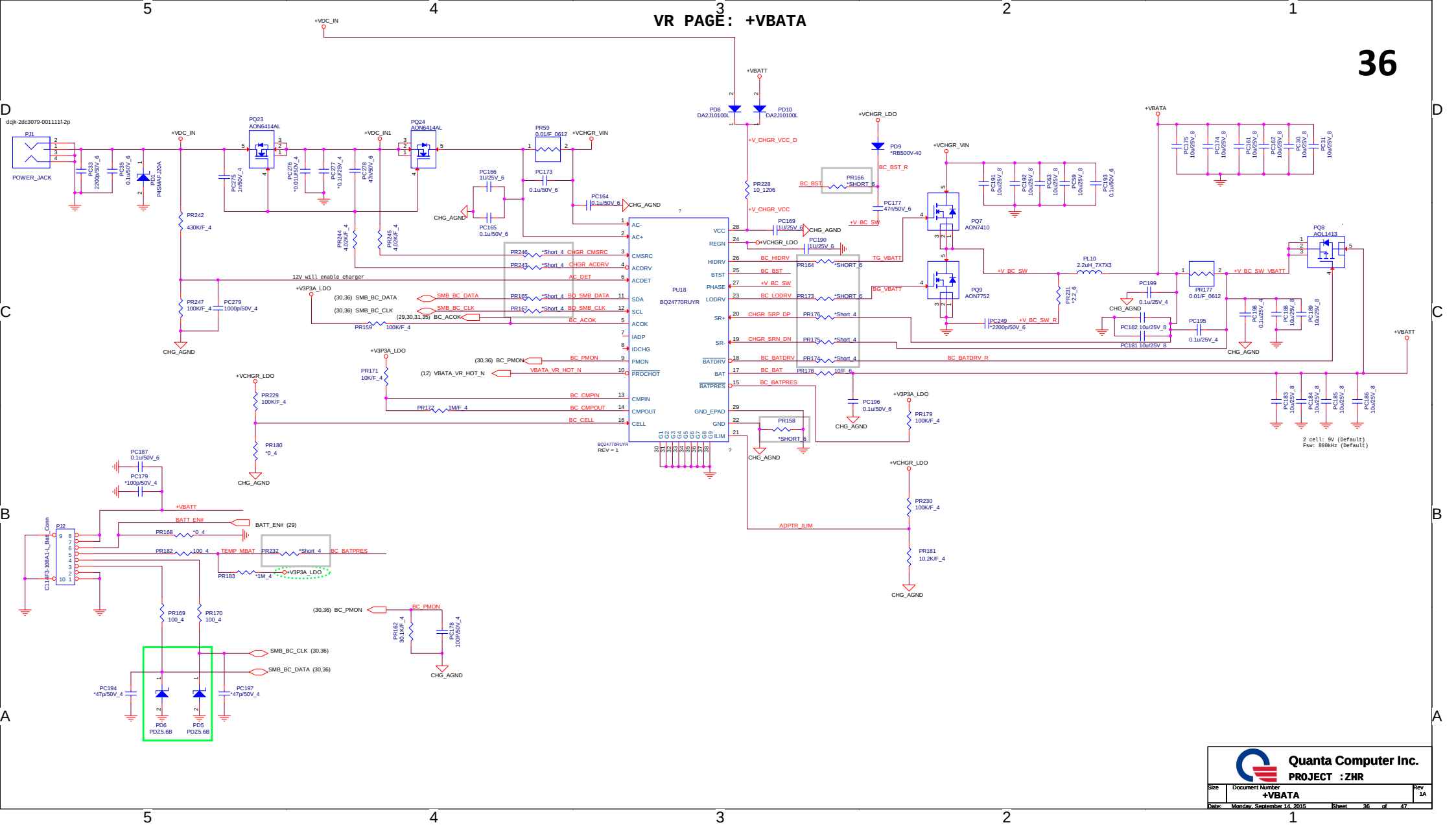

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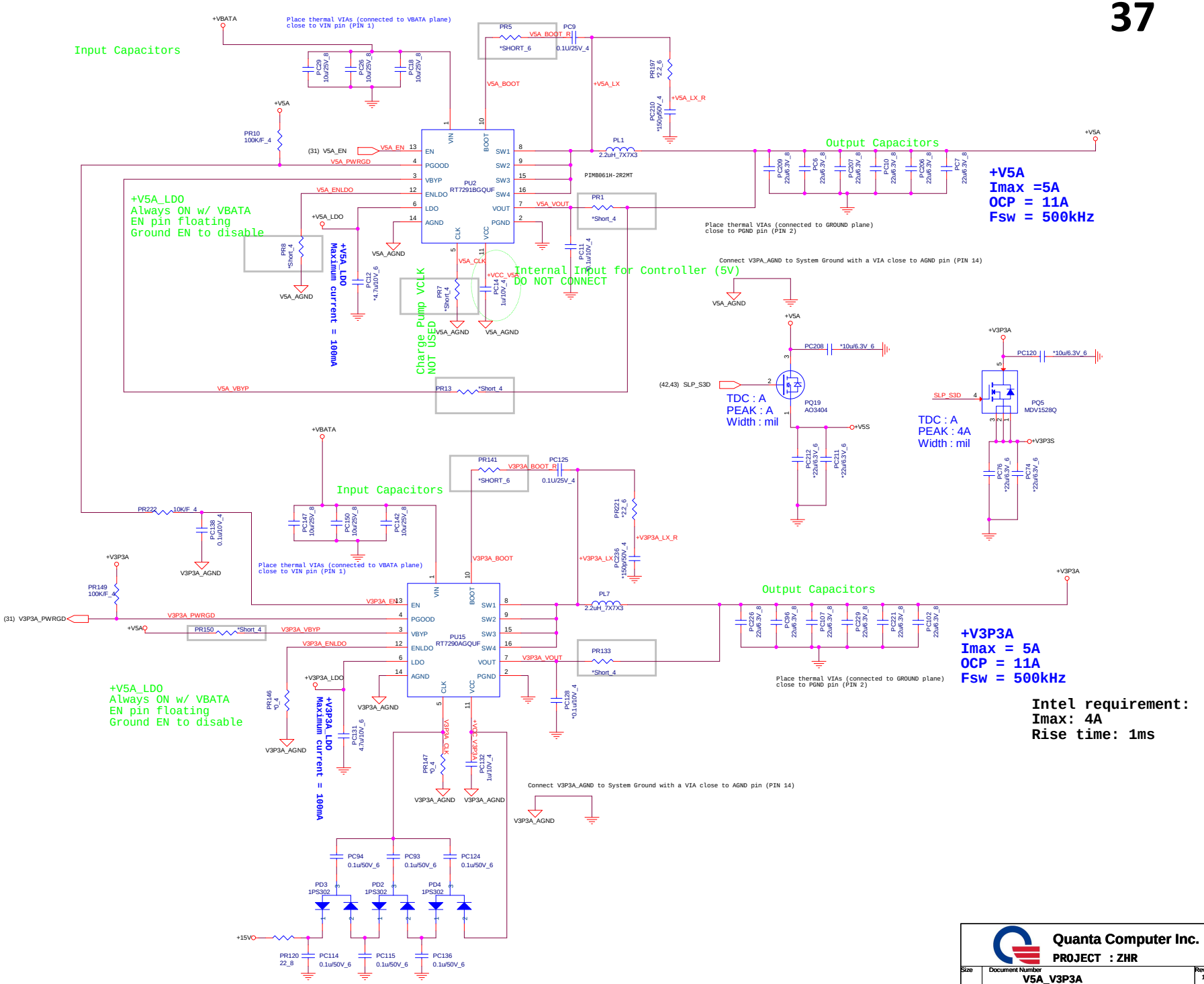
VR PAGE: +V5A & +V3P3A



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	V5A_V3P3A		1A
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VR PAGE: VCC_CPU

SET1:
Comp. Ramp factor = 267%
DVID width = 72us
DVID threshold = 15mV

SET2:
Icc,max = 7A
QR trigger = disable
QR width / Ton = 111%

SET3:
ZCD threshold = 75mV
Anti-overshoot = enabled
Fsw > 500kHz
VR Address = 0

REQ = 19.43kohm

Place Cin close to FET VIN pin
(1uF closer to VIN)

SVID Interface

Input Capacitors

+VCC_CPU
Imax =7 A
OCP = 8.96A (128%)
Load-line = 0ohm

Differential routing w/ VCC_SENSEP

Differential routing w/ VCC_SENSEN

VBOOT = 1V

GND

RT8175A

Output Capacitors

Loop Compensation

Place Cout close to BGA loading point

Differential Routing

Fsw = 789.76kHz

Max Current = 15A
Ron_HS = 15.7mohm
Ron_LS = 7.0mohm

0.25W

Quanta Computer Inc.	
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VR PAGE : +VGG

SET1:
Comp. Ramp factor = 267%
DVID width = 72us
DVID threshold = 15mV

SET2:
Icc,max = 13A
QR trigger = disable
QR width / Ton = 111%

SET3:
ZCD threshold = 75mV
Anti-overshoot = enabled
Fsw > 500kHz
VR Address = 5

Place Cin close to FET VIN pin
(1uF closer to VIN)

+VGG_CPU
Imax =13 A
OCP = 16.64A (128%)
Load-line = 0ohm

REQ = 10.462kohm

SVID Interface

Input Capacitors

Differential routing w/ VCC_SENSEP

Differential routing w/ VCC_SENSEN

Differential Routing

Loop Compensation

Place Cout close to BGA loading point

Output Capacitors

RT8175A

GND

Fsw = 803.43kHz

BCRD 5.1K

Max Current = 15A
Ron_HS = 15.7mohm
Ron_LS = 7.0mohm

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VR PAGE: +VDDQ

40

Fsw=500kHz
Non-Tracking Discharge

OCP~7.8A

0603

TPS51716

+VDDQ_VTT
Imax_VTT = 200mA

+VDDQ
Imax = 5A

Vout=1.35V

Place 47uF closer to VR Output

Quanta Computer Inc.		
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VR PAGE : +Vnn

SET1:
Comp. Ramp factor = 267%
DVID width = 72us
DVID threshold = 15mV

SET2:
Icc,max = 4.0 A
QR trigger = disable
QR width / Ton = 111%

SET3:
ZCD threshold = .75mV
Anti-overshoot = enabled
Fsw > 500kHz
VR Address = 01b

JP12 *NVN@0.002_1206 +VNN +V1P05A

VW02.2 - Resistor value change :
R3A1PD -> 33.2K
R3A2PD -> 4.7K
R3A3PD -> 976

+VNN_VREF PR104 VN@33.2K/F_4 PR204 VN@4.7K/F_4 PR101 VN@976/F_4 VNN_IMON_R2 VNN_IMON_R1 VNN_IMON

REQ = 38.86 kohm

SVID Interface

Place Cin close to FET VIN pin
(1uF closer to VIN)

+VBATA

Input Capacitors

PC108 VN@10u/16V_6 PC107 VN@10u/16V_6 PC105 VN@10u/16V_6 PC106 VN@1u/25V_6

+VNN : 0.78 -1.2v
Imax =3.5 A
OCP = 5.0 A (128%)
Load-line = 0ohm

PC103 VN@0.47u/6.3V_4 PR203 VN@100K/F_4 +VNN_VREF VNN_IBIAS

VNN_VCLK (31) VNN_VDIO (31) VNN_ALERT_N (31)

PR208 *VN@Short_4 VNN_RGND GND near +VGG GND

+V3P3A PR81 VN@10K/F_4

(31) VNN_EN VNN_EN
VNN_PWRGD
(12) VNN_VR_HOT_N VNN_VR_HOT_N

PU10 RT8175A

VRON	26		
VR_READY	17		
VR_HOT#	12		
IMON	31		
VREF	1		
IBIAS	10		
VCLK	15		
VDIO	13		
ALERT#	14		
RGND	5		
BOOT1	22		
UGATE1	25		
PHASE1	23		
LGATE1	20		
PGND	19		
DRVEN2	24		
DRVEN1	18		
SET3	9		
SET1	7		
SET2	8		
SETGND	30		
Vbootsel	29		
VSEN			
COMP	2		
FB	3		
VCC	6		
TSEN	11		
TONSET	16		
PVCC	21		
NC	32		
ISEN1N	27		
ISEN1P	28		
EGND	33		

GND

PR79 *VN@SHORT_6 VNN_BOOT_R PC78 VN@0.1U/25V_4

PR98 *VN@Short_4 PR97 *VN@Short_4 VNN_UGATE1 VNN_TG VNN_LGATE1 VNN_BG

CSD67381P PU13 VN@CSD67381P VIN VSW PGND TG BG

Max Current = 15A
Ron_HS = 15.7mohm
Ron_LS = 7.0mohm

PL6 VN@1uH_7X7X3 +VNN_LX JP11 VN@0.001_3720 +VNN_OUT 1W

PR87 *VN@2_6 +VNN_LX_R PC91 *VN@10p/50V_4

PR89 *VN@Short_4 PR88 *VN@Short_4

PR201 *VN@Short_4 VNN_DRVEN2 VNN_DRVEN1

VW02.2 - changed to +VNN_VCC

VW02.2 - Resistor value change :
R3A2PD -> 1.15K
R3A3PD -> 681
R3A30PD -> 392
R3A1PD -> 221
R3A22PD -> 13.7 K

Design Note : ->
optimized for standby current

+VNN_VCC PR129 VN@80.6K/F_4 PR130 VN@13.7K/F_4 PR131 VN@1.15K/F_4 VNN_SET3_RU VNN_SET1_RU VNN_SET2_RU PR119 VN@681/F_4 PR117 VN@1.15K/F_4 PR118 VN@39.2K/F_4 VNN_SET1 VNN_SET2 VNN_SET3 PR214 VN@976/F_4 PR213 VN@23.7K/F_4 PR215 VN@221/F_4 VNN_SET1_RD VNN_SET2_RD VNN_SET3_RD PR218 VN@365/F_4 PR219 VN@221/F_4 PR220 VN@392/F_4 VNN_SETGND

VB00T = 1.6V

PR202 VN@100K/F_4 VNN_SETGND PR100 VN@100K/F_4 PR116 *VN@Short_4 VNN_SENSE_R +VNN_SENSEP (12,41,42)

PR125 VN@10K/F_4 PR111 VN@75K/F_4 VNN_COMP PR123 *VN@10K/F_4 PC121 VN@270p/50V_4 PC110 VN@22p/50V_4 VNN_FB

Loop Compensation

PC109 VN@2.2u/10V_4 PR80 *VN@SHORT_6 PC79 VN@2.2u/10V_4

PR83 VN@15K/F_4 VNN_TONSET_RTON PR78 VN@634K/F_4 VNN_TONSET_R PR82 VN@1/F_4 PC77 VN@2.2u/10V_4

Fsw = 803.43kHz

TP_VNN_NP

VNN_ISEN1P_DP VNN_ISEN1N_DN VNN_ISEN1N_R_DN PR90 VN@681/F_4 PC90 VN@0.1U/10V_4

Differential Routing

VNN OFFSET BACKUP CIRCUIT

VNN OFFSET CIRCUIT

PR113 VN@5.6K/F_4 VNN_SEN_R VNN_TSEN

B = 4250 +/- 1%
Trip at 100degC

PR121 VN@100K/F_4_4250NTC PR140 VN@100K/F_4 PR109 VN@4.65K/F_4

+V1P05A (43) SLP_S3#_F_F PQ20 *VN@2N7002K

+VNN_SENSEP_F1 PR67 *VN@100/F_4 +VNN_SENSEP PR103 *VN@100K/F_4 +VNN_SENSEP_F2 PR239 *VN@0_4 SLP_S3#_F_R PQ21 *VN@2N7002K PC281 *VN@0.1U/10V_4

+V3P3A_PRIME (30,31,34,39) PCH_SLP_S3_L PR240 *VN@Short_4 PQ22 VN@BSS84 PR248 *VN@100K/F_4 PR241 VN@309K/F_4 VNN_FB

Output Capacitors

VW02.2 output caps are changed to 5X47 uF

PC228 PC113 PC230 PC231 PC122 PC107 PC227 PC38 PC224 PC235 VN@22u/6.3V_6

Place Cout close to BGA loading point

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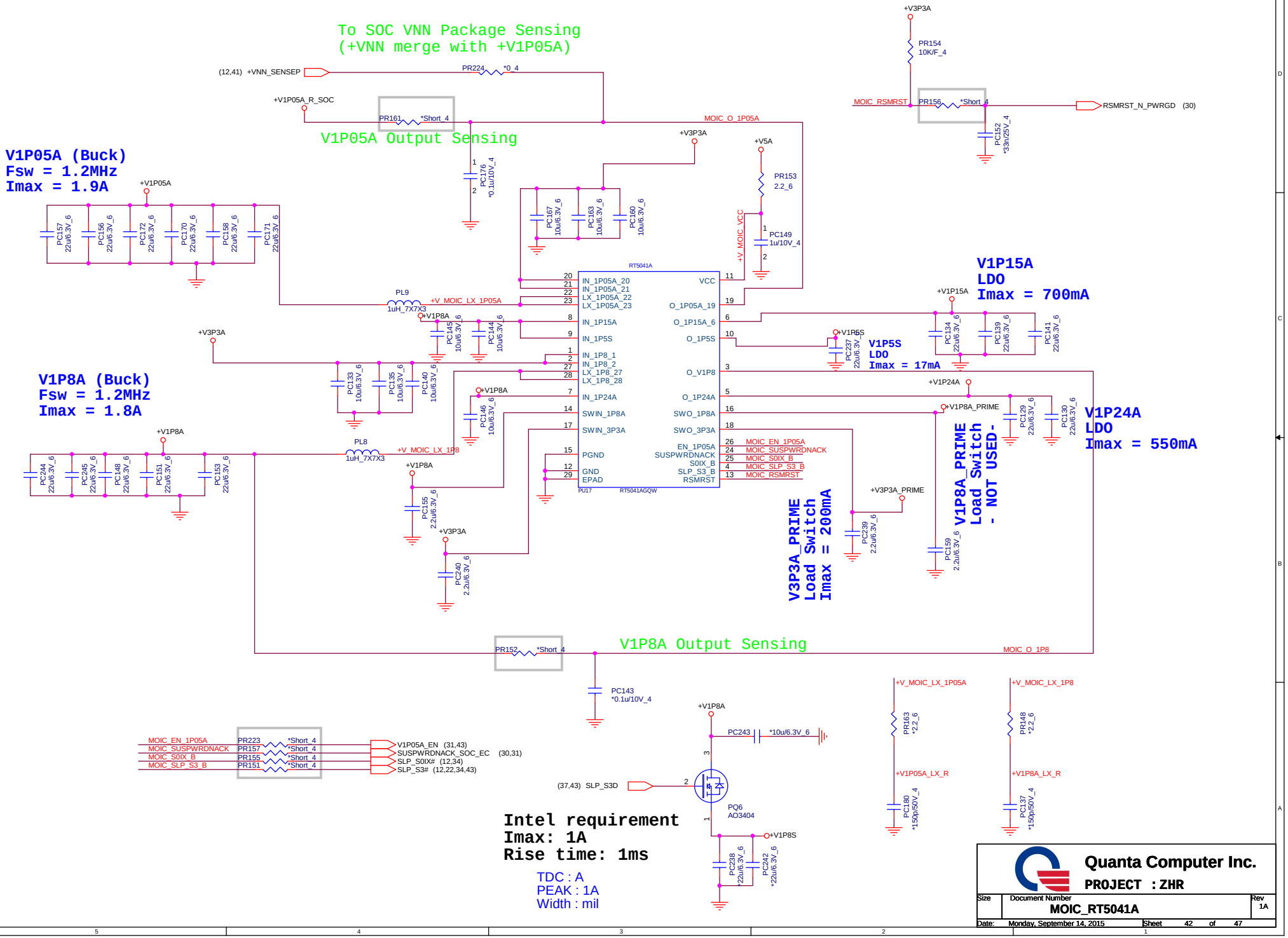
VR PAGE: MOIC


To SOC VNN Package Sensing
(+VNN merge with +V1P05A)
V1P05A Output Sensing
V1P05A (Buck)
Fsw = 1.2MHz
Imax = 1.9A
V1P8A (Buck)
Fsw = 1.2MHz
Imax = 1.8A
V1P15A
LDO
Imax = 700mA
V1P5S
LDO
Imax = 17mA
V1P24A
LDO
Imax = 550mA
V3P3A_PRIME
Load Switch
Imax = 200mA
V1P8A_PRIME
Load Switch
- NOT USED-
V1P8A Output Sensing
Intel requirement
Imax: 1A
Rise time: 1ms
TDC : A
PEAK : 1A
Width : mil
RT5041A
RT5041AGQW
(12,41) +VNN_SENSEP
+V1P05A_R_SOC
MOIC_O_1P05A
MOIC_O_1P8
RSMRST_N_PWRGD (30)
V1P05A_EN (31,43)
SUSPWRDNACK_SOC_EC (30,31)
SLP_S0IX# (12,34)
SLP_S3# (12,22,34,43)
(37,43) SLP_S3D
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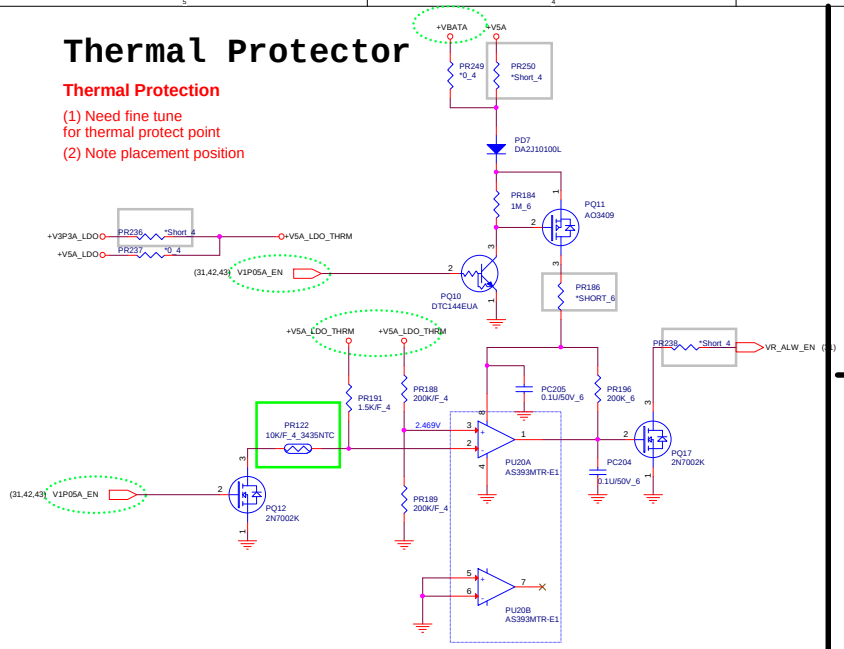
Thermal Protector

Thermal Protection

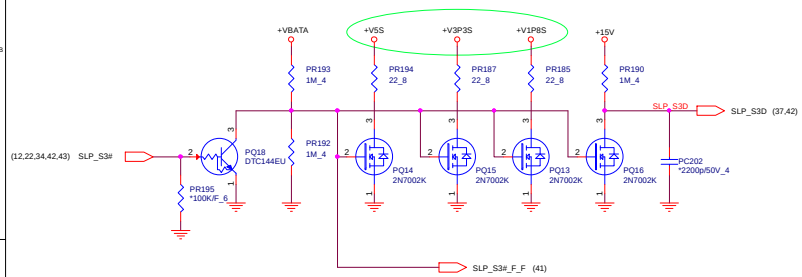
(1) Need fine tune
for thermal protect point

(2) Note placement position



For EC control thermal protection (output 3.3V)

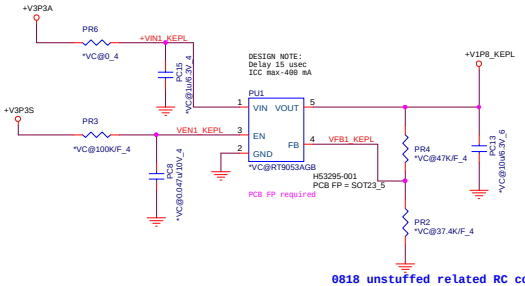
Discharger of S0 power rails



KEPLER VR

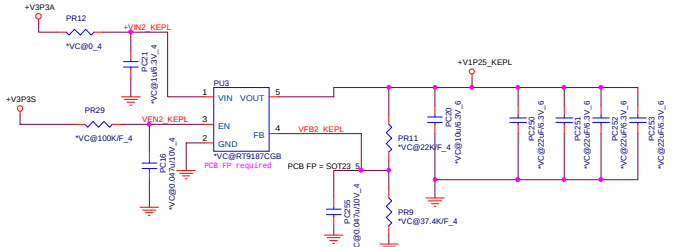
43

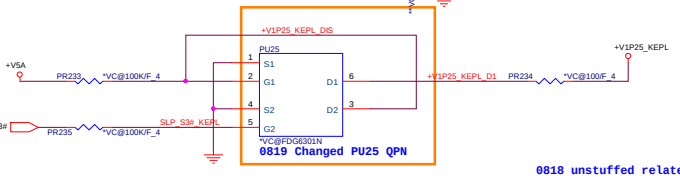
Video codec(VDC)



0818 unstuffed related RC components of Kepler

Video codec(VDC)

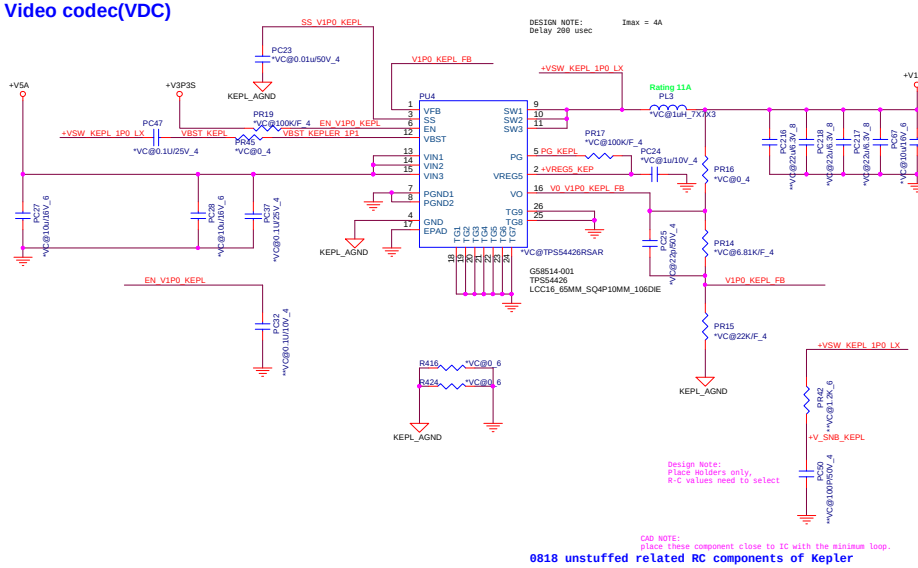




0819 Changed PU25 QPN

0818 unstuffed related RC components of Kepler

Video codec(VDC)



0818 unstuffed related RC components of Kepler

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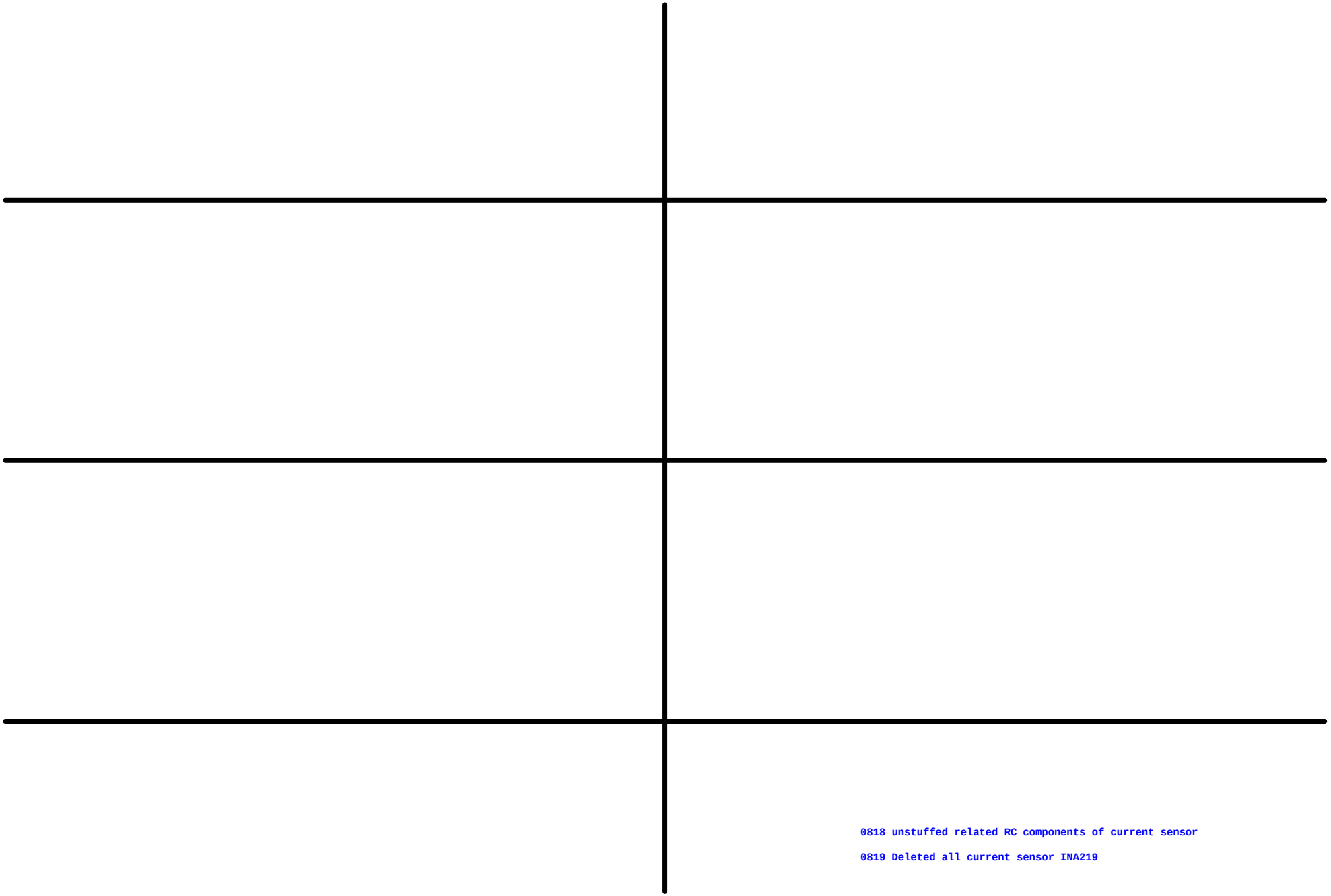
INA DEVICES 1



0818 unstuffed related RC components of current sensor

0819 Deleted all current sensor INA219

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INA DEVICES 2

0818 unstuffed related RC components of current sensor

0819 Deleted all current sensor INA219

Model	Version	CHANGE LIST	46

ZHR/ZHRA — **1A**

12/24
A01 Removed voltage divider of M0_OCAVREF and M0_ODQVREF,renamed M0_OCAVREF and M0_ODQVREF (Page 6)
A02 Removed voltage divider of M0_OCAVREF and M0_ODQVREF,renamed M0_OCAVREF and M0_ODQVREF(Page 7)
A03 Deleted RCOMP resistor (Page 8)
A04 changed damping resistors of SPI ROM from 22ohm to 10 ohm (Page 9)
A05 Swapped PCIe/CLKREQ/CLK between Video codec and WLAN (Page 9)
A06 Net name of WIFI_32KHz changed to SDCARD_WP (Page 10)
A07 Changed damping resistors of VCC sensing from 2.2ohm to 10Ω ohm(Page 12)
A08 Deleted C3138,C3137(Page 13)
A09 added 1K resistor on PWR_SD_GATE_EN,discharger of SD power supply made as placeholder (Page 19)
A10 Connected EC_SERVO_JTAG_RST_N signal from A25 of EC to pin 28 of Servo,Stuff R956/R958 (Page21)
A11 Net name of WIFI_32KHz changed to SDCARD_WP (Page23)
A12 Add power gating forWiFi power,Change PCIe mapping of WLAN (Page24)
A13 Add power gating for LTE power(Page 25)
A14 co-layout ST with Infineon TPM, if change to ST,RA,RB,RD,RE,RF are unstuffed , ST PN is T33ZP24AR28PVSM,Change the power option of TPM to +V3P3A_PRIME (Page 27)
A15 Add power gating for Track pad power(Page 29)
A16 Connected EC_SERVO_JTAG_RST_N signal from A25 of EC to pin 28 of Servo,remove RAMID1/2,unstuff R981,tie to WP pin of EC ROM,rename RAM_ID0 to BOARD_ID0(Page38)
A17 Change PCIe mapping of Video Codec (Page 32)
A18 Add power gating for Touch screen power (Page33)
A19 add voltage divider for SLP_S3#/SLP_S4# level shifter(Page34)
A20 Removed BC_IADP and BC_IDCHG connections(Page 36)
A21 Delete offpage of +V1P05A_OUT(Page 42)
A22 Change sensing point to +V1P05A_R_SOC (Page 44)

12/26
A23 Add Footprint of Video codec (Page 32)

01/02
A24 stuff back Swapped Drain and source wiring of Q3057/Q3076(Page 9)
A25 Changed SD slot to push-push type (Copied from DC7) (Page 19)
A26 Added one more 10uF to meet 1x 22uF closely,Changed R340 to 0 ohm,Added one more 0 ohm for suffering 1.5A rating(Page 20)
A27 unstuffed R64/R65 (Page 22)
A28 Added level shifters for MIC present pin and MIC INT,Add option path for I2C of MIC SW, default is USB charger path (Page 27)
A29 added pullup for LID_OPEN_OUT2_R,Renamed from LID_OPEN_R to LID_OPEN_OUT1_R,Renamed to LID_OPEN_OUT2_R,added Diode of isolation for LID_OPEN_OUT2_L (Page 30)
A30 Changed Q35 to Level shifter,Added Level shifter for MIC I2C signals (Page 35)
A31 Changed slave address of current sensor in order to sync with BCRD(Page 44,45)

01/03
A32 changed C load of PCH 32,768K from 15pF to 18pF (Page 12)
A33 corrected the net name of PP3300_DSW(Page 16)
A34 corrected the net name of PP1800_PCH (Page 20)
A35 changed R3216 to 2.7K(Page 23)
A36 deleted external S0 pullup of AUDIO_CODEC_IRQ (Page 26)
A37 stuffed R353, unstuffed R581, depend on leakage debugging then decide on this(Page 27)
A38 corrected the net name of PP5000_DSW,stuffed R474 ,changed the power button of KB to Lock function,stuffed R475(Page29)
A39 moved pullup of thermal I2C to thermal IC page,merged SMBUS of BATT and Thermal, besides Sensor I2C is changed from SMBUS1 to I2C1,re-named for mergering SMBUS of BATT and Thermal(Page 30)
A40 corrected the name name of RTC power,deleted redundant R1053,Changed the damping resistor of SVID alert from 0 ohm to 49.9 (Page 31)
A41 Deleted diode which prevent leakage from going to sensor,Changed pull up power of GYRO_INT2 to +V3P3S,deleted RST pin of Touch screen, using VDD reset with RC delay,removed option of G-Sensor power supply(Page 33)
A42 remove offpage of MIC0 own signals and V1DSA_EN is input pin for MIC(Page 42)

01/05
A43 deleted external pull ups of I2C due to Intel mentioned there have strongly internal pullups in SoC (Page 10)
A44 changed Q3074 single MOSFET instead of dual, changed SDIO power circuitry to meet Intel's timing requirement for transistion between 1.8V and 3.3V (Page 19)
A45 Changed connection of EC WP (Page 38)
A46 Added "SGX" in value as a BOM option for G-sensor(Page 33)
A47 changed Level shifter of SERIRQ to MOSFET type,unstuffed pull down of PCH_RSMRST_L,Added level shifter for EC WP (Page 34)
A43 go for optional connection of Touch Pad I2C/INT directly,go for optional connection of Audio I2C thru level shifter (Page 35)
A44 Added 3 power units for Kepler (Page 43)

01/06
A45 Added the connection of LID_OPEN_OUT2_L(Page 26)
A46 Changed R144 to 4.7K(Page 29)
A47 correct net name for WiFi power(Page 35)
A48 reserve placeholder R212,R218 for additional RAM ID (Page 7)

01/07
A49 use 100K instead of 10k for empty resistor (Page 23)
A50 corrected net name of pin26 (Page 25)
A51 deleted the optional of USB charger (Page 27)
A52 Deleted USB charger IC,Stuffed USB power switch (Page 28)
A53 USB_ILIM_SEL to left NC,USB_CTL1 to left NC(Page 30)
A54 corrected PU21,PU31,PU32 Footprint(Page 43)

01/08
A55 added 4 pins for RAMID (Page 10)
A56 corrected Footprint of SDID power IC(Page 19)
A57 for layout, changed +V3P3A_EC to +V3P3A (Page 21,31,34)
A58 Swapped CDEX1 and CDEX2 (Page 25)
A59 Changed USB CRC to PCB-CRC (Page 28)
A60 Lock works by KB matrix, not GPIO, remove connection (Page 29)
A61 added dedicated 1uF and 0 ohm (placeholder) on Ball C9,added 0 ohm (placeholder) on Ball G12/H12(Page 32)
A62 R837 is stuffed that based on M.2 spec(Page 35)
A63 removed +VDDQ_VTT_OUT (Page 40)

01/09
A64 change RAM ID0 form Ball AG1 to AF3,changed RAM ID1 form Ball V6 to AE4, RAM ID3 from Ball B8 to AD2,Removed VNN I2C due to VNN is SVID type(Page9,10)
A65 added VNN_VR_HOT_N (Page12)
A66 changed Fin10 from +V3P3VA to GND(Page 27)
A67 Changed L5/L6 footprint (Page 28)
A68 VNN I2C disconnection due to VNN is SVID type (Page 30)
A69 Added VNN SVID ALERT connection,Added VNN SVID DATA connection,Added VNN SVID CLK connection(Page 31)
A70 Removed VNN level shifter due to VNN is SVID type(Page 35)
A71 added 3 GND pin on ORCAD library for PU10, PU21(Page 36,43)
A72 added placeholder cap for S0 power input (Page 37,42)
A73 added 5 GND pin on ORCAD library for PU22(Page 40)

01/12
A74 added soft start for AC1N,stuffed PR373 for 3 cell battery ,due to embeded battery, removed the TEMP_MBAT(Page36)
A75 swapped PR169 and PC69,swapped PR171 and PC110 (Page37)
A76 removed offpage of MOSC_EDMSIT(Page 42)
A77 Add bridge resistors for Kepler AGND (Page 43)
A78 unstuffed R3722/R3723 due to w/o quad mode,Changed MOSFET with higer switching speed Q3075,Q3076 (Page 9)
A79 stuffed C199 (Page 16)
A80 added voltage inverter due to CD/WP are normal close,added 0 ohm for SDID discharger circuitery ,changed SDMMC3_PWR_EN_N_G Pullup value to 10K(Page 19)
A81 deleted R42 due to level shifter was deleted(Page 24)
A82 added caps placeholder for EMI(Page 28)
A83 separated KBC_AGND,Changed KBC_AGND(Page 38)
A84 Added empty 0.1uF from Ball G12 to H12(Page32)

01/13
A85 changed Footprint of WiFi NGFF (Page24)
A86 swapped pins of KB ESD for layout(Page 29)
A87 Swapped pin of RP1 for layout (Page 30)
A88 defult un-stuff VNN components (Page 31,41,44)

01/15
A89 corrected net name of eMMC RClK (Page 19)
A90 Swapped USBP/N for layout (Page 27)
A91 moved diode from input to output of USB load switch,added screw holes(Page 28)
A92 Merge KBC_AGND with DGND (Page 38)
A93 changed R1057,PR340 from 10K to 100K (Page 31,36)

01/16
A94 Changed PWR button connection (Page29,31)
A95 Changed SMC_ONOFF_N connection (Page31)

01/18
A96 added RAMID table, dfault optional of BOM is for Samsung 4GB (Page 10)
A97 Added eMMC table ,dfault optional of BOM is for Samsung 32G (Page 19)
A98 deleted TP189 for layout (Page 38)

01/19
A99 added back connection(USB_ILIM_SEL,USB_CTL1) for USB charger (Page 30)
A100 PR42 Changed resistor value tolerance as 5% (Page43)
A101 changed the connector from 30 pin to 34 pin, and added back connection for USB charger (Page 27)
A102 added back USB charger controller (Page28)

01/20
A103 Changed QPN for PU14 (Page 38)
A104 deleted jump of +V1P8A_PRIME for layout (Page42)
A105 C280/C310 are changed to 0402(Page 13)
A106 swapped L+/L- of SPK (Page26)
A107 Swapped pin of L4 for layout (Page 28)
A108 Changed QPN of USB charger IC (Page28)

01/21
A109 adding zero ohm x3 for +V1P05A_R_SOC layout improvement(Page 13)
A110 Changed pin14/15 of SD card to NPTH (Page19)
A111 Changed Hole2 to NPH (Page 28)

01/23
A112 Changed QPN of R88/R105/PR226/PR138/PR49/PR181/PR214 (Page32,36,38,39,41)
A113 Moved C10 from C4B to C4A for layout, exchanged VTT decoupling caps between CHA and CHB for layout(Page 17)
A114 Moved C8 from CHA to CHB for layout, but keep being stuffed in single channel SKU.exchanged VTT decoupling caps between CHA and CHB for layout (Page18)

01/28
A115 deleted SPI Quad mode connection (Page 9)
A116 JP2E/JP1/JP7/JP6/JP11 is changed to 0.001 ohm(Page36,37,39,41)
A117 corrrected PU11 to be stuffed(Page45)

3A

03/01
B01 Added BOARD_ID1/BOARD_ID2,and for DVT1,changed board ID from 000 to 001(R612 is stuffed, R616 is un-stuffed (Page 38)
B02 Added 100k series R on SPI_WP_ME to separate from EC pin for hacking(Page 38)
B03 Removed VBATA_VR_HOT_N from EC,added un-stuffed resistor and TP for debugging use(Page 38)
B04 Added EC_WAKE_L latch circuitry for EC HIB mode support (Page 38)
B05 Changed PR229 from 1M to 100K for battery cell configuration error (Page 36)
B06 Added 4x22uF on +V1P25_KEPL (Page 43)
03/02
B07 Moved STARTUP_LATCH_SET from GPIO46 to GPIO201(Page 38)
03/04
B08 added option of either power or GND connection for SoC Ball V29, added 2 caps (Page 13)
B09 added option of either power or GND connection for SoC Ball M41,P41, added 2 caps (Page 14)
B10 added option of either power or GND connection for SoC Ball T40,P40, added 2 caps (Page 14)
B11 changed back to non-USB charger SKU (Page 28)
B12 Changed pullup on KB_BOW02_5V to 100K (Page 29)
B13 Changed pull down on KB_ACPRESENT_4137 to 1M (Page 29)
03/05
B14 added 4x1uF,6x22uF,1x10uF on DDR_V1P05A (Page 13)
B15 corrected source of power net of SoC Ball M41,P41(Page 14)
B16 unstuffed Q33,R565 stuffed R314,R188,WiFi power is connected to +V3P3A directly, not thru power gating (Page 24)
B17 unstuffed Q15, stuffed R185,R486,R498,LTE power is connected to +V3P3A directly, not thru power gating (Page 25)
B18 Changed C115 QPN (Page 25)
B19 Changed QPN of Track pad connector (Page 29)
B20 Changed power domain of G-sensor SMBUS pullup (Page 30)
B21 Added a TP for EC_GPIO12,Deleted R388 (Page 38)
B22 Removed EC_VNN_I2C3_ALERT_N from EC, added un-stuffed resistor and TP for debugging use(Page 38)
B23 separated SMBUS of BATT and Thermal IC, renamed net name ,Moved Thermal SMBUS from I2C8_CLK0 to I2C3_CLK0 (Page 38)
B24 Changed GPIO123 from EC_WAKE_L to EC_STRAP_GPIO1,Changed pullup on EC_WAKE)L to 100K,removed R337 and R341 (Page 38)
B25 unstuffed R261,LTE power is connected to +V3P3A directly, not thru power gating(Page 38)
B26 changed VDDQ_VTT enabled pin from SLP_SX to SLP_S3 (Page 31)
B27 Added 0E resistor on TOUCHPANEL_PWREN,unstuffed R512, Q15, stuffed R7,R17touch screen power is connected to +V5A directly, not thru power gating (Page 33)
B28 renamed the net name of thermal SMBUS and move the pull up to EC page (Page 33)
B29 SLP_SX related components are stuffed(Page 34)
B30 renamed the net name of Battery/Charger (Page 36)
B31 Change pullup on V5A_PWRGD from +V5A_LDO to +V5A (Page 37)
B32 Changed JP1 from 0.001 to 0.002 (Page 37)
B33 Changed pullup on V3A_PWRGD from +V3P3A_LDO to +V3P3A (Page 37)
B34 Changed 5V solution from RT7291A to RT7291E (Page 37
B35 Deleted pullup on VGG_VR_HOT_N,VNN_VR_HOT_N (Page 39,41)
B36 Added 22uF cap on +VDDQ_M0_M1_R(Page 40)
B37 Added net name VNN_RGND (Page 41)
B38 Changed the pin1 of PR161 from +V1P05A to +V1P05A_R_SOC,Changed PC176 from 1uF to 0.1uF (Page 42)
B39 Changed PC8,PC16 from 0.1uF to 0.047uF,and PC23 from 0.047uF to 0.01uF, and PR11 from 47K to 22K, PR15 from22.1K to 22K, and unstuff PR42/PC58 (Page 43)
B40 Added MOSFET on SRTCRST# and SoC_RTEST#,controllered by EC (Page 12)
03/06
B41 un-stuffed R246 (Page 9)
B42 Changed Footprint of Hole2(Page 28)
B43 Changed pullup on SPI_WP1_ME from 10K to 100K (Page 38)
B44 added pull down on VP9 JTAG_TEST_MODE, Added R513/C417 on VDD of Video codec, connnected VDD power from +V1P05A_CODEC_VDD to +V1P05A_CODEC (Page 32)
B45 stuffed level shifts for Touch screen I2C/INT signals,Q3,Q5,Q43 are stuffed, R18,R31,R403 are unstuffed (Page 35)

DOC NO.	PROJECT MODEL:	Chrome	APPROVED BY:		DATE:		Quanta Computer Inc. PROJECT : ZHR
	PART NUMBER:		DRAWING BY:		REVISON:		Change No-1

Model	Version	CHANGE LIST
ZHR/ZHRA	3A	B46 Connected Battery TEMP to charger IC present pin,and PR183 unstuffed (Page 36) B47 Changed +V1P05A sensing point of current sensor PU16 (INA219) (Page 44) 03/09 B48 Deleted TP87,TP88 (Page 9) B49 connected CORE_V1P15_S0ix,FUSE_V1P15_S0ix,VCCSRAMGEN_1P15 to +1P15A directly, and Deleted R168,R493(Page 13) B50 unstuffed R254, stuff R255 for isolate SERIRQ from TPM (Page 27) B51 Changed and stuffed ESD solution from Varistors to TVS for USB3 port (Page 28) B52 added back and unstuffed the USB charger, keep reserving this feature, and Added option 0E on USB I/F, default stuff them for non-USB charger(Page 28) B53 Stuffed C242, unstuffed C268 ,connected R92 to +V1P05A_CODEC(Page 32) B54 changed power net of these caps to +V1P05A_CODEC_VDD (Page 32) B55 renamed the net name of thermal SMBUS and move the pull up to EC page (Page 33) 03/10 B56 Added offpage on SMBUS for external level shifter(Page 16) B57 added Discharge circuitry on +VSDIO (Page 19) B58 Swap pin of L7 for layout and Swap pin5/6 of U29 for layout (Page 28) B59 Added a diode for protection of draw current from sysytem to servo board (Page 30) B60 added OR gate for VSA_EN(Page 31) B61 Added level shifter on CLKREQ of Video codec;unstuffed R96,R100,R91,R88;Changed R119/R128 from 5% to 1% tolerant resistors (Page 32) B62 Changed drain PU of SLP_S3/SLP_S4 from +V3P3A_PRIME to +V3P3A for avoiding the glitch(Page 34) B63 Added level shifter on SMBUS from SoC to XDP, it will be un-stuffed in MP(Page 35) B64 Added Discharge Circuit for +V1P25_KEPL (Page 41) 03/11 B65 changed connection of KB ESD power to +VSA(Page 29) B66 renamed EC_SMI_3P3_L ,EC_SOC_WAKE_SCI_N,EC_KBD_IRQ#,PCH_WAKE_EC_L,EC_REST_L for added level shifters (Page 30) B67 Added 5 FETs as level shifters on EC OD GPIOs (Page 34) B68 stuffed PR8, and unstuffed PC12 to disable +VSA_LDO1 (Page 37) B69 Changed Acer thermal protection circuit--> changed the pullup power source of input pins of OP AMP from +VSA_LDO to +V3P3A_LDO, added option for them, default is stuffed for +V3P3A_LDO(Page 43) 03/12 B70 stuffed R292/R261 for making connection of SPI_WP/SPI_HOLE from servo board(Page 9) B71 added KBD_ALERT pin to notify SoC to lock ME FW Keep reserving this feature in DVT build (Page 10) B72 unstuffed all VNN related components due to all SKUs in DVT1 are Fixed VNN(Page 12) B73 Changed QPN of eMMC from samsung32G to Hynix32G(Page 19) B74 deleted R138 (Page 23) B75 unstuffed R788/R791/R792/R793/U37/C403 for USB charger support(Page 28) B76 added KBD_ALERT pin to notify SoC to lock ME FW (Page 30) B77 unstuffed all VNN related components due to all SKUs in DVT1 are Fixed VNN, and stuff the option of Fixed VNN (Page 31) B78 unstuffed R169,R171, changed the value of R232/R438 for Fixed VNN SKU (Page 31) B79 unstuffed R180,R186,R175,changed the value of R230/R427 for Fixed VNN SKU(Page 31) B80 unstuffed all VNN related components due to all SKUs in DVT1 are Fixed VNN, and stuff the option of Fixed VNN(Page 41,44) B81 Added PR238 0E on VR_ALW_EN (Page 43) B82 Added antuffed cap on pin4 of PU1(Page 43) 03/13 B83 Changed 620 ohm to 619 ohm for PUR request(Page 22)
	3B	03/27 C01 Changed some of 0 ohm to short pad 04/16 C02 Changed pullup on +VSDIO power switch enabled pin to +V3P3A_PRIME for SoC G3 leakage,Changed C419 from 0.01uF to 0.1uF (Page 19) C03 Added VP9_CODEC_RESET# to reset VP9 (Page 30, 32) C04 EC SMBUS and I2C PUs changed to 10K (Page 30) C05 Connected EC_WIB_L between EC and WaKe circuit (Page 29,31) C06 Changed from OR Gate to diode OR for VSA_EN(Page 31) C07 renamed GND_H12 to KEPL_GND,Added TP on VP9 UART and SPI,Added 0E options , but un-stuffed on VDD33_USB,DVDD_USB,VP_USB (Page 32) C08 Changed VP9 X'tal C_load from DGND to KEPL_GND,Changed VP9 X'tal C_load to 33pF, it would be fine tuned on MP stuffed board(Page 32) C09 Added +VSS options to Touch screen(Page 33) C10 Provided option to pullup PLTRST# to +V3P3S, Changed pullup power of XDP SMBUS from +V3P3A to +V3P3S (Page 34,35) 04/20 C11 moved SDCARD_WP from GPIO_SUS5 to I2C_6_DAT, renamed the net of GPIO_SUS5 and made Q95 as stuff to enable ME lock feature (Page 10,23) C12 moved SDCARD_WP to I2C_6_DAT, made option of EC I2C as unstuff (Page 10) C13 added 100 ohm in series with +VNN_SENSEP(Page 12) C14 made C409,C408,C410,C414 as un-stuffed (Page 13) C15 Before making conclusion for power gate of WiFi to be stuffed or not,in order to prevent the leakage from this circuit, made the R201,R494,R495 as unstuff(Page 24) C16 Before making conclusion for power gate of LTE to be stuffed or not,in order to prevent the leakage from this circuit, made the R207,R172,R498 as unstuff(Page 25) C17 disconnected AGND between Audio code to CH13 (Page 26) C18 Changed TPM power domain from S0 to S5 power for leakage issue (made R249 as unstuff and R240 as stuff, and made a dedicated TPM PLTRST#(Page 27) C19 deleted AGND, connected to DGND directly thru 0 ohm resistor for recording noise, adjusted pin mapping of audio signals for adding one more GND, made GND option on the pin of +V3P3A, default on pin19 is power pin(Page 27) C20 added diode on EC_RST# to prevent back drive from HW RST IC to EC (Page 29) C21 Changed Board_ID PU/PD≈ from 3K to 100K, removed BATT_IN# connection to EC GPIO62, made a disconnection on CORE_PWROK_R to EC (Page 30) C22 Simplified VP9 CLKREQ level shifter (there has internal pull up in VP9) (Page 32) C23 Added diode and removed PU on GYRO_INT1 and GYRO_INT2, Added option to +V3P3A for Gensor power(Page 33) C24 made option of LS on EC I2C as unstuff, added a level shifter with gate at 1.8S added for TPM reset and added 0 ohm option between TPM_PLTRST# and PLTRST# (Page 34) C25 Changed pullup power of XDP SMBUSback to V3P3A, and Touch INT connected to GPIO_SUS1(Page 35) 04/22 C26 added pullup R591 at 1.8V,made the pull up at 3.3V unstuffed, Changed Q26 from 2N7002 to PJA138K for changing Vg from 3.3V to 1.8V(Page 9) C27 changed R291 from 1K to 10K (Page 28) C28 unstuffed R296 due to added pullup at 1.8V closed to SPI ROM, added option on EC SPI WP, SPI_WP_HE is connected to screw directly, let it NC from screw(Page 30) C29 stuffed R584 for ME lock enabling, change PU on G-sensor I2C to +V3P3A_EC, made them un-stuffed, they are pulled up at the other side of level shifter(Page 30) C30 added EC_ACDET_CTRL on GPIO50 (Page 30) C31 Added level shifters option on Gensor I2C if sensors need to work in S3/S5, default design is working on S0 only as Cyan pre-EVT (Page 35) C32 changed FR230 from 10K to 100K and PR181 from 1.62K to 10.2K (Page 36) C33 Changed Charger soft start circuitry using P MOS, added AC detect disable circuit to minimise the power onsumption in S5(Page 36) C34 added AC DET Disable circuit which is used to minimise the power consumption in S5 in DC mode (Page 36) C35 changed PR94/PR307 from 10K to 100K, and changed the net +VSA in VCC page to +VCC_VCC,changed pin4 of VCC0 from +VSA to +V5S,PR126 from 0.01ohm to 0 ohm(Page 38) C36 added 0.1uF on VCC_EN, and changed one of decoupling caps of +VCC from 330uF_7343 to 22uF MLCC, made the MLCC as un-stuffed (Page 38) C37 changed +VSA in VGG page to +VGG_VCC, added 0.1uF on VGG_EN,changed PR55/PR54 from 10K to 100K, changed pin4 of VGG from +VSA to +V5S,PR32 from 0.01 to 0 (Page 39) C38 changed the decoupling caps of +VGG from 330uF_7343 to 22uF MLCC (Page 39) C39 changed PR282/PR198 from 10K to 100K, Added offset circuit to the VNNSENSEP and added offset circuit to the VNN to support +VNN voltage to min in S3 (Page 41) 04/24 C40 added R674 for layout (Page 26) C41 changed EC symbol to correct GPIO134 (Page 30) C42 swapped TOUCHPANEL_PWREN and EC_ACDET_CTRL,removed R497 (Page 30) C43 Changed PF of PQ23,PQ24 for layout estimation ,Changed the soft start circuit back to pre-EVT design(Page 36) C44 Changed PQ22 to AO3409 P-MOS (Page 41) 04/27 C45 Changed Gate power of HDMI level shifters from +V1P8S to +V1P8S for leakage issue(Page 22) C46 Changed PD of EC_WIB_L from 10K to 100K (Page 31) 04/28 C47 Deleted 0 ohm of I2C_6_SCL/ I2C_6_SDA (Page 10) C48 Deleteid APS related circuit (Page 16) C49 stuffed all caps on SD3 interface for EMI request, Deleted R205,R206,R198,R194 (Page 19) C50 unstuffed R573 R570, there have internal PUs in SoC (Page 27) C51 changed pullup of R788 and R790 from +V3P3A_EC to +V3P3A for layout (Page 28) C52 changed PU option of G-Sensor I2C from +V3P3S to +V3P3A, disconnected I2C between EC and SoC (Page 30) C53 corrected the mark of value of R9,R22,R383 as to be un-stuffed, changed power source of G-sensor from "S" to "A"(Page 33) C54 Deleted level shifters between EC to SoC (Page 34) C55 Deleted level shifters of G-sensor I2C, default power source of G-sensor changed from "S" to "A"(Page 35) 04/30 C56 changed Footprint of L2/L3 (Page 28) C57 added the gate for disabling Trackpad INT during S3 if the lid angle>180, made un-stuff before EC is not ready (Page 29) C58 replaced EC_ACDET_CTRL with TP_INT_DISABLE for disabling Trackpad INT during S3 in yoga mode (Page 30) C59 deleted AC DET Disable circuit (Page 36) C60 Changed PQ22 pin1 from +V3P3A to +V3P3A_PRIME(Page 41) 05/04 C61 changed C load of Y2/Y3 from 18pF to 15pF(Page 10, 12) C62 deleted option R251 of ball V29 to be grounded, deleted option R650 of ball M41/P41 to be grounded (Page 14) C63 NC pin35 of Daughter board CONN, changed PP of Hole10 (Page 27, 28) C64 stuffed PD 8417 on TRACKPAD_PWREN (Page 29) C65 added 0E option on GS2 INT, diode D28 is un-stuff, added 0E option on GS1 INT, diode D27 is un-stuffed (Page 33) C66 deleted PC258,PC260, added back back caps 330uF/7343 (Page 39) C67 added 100k PD on pin2 of PQ22 , added 0.1uF on pin2 of PQ21(Page 41) 05/05 C68 stuffed variable VNN related part, R140 (Page 12) C69 Added PA01 (Page 28) C70 changed PU PWR of COREPWROK from +V3P3A to +V3P3A_PRIME(Page 31) C71 For variable VNN support, stuffed R171,R169, changed R232, R438 from 200 ohm to 301 ohm, stuffed R180,R186, changed R230, R427 from 301 ohm to 453 ohm, stuffed R175,stuffed R443, R468, R497,Q50, unstuffed R452,R489,Q53(Page 31) C72 changed PU PWR of ALL_SYS_PWRGD from +V3P3A to +V3P3S and added option PU to +V3P3A_PRIME (Page 31) C73 changed back to double FETs LS for VP9 CLK REQ (Page 32) C74 changed PU PWR of PLTRST from +V3P3A to +V3P3A_PRIME (Page 34) C75 Changed PR242 from 392K to 430K, PR247 from 110K to 100K, changed PR174 from 4.02k to 0 ohm (Page 36) C76 changed PU PWR of VCC_PWRGD from +V3P3A to +VCC_VCC thru 20K (Page 38) C77 unstuffed PC259, PC262, changed PU PWR of VGG_PWRGD from +V3P3A to +VGG_VCC thru 20K(Page 39) C78 unstuffed all parts of VNN OFFSET BACKUP CIRCUIT, Changed PR67 to 100 ohm, made double star symbol as un-stuffed even on Dynamic VNN SKU (Page 41) C79 unstuffed PR248 on dynamic VNN SKU,changed PR241 from 100K to 115K , BOM change for variable VNN support(Page 41) C80 BOM change for variable VNN support, stuffed RC232,PC233,PU23(Page 41) 05/06 C81 changed QPN of U1011(Page 31) C82 changed QPN of PU3 from RT9053 to RT9187 (Page 43) 05/07 C83 changed Footprint of L2/L3 (Page 28) C84 changed R356 to 1M (Page 29) C85 stuffed Q96 for enabling this feature in EVT, added PD for default setting and added 360@ in front of value for BOM option for convertible SKU only (Page 29) C86 changed connection of output of U1810, stuffed R236 (Page 31) C87 revised the voltage rating of PC276 from 25V to 50V(Page 36) C88 changed PQ22 to BSS84 (Page 41)
	3C	07/03 D01 Changed some of 0 ohm to short pad D02 for DVT, changed board ID from 010 to 011,stuffed R612 and un-stuffed R616 (Page 30) D03 Changed pullups of Battery SMBUS to 4.7K (Page 30) D04 Changed PR241 to 470K which was stuffed in EVT build already (Page 41) D05 Added power option for thermal protector and stuff PR250 as default (Page 43) 07/05 D06 Added option resistors on LID_OPEN_OUT2_L_CONN for MIC detection issue, stuffing R675 as default (Page 27) D07 added option path on Headset jack detection,stuffed double invertor as default, unstuffed Q38 (Page 35) 07/09 D08 Stuffed R454,R184 and unstuffed R460,R178 for DVT main SKU configuration (Page 10) D09 added ESD protection on TRACKPAD_INT#,EDP_HPD,PCH_DISP_ON,RF_EN,LID_OPEN_OUT1_R lines (Page 10,20,24,30) D10 Changed Footprint of removing mylar for factory side request (Page 27) D11 Changed X'tal of EC chip from 12.5pF to 9pF,the C load C360,C365 are changed accordingly (Page 30) D12 Changed R618 from 0 ohm to 2.2 ohm as ESD protection on EC power line (Page 30) D13 changed power source of touch screen from +V5A to +V5S for S3 power saving, (Page 33) D14 Changed QPN of 3V VR (Page 37) 07/13 D15 Changed resistors value of voltage divider R404,R468, R55,R60 for S3 power saving,Changed LTE related components to "no stuff" (Page 25,35) D16 Changed R439 from 10K to 100K for S3 power saving (Page 35) D17 changed PR35 to 1.05K and PR34 to 1.15K for OCP increasing (Page 39) D18 Changed PR241 to 300K to get more power saving (Page 41) 07/14 D19 changed resistors value of RAMID from 10K to 100K for power saving ,Changed Hole4 Footprint (Page 10, 28) 07/16 D20 Added PAD9-15 as ESD protection,Changed Hole4 Footprint (Page 28) D21 added +V5S_VGG power switch for meeting RTB175A power sequence (Page 39) 07/17 D22 Changed Q39 to PJA138K (Page 29) D23 Changed PU26 to TPS22930 (Page 39) 07/29 D24 changed R539 from 10 ohm to 200 ohm, and re-wired pin14 of header to HW reset IC,making a connection change on EC_RST# for Auto recovery mode issue (Page 21,29) D25 unstuffed R188,Q16,R197,Q57,Q58 after the validation of S3 battery life is done and no issue on WiFi (Page 24) D26 added PS circuitry for TS power if no separated PS pin is assigned (Page 33) 07/30 D27 added three pathes to reset touch screen, D29 is stuffed by default,changed power source to the output of load switch (Page 33) D28 added one more path of touch power by additional load switch , it is stuffed by default (Page 33) 07/31 D29 unstuffed D29,R247 and R7,stuffed back R17 as by default (Page 33)
	3D	08/18 E01 Changed some of 0 ohm to short pad