1. Schematic Page Description :

ZHQ/Hugo Schematic Ver : 1.0

I2C table

Function	Channel	Read	Write
Touch pad	I2C0	0x67	
Audio codec	I2C1	0x21	0x20
Light sensor	I2C4		

Function	Channel
PP3300_DSW	0x42
PP5000	0x41
PP1350	0x49
PP1050_PCH	0x43
PP1000_PCH	0x47

SMBus table

Function	Channel	Address
Battery	SMB0	
Thermal	SMB2	0x4C

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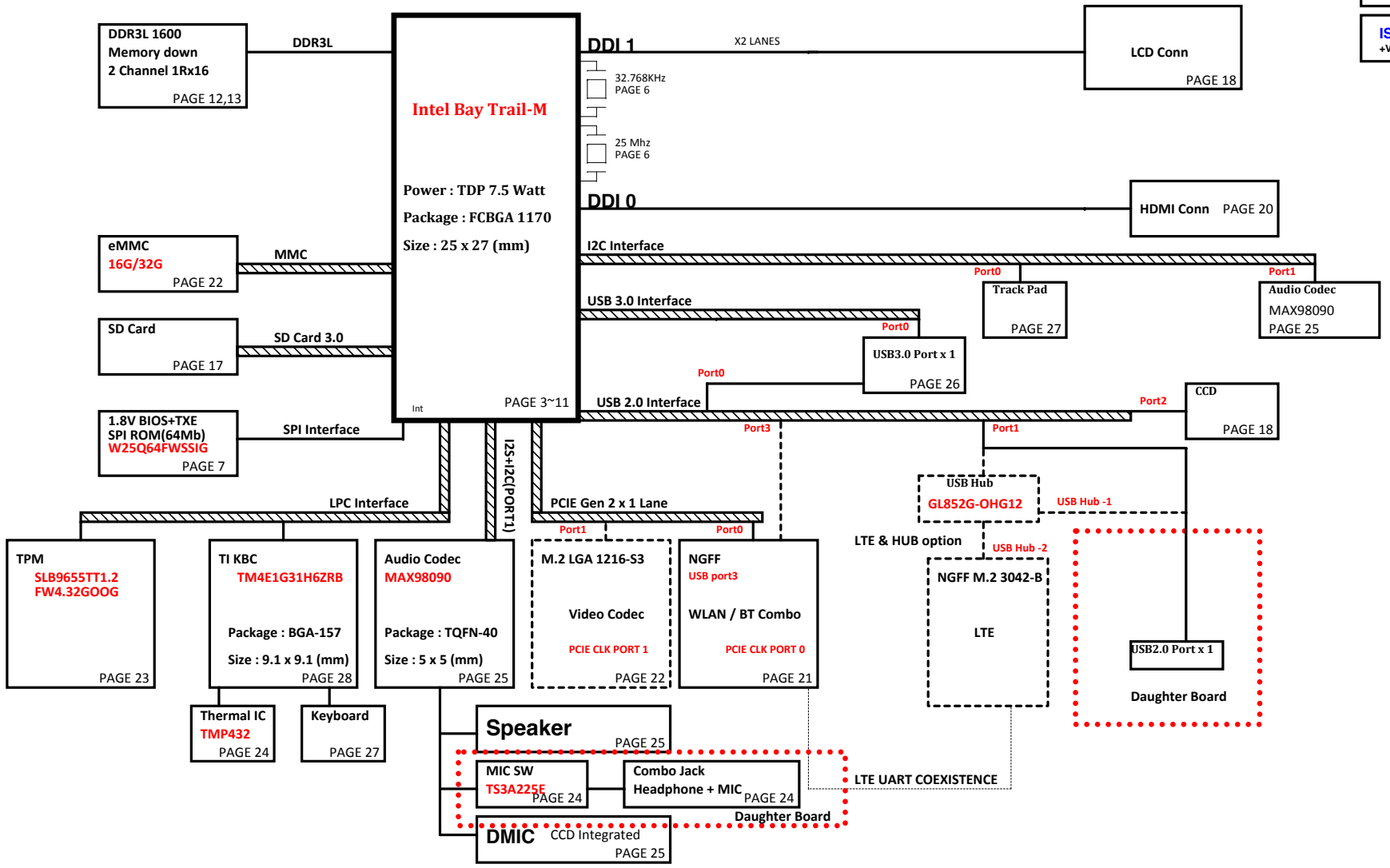
ZHQ/Hugo

Intel Bay Trail-M Platform Block Diagram

SKUA DC N2820
AJSR1SGUT03 --CPU(1170P)N2820 2.13G SR1SG(FCBGA)STNBSQ

BQ24715 Batery Charger	TPS51216 PP1350
TPS51225 PP3300_DSW/PP5000	NB671GQ-Z PP1000_PCH
ISL95833HRTZ-T +VCC_CORE/+VCC_GFX	Thermal Protection Discharger



BOM value option:
SX@ => SOiX
NSX@=>none SOiX
HUB@=>USB HUB
3G@ => LTE
GD@ =>Google debug

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	Block Diagram	1A

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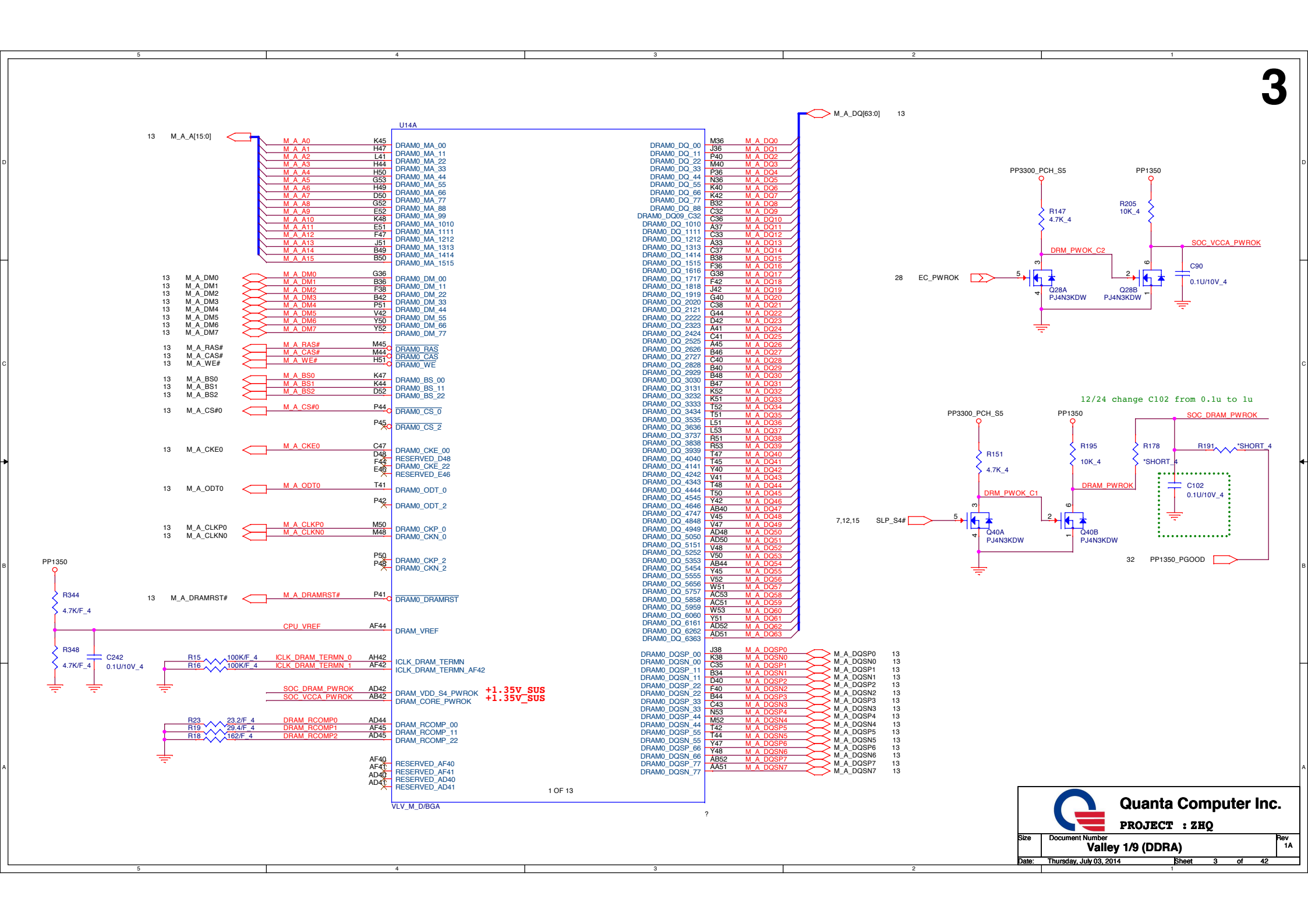
3
U14A
13 M_A_A[15:0]
M_A_A0 K45 DRAM0_MA_00
M_A_A1 H47 DRAM0_MA_11
M_A_A2 L41 DRAM0_MA_22
M_A_A3 H44 DRAM0_MA_33
M_A_A4 H50 DRAM0_MA_44
M_A_A5 G53 DRAM0_MA_55
M_A_A6 H49 DRAM0_MA_66
M_A_A7 D50 DRAM0_MA_77
M_A_A8 G52 DRAM0_MA_88
M_A_A9 E52 DRAM0_MA_99
M_A_A10 K48 DRAM0_MA_1010
M_A_A11 E51 DRAM0_MA_1111
M_A_A12 F47 DRAM0_MA_1212
M_A_A13 J51 DRAM0_MA_1313
M_A_A14 B49 DRAM0_MA_1414
M_A_A15 B50 DRAM0_MA_1515
13 M_A_DM0 M_A_DM0 G36 DRAM0_DM_00
13 M_A_DM1 M_A_DM1 B36 DRAM0_DM_11
13 M_A_DM2 M_A_DM2 F38 DRAM0_DM_22
13 M_A_DM3 M_A_DM3 B42 DRAM0_DM_33
13 M_A_DM4 M_A_DM4 P51 DRAM0_DM_44
13 M_A_DM5 M_A_DM5 V42 DRAM0_DM_55
13 M_A_DM6 M_A_DM6 Y50 DRAM0_DM_66
13 M_A_DM7 M_A_DM7 Y52 DRAM0_DM_77
13 M_A_RAS# M_A_RAS# M45 DRAM0_RAS
13 M_A_CAS# M_A_CAS# M44 DRAM0_CAS
13 M_A_WE# M_A_WE# H51 DRAM0_WE
13 M_A_BS0 M_A_BS0 K47 DRAM0_BS_00
13 M_A_BS1 M_A_BS1 K44 DRAM0_BS_11
13 M_A_BS2 M_A_BS2 D52 DRAM0_BS_22
13 M_A_CS#0 M_A_CS#0 P44 DRAM0_CS_0
P45 DRAM0_CS_2
13 M_A_CKE0 M_A_CKE0 C47 DRAM0_CKE_00
D48 RESERVED_D48
F43 DRAM0_CKE_22
E46 RESERVED_E46
13 M_A_ODT0 M_A_ODT0 T41 DRAM0_ODT_0
P42 DRAM0_ODT_2
13 M_A_CLKP0 M_A_CLKP0 M50 DRAM0_CKP_0
13 M_A_CLKN0 M_A_CLKN0 M48 DRAM0_CKN_0
P50 DRAM0_CKP_2
P48 DRAM0_CKN_2
13 M_A_DRAMRST# M_A_DRAMRST# P41 DRAM0_DRAMRST
CPU_VREF AF44 DRAM_VREF
R15 100K/F_4 ICLK_DRAM_TERMN_0 AH42 ICLK_DRAM_TERMN
R16 100K/F_4 ICLK_DRAM_TERMN_1 AF42 ICLK_DRAM_TERMN_AF42
SOC_DRAM_PWROK AD42 DRAM_VDD_S4_PWROK +1.35V_SUS
SOC_VCCA_PWROK AB42 DRAM_CORE_PWROK +1.35V_SUS
R23 23.2/F_4 DRAM_RCOMP0 AD44 DRAM_RCOMP_00
R19 29.4/F_4 DRAM_RCOMP1 AF45 DRAM_RCOMP_11
R18 162/F_4 DRAM_RCOMP2 AD45 DRAM_RCOMP_22
AF40 RESERVED_AF40
AF41 RESERVED_AF41
AD40 RESERVED_AD40
AD41 RESERVED_AD41
1 OF 13
VLV_M_D/BGA
PP1350
R344 4.7K/F_4
R348 4.7K/F_4
C242 0.1U/10V_4
M_A_DQ[63:0] 13
DRAM0_DQ_00 M36 M_A_DQ0
DRAM0_DQ_11 J36 M_A_DQ1
DRAM0_DQ_22 P40 M_A_DQ2
DRAM0_DQ_33 M40 M_A_DQ3
DRAM0_DQ_44 P36 M_A_DQ4
DRAM0_DQ_55 N36 M_A_DQ5
DRAM0_DQ_66 K40 M_A_DQ6
DRAM0_DQ_77 K42 M_A_DQ7
DRAM0_DQ_88 B32 M_A_DQ8
DRAM0_DQ09_C32 C32 M_A_DQ9
DRAM0_DQ_1010 C36 M_A_DQ10
DRAM0_DQ_1111 A37 M_A_DQ11
DRAM0_DQ_1212 C33 M_A_DQ12
DRAM0_DQ_1313 A33 M_A_DQ13
DRAM0_DQ_1414 C37 M_A_DQ14
DRAM0_DQ_1515 B38 M_A_DQ15
DRAM0_DQ_1616 F36 M_A_DQ16
DRAM0_DQ_1717 G38 M_A_DQ17
DRAM0_DQ_1818 F42 M_A_DQ18
DRAM0_DQ_1919 J42 M_A_DQ19
DRAM0_DQ_2020 G40 M_A_DQ20
DRAM0_DQ_2121 C38 M_A_DQ21
DRAM0_DQ_2222 G44 M_A_DQ22
DRAM0_DQ_2323 D42 M_A_DQ23
DRAM0_DQ_2424 A41 M_A_DQ24
DRAM0_DQ_2525 C41 M_A_DQ25
DRAM0_DQ_2626 A45 M_A_DQ26
DRAM0_DQ_2727 B46 M_A_DQ27
DRAM0_DQ_2828 C40 M_A_DQ28
DRAM0_DQ_2929 B40 M_A_DQ29
DRAM0_DQ_3030 B48 M_A_DQ30
DRAM0_DQ_3131 B47 M_A_DQ31
DRAM0_DQ_3232 K52 M_A_DQ32
DRAM0_DQ_3333 K51 M_A_DQ33
DRAM0_DQ_3434 T52 M_A_DQ34
DRAM0_DQ_3535 T51 M_A_DQ35
DRAM0_DQ_3636 L51 M_A_DQ36
DRAM0_DQ_3737 L53 M_A_DQ37
DRAM0_DQ_3838 R51 M_A_DQ38
DRAM0_DQ_3939 R53 M_A_DQ39
DRAM0_DQ_4040 T47 M_A_DQ40
DRAM0_DQ_4141 T45 M_A_DQ41
DRAM0_DQ_4242 Y40 M_A_DQ42
DRAM0_DQ_4343 V41 M_A_DQ43
DRAM0_DQ_4444 T48 M_A_DQ44
DRAM0_DQ_4545 T50 M_A_DQ45
DRAM0_DQ_4646 Y42 M_A_DQ46
DRAM0_DQ_4747 AB40 M_A_DQ47
DRAM0_DQ_4848 V45 M_A_DQ48
DRAM0_DQ_4949 V47 M_A_DQ49
DRAM0_DQ_5050 AD48 M_A_DQ50
DRAM0_DQ_5151 AD50 M_A_DQ51
DRAM0_DQ_5252 V48 M_A_DQ52
DRAM0_DQ_5353 V50 M_A_DQ53
DRAM0_DQ_5454 AB44 M_A_DQ54
DRAM0_DQ_5555 Y45 M_A_DQ55
DRAM0_DQ_5656 V52 M_A_DQ56
DRAM0_DQ_5757 W51 M_A_DQ57
DRAM0_DQ_5858 AC53 M_A_DQ58
DRAM0_DQ_5959 AC51 M_A_DQ59
DRAM0_DQ_6060 W53 M_A_DQ60
DRAM0_DQ_6161 Y51 M_A_DQ61
DRAM0_DQ_6262 AD52 M_A_DQ62
DRAM0_DQ_6363 AD51 M_A_DQ63
DRAM0_DQSP_00 J38 M_A_DQSP0 M_A_DQSP0 13
DRAM0_DQSN_00 K38 M_A_DQSN0 M_A_DQSN0 13
DRAM0_DQSP_11 C35 M_A_DQSP1 M_A_DQSP1 13
DRAM0_DQSN_11 B34 M_A_DQSN1 M_A_DQSN1 13
DRAM0_DQSP_22 D40 M_A_DQSP2 M_A_DQSP2 13
DRAM0_DQSN_22 F40 M_A_DQSN2 M_A_DQSN2 13
DRAM0_DQSP_33 B44 M_A_DQSP3 M_A_DQSP3 13
DRAM0_DQSN_33 C43 M_A_DQSN3 M_A_DQSN3 13
DRAM0_DQSP_44 N53 M_A_DQSP4 M_A_DQSP4 13
DRAM0_DQSN_44 M52 M_A_DQSN4 M_A_DQSN4 13
DRAM0_DQSP_55 T42 M_A_DQSP5 M_A_DQSP5 13
DRAM0_DQSN_55 T44 M_A_DQSN5 M_A_DQSN5 13
DRAM0_DQSP_66 Y47 M_A_DQSP6 M_A_DQSP6 13
DRAM0_DQSN_66 Y48 M_A_DQSN6 M_A_DQSN6 13
DRAM0_DQSP_77 AB52 M_A_DQSP7 M_A_DQSP7 13
DRAM0_DQSN_77 AA51 M_A_DQSN7 M_A_DQSN7 13
?
PP3300_PCH_S5
PP1350
R147 4.7K_4
R205 10K_4
DRM_PWOK_C2
SOC_VCCA_PWROK
C90 0.1U/10V_4
28 EC_PWROK
Q28A PJ4N3KDW
Q28B PJ4N3KDW
12/24 change C102 from 0.1u to 1u
PP3300_PCH_S5
PP1350
SOC_DRAM_PWROK
R151 4.7K_4
R195 10K_4
R178 *SHORT_4
R191 *SHORT_4
DRAM_PWROK
DRM_PWOK_C1
C102 0.1U/10V_4
7,12,15 SLP_S4#
Q40A PJ4N3KDW
Q40B PJ4N3KDW
32 PP1350_PGOOD
Quanta Computer Inc.
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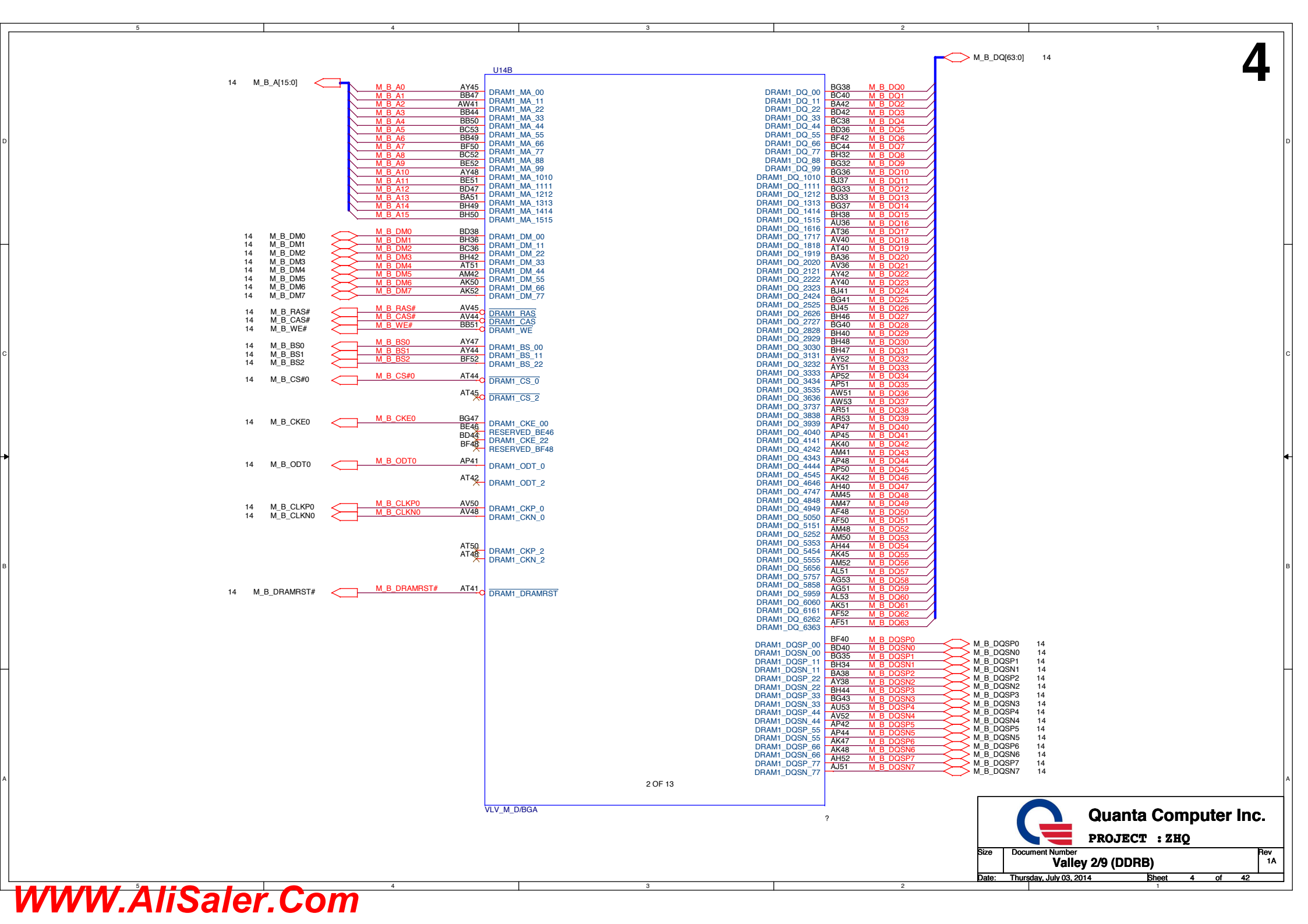
4
U14B
14 M_B_A[15:0]
M_B_A0 AY45
M_B_A1 BB47
M_B_A2 AW41
M_B_A3 BB44
M_B_A4 BB50
M_B_A5 BC53
M_B_A6 BB49
M_B_A7 BF50
M_B_A8 BC52
M_B_A9 BE52
M_B_A10 AY48
M_B_A11 BE51
M_B_A12 BD47
M_B_A13 BA51
M_B_A14 BH49
M_B_A15 BH50
DRAM1_MA_00
DRAM1_MA_11
DRAM1_MA_22
DRAM1_MA_33
DRAM1_MA_44
DRAM1_MA_55
DRAM1_MA_66
DRAM1_MA_77
DRAM1_MA_88
DRAM1_MA_99
DRAM1_MA_1010
DRAM1_MA_1111
DRAM1_MA_1212
DRAM1_MA_1313
DRAM1_MA_1414
DRAM1_MA_1515
14 M_B_DM0
14 M_B_DM1
14 M_B_DM2
14 M_B_DM3
14 M_B_DM4
14 M_B_DM5
14 M_B_DM6
14 M_B_DM7
M_B_DM0 BD38
M_B_DM1 BH36
M_B_DM2 BC36
M_B_DM3 BH42
M_B_DM4 AT51
M_B_DM5 AM42
M_B_DM6 AK50
M_B_DM7 AK52
DRAM1_DM_00
DRAM1_DM_11
DRAM1_DM_22
DRAM1_DM_33
DRAM1_DM_44
DRAM1_DM_55
DRAM1_DM_66
DRAM1_DM_77
14 M_B_RAS#
14 M_B_CAS#
14 M_B_WE#
M_B_RAS# AV45
M_B_CAS# AV44
M_B_WE# BB51
DRAM1_RAS
DRAM1_CAS
DRAM1_WE
14 M_B_BS0
14 M_B_BS1
14 M_B_BS2
M_B_BS0 AY47
M_B_BS1 AY44
M_B_BS2 BF52
DRAM1_BS_00
DRAM1_BS_11
DRAM1_BS_22
14 M_B_CS#0
M_B_CS#0 AT44
DRAM1_CS_0
AT45
DRAM1_CS_2
14 M_B_CKE0
M_B_CKE0 BG47
BE46
BD44
BF48
DRAM1_CKE_00
RESERVED_BE46
DRAM1_CKE_22
RESERVED_BF48
14 M_B_ODT0
M_B_ODT0 AP41
DRAM1_ODT_0
AT42
DRAM1_ODT_2
14 M_B_CLKP0
14 M_B_CLKN0
M_B_CLKP0 AV50
M_B_CLKN0 AV48
DRAM1_CKP_0
DRAM1_CKN_0
AT50
AT48
DRAM1_CKP_2
DRAM1_CKN_2
14 M_B_DRAMRST#
M_B_DRAMRST# AT41
DRAM1_DRAMRST
2 OF 13
VLV_M_D/BGA
?
M_B_DQ[63:0] 14
DRAM1_DQ_00 BG38 M_B_DQ0
DRAM1_DQ_11 BC40 M_B_DQ1
DRAM1_DQ_22 BA42 M_B_DQ2
DRAM1_DQ_33 BD42 M_B_DQ3
DRAM1_DQ_44 BC38 M_B_DQ4
DRAM1_DQ_55 BD36 M_B_DQ5
DRAM1_DQ_66 BF42 M_B_DQ6
DRAM1_DQ_77 BC44 M_B_DQ7
DRAM1_DQ_88 BH32 M_B_DQ8
DRAM1_DQ_99 BG32 M_B_DQ9
DRAM1_DQ_1010 BG36 M_B_DQ10
DRAM1_DQ_1111 BJ37 M_B_DQ11
DRAM1_DQ_1212 BG33 M_B_DQ12
DRAM1_DQ_1313 BJ33 M_B_DQ13
DRAM1_DQ_1414 BG37 M_B_DQ14
DRAM1_DQ_1515 BH38 M_B_DQ15
DRAM1_DQ_1616 AU36 M_B_DQ16
DRAM1_DQ_1717 AT36 M_B_DQ17
DRAM1_DQ_1818 AV40 M_B_DQ18
DRAM1_DQ_1919 AT40 M_B_DQ19
DRAM1_DQ_2020 BA36 M_B_DQ20
DRAM1_DQ_2121 AV36 M_B_DQ21
DRAM1_DQ_2222 AY42 M_B_DQ22
DRAM1_DQ_2323 AY40 M_B_DQ23
DRAM1_DQ_2424 BJ41 M_B_DQ24
DRAM1_DQ_2525 BG41 M_B_DQ25
DRAM1_DQ_2626 BJ45 M_B_DQ26
DRAM1_DQ_2727 BH46 M_B_DQ27
DRAM1_DQ_2828 BG40 M_B_DQ28
DRAM1_DQ_2929 BH40 M_B_DQ29
DRAM1_DQ_3030 BH48 M_B_DQ30
DRAM1_DQ_3131 BH47 M_B_DQ31
DRAM1_DQ_3232 AY52 M_B_DQ32
DRAM1_DQ_3333 AY51 M_B_DQ33
DRAM1_DQ_3434 AP52 M_B_DQ34
DRAM1_DQ_3535 AP51 M_B_DQ35
DRAM1_DQ_3636 AW51 M_B_DQ36
DRAM1_DQ_3737 AW53 M_B_DQ37
DRAM1_DQ_3838 AR51 M_B_DQ38
DRAM1_DQ_3939 AR53 M_B_DQ39
DRAM1_DQ_4040 AP47 M_B_DQ40
DRAM1_DQ_4141 AP45 M_B_DQ41
DRAM1_DQ_4242 AK40 M_B_DQ42
DRAM1_DQ_4343 AM41 M_B_DQ43
DRAM1_DQ_4444 AP48 M_B_DQ44
DRAM1_DQ_4545 AP50 M_B_DQ45
DRAM1_DQ_4646 AK42 M_B_DQ46
DRAM1_DQ_4747 AH40 M_B_DQ47
DRAM1_DQ_4848 AM45 M_B_DQ48
DRAM1_DQ_4949 AM47 M_B_DQ49
DRAM1_DQ_5050 AF48 M_B_DQ50
DRAM1_DQ_5151 AF50 M_B_DQ51
DRAM1_DQ_5252 AM48 M_B_DQ52
DRAM1_DQ_5353 AM50 M_B_DQ53
DRAM1_DQ_5454 AH44 M_B_DQ54
DRAM1_DQ_5555 AK45 M_B_DQ55
DRAM1_DQ_5656 AM52 M_B_DQ56
DRAM1_DQ_5757 AL51 M_B_DQ57
DRAM1_DQ_5858 AG53 M_B_DQ58
DRAM1_DQ_5959 AG51 M_B_DQ59
DRAM1_DQ_6060 AL53 M_B_DQ60
DRAM1_DQ_6161 AK51 M_B_DQ61
DRAM1_DQ_6262 AF52 M_B_DQ62
DRAM1_DQ_6363 AF51 M_B_DQ63
DRAM1_DQSP_00 BF40 M_B_DQSP0 M_B_DQSP0 14
DRAM1_DQSN_00 BD40 M_B_DQSN0 M_B_DQSN0 14
DRAM1_DQSP_11 BG35 M_B_DQSP1 M_B_DQSP1 14
DRAM1_DQSN_11 BH34 M_B_DQSN1 M_B_DQSN1 14
DRAM1_DQSP_22 BA38 M_B_DQSP2 M_B_DQSP2 14
DRAM1_DQSN_22 AY38 M_B_DQSN2 M_B_DQSN2 14
DRAM1_DQSP_33 BH44 M_B_DQSP3 M_B_DQSP3 14
DRAM1_DQSN_33 BG43 M_B_DQSN3 M_B_DQSN3 14
DRAM1_DQSP_44 AU53 M_B_DQSP4 M_B_DQSP4 14
DRAM1_DQSN_44 AV52 M_B_DQSN4 M_B_DQSN4 14
DRAM1_DQSP_55 AP42 M_B_DQSP5 M_B_DQSP5 14
DRAM1_DQSN_55 AP44 M_B_DQSN5 M_B_DQSN5 14
DRAM1_DQSP_66 AK47 M_B_DQSP6 M_B_DQSP6 14
DRAM1_DQSN_66 AK48 M_B_DQSN6 M_B_DQSN6 14
DRAM1_DQSP_77 AH52 M_B_DQSP7 M_B_DQSP7 14
DRAM1_DQSN_77 AJ51 M_B_DQSN7 M_B_DQSN7 14
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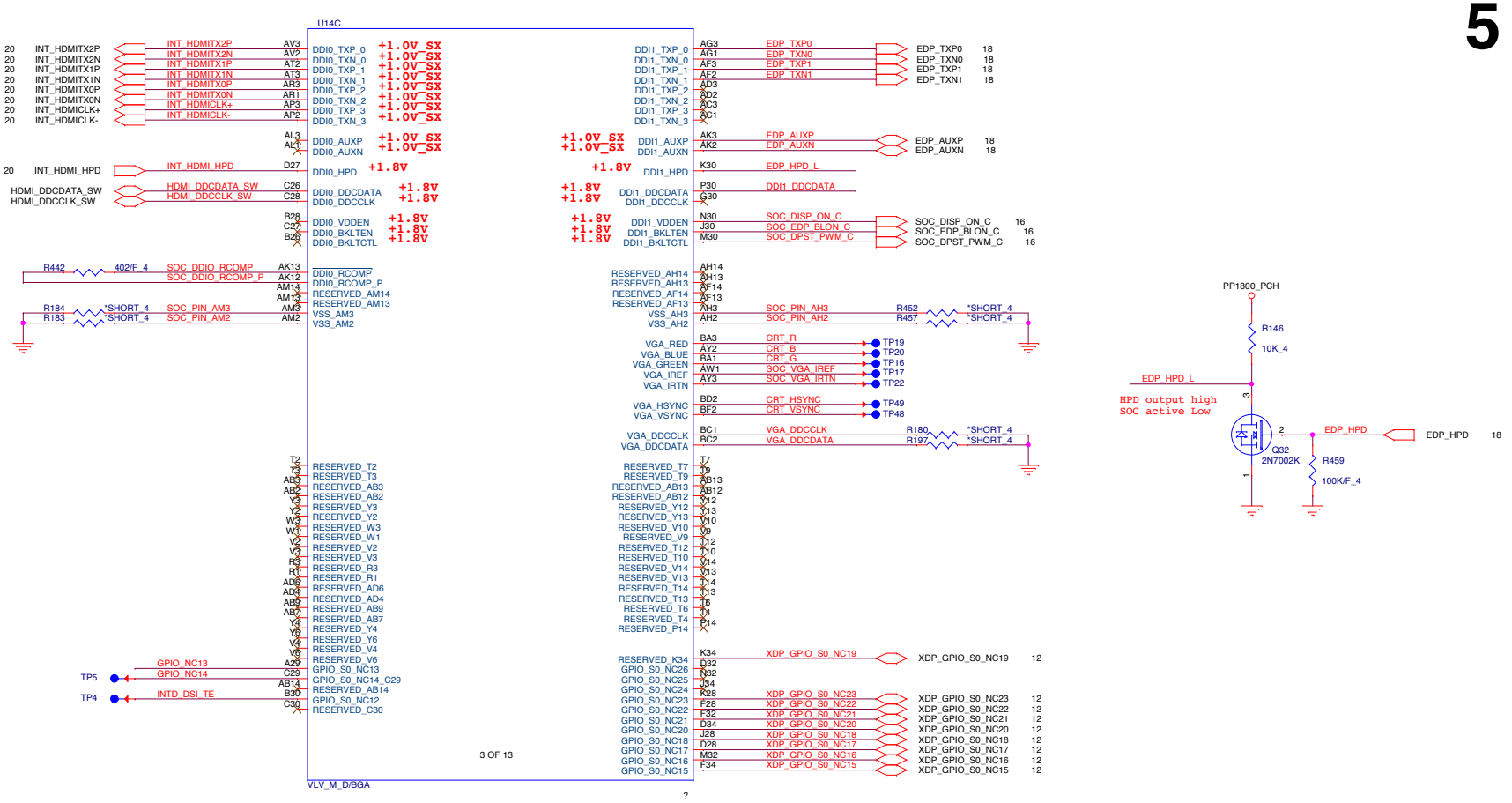
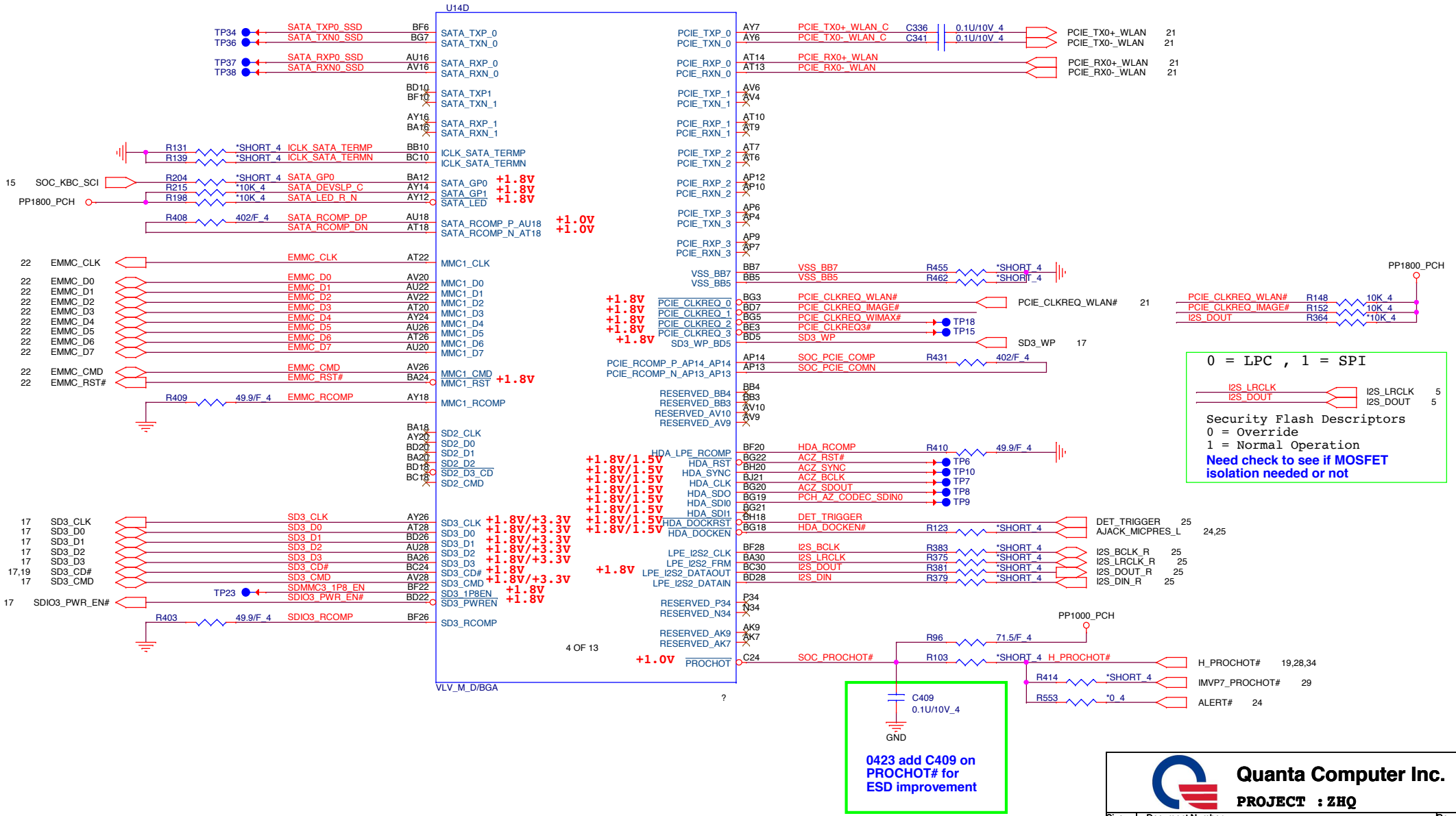


BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged **1 = Top address bit is inverted**	using SoC internal PU
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC **1 = SPI**	using SoC internal PU
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override **1 = Normal operation**	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	using SoC internal PU
GPIO_SO_NC_13				



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0423 add C408 on CORE_PWROK for ESD improvement

CORE_PWROK C408 0.1U/10V_4 GND

CRYSTAL 25MHZ

C106 12P/50V_4 — XTAL25_IN — Y3 25MHZ +-10PPM — R188 1M_4 — XTAL25_OUT — C105 12P/50V_4

2nd BG625000121(HHE)

U14E

XTAL25_IN AH12 ICLK_OSCIN
XTAL25_OUT AH10 ICLK_OSCOUT
AD9 RESERVED_AD9
R466 4.02K/F_4 ICLK_ICOMP AD14 ICLK_ICOMP
R467 47.5/F_4 ICLK_RCOMP AD13 ICLK_RCOMP
AD10 RESERVED_AD10
AD12 RESERVED_AD12

21 CLK_PCIE_WLANN CLK_PCIE_WLANN AF6 PCIE_CLKN_00
21 CLK_PCIE_WLANP CLK_PCIE_WLANP AF4 PCIE_CLKP_00
AF9 PCIE_CLKN_11
AF7 PCIE_CLKP_11
AK4 PCIE_CLKN_22
AK6 PCIE_CLKP_22
AM4 PCIE_CLKN_33
AM6 PCIE_CLKP_33
AM10 RESERVED_AM10
AM9 RESERVED_AM9

PP1800_PCH
R150 10K_4 KBD_IRQ#

PP1800_PCH_ME
R501 3.3K/F_4 SOC_SPI_CS#

PP1800_PCH_S5
R108 10K_4 PCH_WAKE#
R122 10K_4 TRACKPAD_INT#
R117 *10K_4 SOC_JTAG2_TDO
R136 10K_4 PCH_SPI_WP_D
R111 TS@10K_4 TOUCH_INT#

25 I2S_MCLK — I2S_MCLK BH7 PMC_PLT_CLK_00 +1.8V
BH5 PMC_PLT_CLK_11 +1.8V
BH4 PMC_PLT_CLK_22 +1.8V
BH6 PMC_PLT_CLK_33 +1.8V
BH3 PMC_PLT_CLK_44 +1.8V
28 KBD_IRQ# — KBD_IRQ# BJ9 PMC_PLT_CLK_55 +1.8V
12 SRT_CRST# — SRT_CRST# C12 ILB_RTC_RST

12 XDP_H_TCK — D14 TAP_TCK +1.8V_S5
12 XDP_H_TRST# — G12 TAP_TRST +1.8V_S5
12 XDP_H_TMS — F14 TAP_TMS +1.8V_S5
12 XDP_H_TDI — F12 TAP_TDI +1.8V_S5
12 XDP_H_TDO — G16 TAP_TDO +1.8V_S5
12 XDP_H_PRDY# — D18 TAP_PRDY +1.8V_S5
12 XDP_H_PREQ#_C — F16 TAP_PREQ +1.8V_S5
AT34 RESERVED

SOC_SPI_CS# C23 PCU_SPI_CS_00 +1.8V_S5
C21 PCU_SPI_CS_11 +1.8V_S5
SOC_SPI_MISO B22 PCU_SPI_MISO +1.8V_S5
SOC_SPI_MOSI A21 PCU_SPI_MOSI +1.8V_S5
SOC_SPI_CLK C22 PCU_SPI_CLK +1.8V_S5

28 PCH_WAKE_L — R107 *SHORT_4 PCH_WAKE# B18 GPIO_S5_0 +1.8V_S5
27 TRACKPAD_INT# — TRACKPAD_INT# B16 GPIO_S5_1 +1.8V_S5
16 TOUCH_INT# — TOUCH_INT# C18 GPIO_S5_2 +1.8V_S5
16 LTE_WAKE# — LTE_WAKE# A17 GPIO_S5_3 +1.8V_S5
SOC_JTAG2_TDO C17 GPIO_S5_4 +1.8V_S5
16 PMC_SUSCLK1 — PMC_SUSCLK1 C16 GPIO_S5_5 +1.8V_S5
PCH_SPI_WP_D B14 GPIO_S5_6 +1.8V_S5
15 SOC_KBC_SMI — R424 *SHORT_4 SOC_GPIO7 C15 GPIO_S5_7 +1.8V_S5

C13
25 MUX_AUD_INT1# — MUX_AUD_INT1# A13 GPIO_S5_8
16 WIFI_DISABLE# — WIFI_DISABLE# C19 GPIO_S5_9
GPIO_S5_10
R402 49.9/F_4 SOC_GPIO_RCOMP N26 GPIO_RCOMP

5 OF 13
VLV_M_D/BGA

+1.8V SIO_UART1_RXD AU34 ALS_INT#
+1.8V SIO_UART1_TXD AV34
+1.8V SIO_UART1_RTS BA34 TOUCH_INT_L_DX — TOUCH_INT_L_DX 16
+1.8V SIO_UART1_CTS AY34

+1.8V SIO_UART2_RXD BF34 SIO_UART2_RXD — TP31
+1.8V SIO_UART2_TXD BD34 SIO_UART2_TXD — TP33
+1.8V SIO_UART2_RTS BD32
+1.8V SIO_UART2_CTS BF32

+1.8V_S5 PMC_SUSPWRDNACK D26 PMC_SUSPWRDNACK — PMC_SUSPWRDNACK 15
+1.8V_S5 PMC_SUSCLK0_G24 G24 PMC_SUSCLK0 — PMC_SUSCLK0 16
+1.8V_S5 PMC_SLP_S0IX F18 SLP_S0IX# — SLP_S0IX# 15
+1.8V_S5 PMC_SLP_S4 F22 SLP_S4# — SLP_S4# 3,12,15
PMC_SLP_S3 D22 SLP_S3# — SLP_S3# 12,15
GPIO_S514_J20 J20
+1.8V_S5 PMC_ACPRESENT D20 ACPRESENT — ACPRESENT 16
+1.8V_S5 PMC_WAKE_PCIE_0 F26 SOC_PMC_WAKE# — SOC_PMC_WAKE# 16
+1.8V_S5 PMC_BATLOW K26 PMC_BATLOW#
+1.8V_S5 PMC_PWRBTN J26 SOC_PWRBTN# — SOC_PWRBTN# 12,15
+1.8V BG9 SOC_REST_BTN# — SOC_REST_BTN# 12,19
+1.8V_S5 PMC_RSTBTN F20 SOC_PLTRST# — SOC_PLTRST# 12,15
PMC_PLTRST J24
GPIO_S517_J24
+1.8V_S5 PMC_SUS_STAT G18 PMC_SUS_STAT# — SUS STAT OUTPUT PORT — PMC_SUS_STAT# 15

+3V_RTC ILB_RTC_TEST C11 SOC_RTEST# — SOC_RTEST# 12

+3V_RTC PMC_RSMRST B10 SOC_RSMRST# — SOC_RSMRST# 12,15
+3V_RTC PMC_CORE_PWROK B7 CORE_PWROK R448 *SHORT_4 — CORE_PWROK_R 12,28

ILB_RTC_X1 C9 RTC_X1
ILB_RTC_X2 A9 RTC_X2
ILB_RTC_EXTPAD B8 BRTC_EXTPAD C101 0.1U/10V_4

SPEC 512177 INPUT PORT
+1.0V SVID_ALERT B24 SVID_ALERT#_SOC R90 20/F_4 VR_SVID_ALERT# — VR_SVID_ALERT# 34
+1.0V SVID_DATA A25 SVID_DATA_SOC R84 16.9/F_4 VR_SVID_DATA — VR_SVID_DATA 34
+1.0V SVID_CLK C25 SVID_CLK_SOC R81 *SHORT_4 VR_SVID_CLK — VR_SVID_CLK 34

SIO_PWM_00 AU32
SIO_PWM_11 AT32 SIO_PWM1 — TP32

+1.8V_S5 GPIO_S5_22 K24 XDP_GPIO_DFX0 — XDP_GPIO_DFX0 12
+1.8V_S5 GPIO_S5_23 N24 XDP_GPIO_DFX1 — XDP_GPIO_DFX1 12
+1.8V_S5 GPIO_S5_24 M20 XDP_GPIO_DFX2 — XDP_GPIO_DFX2 12
+1.8V_S5 GPIO_S5_25 J18 XDP_GPIO_DFX3 — XDP_GPIO_DFX3 12
+1.8V_S5 GPIO_S5_26 M18 XDP_GPIO_DFX4 — XDP_GPIO_DFX4 12
+1.8V_S5 GPIO_S5_27 K18 XDP_GPIO_DFX5 — XDP_GPIO_DFX5 12
+1.8V_S5 GPIO_S5_28 K20 XDP_GPIO_DFX6 — XDP_GPIO_DFX6 12
+1.8V_S5 GPIO_S5_29 M22 XDP_GPIO_DFX7 — XDP_GPIO_DFX7 12
+1.8V_S5 GPIO_S5_30 M24 XDP_GPIO_DFX8 — XDP_GPIO_DFX8 12

+1.8V SIO_SPI_CS# AV32 SIO_SPI_CS# — TP134
+1.8V SIO_SPI_MISO BA28 SIO_SPI_MISO — TP135
+1.8V SIO_SPI_MOSI AY28 SIO_SPI_MOSI — TP136
+1.8V SIO_SPI_CLK AY30 SIO_SPI_CLK — TP137

02/27 Change to TP for S3 leakage on PP1800_PCH issue.

PP1800_PCH_S5
PMC_SUSPWRDNACK R413 10K_4
ACPRESENT R397 2.2K_4
SOC_PMC_WAKE# R412 10K_4
PMC_BATLOW# R399 10K_4

PP1800_PCH
ALS_INT# R418 10K_4
TOUCH_INT_L_DX R363 10K_4
SOC_REST_BTN# R441 10K_4

SOC_REST_BTN# R468 *SHORT_4 EC_REST_L 28
9/6 Add EC_REST_L for warm boot, EC side is OD type

RTC Clock 32.768KHz

RTC_X1 C91 15P/50V_4
R161 10M_4 Y2 32.768KHZ
RTC_X2 C92 15P/50V_4

2nd BG332768453

PP1000_PCH
ALERT Close to SOC — R88 73.2/F_4 — R360 73.2/F_4 — R374 73.2/F_4 — DATA, CLK CLOSE TO VR
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA

RTC Circuitry(RTC)

30mils
+3V_RTC
R138 20K/F_4 — SOC_RTEST#
C89 1U.3V_4
PP3300_RTC
R116 *SHORT_6 — R130 20K/F_4 — SRT_CRST#
C85 1U/6.3V_4
C84 1U/6.3V_4

SPI_FLASH

PP1800_PCH_ME
PP3300_PCH_S5
C355 0.1U/10V_4
PP1800_PCH
R158 *0_6 PP1800_PCH_ME_1
PP1800_PCH_ME
R488 *3.3K/F_4 SPI_WP_ME_ROM
PP1800_PCH_S5
R157 *SHORT_6
R500 3.3K/F_4 SPI_HOLD_ME
Q29 PJA138K
Default PD (pin3)

U22
VCC SPI_SI — SOC_SPI_MOSI_R — R472 22/F_4 SOC_SPI_MOSI
SPI_SO — SOC_SPI_MISO_R — R487 22/F_4 SOC_SPI_MISO
CS# — SOC_SPI_CS#_R — R503 22/F_4 SOC_SPI_CS#
WP# SPI_SCK — SOC_SPI_CLK_R — R480 22/F_4 SOC_SPI_CLK
SPI_HOLD GND
SPI_FLASH
soic8-7_9-1_27
AKE5EZN0N00
IC FLASH (8P) W25Q64FWSSIG (SOIC)

LAYOUT CLOSE TO SPI ROM
R471 *SHORT_4 PCH_SPI_SI_R 19
R479 *SHORT_4 PCH_SPI_SO_R 19
R470 *SHORT_4 PCH_SPI_CS0#_R 19
R481 *SHORT_4 PCH_SPI_CLK_R 19

SPI NOR FLASH

SPI ROM needs power in S3/S5 for the TXE (Trusted execution engine).

near SPI ROM as possible

SPI_WP_ME R133 *SHORT_4 GPIO_SPI_WP 19 — To debug header
SPI_HOLD_ME R513 *SHORT_4 SPI_HOLD#_BIOS 19

Q27 2N7002K
PCH_SPI_WP_D — PCH_SPI_WP_D connect to GPIO58 at GRB — To PCH
SPI_WP_ME — SPI_WP_ME 26,28 — From Screw/EC

PP1800_PCH_ME
C115 0.1U/10V_4
3.3V
SPI_WP_ME R165 *SHORT_4 SPI_WP_ME_ROM_Q
U19 74LVC1G34
SPI_WP_ME_ROM
R179 100K_4
LAYOUT CLOSE TO SPI ROM

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4/22 update the DRMA ID table

Vender	RAM_ID 210	Q P/N	Mfr. PN	Freq.	Size	Pice
Micron	0x000		MT41K256M16HA-125	1600MHz	4GB	8
Hynix	0x001	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz	4GB	8
Micron	0x010	AKD5DGSTL07	MT41K128M16JT-125M:K	1600MHz	2GB	8
Hynix	0x011	AKD5PGSTW03	H5TC4G63MFR-PBA	1600MHz	2GB	4
Micron	0x100		MT41K256M16HA-125	1600MHz	2GB	4
Hynix	0x101	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz	2GB	4
Kingston	0x110	AKD5PZSTP02	D2516EC4BXGGB	1600MHz	4GB	8
Hynix	0x111	AKD5PGSTW03	H5TC4G63MFR-PBA	1600MHz	4GB	8

02/14 Change RMID to 001.

RAM ID

PP1800_PCH_S5

R186 *1K_4 RAM_ID0 R202 1K_4
R187 1K_4 RAM_ID1 R203 *1K_4
R196 1K_4 RAM_ID2 R192 *1K_4
R612 *1K_4 RAM_ID3 R613 *1K_4

02/27 Reserve RAM_ID3 for memory BOM option.

PORT 1 USB CONN
PORT 2 LTE
PORT 3 NA
PORT 4 NA

MB USB3.0
HUB1
CCD
BT

16 LTE_DISABLE# LTE_DISABLE#

RAM_ID0 RAM_ID1 RAM_ID2 RAM_ID3

26 USBP0+ USBP0- 17 USBP1+ USBP1- 18 USBP2+ USBP2- 21 USBP3+ USBP3-

USB_DP0 USB_DN0 USB_DP1 USB_DN1 USB_DP2 USB_DN2 USB_DP3 USB_DN3

R437 1K/F_4 ICLK_USB_TERMN_0 R425 1K/F_4 ICLK_USB_TERMN_1 ICLK_USB_TERMN_D10 ICLK_USB_TERMN

15,26 USB_OC0# R97 10K_4 USB_OC0# PP1800_PCH_S5 R189 10K_4 USB_OC1# 15,24 USB_OC1#

USB_OC_00 USB_OC_11 +1.8V_S5 +1.8V_S5

R443 45.3/F_4 USB_RCOMP USB_RCOMPO USB_RCOMPI

R436 *0_4 USB_PLL_MON USB_PLL_MON

USB_HSIC0_DATA USB_HSIC0_STROBE

USB_HSIC1_DATA USB_HSIC1_STROBE

R185 45.3/F_4 USB_HSIC_RCOMP USB_HSIC_RCOMP

R415 49.9/F_4 LPC_RCOMP LPC_RCOMP

23 PCLK_TPM R446 *0_4

28 CLK_PCI_EC 28 LPC_CLKRUN_L R449 *SHORT_4 CLK_PCI_EC_R R112 22/F_4 SOC_CLKOUT_1 LPC_CLKRUN_L R109 *SHORT_4 SOC_CLKRUN#

23,28 LPC_LAD0 23,28 LPC_LAD1 23,28 LPC_LAD2 23,28 LPC_LAD3 23,28 LPC_LFRAME# R115 22/F_4 SOC_CLKOUT_0 15 SOC_SERIRQ

LPC_LAD0 LPC_LAD1 LPC_LAD2 LPC_LAD3 LPC_LFRAME# SOC_CLKRUN# SOC_SERIRQ

ILB_LPC_AD_00 ILB_LPC_AD_11 ILB_LPC_AD_22 ILB_LPC_AD_33 ILB_LPC_FRAME ILB_LPC_CLK_00 ILB_LPC_CLK_11 ILB_LPC_CLKRUN ILB_LPC_SERIRQ

+1.8V/+3.3V +1.8V/+3.3V +1.8V/+3.3V +1.8V/+3.3V +1.8V/+3.3V +1.8V/+3.3V +1.8V/+3.3V +1.8V/+3.3V +1.8V

PP1800_PCH

R120 2.2K_4 SMB_SOC_DATA R125 2.2K_4 SMB_SOC_CLK R141 2.2K_4 SMB_SOC_ALERTB

12 SMB_SOC_DATA 12 SMB_SOC_CLK SMB_SOC_DATA SMB_SOC_CLK SMB_SOC_ALERTB

PCU_SMB_DATA PCU_SMB_CLK PCU_SMB_ALERT +1.8V +1.8V +1.8V

0424 reserve R483 for CLKRUN# disable

GND R483 *0_4 SOC_CLKRUN#

U14F

GPIO_S5_31 GPIO_S5_32 GPIO_S5_33 GPIO_S5_34 GPIO_S5_35 GPIO_S5_36 GPIO_S5_37 GPIO_S5_38 GPIO_S5_39 GPIO_S5_40 GPIO_S5_41 GPIO_S5_42 GPIO_S5_43

RESERVED_M10 RESERVED_M9 RESERVED_P7 RESERVED_P6 RESERVED_M7 USB3_REXT0 RESERVED_P10 RESERVED_P12 RESERVED_M4 RESERVED_M6

USB3_RXP0 USB3_RXN0 USB3_TXP0 USB3_TXN0

USB3_P0_REXT R440 1.24K/F_4

RESERVED_H8 RESERVED_H7 RESERVED_H5 RESERVED_H4

SOC_UART_TX R420 SOC_UART_RX *0_4 Un-Stuff for Test Only

+1.8V GPIO_S0_SC_55 +1.8V GPIO_S0_SC_56 +1.8V GPIO_S0_SC_57 +1.8V GPIO_S0_SC_58 +1.8V GPIO_S0_SC_59 +1.8V GPIO_S0_SC_60 +1.8V GPIO_S0_SC_61

TRACKPAD_INT_DX GPIO_S0_SC_56 SOC_UART_TX SIM_DET_C EC_IN_RW_C SOC_UART_RX

TRACKPAD_INT_DX 27 GPIO_S0_SC_56 5 SOC_UART_TX 19 SIM_DET_C 16 EC_IN_RW_C 16 SOC_UART_RX 19

+1.8V ILB_8254_SPKR

+1.8V SIO_I2C0_DATA +1.8V SIO_I2C0_CLK I2C_0_SDA_C R102 22/F_4 I2C_0_SCL_C R95 22/F_4 I2C_0_SDA_R 16 I2C_0_SCL_R 16 Touch pad

+1.8V SIO_I2C1_DATA +1.8V SIO_I2C1_CLK I2C_1_SDA_C R89 22/F_4 I2C_1_SCL_C R83 22/F_4 I2C_1_SDA_R 25 I2C_1_SCL_R 25 Audio Codec

+1.8V SIO_I2C2_DATA +1.8V SIO_I2C2_CLK

+1.8V SIO_I2C3_DATA +1.8V SIO_I2C3_CLK

+1.8V SIO_I2C4_DATA +1.8V SIO_I2C4_CLK I2C_4_SDA R625 *TS@22/F_4 I2C_5_SDA I2C_4_SCL R626 *TS@22/F_4 I2C_5_SCL Light sensor

+1.8V SIO_I2C5_DATA +1.8V SIO_I2C5_CLK I2C_5_SDA_C R71 TS@22/F_4 I2C_5_SDA 16 I2C_5_SCL_C R65 TS@22/F_4 I2C_5_SCL 16 Touch panel

+1.8V SIO_I2C6_DATA +1.8V SIO_I2C6_CLK

GPIO_S0_SC_092 GPIO_S0_SC_093 I2C_NFC_SDA I2C_NFC_SCL NFC

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VLV_M_D/BGA

PP1800_PCH

TRACKPAD_INT_DX R433 10K_4 SIM_DET_C R422 10K_4

I2C_0_SDA_R R438 4.7K_4 I2C_0_SCL_R R432 4.7K_4 I2C_1_SDA_R R421 4.7K_4 I2C_1_SCL_R R416 4.7K_4

I2C_4_SDA R398 *4.7K_4 I2C_4_SCL R394 *4.7K_4 I2C_5_SDA R392 TS@4.7K_4 I2C_5_SCL R389 TS@4.7K_4

I2C_NFC_SDA R368 *4.7K_4 I2C_NFC_SCL R367 *4.7K_4

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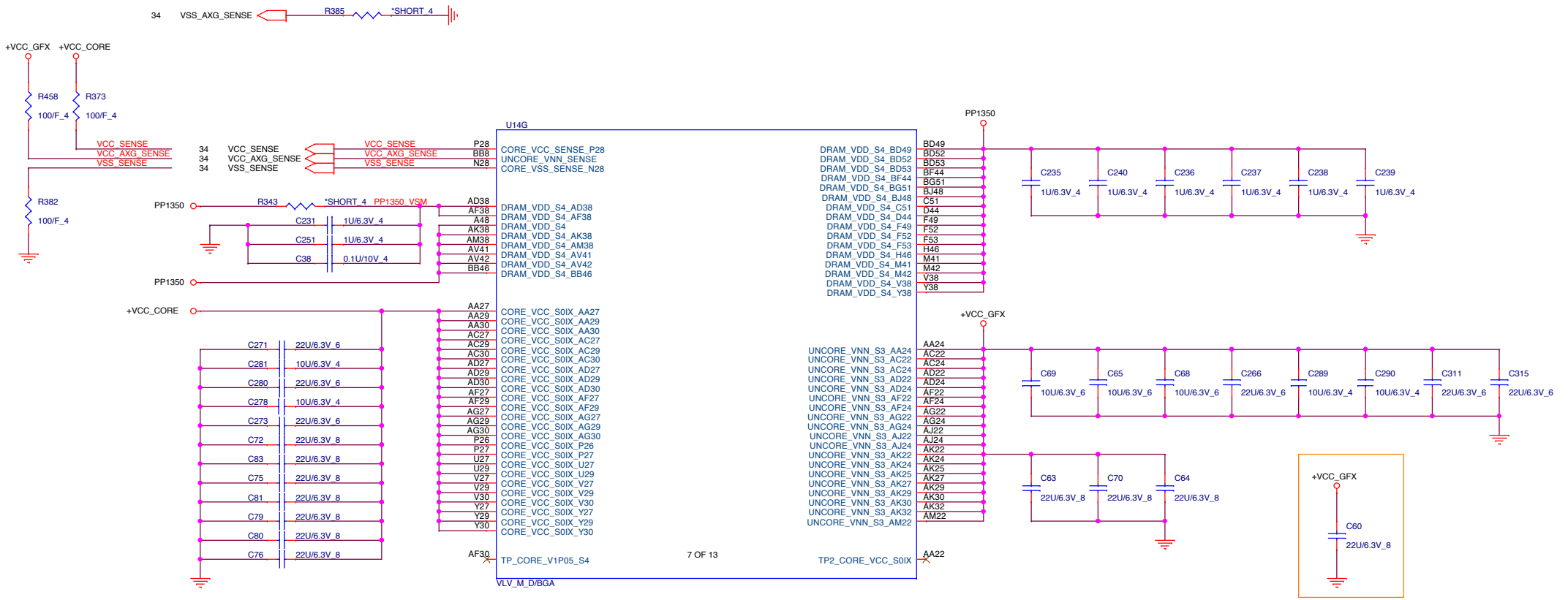
1031 for layout suggestion by intel,
VSS_AXG_SENSE didn't connect to VSS_SENSE,
will connect the GND via near VCC_AXG_SENSE

1031 for layout, add 0hm between
GND and VSS_AXG_SENSE



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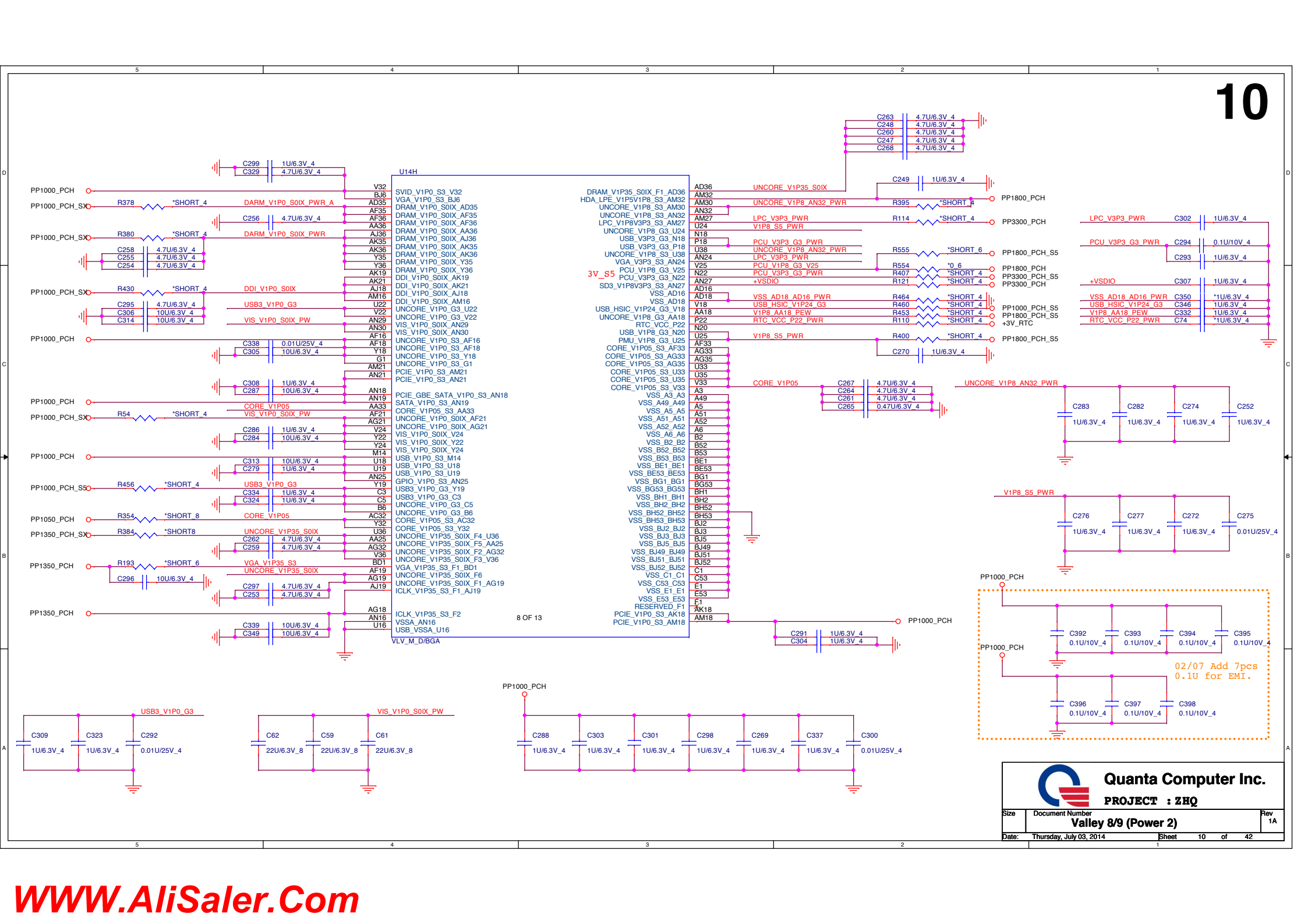

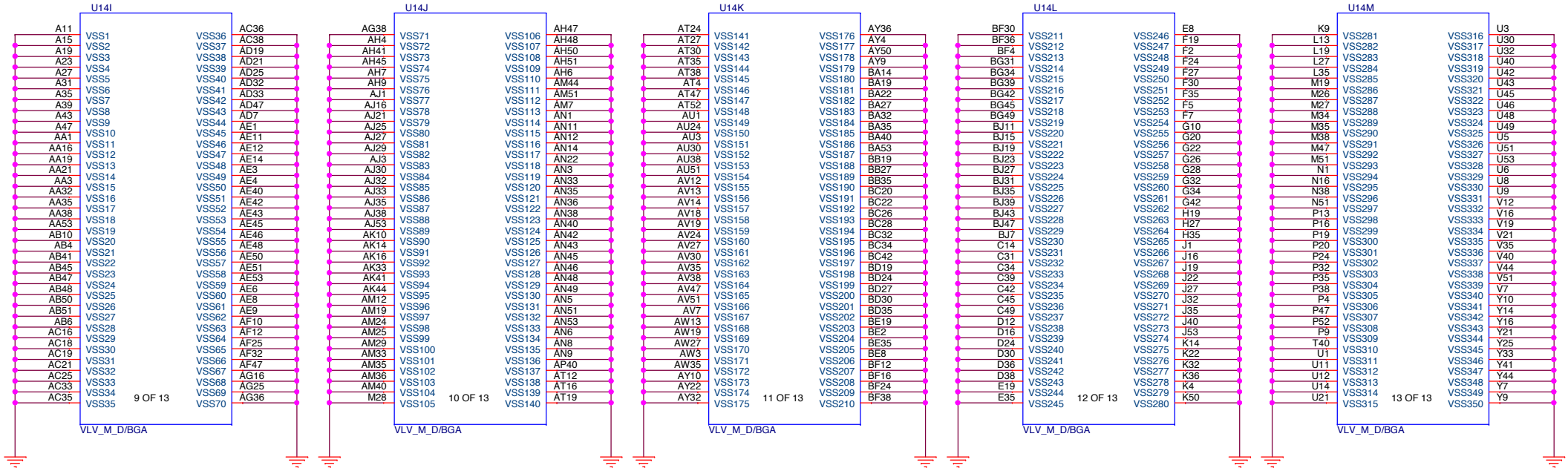

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	Valley 9/9 (GND)	1A
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INTEL Debug Port

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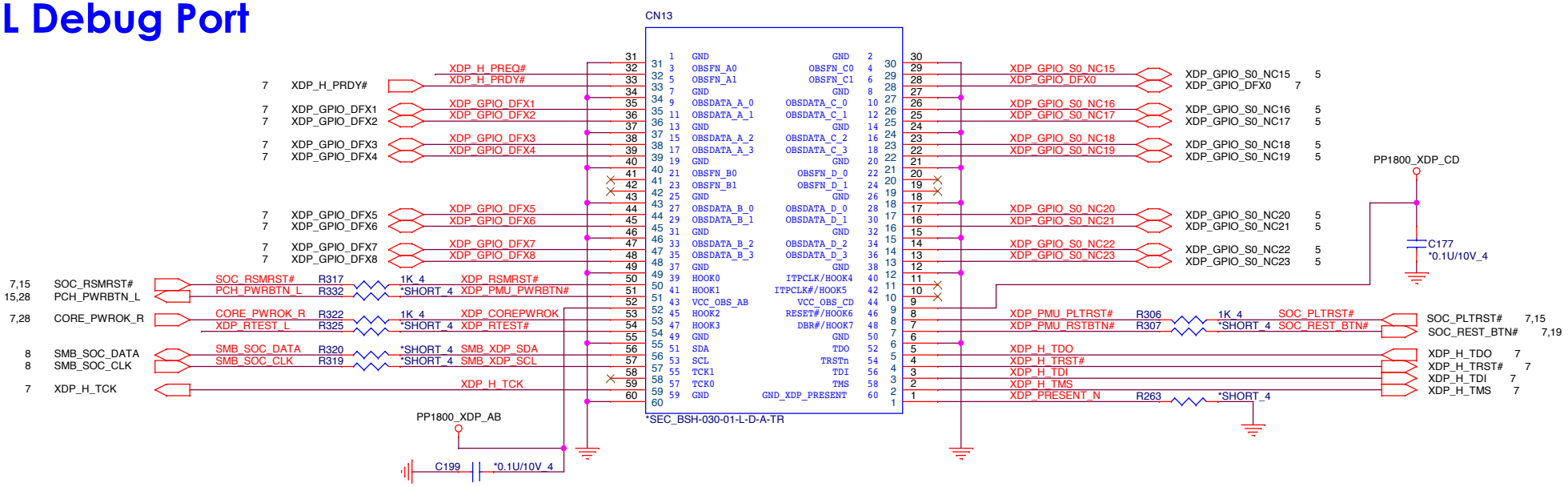
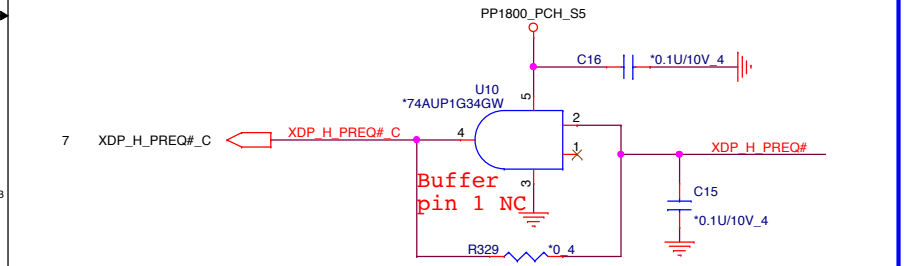
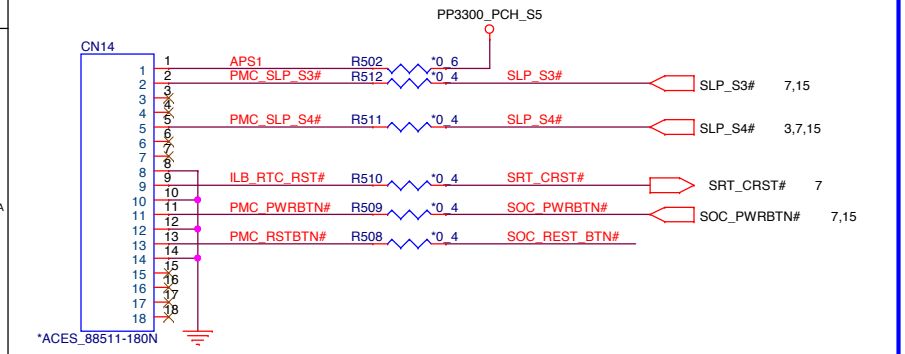


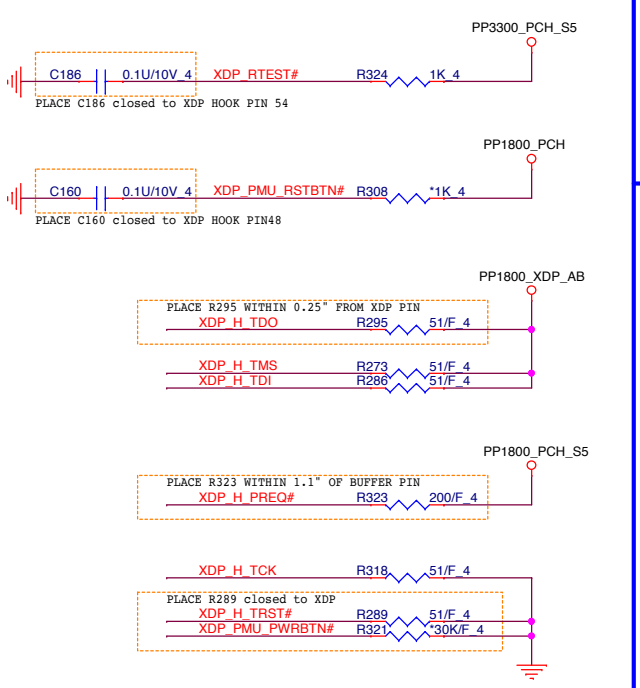
XDP



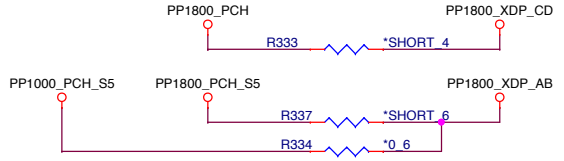
APS



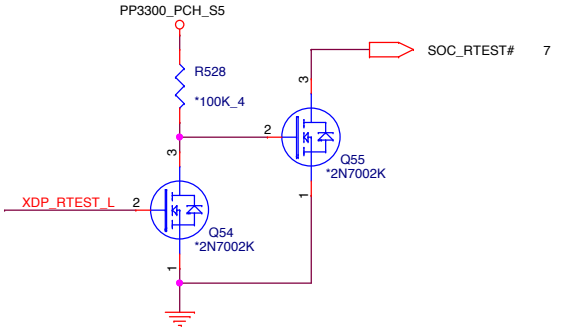
XDP



INTEL Debug Port Power



XDP Reset



Quanta Computer Inc.

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	CPU XDP / APS	1A

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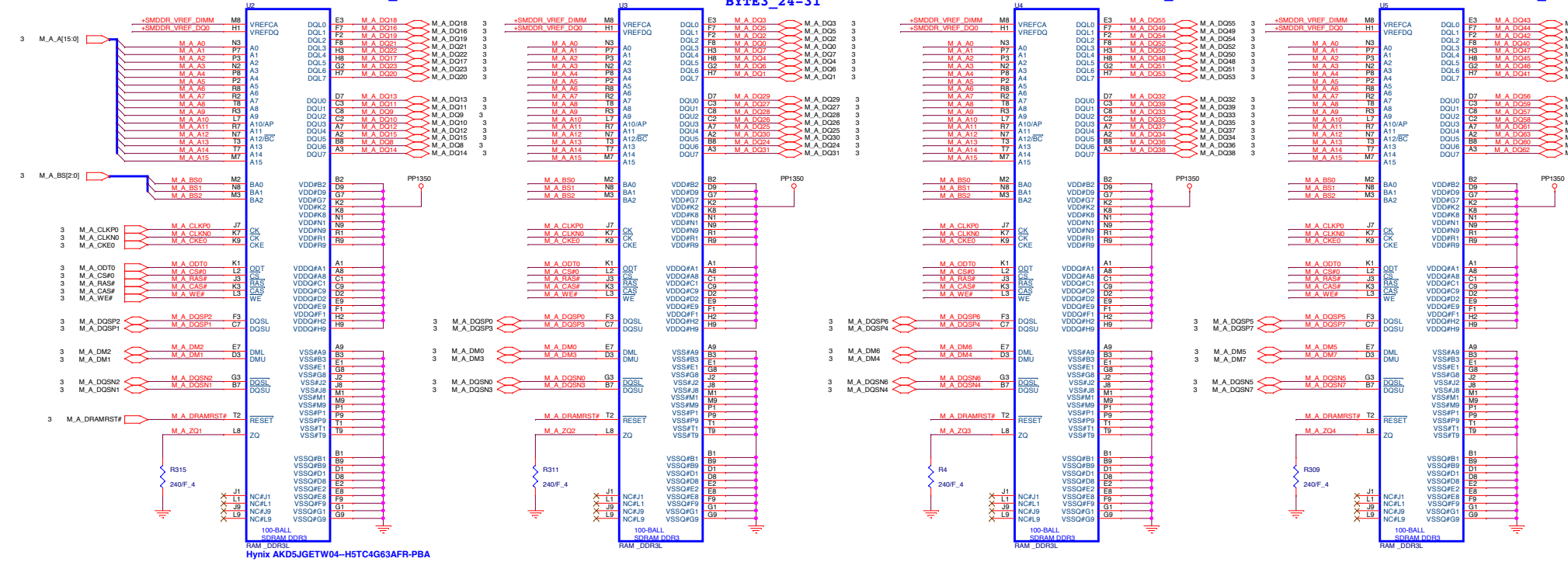
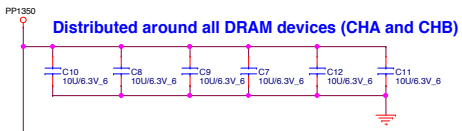
BYTE2_16-23
BYTE1_8-15
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE6_48-55
BYTE5_40-47
BYTE7_56-63

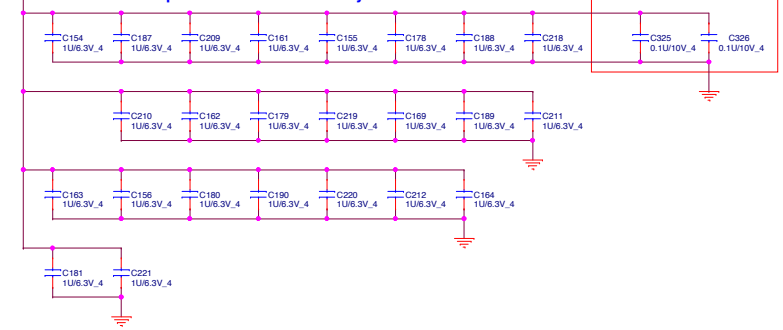


Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

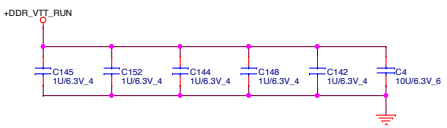
Distributed around all DRAM devices (CHA and CHB)



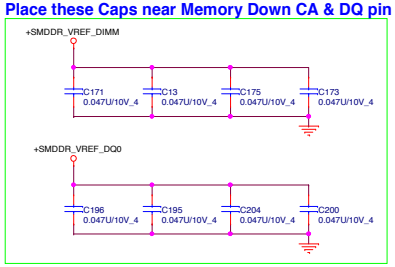
Place these Caps near each X16 Memory Down

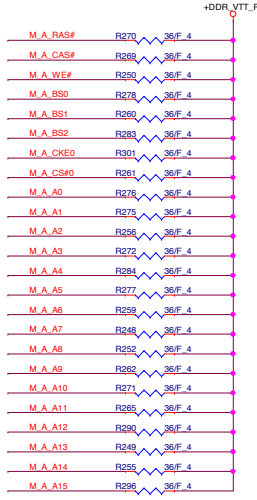


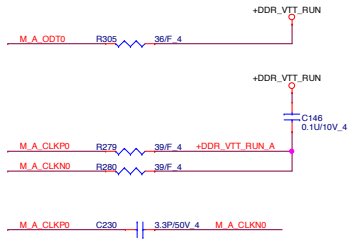
1205 add 0.1uFx2 on PP1350 for EMI request



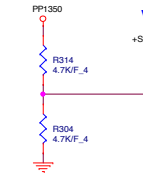
Place these Caps near Memory Down CA & DQ pin



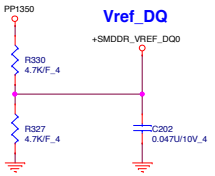




M1 solution



M1 solution



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BYTE2_16-23
BYTE3_24-31
BYTE0_0-7
BYTE1_8-15
BYTE6_48-55
BYTE4_32-39
BYTE5_40-47
BYTE7_56-63

Hynix AKD5JGETW04--H5TC4G63AFR-PBA

Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1333Mhz 4Gb

Place these Caps near each X16 Memory Down

Place these Caps near Memory Down CA & DQ pin

M1 solution

Vref_DQ

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Size: Document Number: DDR3L MEMORY DOWNx16 CH-B Rev: 1A
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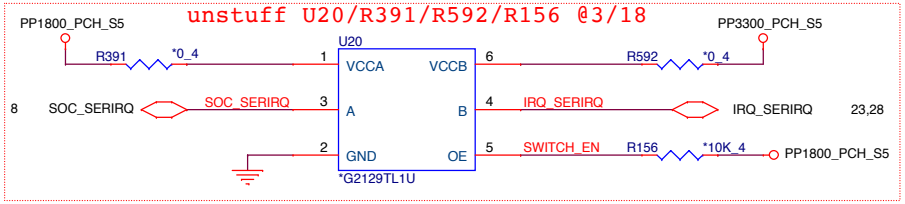
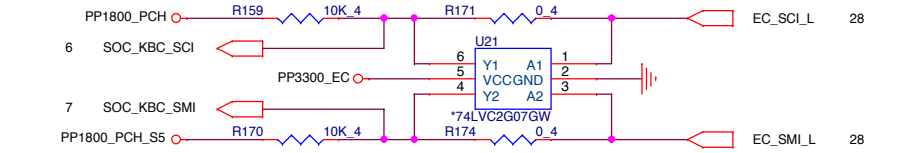
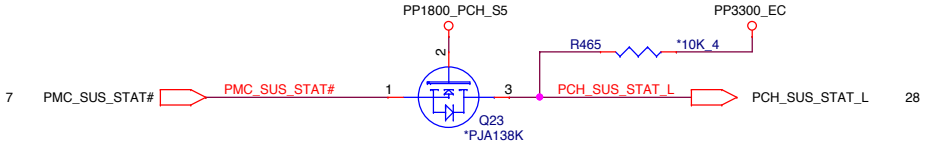
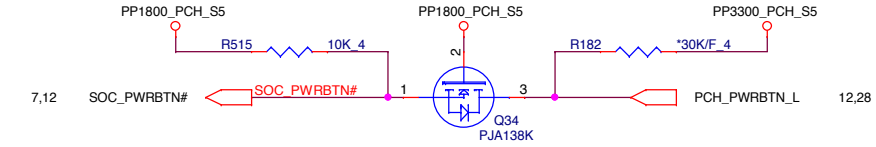
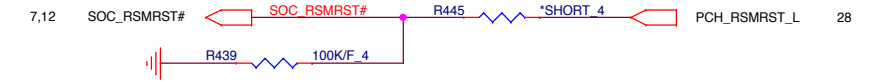
PWRON SEQUENCE

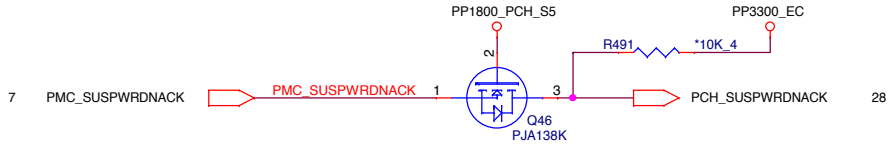




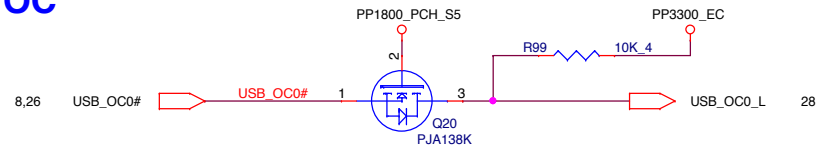


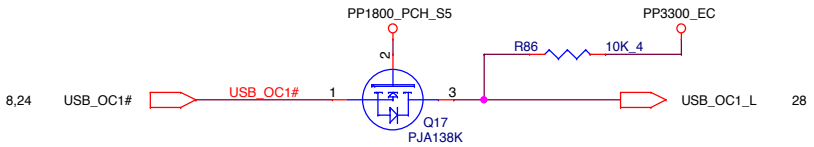






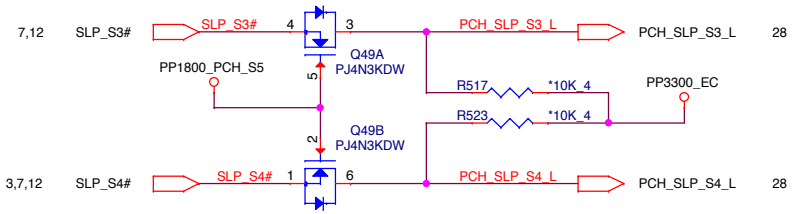
USB OC

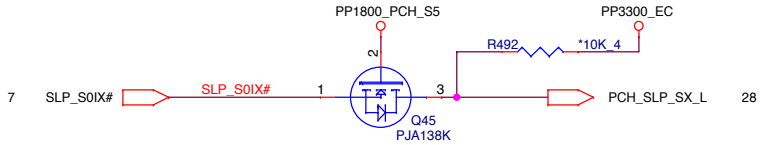


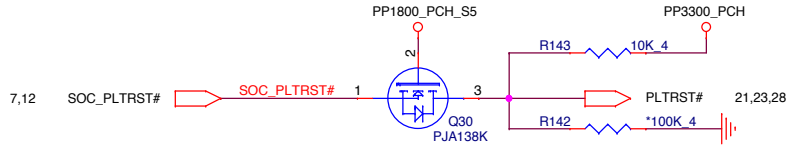


PWRON SEQUENCE

15







02/27 Cancel level shift for S3 leakage on PP1800_PCH issue.

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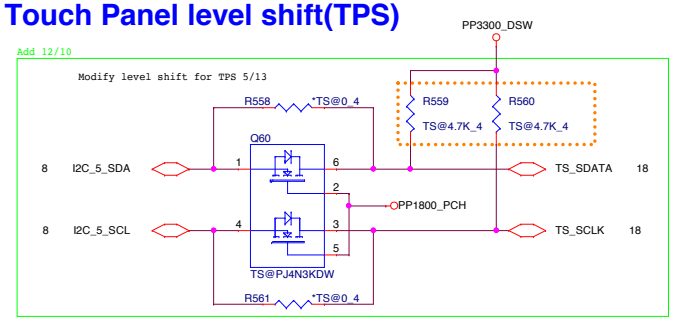
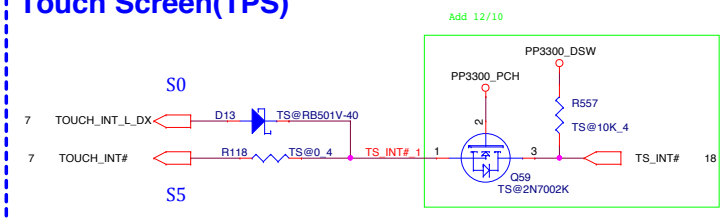
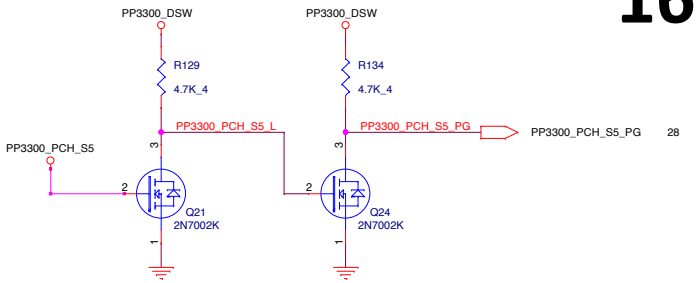
Touch Panel level shift(TPS)



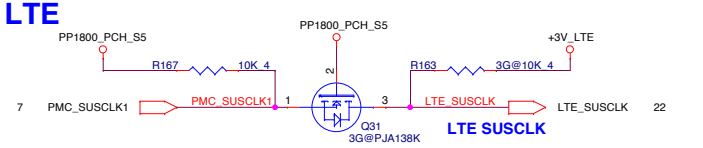
Touch Screen(TPS)

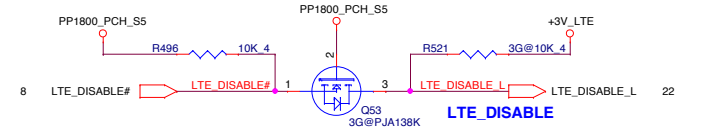


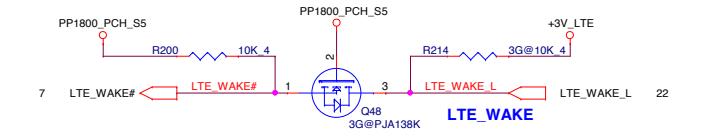
S5 Power Good(+3V_S5)

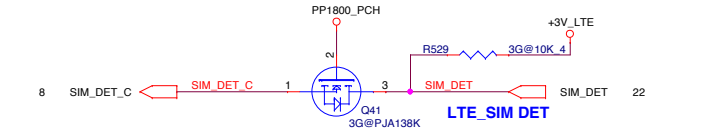


LTE

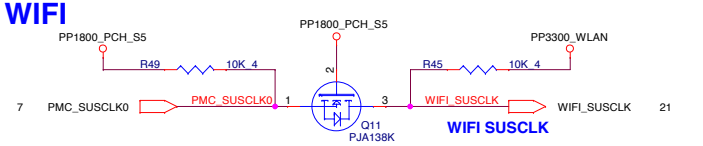


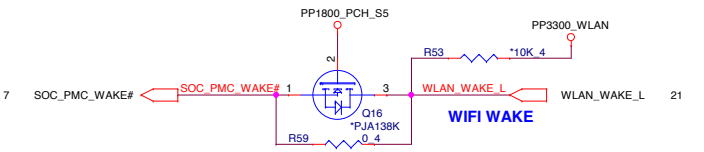


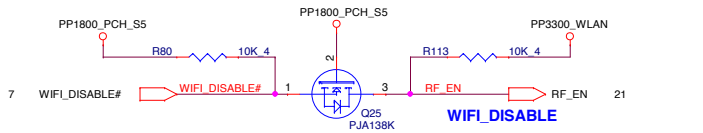




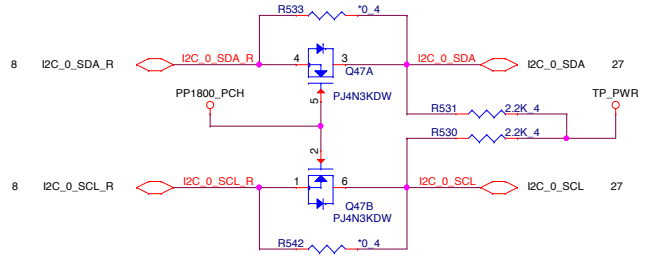
WIFI



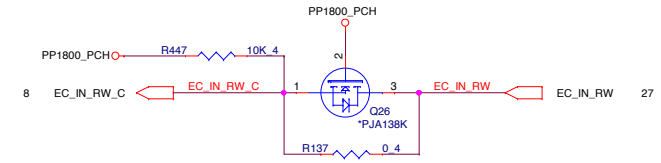




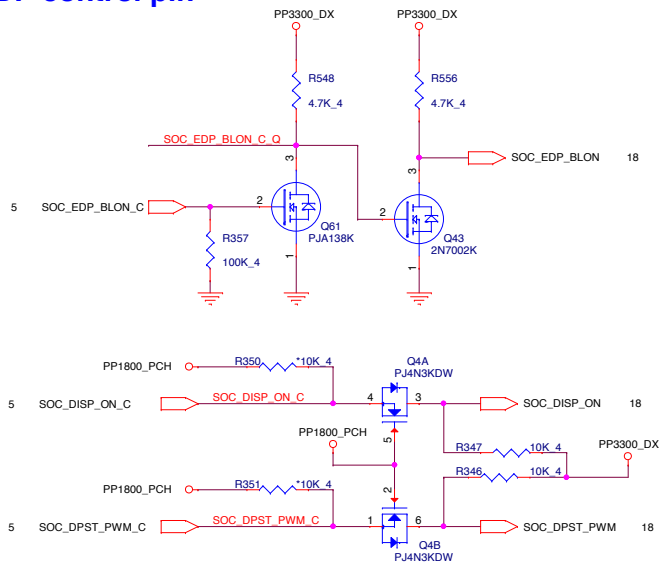
Track Pad



HW RESET

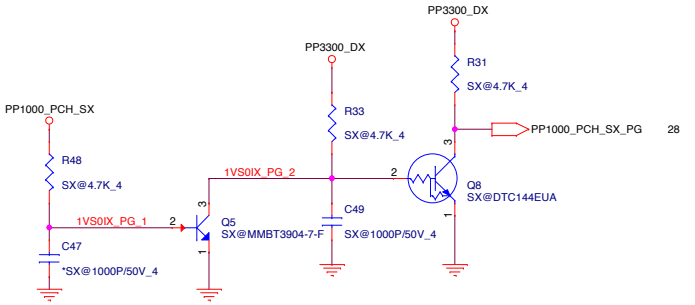


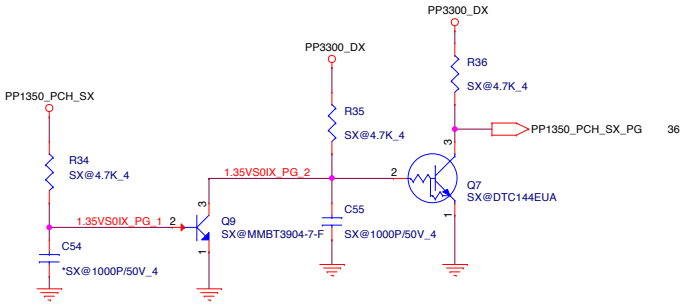
eDP control pin



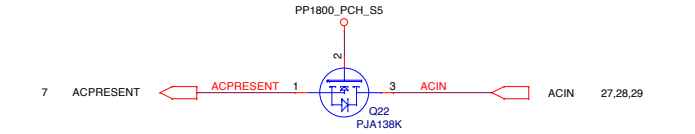
S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed





AC Detect



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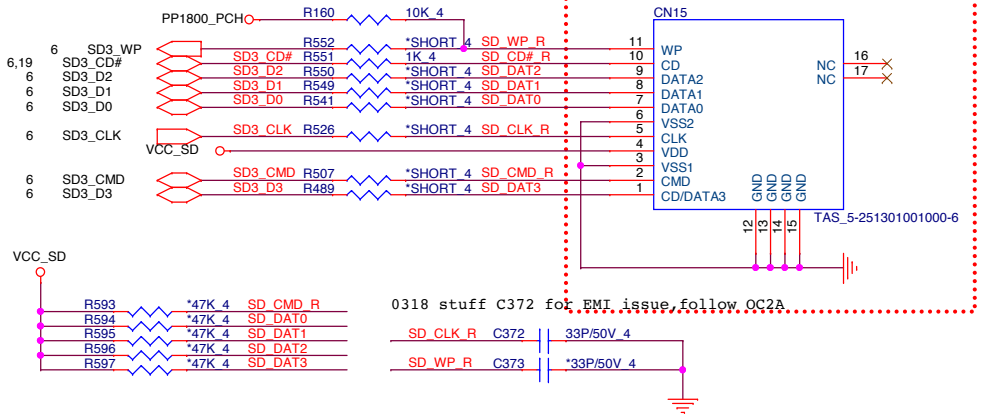
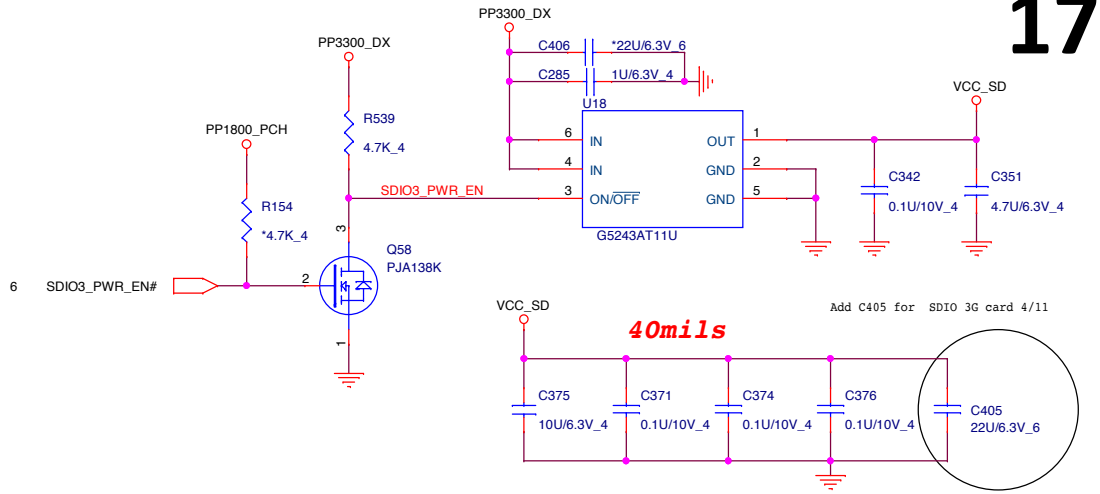
SD/MMC CARD READER CONNECTOR (CBS)

03/18 Change SD card to full card socket for ME request.

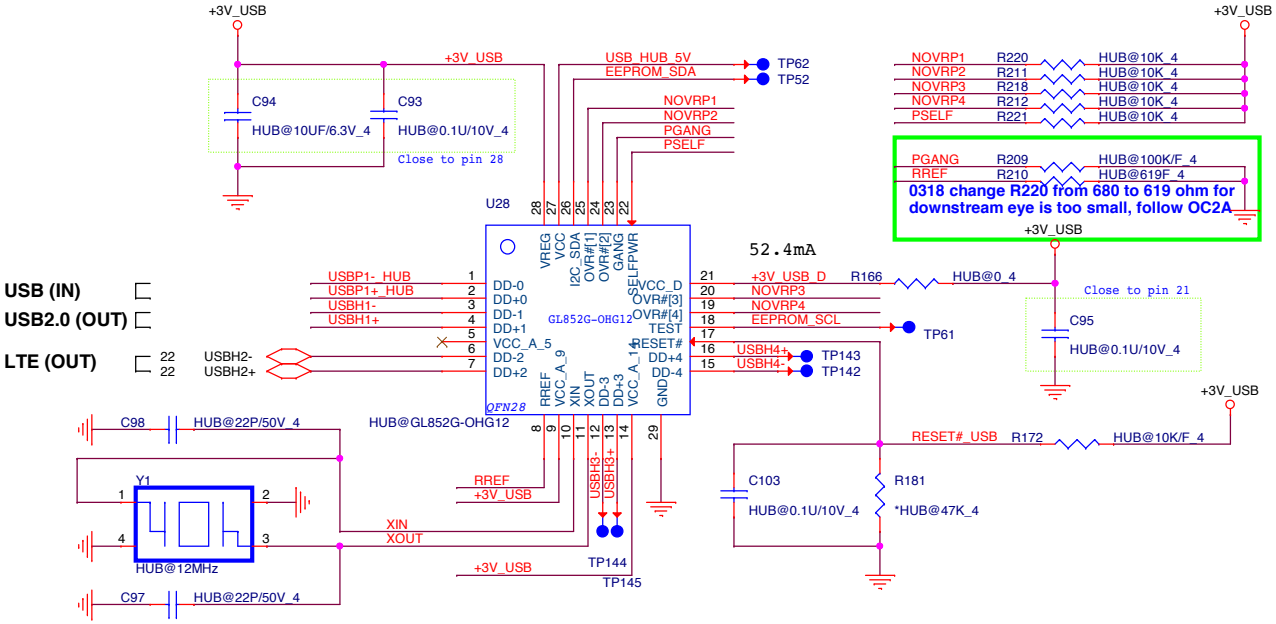
This is full size SD card



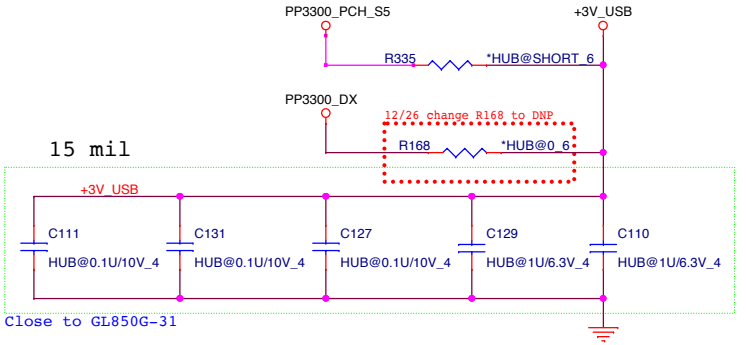
SD card power (CBS)



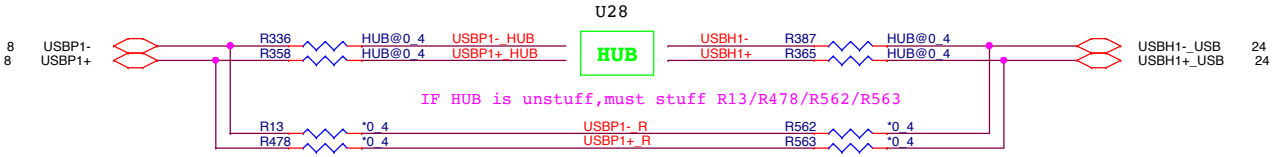
USB HUB (HUB)



USB HUB power (HUB)



USB option for LTE/USB2.0 (HUB)



To IO/B

USB 2.0 CONN

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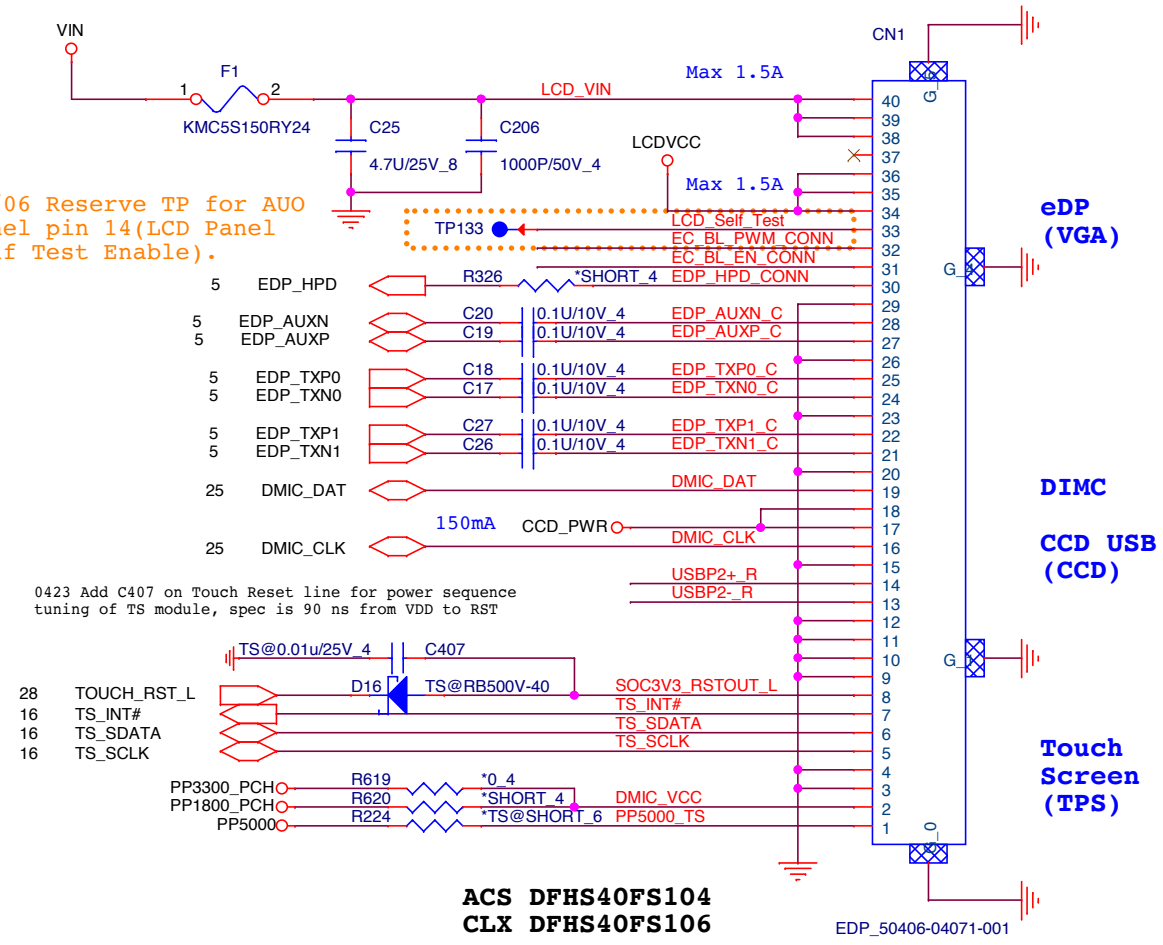
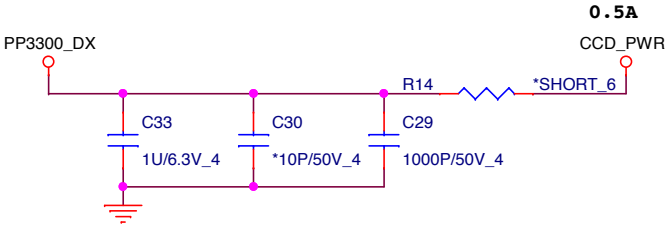
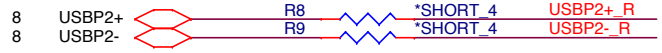
LCD CONN



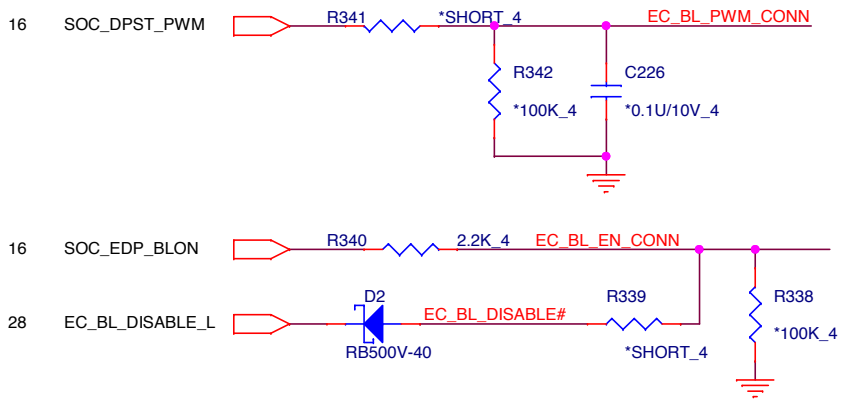
CCD Power(CCD)



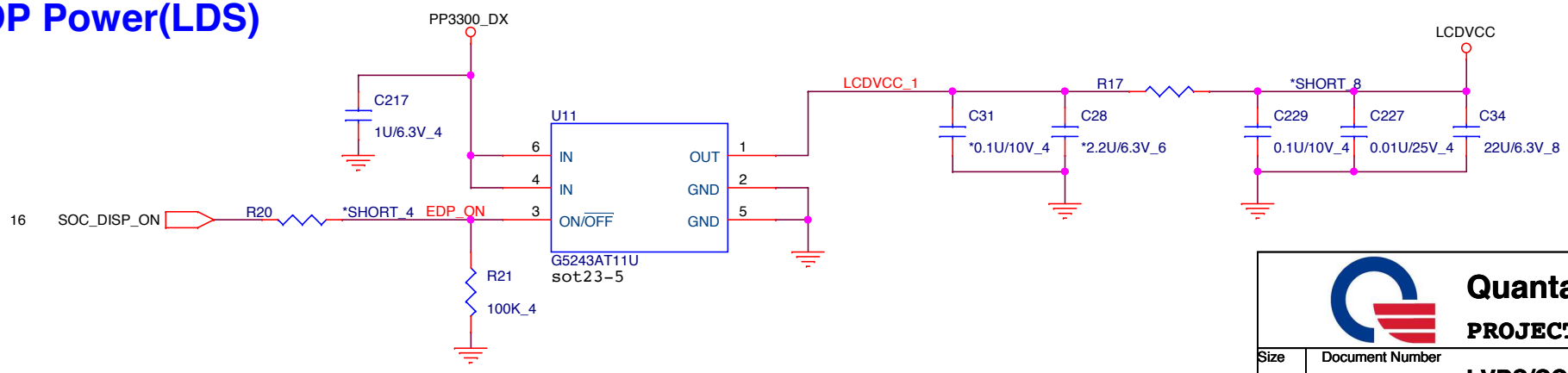
CCD USB(CCD)



eDP panel control(LDS)



eDP Power(LDS)



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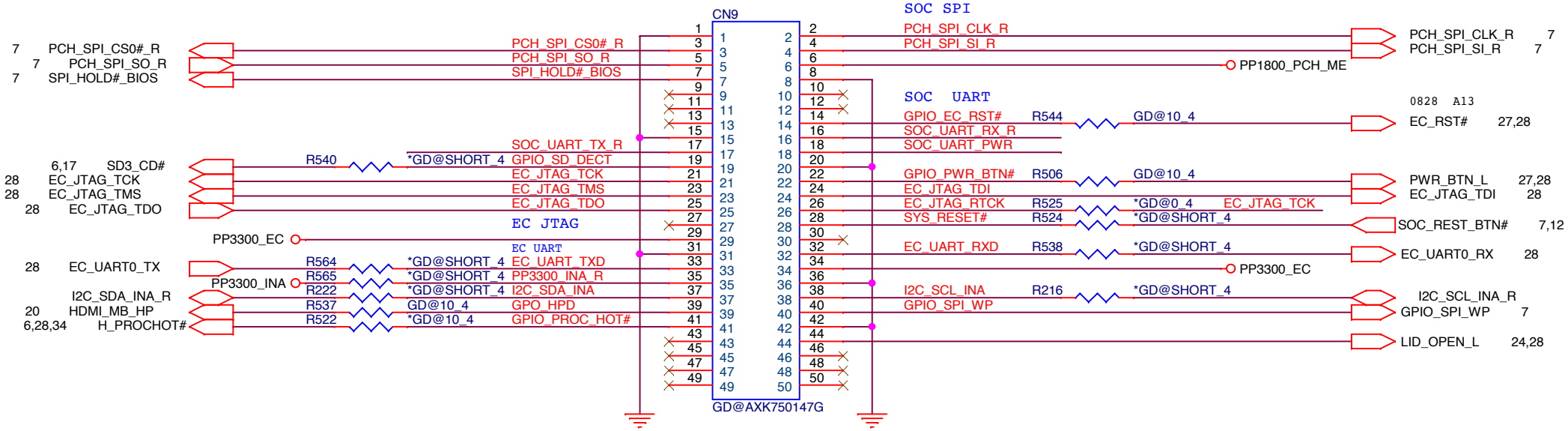
GOOGLE Debug Port(MPC)

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD

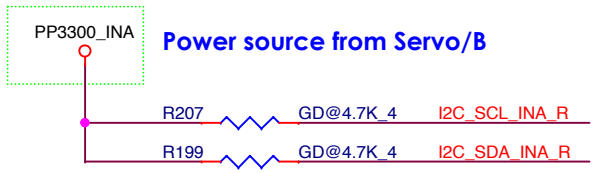
19

50 pin BTB is MUST, don't use 42 pin

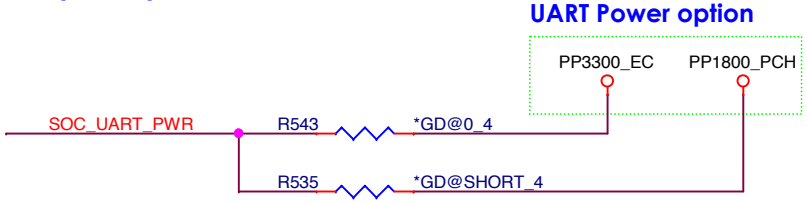
Socket part number AXK750147G



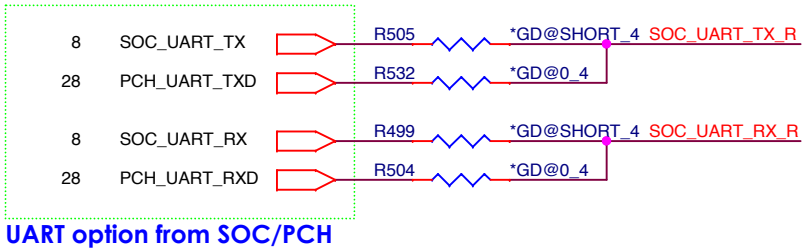
Servo/B I2C Power(MPC)



UART Power(MPC)



UART(MPC)



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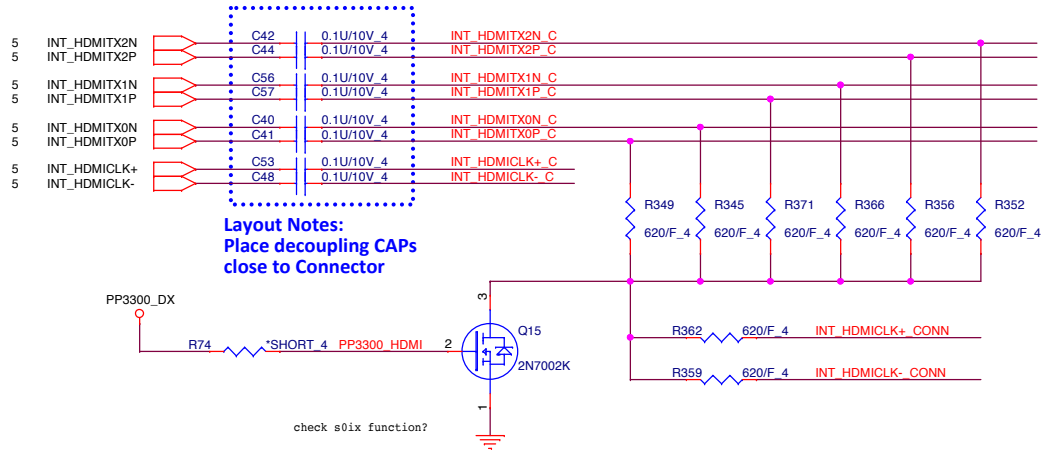
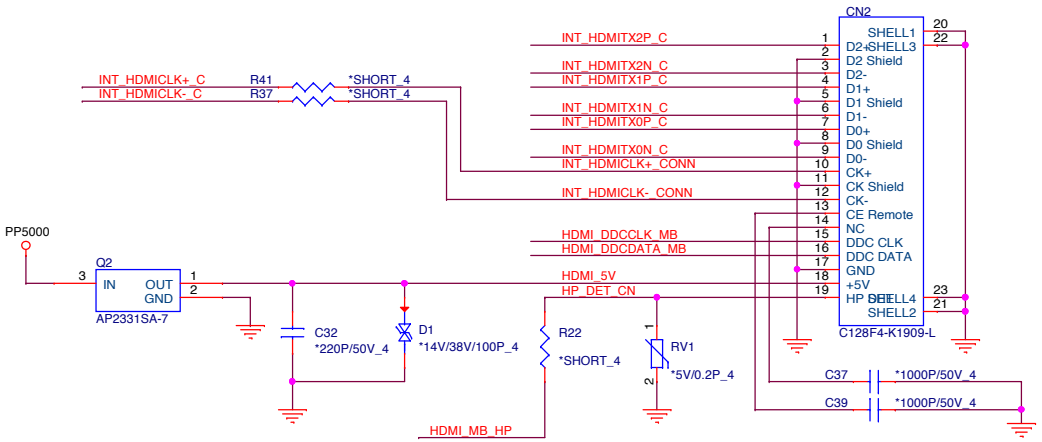
HDMI Cost Reduced level shift (HDM)

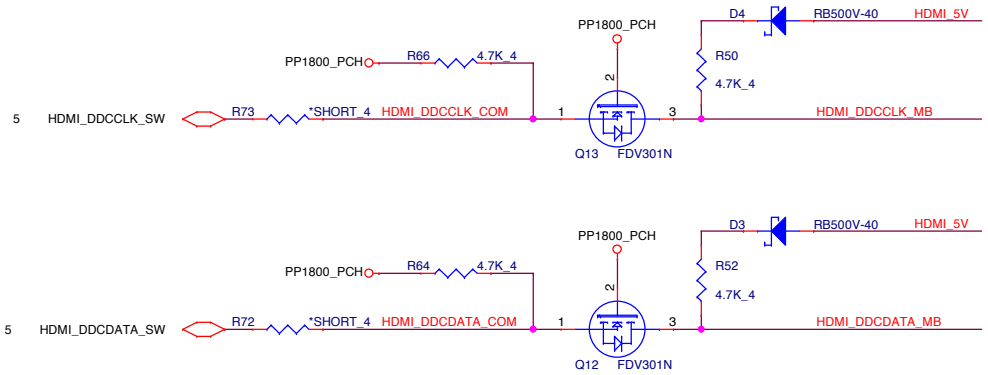


HDMI connector (HDM)

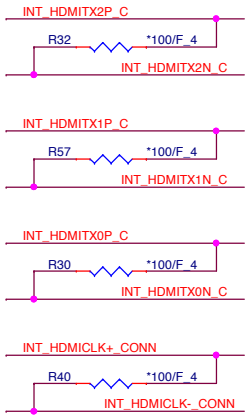
20



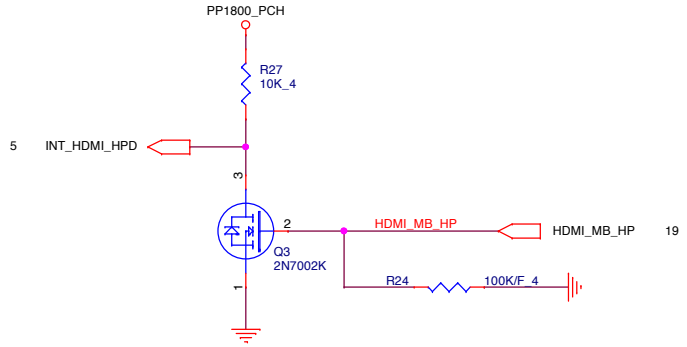
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



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WIFI/BT COMBO NGFF E KEY(MNC)

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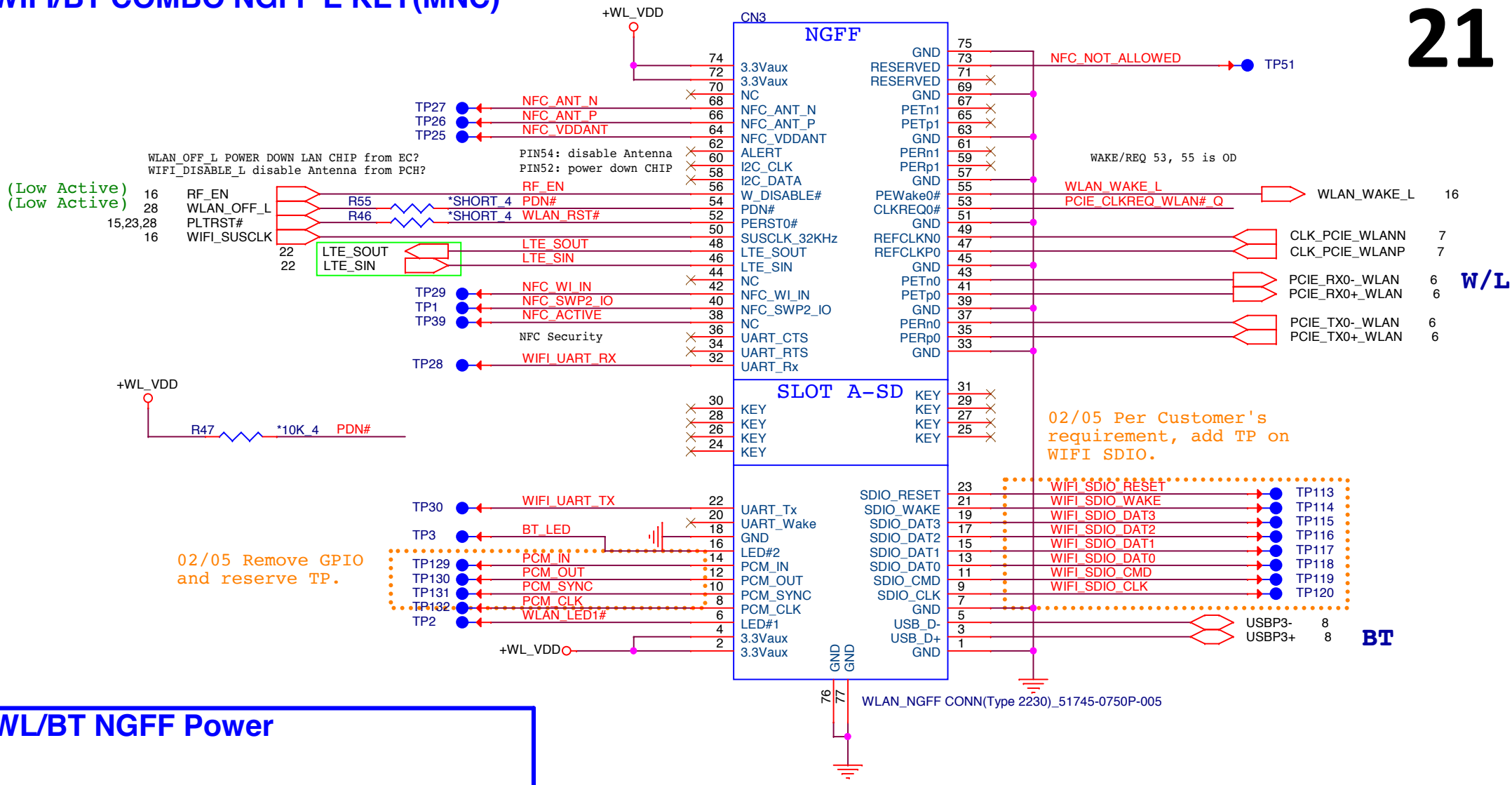
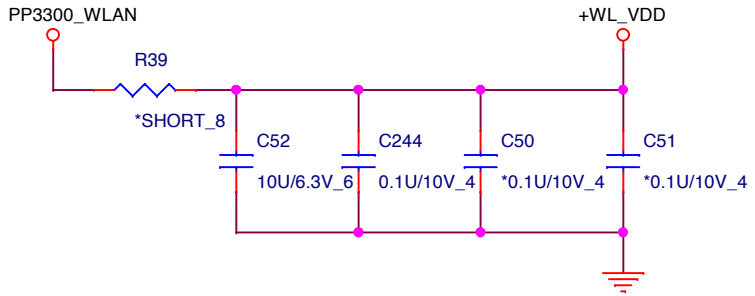
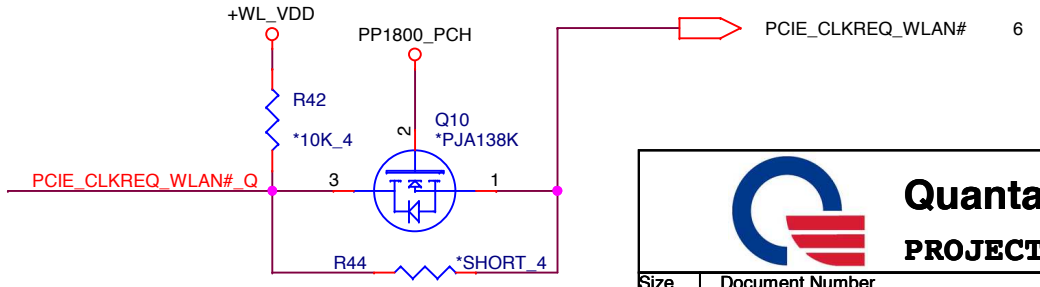


WL/BT NGFF Power





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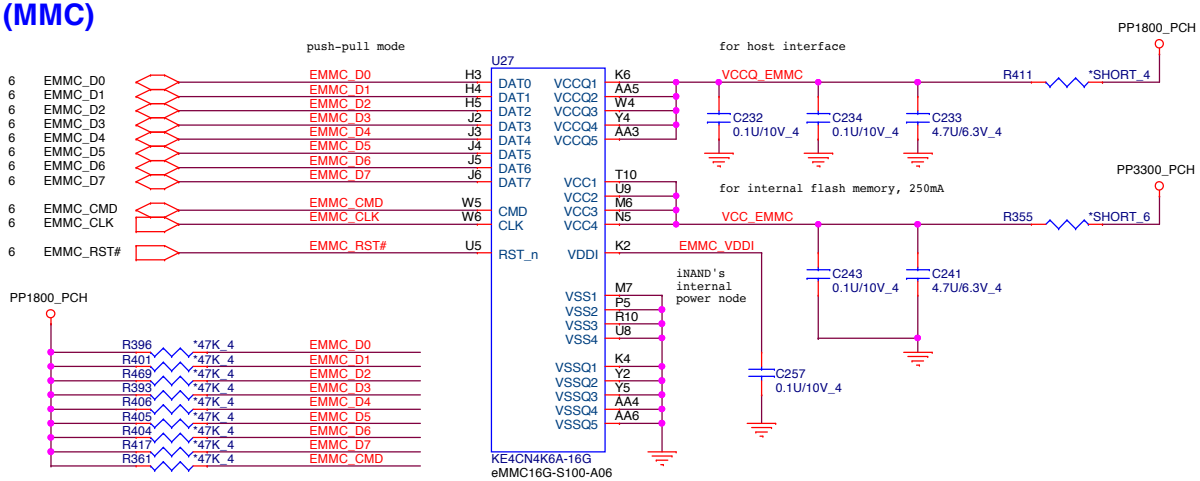
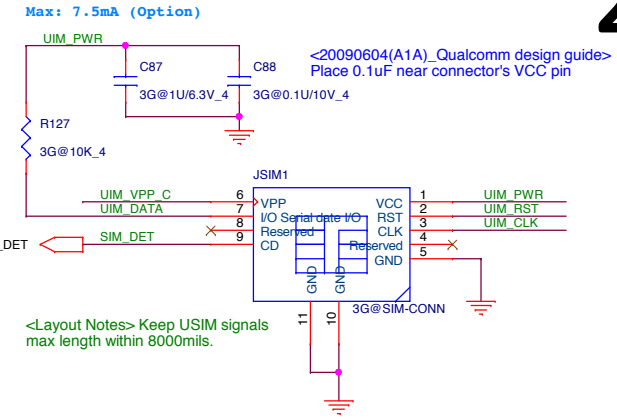
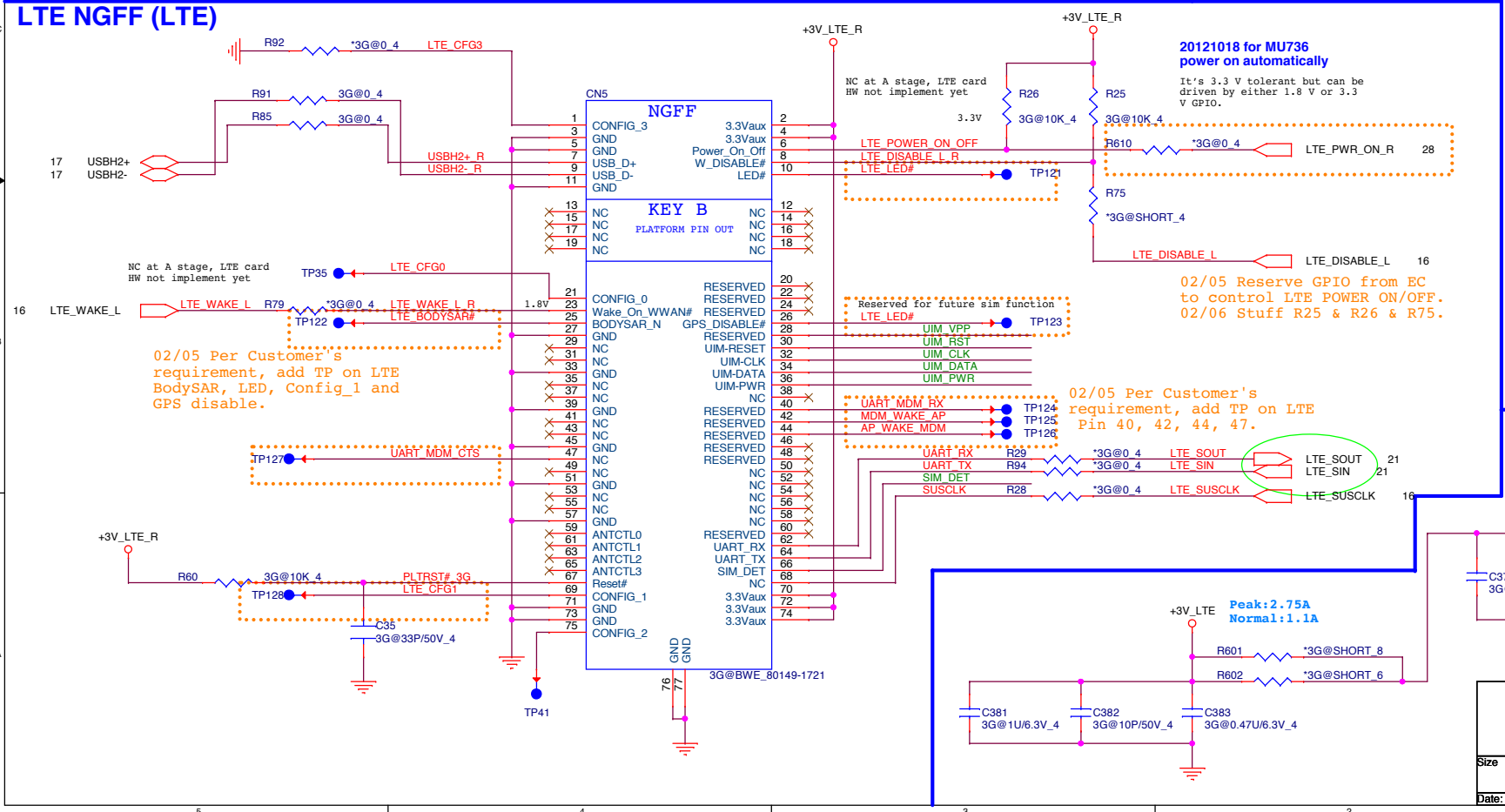
EMMC (MMC)

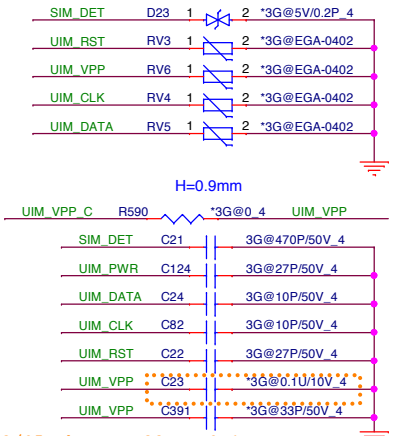


MultiMedia SIM (MNC)

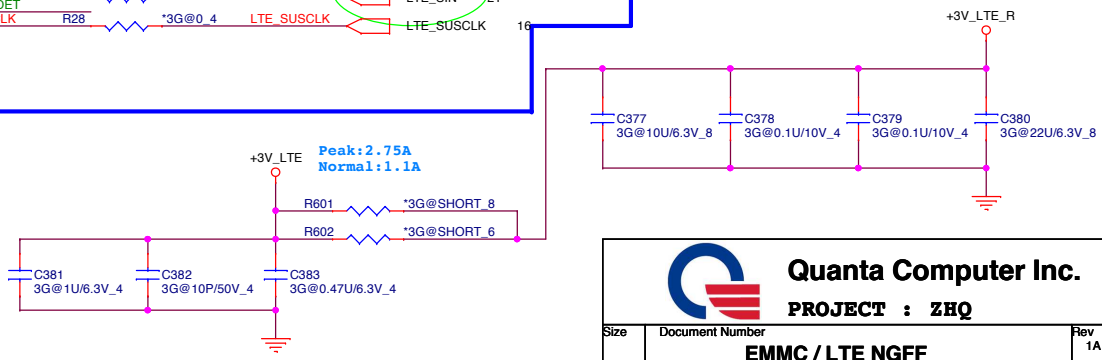


LTE NGFF (LTE)





LTE NGFF Power



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	EMMC / LTE NGFF	1A
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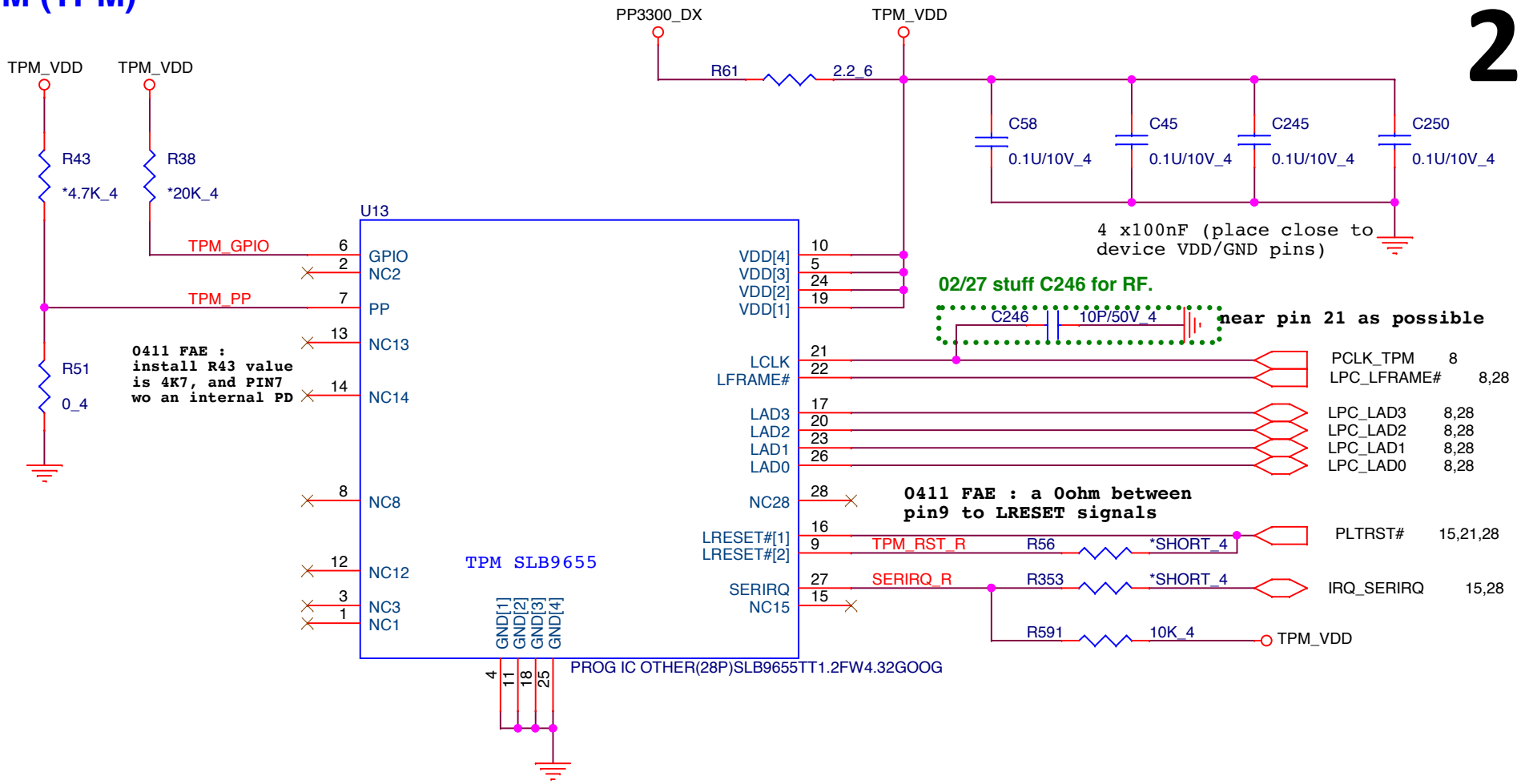
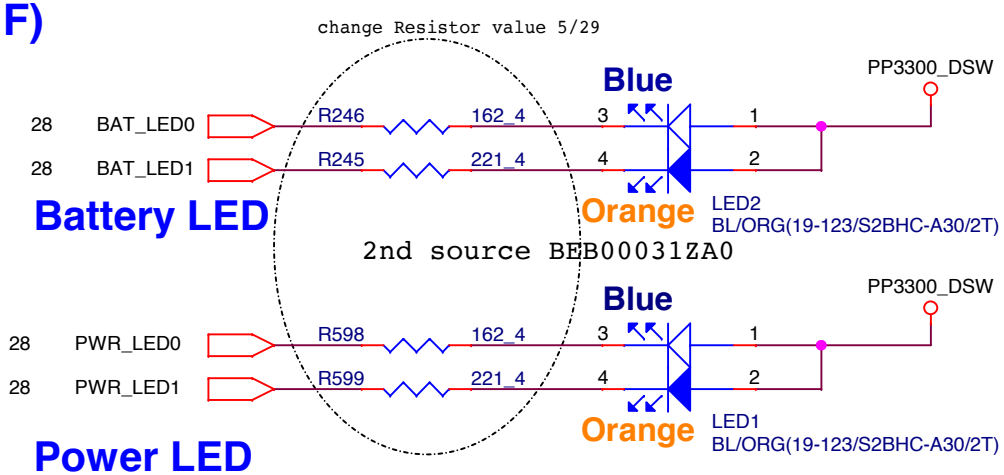
TPM (TPM)



LED(UIF)



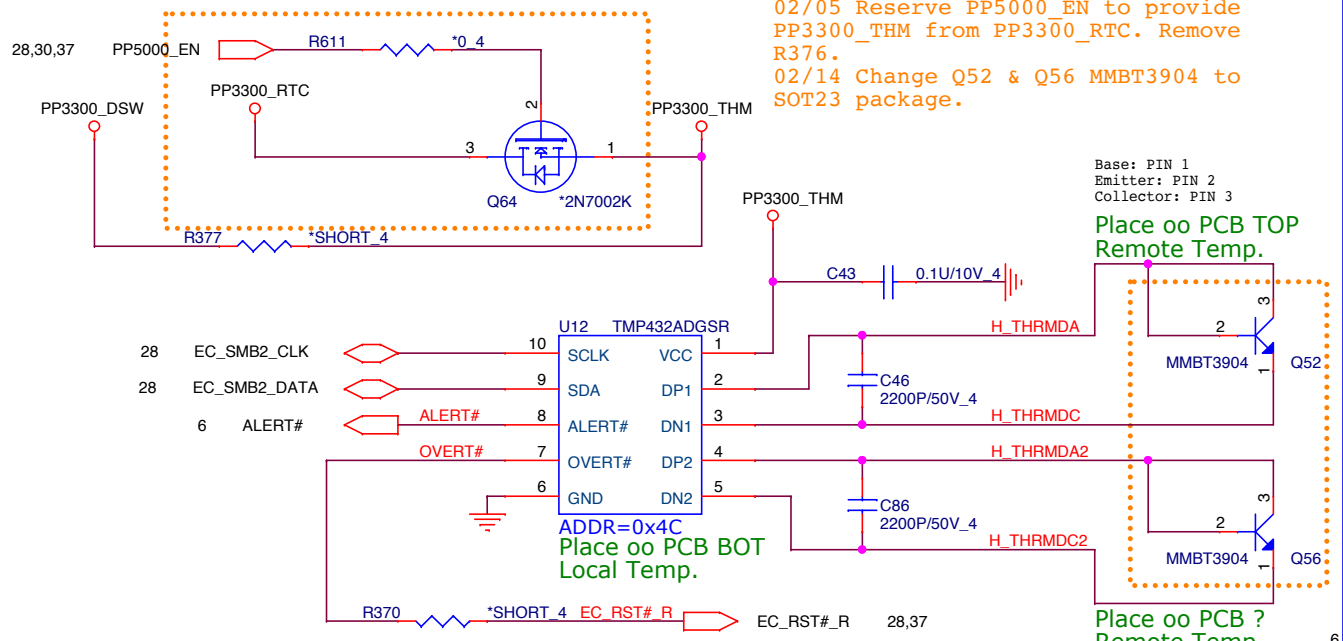
Quanta Computer Inc.

PROJECT : ZHQ

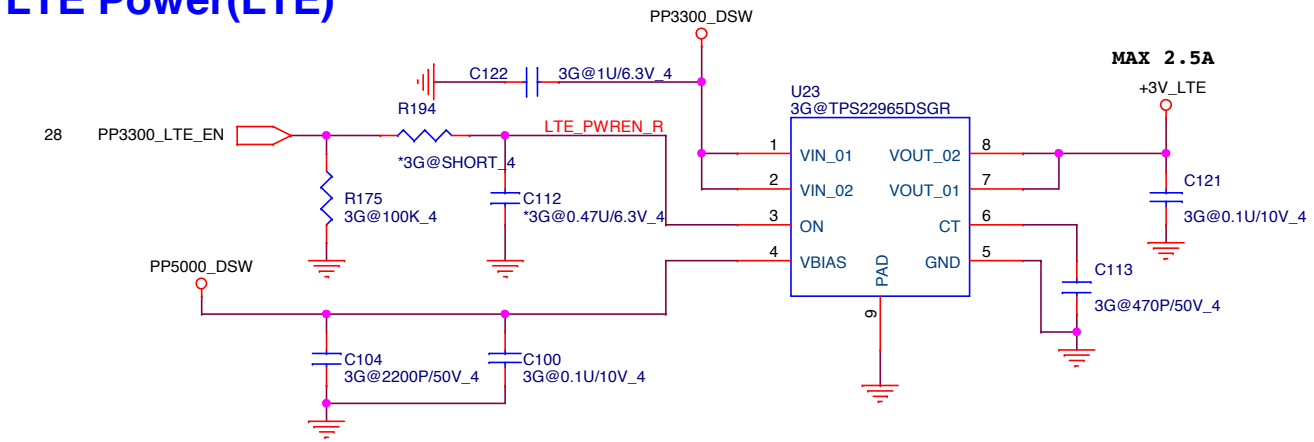
Size	Document Number	Rev
	TPM SLB9655 / LED	1A
Date: Thursday, July 03, 2014	Sheet 23 of 42	

Thermal Sensor(THM)

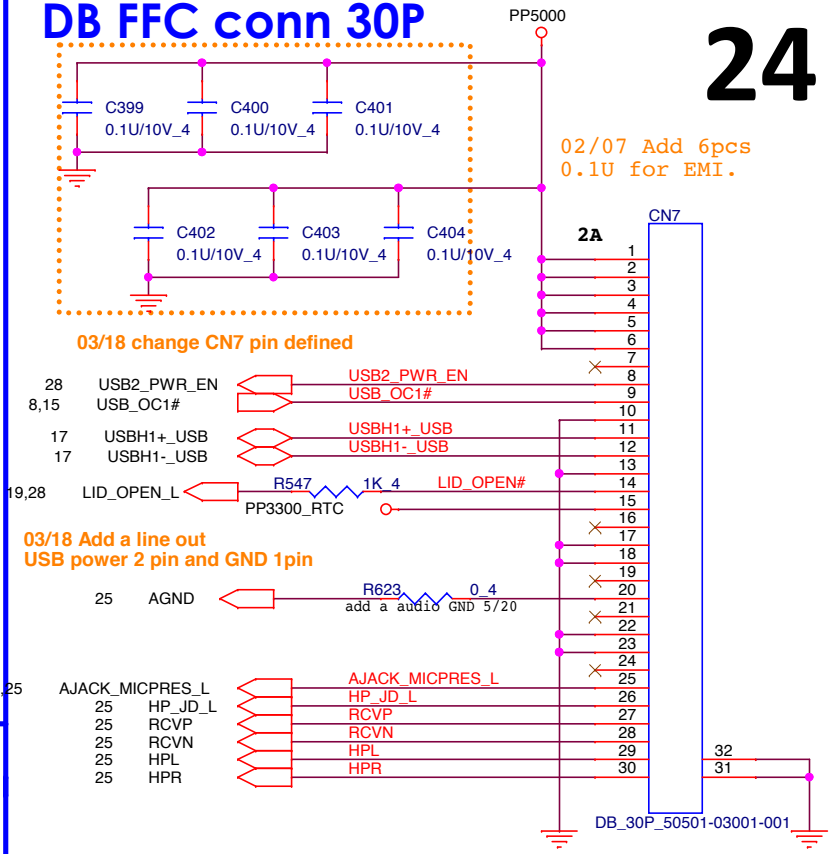
02/05 Reserve PP5000_EN to provide PP3300_THM from PP3300_RTC. Remove R376.
02/14 Change Q52 & Q56 MMBT3904 to SOT23 package.



LTE Power(LTE)



DB FFC conn 30P



USB 2.0_ILIM_SEL (USB)

01/28 remove USB ILIM SEL.

Quanta Computer Inc.
PROJECT : ZHQ

Size	Document Number	Rev
	DB/Thermal sensor/LTE PWR	1A
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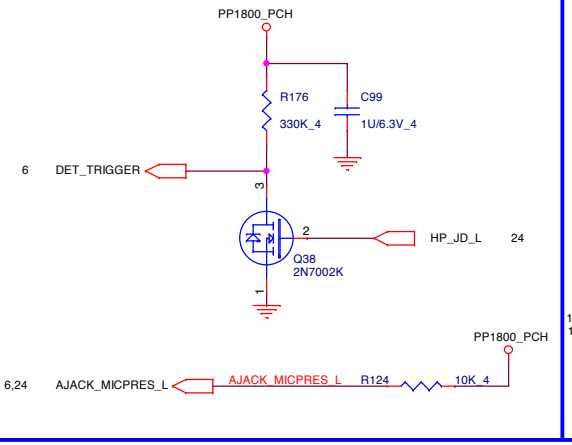
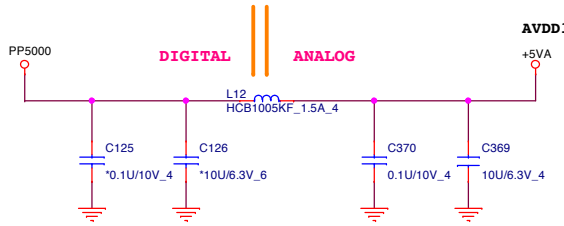
AUDIO CODEC (ADO)

25

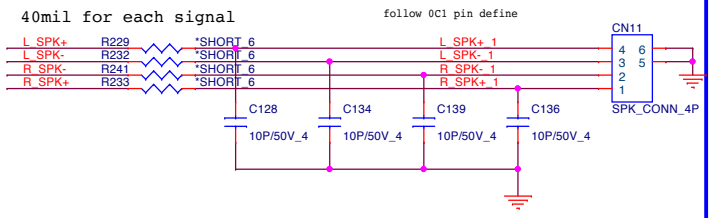
SOC DET (ADO)



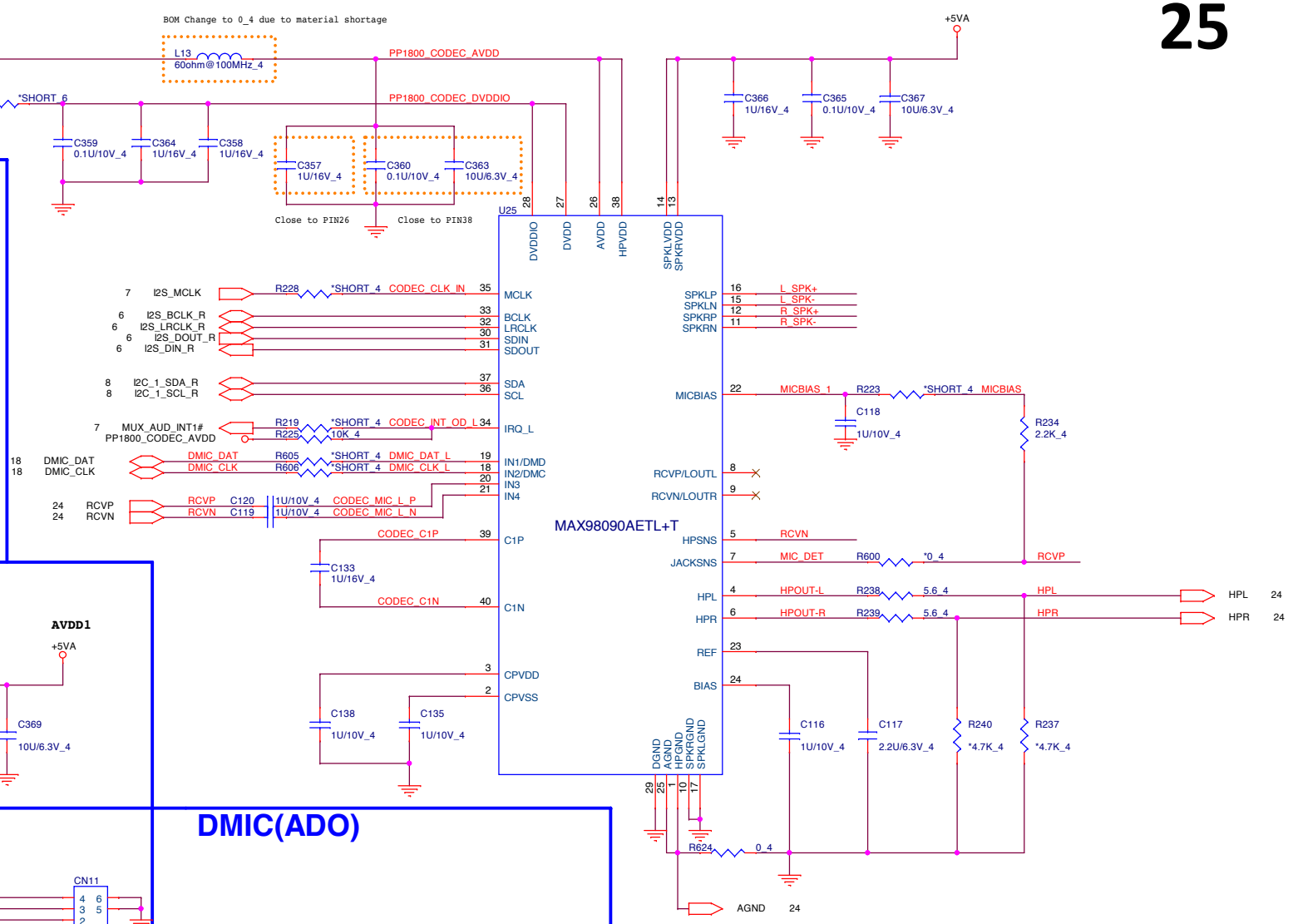
Codec PWR 5V (ADO)



Internal Speaker (ADO)

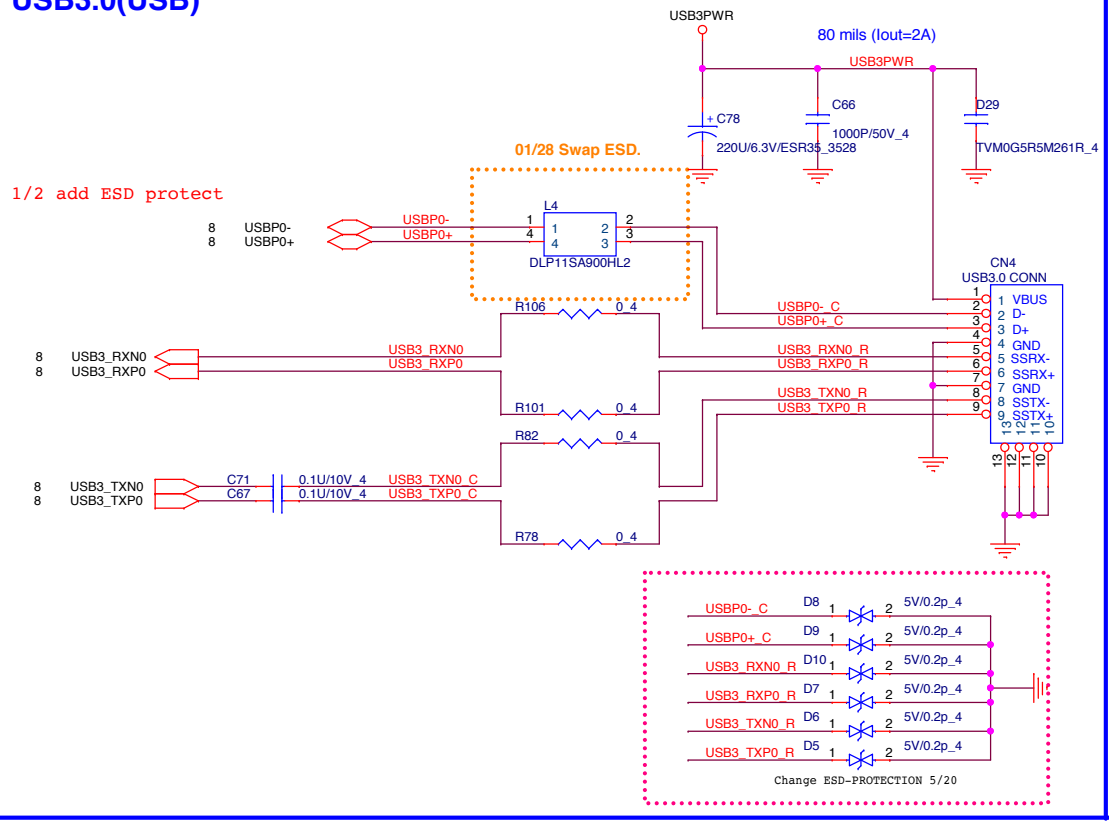


DMIC(ADO)



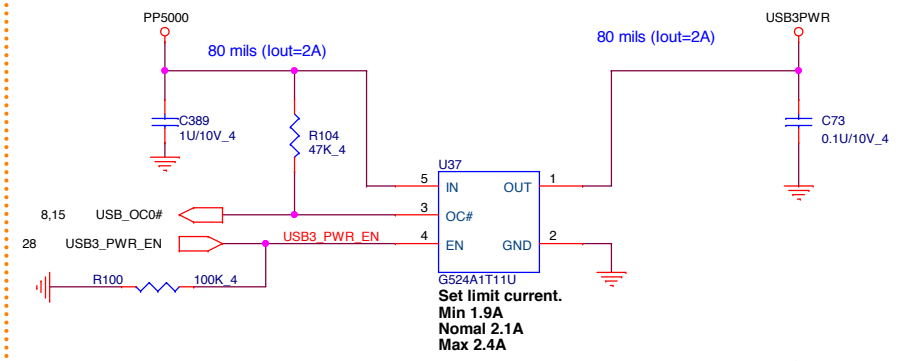
Quanta Computer Inc.
PROJECT : ZHQ
Size | Document Number | Rev
Audio Codec/SPK/DMIC | 1A
Date: Thursday, July 03, 2014 | Sheet 25 of 42

USB3.0(USB)



USB Switch

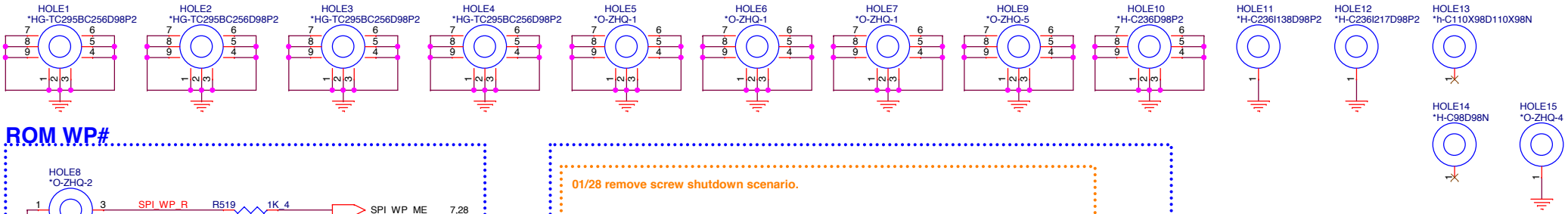
01/28 Change USB power chagreg to power switch.
Need update footprint.
02/11 Change USB power switch (U37) from G547F1P81U to G524C1T11U.



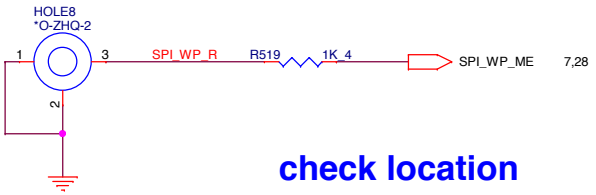
change USB power SW from G524C1T11U to G524A1T11U 3/18

HOLE(OTH)

02/13 Update hole footprint.



ROM WP#



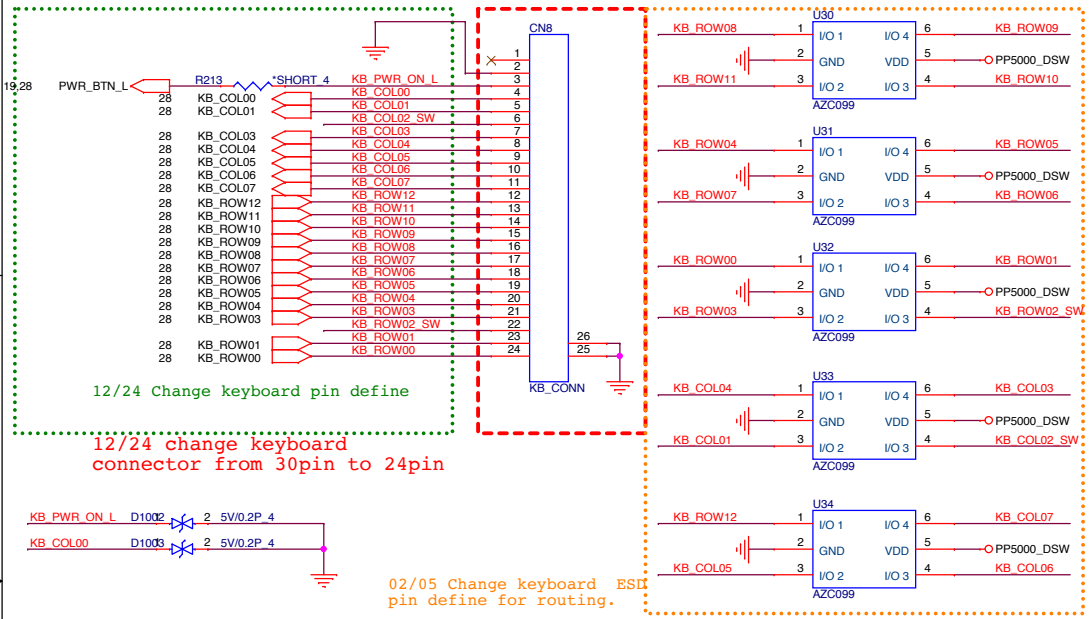
check location

01/28 remove screw shutdown scenario.

Quanta Computer Inc.
PROJECT : ZHQ

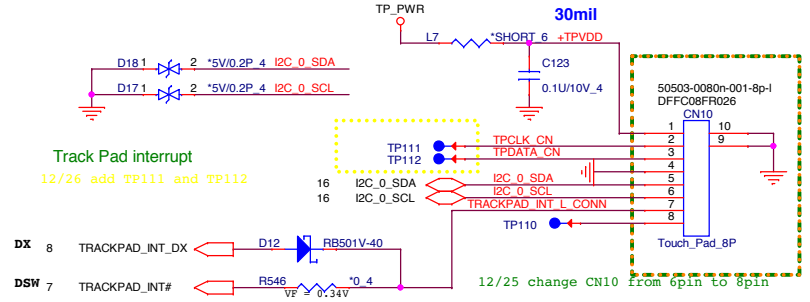
Size	Document Number	Rev
	USB3/Hole	1A
Date: Thursday, July 03, 2014	Sheet 26 of 42	

K/B (KBC)



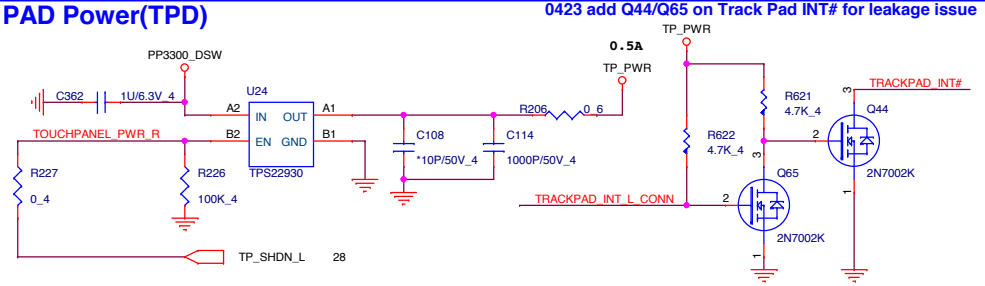
Track PAD BOARD CONN (TPD)

02/07 Swap TP pin definition.

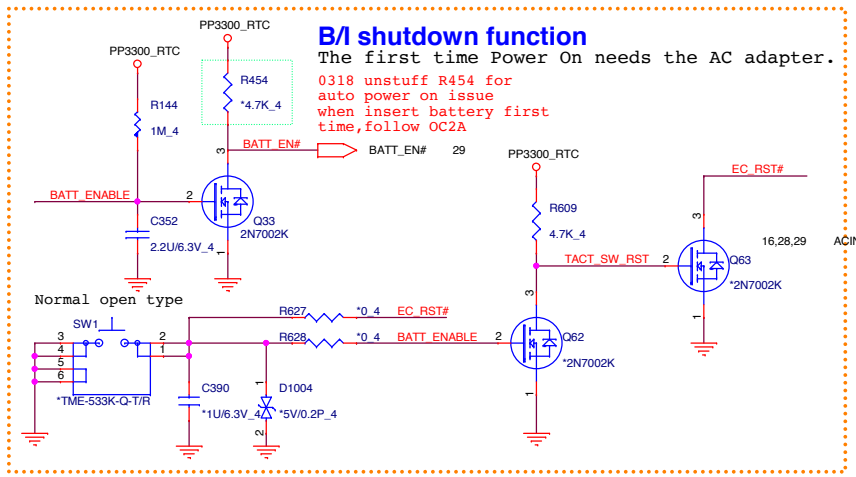


Track PAD Power(TPD)

0423 add Q44/Q65 on Track Pad INT# for leakage issue



HOLELESS RESET 2-CHIP(KBC)

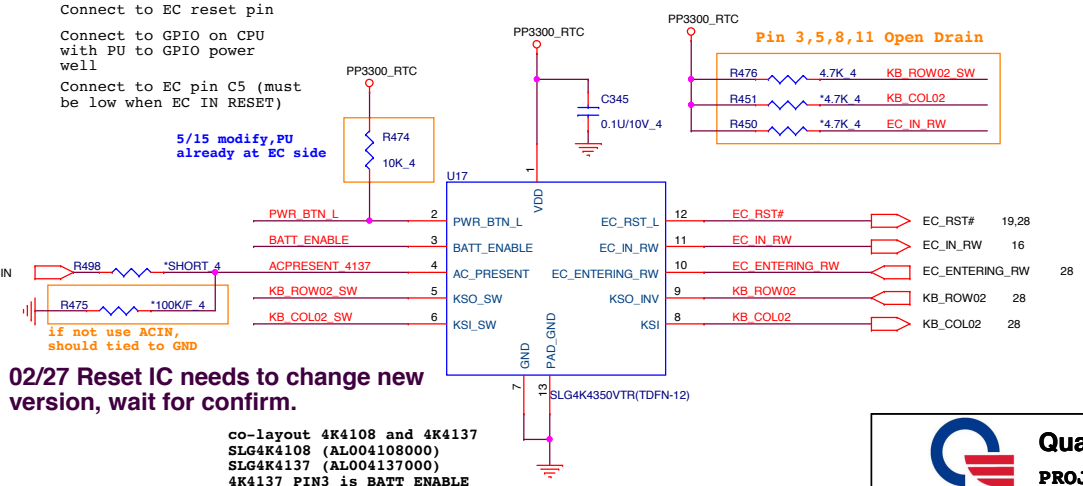


Connect to EC reset pin

Connect to GPIO on CPU with PU to GPIO power well

Connect to EC pin C5 (must be low when EC IN RESET)

5/15 modify,PU already at EC side



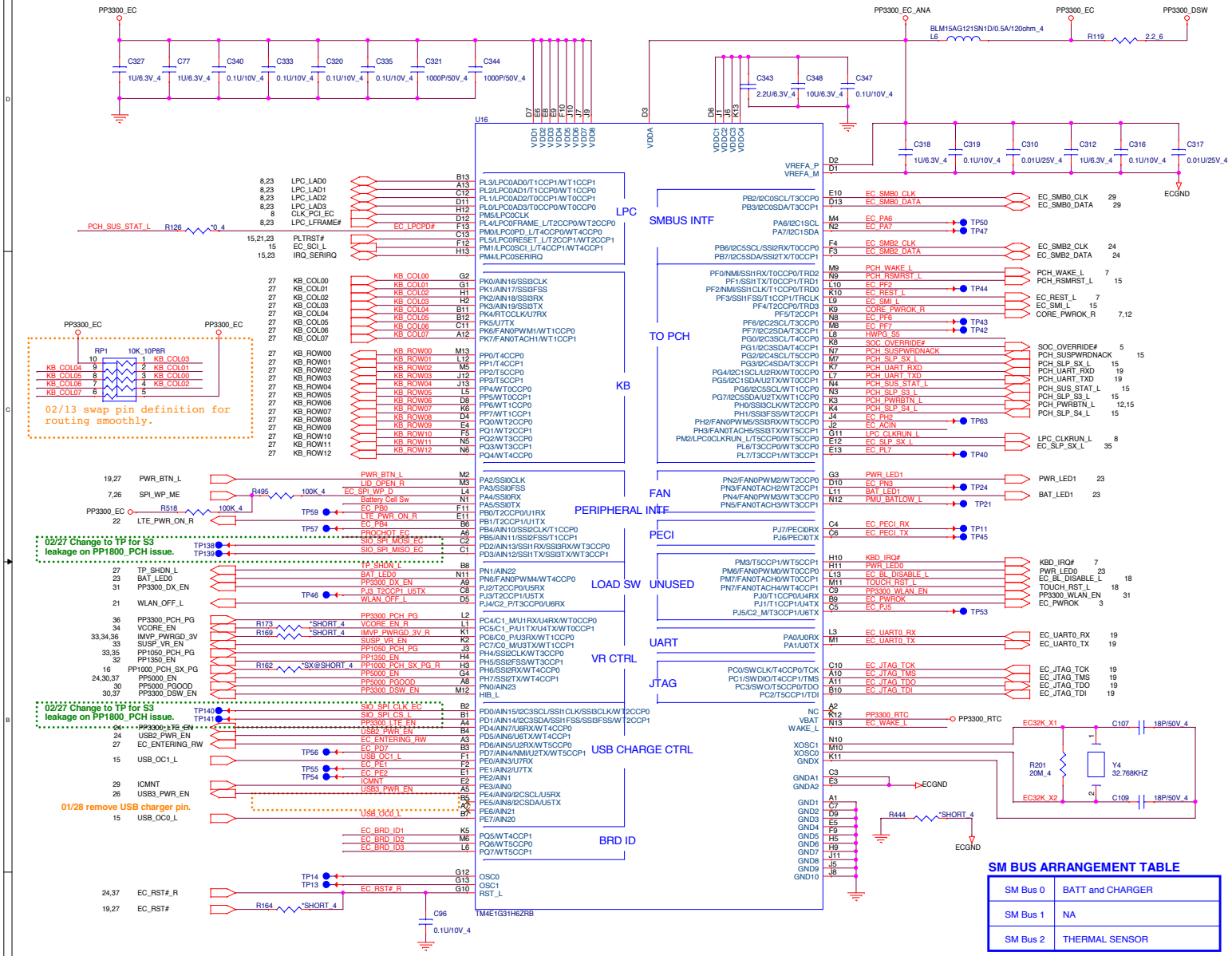
02/27 Reset IC needs to change new version, wait for confirm.

co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

Quanta Computer Inc.
PROJECT : ZHQ

Size	Document Number	Rev
	KB/TP/HW Reset	1A
Date: Thursday, July 03, 2014	Sheet 27 of 42	

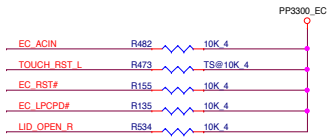
EC(KBC)



SM BUS ARRANGEMENT TABLE

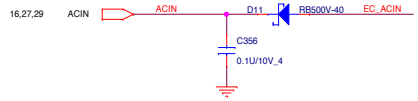
SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

Pull-up(KBC)

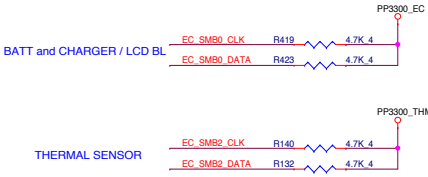


LID_OPEN(KBC)

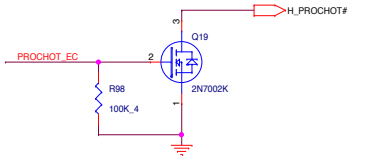
ACIN_EC(KBC)



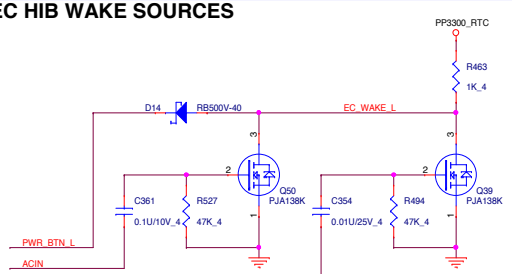
SM BUS/I2C PU(KBC)



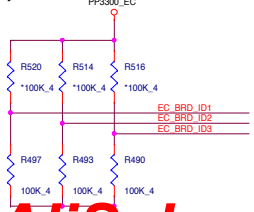
PROCHOT_EC(KBC)



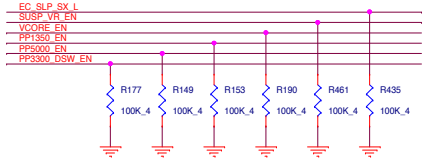
EC HIB WAKE SOURCES



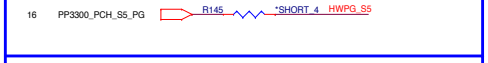
Board_ID(KBC)



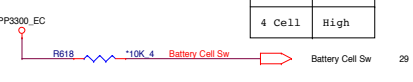
Pull-down(KBC)



HWPG(KBC)



Battery cell select

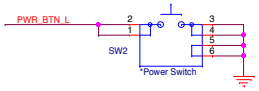


3 Cell	float
4 Cell	High

OD pin list

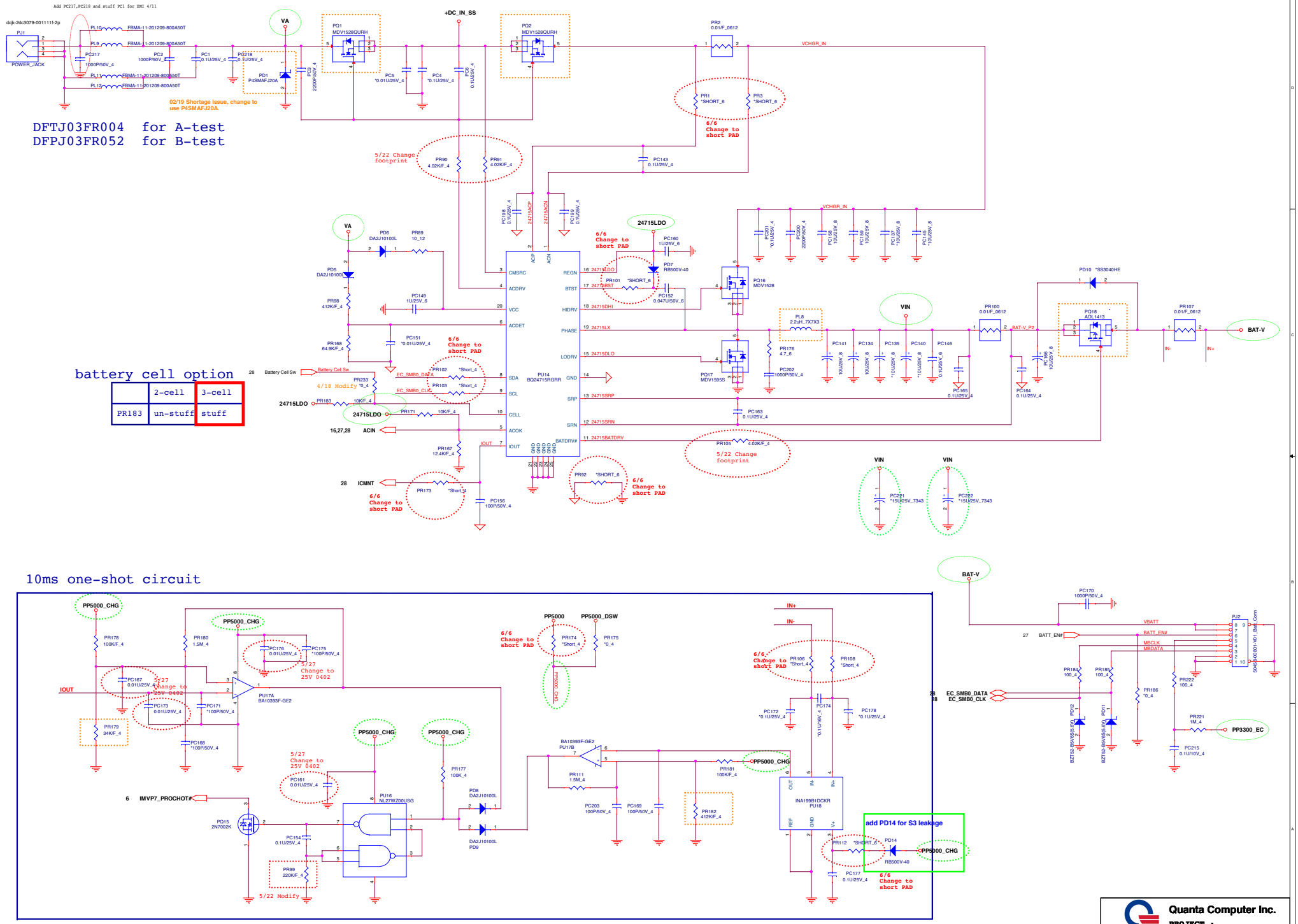
- EC_REST_L
- BAT_LED0
- BAT_LED1
- PCH_RSMRST_L
- SMBUS
- IRQ_SERIRQ
- EC_BL_DISABLE_L

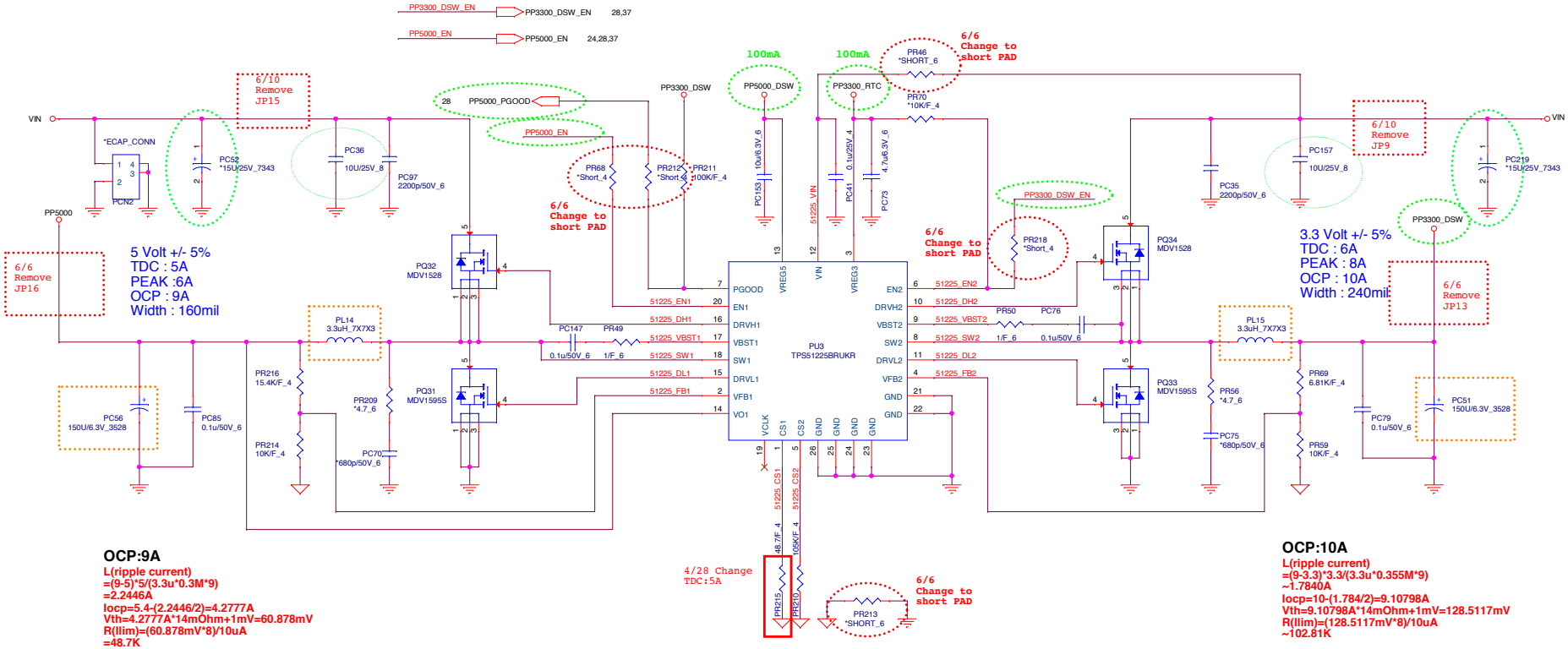
For testing only



Quanta Computer Inc.
PROJECT : ZHQ

Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1A
Date: Thursday, July 03, 2014	Sheet 28 of 42	


Add PC217,PC218 and stuff PC1 for EMI 4/11
dcjk-2dc3079-0011111-2p
POWER_JACK
02/19 Shortage issue, change to use P4SMAFJ20A.
DFTJ03FR004 for A-test
DFPJ03FR052 for B-test
5/22 Change footprint
6/6 Change to short PAD
battery cell option
2-cell
3-cell
PR183
un-stuff
stuff
4/18 Modify
10ms one-shot circuit
5/27 Change to 25V 0402
5/22 Modify
add PD14 for S3 leakage
Quanta Computer Inc.
PROJECT :
Charger(BQ24715)
Thursday, July 03, 2014
Sheet 29 of 42



OCP:9A

L(ripple current)
=(9-5)*5/(3.3u*0.3M*9)
=2.2446A
Iocp=5.4-(2.2446/2)=4.2777A
Vth=4.2777A*14mOhm+1mV=60.878mV
R(Ilim)=(60.878mV*8)/10uA
=48.7K

OCP:10A

L(ripple current)
=(9-3.3)*3.3/(3.3u*0.355M*9)
~1.7840A
Iocp=10-(1.784/2)=9.10798A
Vth=9.10798A*14mOhm+1mV=128.5117mV
R(Ilim)=(128.5117mV*8)/10uA
~102.81K

6/10 Ramp Renove PU22,PU11

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	SYSTEM 5V/3V (TPS51225BRUKR)	1A
Date: Thursday, July 03, 2014	Sheet 30 of 42	

36 PP1800_PCH_S5_PG
28 PP3300_DX_EN

PP1800_PCH_S5_PG
PP3300_DX_EN

PP3300_DSW
PR71 *Short_8
PP3300_DX
PR63 *0_8
PC82 1U/10V_4

6/6 Change to short PAD

28 PP3300_WLAN_EN

PP3300_WLAN_R
PR60 *0_8
PU6
A2 IN OUT A1
EN GND B1
TPS22930
PP3300_WLAN

PP3300_WLAN_EN
PR44 Short_4
PP3300_WLAN_EN_R
PR53 100K/F_4
PC63 *0.1U/50V_6

6/6 Change to short PAD

DX should be earlier than VREN by EC.

PP3300_DSW
PC162 1U/10V_4
PP1800_PCH_S5_PG
PR95 Short_4
PR96 *100K/F_4
PC148 *0.1U/50V_6
PU13
A2 IN OUT A1
B2 EN GND B1
TPS22930
PP3300_PCH_S5

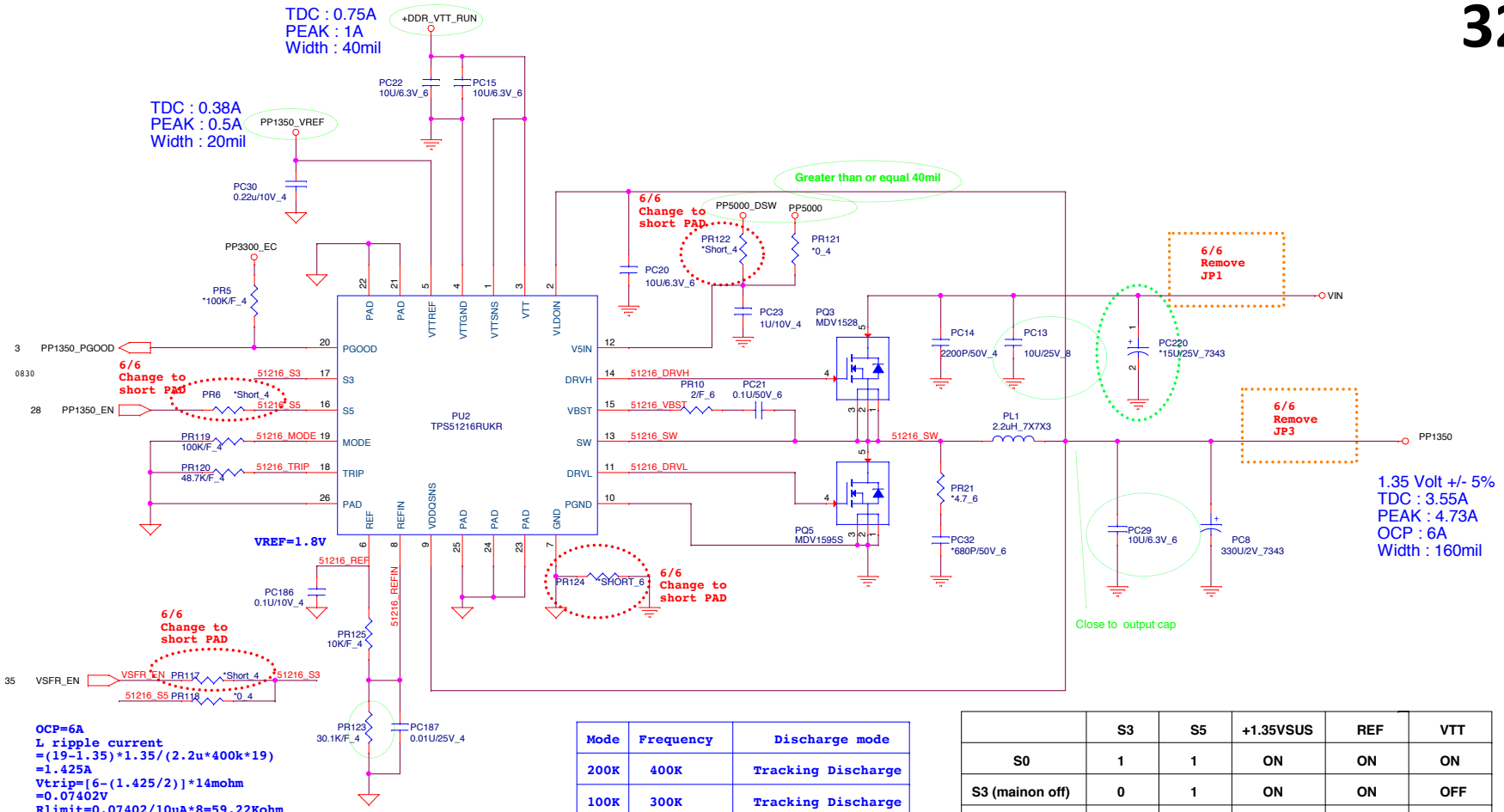
6/6 Change to short PAD

PP3300_DSW
PC17 1U/10V_4
PP3300_DX_EN
PR15 Short_4
PP3300_DX_EN_R
PR14 100K/F_4
PU1
A2 IN1 OUT1 A1
B2 IN2 OUT2 B1
C2 EN GND C1
TPS22964CYZPR
PP3300_DX

6/6 Change to short PAD

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	Load Switch	1A
Date: Thursday, July 03, 2014	Sheet 31 of 42	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

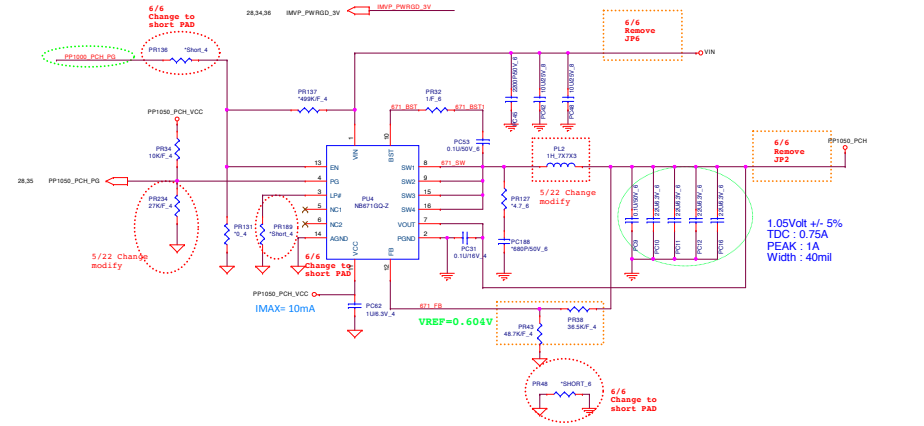
6/10 Ramp Renove PU20

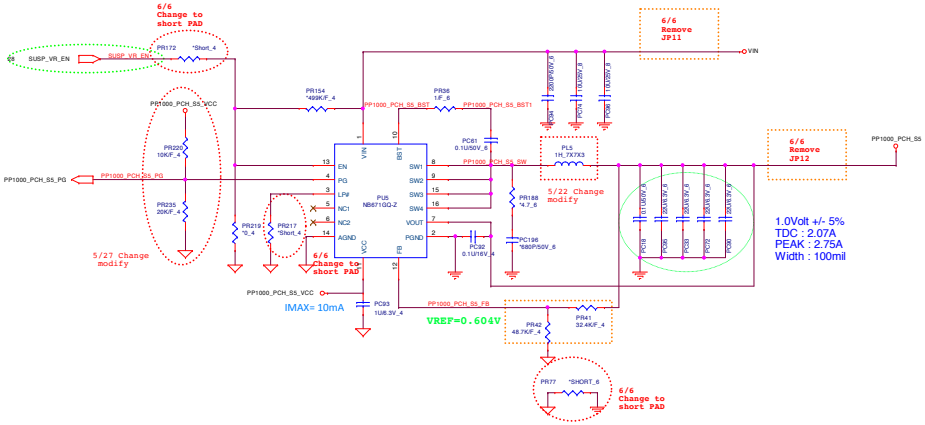
Quanta Computer Inc.

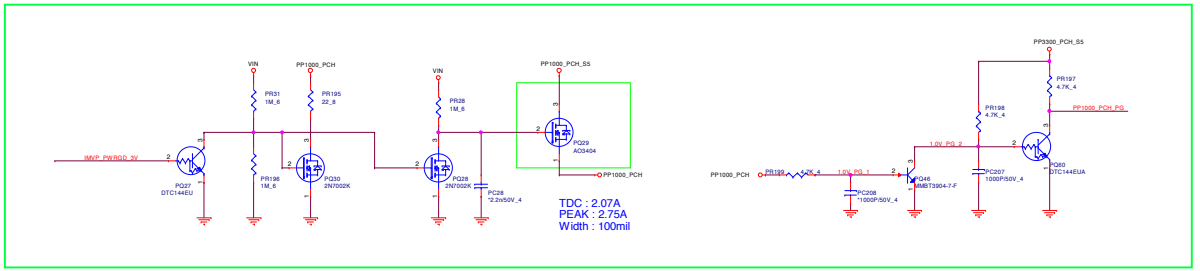
PROJECT :

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	1A

Date: Thursday, July 03, 2014 Sheet 32 of 42

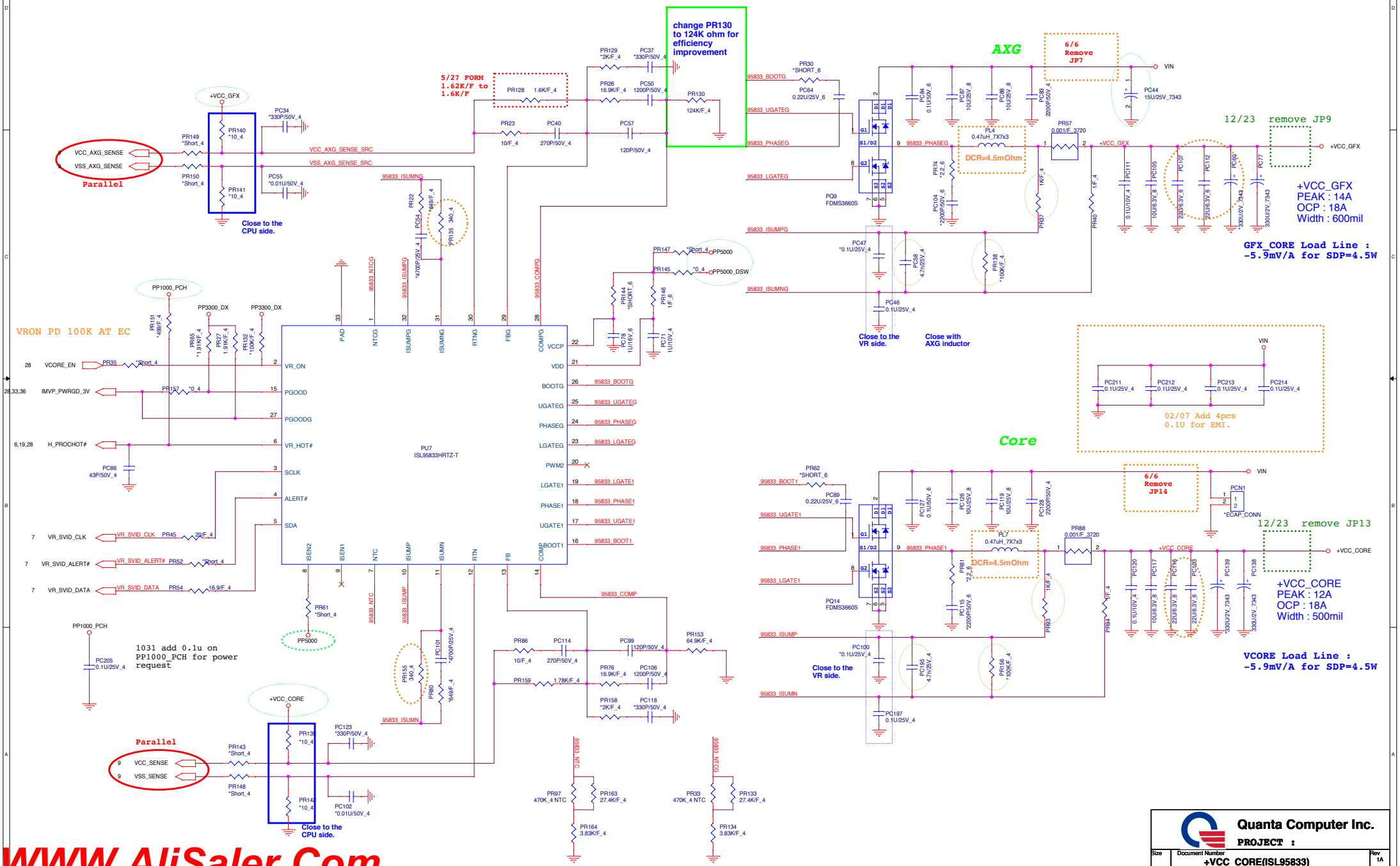




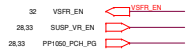


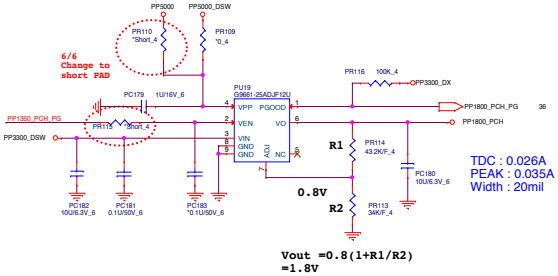
6/10 Ramp Renove PU21,PU23

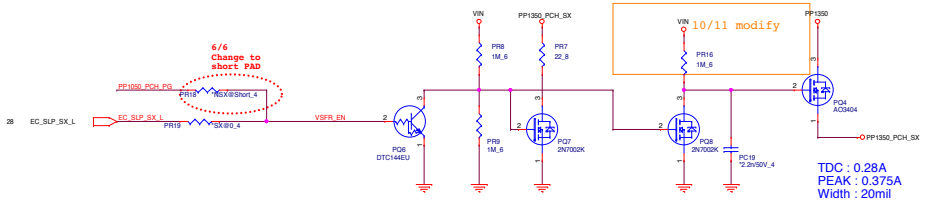
Quanta Computer Inc.
PROJECT :
Size | Document Number | Rev
+1.05V/+1V(NB671LGQ-Z) | 1A
Date: Thursday, July 03, 2014 | Sheet 33 of 42

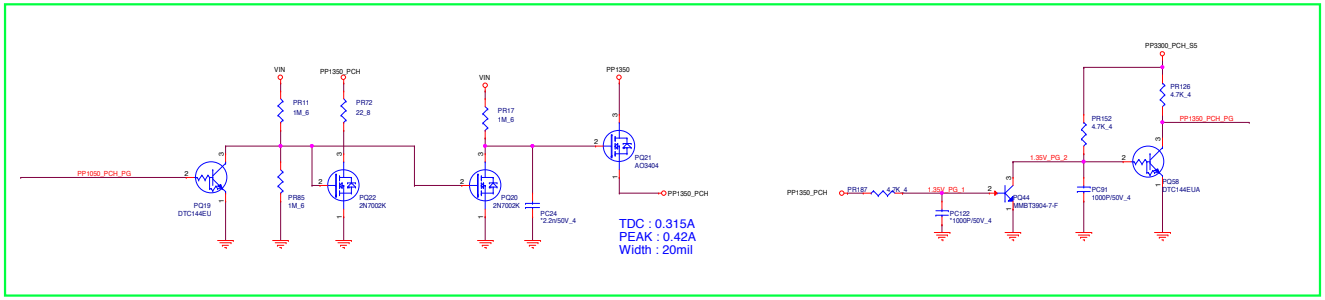


Quanta Computer Inc.
PROJECT :
Size | Document Number: +VCC_CORE(ISL95833) | Rev: 1A
Date: Thursday, July 03, 2014 | Sheet 34 of 42







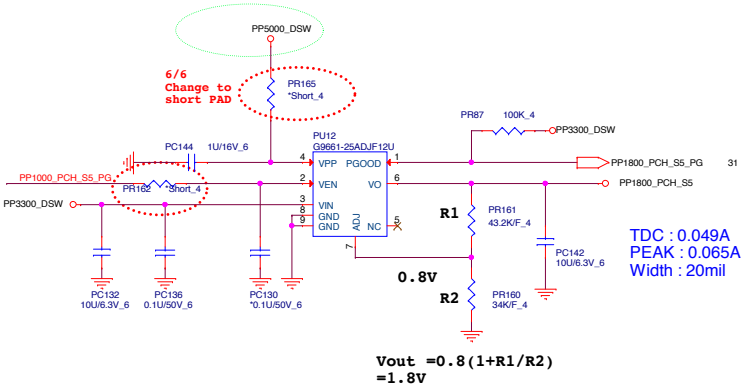


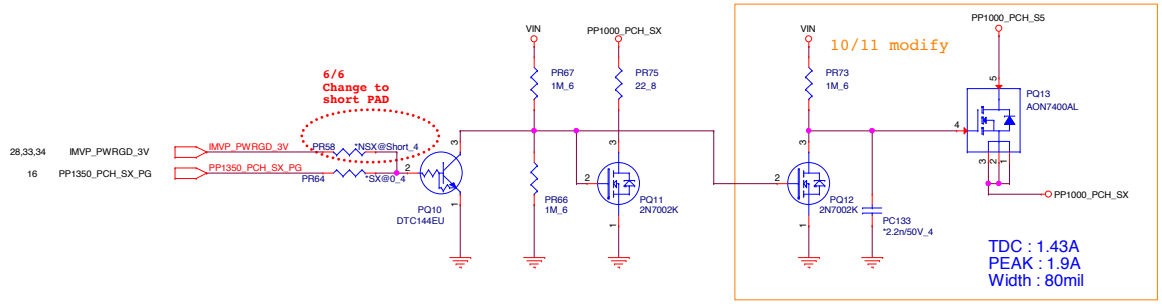
Quanta Computer Inc.

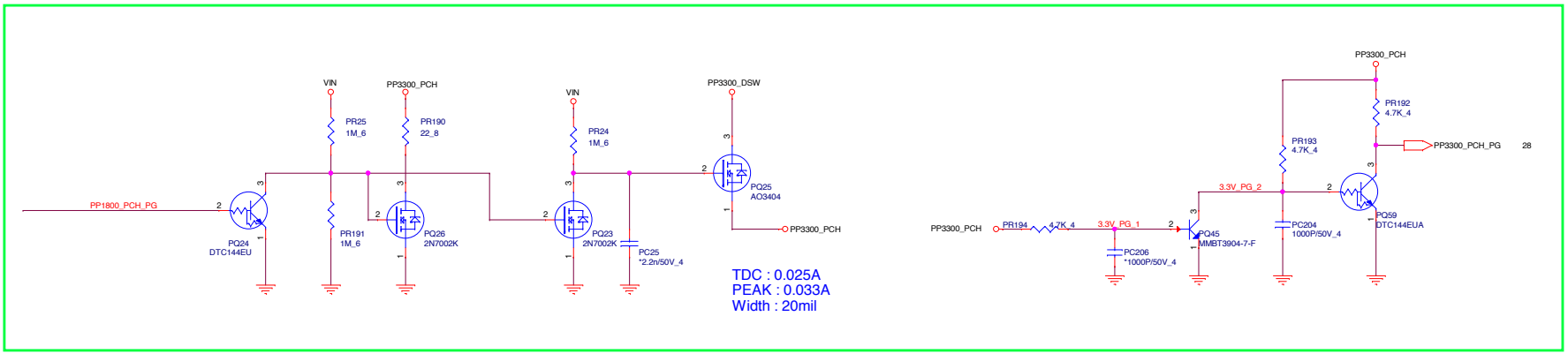
PROJECT : 2

Size	Document Number	Rev
	LDO (1V/1.35V/1.5V/1.8V)	1A
Date: Thursday, July 03, 2014	Sheet 35 of 42	

35 PP1800_PCH_PG
33 PP1000_PCH_S5_PG







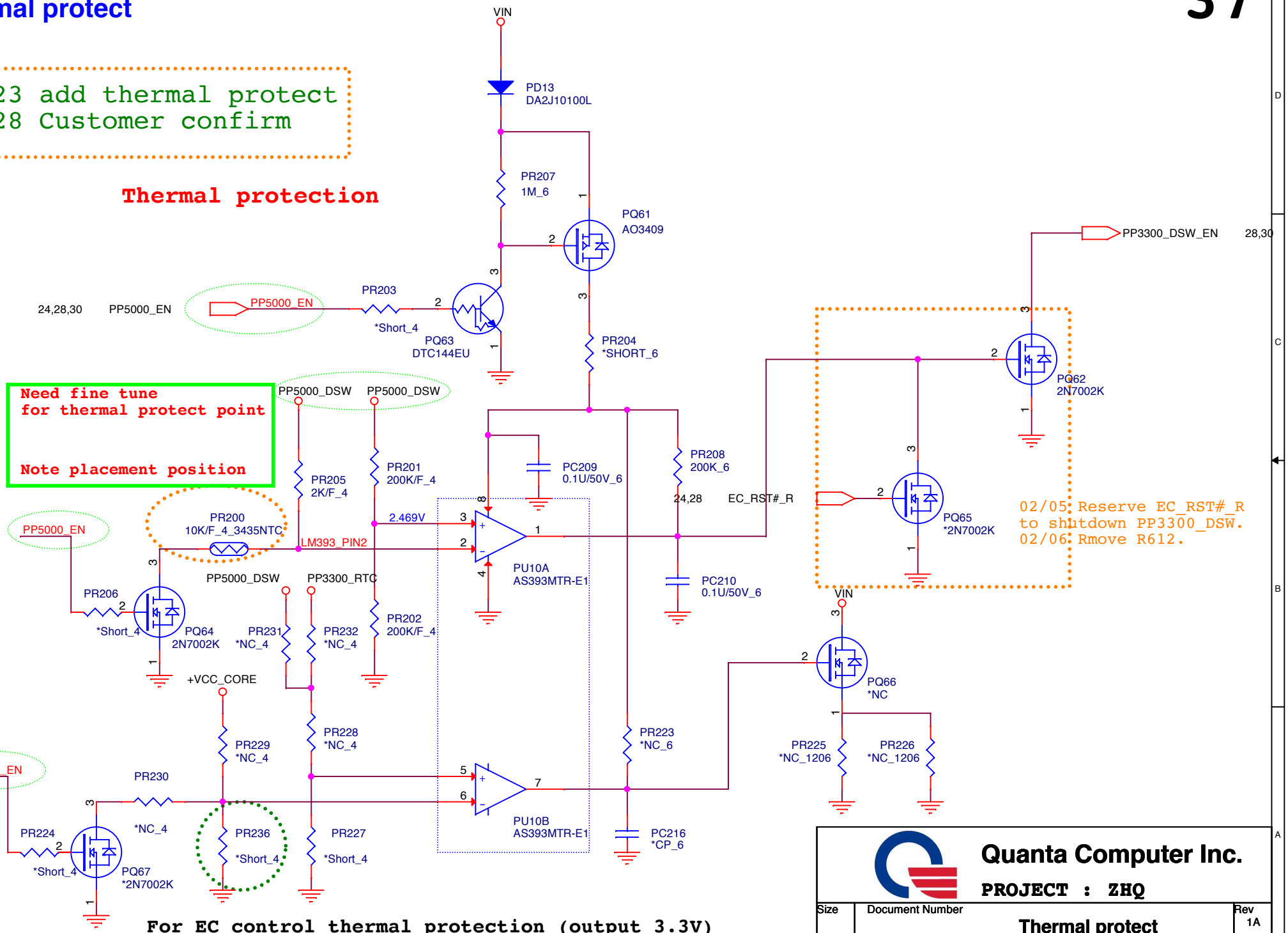
Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	LDO(1.2V/3.3V/1.8V)	1A
Date: Thursday, July 03, 2014	Sheet 36 of 42	

Thermal protect

12/23 add thermal protect
01/28 Customer confirm

Thermal protection

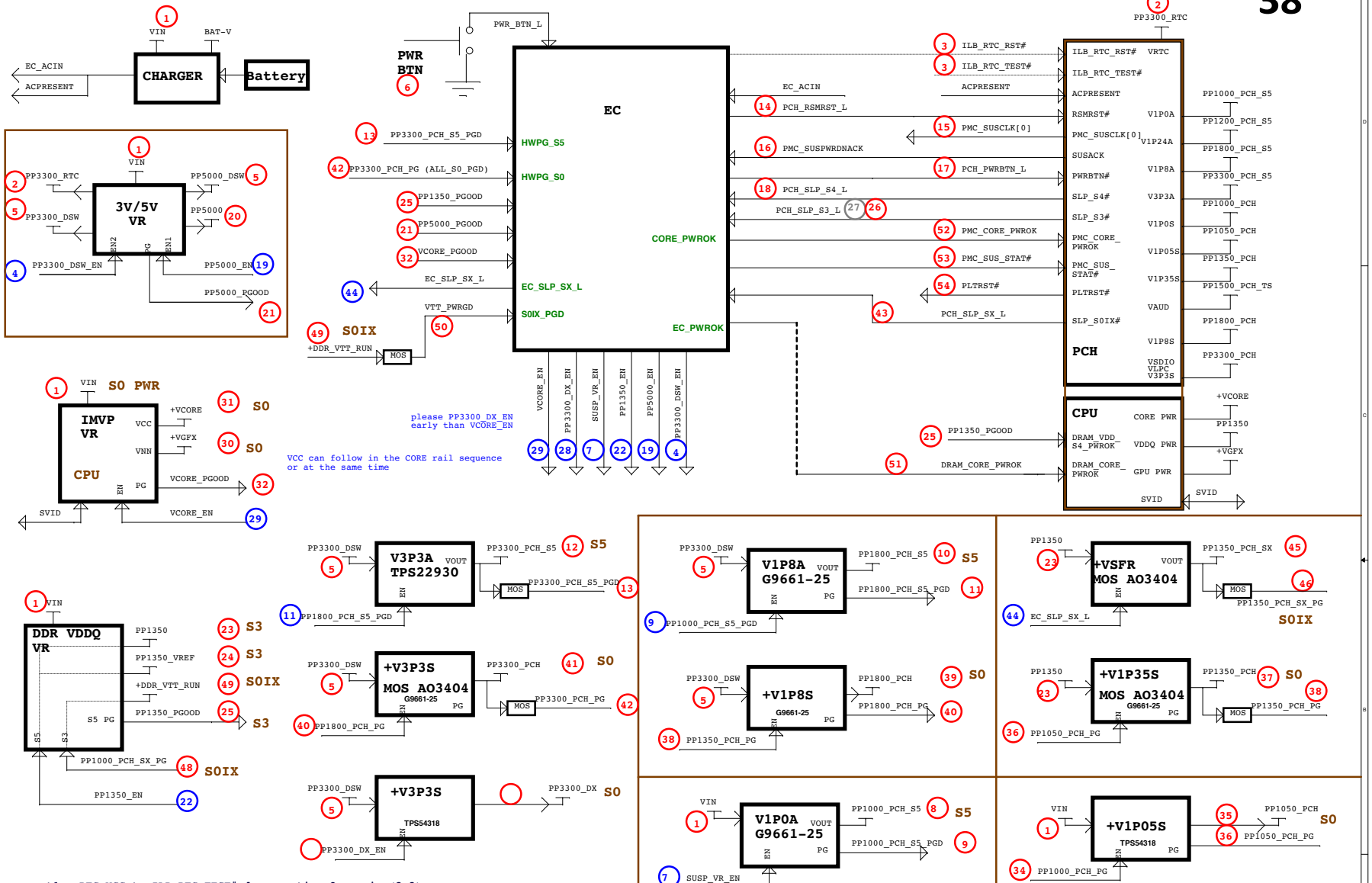


For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZHQ

Size	Document Number	Rev
	Thermal protect	1A
Date: Thursday, July 03, 2014	Sheet 37 of 42	

Support S0iX



t1 : RTC_VCC to ILB_RTC_TEST# de-assertion 9ms -min (2-3)
t1 : RTC_VCC to PMC_RSMRST# de-assertion 9ms-min (2-11)

t2 : V3P3A valid to PMC_RSMRST# de-assertion 10us -min (8-11)

t3 : PMC_RSMRST# to Internal RTC clock stable 100ms -max (11- RTC clock)

t4 : Internal RTC clock stable to PMC_SUSCLK[0] toggling 5ms -min (RTC clock - 12)

t5 : PMC_SLP_S4# de-assertion to PMC_SLP_S3# de-assertion 30us -min (15-25)

t6a : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (no PCIE device) 10ms -min (43-45)
t6b : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by pcie device) 99ms -min (43-45)

t7 : DRAM/PMC_CORE_PWROK to PMC_SUS_STAT# 1ms -min (45-46)

t8 : PMC_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion 60us -min (46-47)

a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling

Quanta Computer Inc.
PROJECT : ZHQ
Power Sequence
Rev 1A
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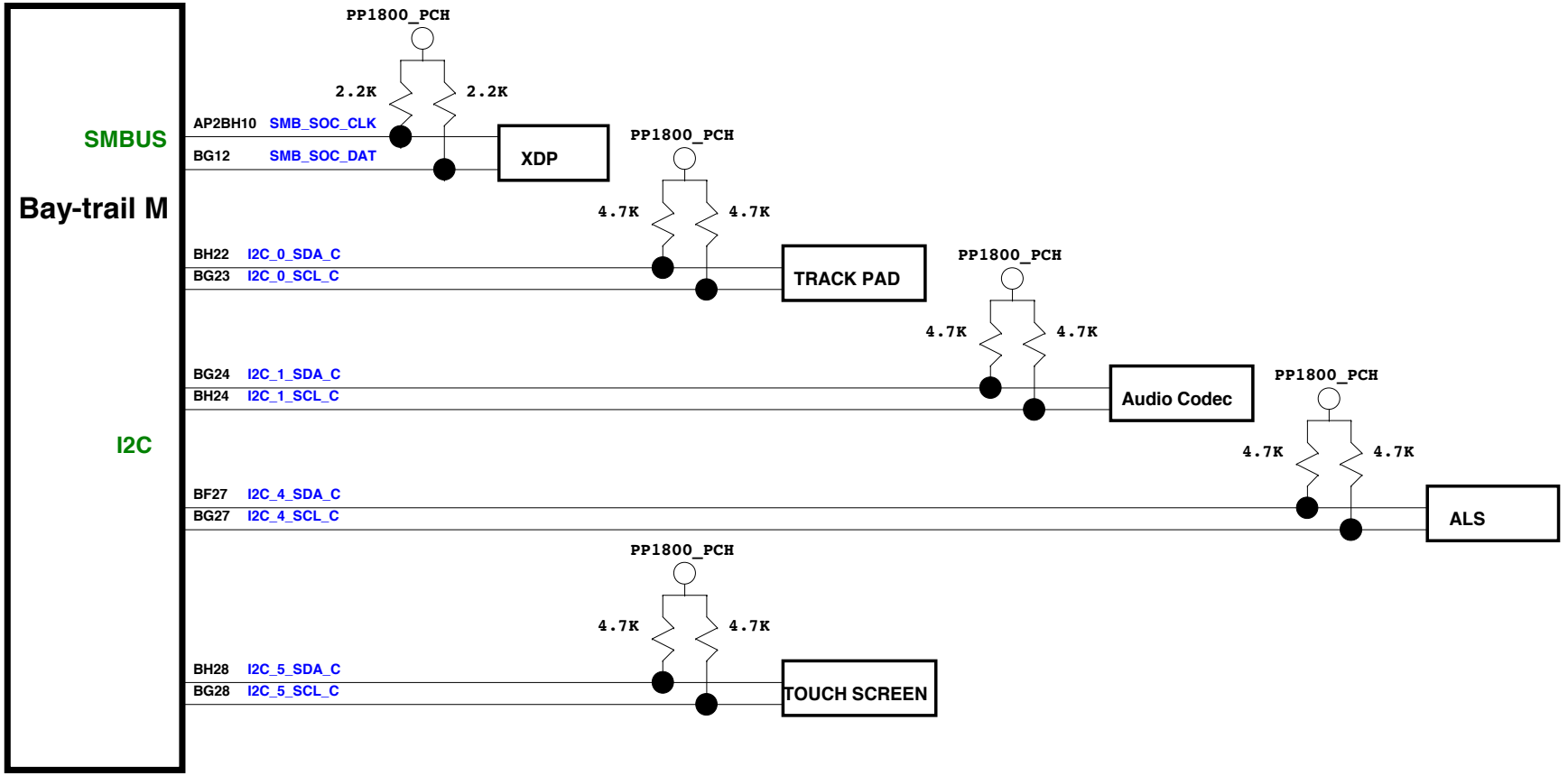

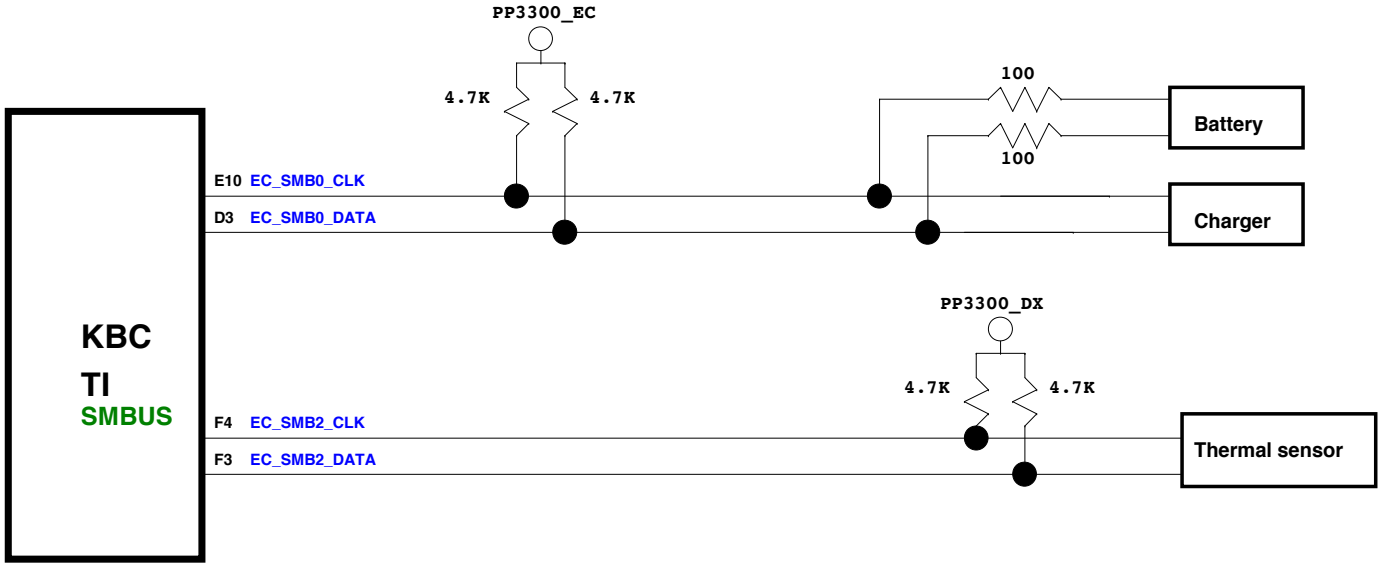

Quanta Computer Inc.
PROJECT : ZHQ
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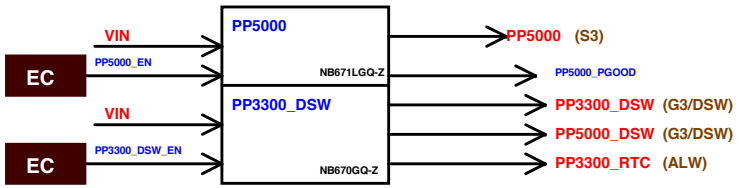
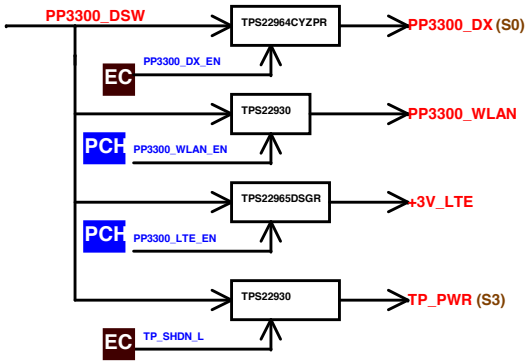
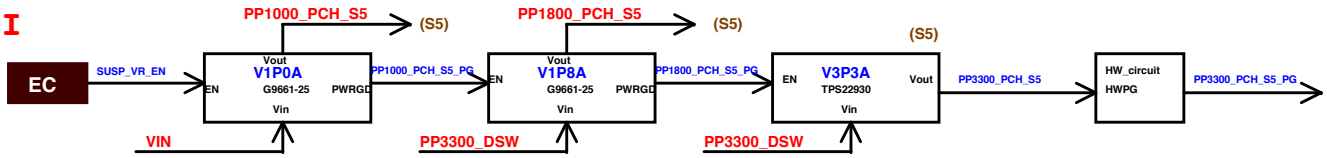
I

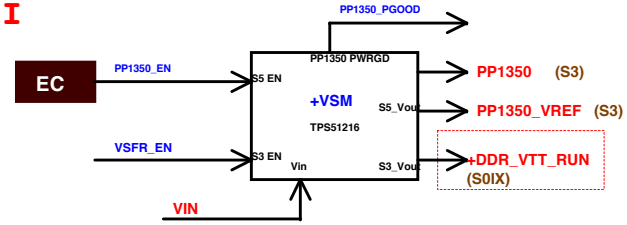


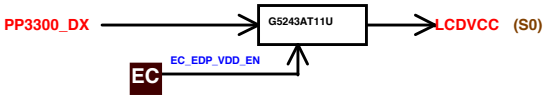


II

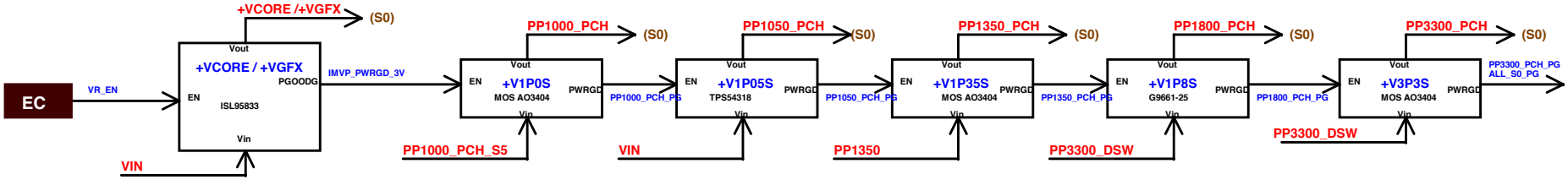


III

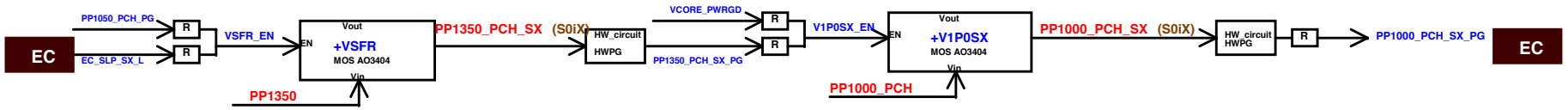


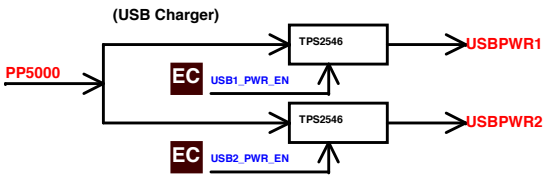


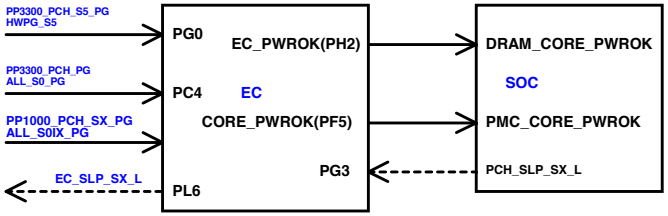
IV



V







Quanta Computer Inc.
PROJECT : ZHQ
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BTM PWR CONTROL | 1A
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Model | Version

CHANGE LIST

1A

12/23
1.(page37) add thermal protect
2.(page34) remove JP9,JP13

12/24
1.(page27) change keyboard pin define.
2.(page3) change C102 from 0.1u to 1u
3.(page27) change keyboard connector from 30pin to 24pin

12/25
1.(page27) change CN10 from 6pin to 8pin and TP pin define
2.(page37) change PU26B to PU10B
3.(page29) change charger solution from bq24715 to bq24717
4. change PL1~PL8 from 7X7X1.8 choke to 7X7X3

12/26
1.(page 7,22) change R590 to R150 and R150 to R590
2.(page27) add TP111 and TP112 reserve for TP PS2
3.(page24) remove PP3300_PCH_S5 and PP3300_DX on CN7

12/27
1.(page17) change R168 to DNP
2.(page26) change bettery cut off switch SW1 from DHPATE2CK03 to DHP0BTEPV00
3.(page26) change USB3.0 connector CN4 from DFFC30FR120 to DFHS09FR234
4.(page27) change TP connector CN10 from DFFC06FR050 to DFFC08FR026

12/31
1.(PAGE25) CHANGE DMIC POWER FROM PP1800_PCH TO PP3300_PCH

1/2
1.(page26) add ESD U35 and U36 for USB3.0

1/3
1.(page20) change HDMI connector from DFHD19MR343 to DFHS19FR106

1/28
1.(page37) Confirm use Thermal protect.
2.(page26) Change to use USB power switch G547F1P81U. Reserve TI ESD solution and remove VARISTOR ESD.
3.(page26) Swap U36 and L4 D+/D- for routing.
4.(page28) Remove KBC USB_ILIM_SEL(Pin B5) & Charger Status(Pin A7) and page24 USB 2.0_ILIM_SEL.
5.(page24) Remove FFC USB power charger pin.
6.(page26) Remove screw shutdown scenario.
7.(page27) Add BI shutdown function.

2/05
1.(page27) Change keyboard ESD pin define for routing.
2.(page21) Per Customer's requirement, Remove GPIO & reserve TP and add TP on WIFI SDIO.
3.(page22) Per Customer's requirement, add TP on LTE BodySAR, LED, Config_1 and GPS disable.
4.(page22) Per Customer's requirement, add TP on LTE Pin 40, 42, 44, 47.
5.(page22) Reserve GPIO from EC to control LTE POWER ON/OFF.
6.(page22) Change C23 to 0.1u.
7.(page37) Reserve EC_RST#_R to thermal shutdown PP3300_DSW.
8.(page24) Reserve PP5000_EN to provide PP3300_THM from PP3300_RTC.
9.(page24) Remove PP3300_DSW & PP3300_PCH_S5 & PP3300_DX because DB won't use it.

2/06
1.(page24) Remove R376.
2.(page37) Remove R612.
3.(page22) Stuff R25 & R26 & R75. Reserve 33p on UIM_VPP for EMI.
4.(page18) Reserve TP for AUO panel pin 14(LCD Panel Self Test Enable).

2/07
1.(page10) Add 7pcs 0.1U for EMI. Location: C392~C398
2.(page24) Add 6pcs 0.1U for EMI. Location: C399~C404
3.(page27) Swap TP pin definition.
4.(page34) Add 4pcs 0.1U for EMI. Location: PC211~PC214

2/11
1.(page all) Modify function code to EMC for ESD/EMI.
2.(page all) Correct all items QPN & Q description.
3.(page all) Correct Power items QPN that include PU17 & PQ13 & PL1~PL8 .
4.(page 26) Change USB power switch (U37) from G547F1P81U to G524C1T11U.

2/13
1.(page 26) Update USB3.0 connector & Hole footprint.
2.(page 28) Swap pin definition for routing smoothly.

2/14
1.(page 24) Change Q52 & Q56 MMBT3904 to SOT23 package.
2.(page 08) Change RMID to 001.

2/19
1.(page 29) Shortage issue, change to use P4SMAFJ20A.

2A

2/27
1.(page 17) Change SD card to half card socket for ME request.
2.(page 34) Core/GFX efficiency improvement. PL4 and PL7 change from 0.24uH to 0.47uH. PR30 and PR62 change from 2.2ohm to 0ohm. PR130 change from 21Kohm to 124Kohm.
3.(page 7 & page 15 & page 28) S3 leakage on PP1800_PCH. Change SIO_SPI_CS#, SIO_SPI_MISO, SIO_SPI_MOSI, SIO_SPI_CLK to TP on page 7, cancel level shift on page 15 and change SIO_SPI_MOSI_EC, SIO_SPI_MISO_EC, SIO_SPI_CLK_EC and SIO_SPI_CS_L to TP on page 28.
4.(page 29) Cancel PR112 and Add one diode RB500V-4 for S3 leakage on PP5000 issue.
5.(page 29) Un-stuff PR183 for 3-cell battery.
6.(page 8) Reserve RAM_ID3 for memory BOM option.
7.(page 27) SLG Reset IC needs to change new version, wait for confirm.
8.(page 23) Stuff C246 for RF.

2B

3/19
1.(page 15) unstuff U20/R391/R592/R156
2.(page 17) Change SD card to full card socket for ME request.
3.(page 24) change CN7 pin defined ,Add 2nd headphone and add USB powrer/gnd pin
4.(page 25) Add 2nd headphone for Education
5.(page 26) change USB Power SW U37 from G524C1T11U to G524A1T11U
6.(page 29~37) update power circuit

3/20
1.(page 28) Add PWR_LED1 pin on U16 G3 pin
2.(page 28) Add LTE_PWR_ON_R pin on U16 E11 pin for LTE power on
3.(page 28) Add Battery cell select pin on U16 N1 pin for 3S/4S select

3/25
1.(page 18) CHANGE POWER FROM PP1800_PCH TO PP3300_PCH and add R619/R620
2.(page 10) C284, C287, C305 ,C313, C296, C339, C349, C314, C306 *9pcs change from CH5101K9B01(1u) to CH6101M9B02(10u)
3.(page 10) C297, C260, C263, C268, C247, C248, C253, C259, C262, C254, C258, C255, C256, C295, C329, C261, C264, C267 *18pcs change from CH5101K9B01(1u) to CH5471M9B00(4.7u)
4.(page 29~37) update power circuit

3/31
1.(page 8) CHANGE DRAM ID table
2.(page 23) CHANGE LED to BL/ORG

4/02
1.(page 25) Remove DMIC onboard circuit
2.(page 18) Add DMIC pin at LVDS connector

4/03
1.(page 25) Remove 2nd headphone for Education

4/11
1.(page 29) Add PC217,PC218 and stuff PC1 for EMI
2.(page 26) nusutff R93,R87 and stuff L4 for EMI
3.(page 17) Add C405 and C406 for SDIO 3G card 4/11

4/18
1.(page 22) CN5 cahgne footprint from NGFF-80149-2121-75P-KB-SMT to NGFF-80149-2121-75P-KB
2.(page 29) Add PR233 for Battery Cell Sw
3.(page 27) Change U24 from AL022930U00 to AL022902T00 for cost down

4/21
1.(page 17) C98/C97 change to 22p for crystal report

4/23
1.(page All) Correct BOM
2.(page 27) Change R546 location and add Q44/Q65 on Track Pad INT# for leakage issue follow 0C9
3.(page 18) Add C407 on Touch Reset line for power sequence tuning of TS module, spec is 90 ns from VDD to RST
4.(page 34) change PC87,PC88,PC119,PC126 to 10uF follow 0C9

Model	Version	CHANGE LIST
	2B	4/23 6.(page 31) Change PC29/PC13 to 10uf follow 0C9 7.(page 31) PC224 change to 0.1u 8.(page 27) Change R144 from 4.7K to 1M and add a cap C352 2.2uF for Battery shipping mode by SLG4350, U17 change to SLG4K4350 9.(page 26) Change C78 to 220uF and Add D29 10.(page 7) add C408 on CORE_PWROK for ESD improvement 11.(page 6) add C409 on PROCHOT# for ESD improvement 12.(page 3) C102 to be changed to 0.1uF on DRAM_PWROK for ESD improvement 4/24 1.(page 8) reserve R483 for CLKRUN# disable follow 0C9 2.(page 27) stuff U30,U31,U32,U33,U34 for ESD 3.(page 30) change PC36 to 10uF
	3C	5/13 1.(page 16) Modify level shift circuit for TPS and BOM changed 5/20 1.(page 26) change ESD-PROTECTION and remove U35/U36 circuit 2.(page 24) Change DB pin defined and add a audio GND for audio issue 5/22 1.(page 25) Add R625 for Audio issue 2.(page 24) Change CN7 pin 29 connect to ANGD for audio issue 3.(page 29) update power schematic 4.(page 33) update power schematic for power sequrence 5/23 1.(page 33) Change PR234 from 20K to 27K and Correct PR235 AGND 2.(page All) Correct BOM 5/26 1.(page 29) Change PJ2 connector from DFHD08MS125 to DFHD08MR201 2.(page 8) Add R625 and R626 for TPS issue 5/29 1.(page 23) Exchange LED1 and LED2 for icon issue 2.(page 23) change R589,R599,R246,R245 for LED light
	3D	6/3 1.(page 26) L4 change P/N from CX900HL2000 to CX900HL2002 2.(page 34) unstuff PC60 and PC139 for cost down 6/6 1.(page 28) change EC P/N to AR0ZHQS1001 for T11 issue 2.(page 3) change R178/R191 to 0402 shortpad for cost down 3.(page 5) change R58/R184/R183/R452/R457/R180/R197 to 0402 shortpad for cost down 4.(page 6) change R103/R123/R131/R139/R204/R375/R379/R381/R383/R414/R455/R462 to 0402 shortpad for cost down 5.(page 7) change R81/R107/R133/R424/R448/R468/R470/R471/R479/R481/R513/R165 to 0402 shortpad and R116/R157 change to 0603 shortpad for cost down 6.(page 8) change R109/R449 to 0402 shortpad for cost down 7.(page 9) change R343/R385 to 0402 shortpad for cost down 8.(page 10) change R54/R110/R114/R121/R378/R380/R395/R400/R407/R430/R453/R456/R460/R464 to 0402 shortpad and R193/R555 change to 0603 shortpad,R354/R384 change to 0805 shortpad for cost down 9.(page 12) change R263/R307/R319/R320/R325/R332 to 0402 shortpad and R337 change to 0603 shotpad for cost down 10.(page 15) change R445 to 0402 shortpad for cost down 11.(page 17) change R489/R507/R526/R541/R549/R550/R552 to 0402 shortpad and R335 change to 0603 shortpad for cost down 12.(page 18) change R20/R326/R339/R341/R620 to 0402 shortpad and R14/R224 change to 0603 shortpad,R17 change to 0805 shortpad for cost down 13.(page 19) change R216/R222/R499/R505/R524/R535/R538/R540/R564/R565 to 0402 shortpad for cost down 14.(page 20) change R72/R73/R74 to 0402 shortpad for cost down 15.(page 21) change R44/R46/R55 to 0402 shortpad andd R39 change to 0805 shortpad for cost down 16.(page 22) change R75/R411 to 0402 shortpad and R355/R602 change to 0603 shortpad, R601 change to 0805 shortpad for cost down 17.(page 23) change R56/R353 to 0402 shortpad for cost down 18.(page 24) change R370/R377/R194 to 0402 shortpad for cost down 19.(page 25) change R219/R223/R605/R606/R228 to 0402 shortpad and change R217/R229/R232/R233/R241 to 0603 shortpad for cost down 20.(page 27) change R213/R498 to 0402 shortpad and change L7 to 0603 shortpad for cost down 21.(page 28) change R145/R162/R164/R169/R173/R444 to 0402 shortpad for cost down 6/9 1.(page 12) unstuff U10 anc C16 for cost down 2.(page 29-36) 1.Removed : JP2,JP3,JP7,JP12JP13,JP14,JP16,JP15,JP9,JP1,JP11,JP6 2.Change to shortpad_4: PR58,PR162,PR165,PR18,PR115,PR110,PR149,PR150,PR147,PR52, PR35,PR143,PR148,PR136,PR189,PR172,PR217,PR6,PR122,PR117,PR95, PR44,PR15,PR68,PR212,PR102,PR103,PR173,PR174,PR106,PR105. 3.Change to shortpad_6: PR144,PR30,PR62,PR48,PR77,PR124,PR46,PR213,PR1,PR3,PR101,PR92,PR112. 4.Change to shortpad_8: PR71 5.Remove CURRENT/POWER MONITOR circuit : PU22,PU11,PU20,PU21,PC191,PC192,PC113,PC131,PC184,PC185,PC189,PC190,PC193,PC194. 6.Keep Vin 7343 Capacity: PC219,PC220,PC221,PC222 6/16 1.(page 37) PR236 and PR227 change to shortpad 2.(page 27) unstuff SW1/Q62/Q63/R609 for Acer request remove reset function. 6/17 1.(page 27) modify EC reset circuit and Add D1002 and D1003 for ESD issue.
		6/23 1.(page 27) change U24 P/N fromAL022902T00 to AL022930U00 for SMT issue 2.(page 27) SW1/C390/R627/R628 unstuff for removed RST buttom 3.(page 18) Remove L1 for SMT request and R8,R9 change to shortpad_4 for cost down. 4.(page 20) Remove L2 for SMT request , R41,R39,R22 change to shortpad_4 for cost down. 5.(page 22) Remove L15 for SMT request. 5.(page 26) Remove L3,L5,R93,R87 for SMT request. 6.(page 34) PR61 change to shortpad_4 for cost down. 7/2 1.(page 37) change PR205 from 1.5K to 2K for throme request

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
PROJECT : ZSQ
Size: Document Number: Change list-2 Rev: 1A
Date: Sheet of

Model	REV
ZHQ	1A

CHANGE LIST

2013/12/23 1. Release first version for ZHQ.
2. (Page 1)Update CN4 QPN , Footprint and Part Description
3. (Page 1)Remove LED1 and R1,R9 and R2
4. (Page 1) Remove NetName PWR LED0 and PWR LED1
5. (Page 1,2,3) Update Function code
6. (Page 1) Remove R6 ,R7 and AGND

2014/01/27 1. Change the page number
Page 1 -> Page 3 , Page 2 -> Page 4 , Page 3 -> Page 5 , Page 4 -> Page 1
2. (Page 2)Add block diagram

2014/01/28 1. (Page 3)Remove CN4 ,Pin23, 24, 26 , Add one TP
2. (Page 4)Change USB charger to USB Switch
3. (Page 2)Change Block diagram

2014/02/03 1. (Page 3)Change CN4 Pin5 pin definition

2014/02/05 1. (Page 3)Remove CN4 Pin10,11,15

2014/02/07 1. (Page 4,5)Change USB2.0/Audio jack connector Part number

2014/02/10 1. (Page 3)Change CN4 input current form 1.5A to 2A
2. (Page 3)Base on DXF, remove the Hole7.
3. (Page 4)Change the C2 QPN.

2014/02/11 1. (Page 4)Change USB power switch (U1) from G547F1P81U to G524C1T11U. Change C3 value from 1U to 2.2U.

2014/02/12 1. (Page 3)Add 0.1u on PP5000 & PP3300_RTC for EMI.
2. (Page 3,4,5) Rename all location

2014/02/13 1. (Page 4)Change C1 from CH7101MT205 to CH7101MT202

2014/03/07 1. (Page 3) Change pin5 pin definiton from DET_TRIGGER_SW to HP_JD_L for Audio.

2014/03/24 1. (page 3) change CN1 pin defined , add USB power/gnd pin for ESD.
2. (page 4) change USB Power SW U2 from G524C1T11U to G524A1T11U for USB.

2014/04/03 1. (page 3) Remove CN3 Pin10 ,11 for Acer request

2014/04/10 1. (page 4) Remove R9,R10.And change L5 from CX1HN900000 to CX12B900000 for USB.
2014/04/14 1. (page 3) Change MR1 from AL008251000 to AL009132003 for Lid.
2014/04/23 1. (page 5) Add D7 , Stuff D1,D2,D3,D4 for ESD.
2014/05/05 1. (page 5) Separate it between AGND and DGND,Add R36,R37,R26,R38,R52,R53,C24,C23 for Audio
2014/05/07 1. (page 3) Separate it between AGND and DGND,Add R54 for Audio
2014/05/16 1. (page 5) Separate it between AGND and DGND,Nustuff R37,R26,R38,R52,R53,C24,C23 for Audio
2014/05/28 1. (page 5) Nustuff R36 for Audio

2014/06/23 1. (page 4) Remove R9,R10 for SMT request

MODEL	FROM	To
Page 02		1A
Page 03		1A
Page 04		1A
Page 05		1A

DOC NO.	PROJECT MODEL :	ZHQ	APPROVED BY:	J.C. Huang	DATE: 2014/04/23
	PART NUMBER:		DRAWING BY:	Dennis Lin	REVISON: 1B

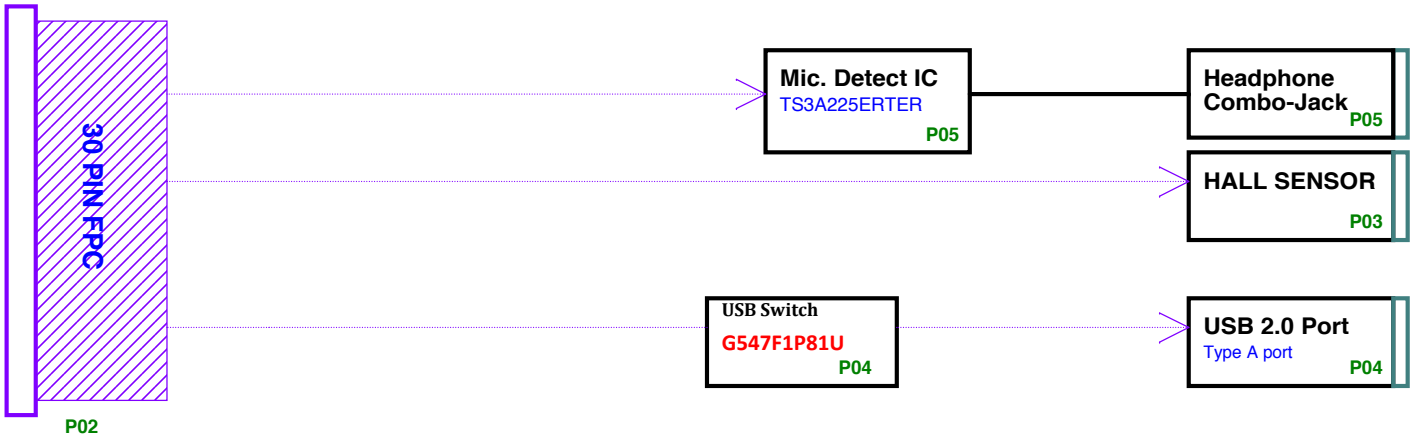
Quanta Computer Inc.
PROJECT : ZHQ

Size	Document Number	Rev
	Change History	1A

Date: Monday, June 23, 2014 Sheet 1 of 5

VER : 1A	
BOM P/N	Description
*	ZHQ IO/B ASSY

Block Diagram
(Audio Headset Switch + Phone Jack + Hall Sensor + USB CONNECTOR)



Schematic Marks

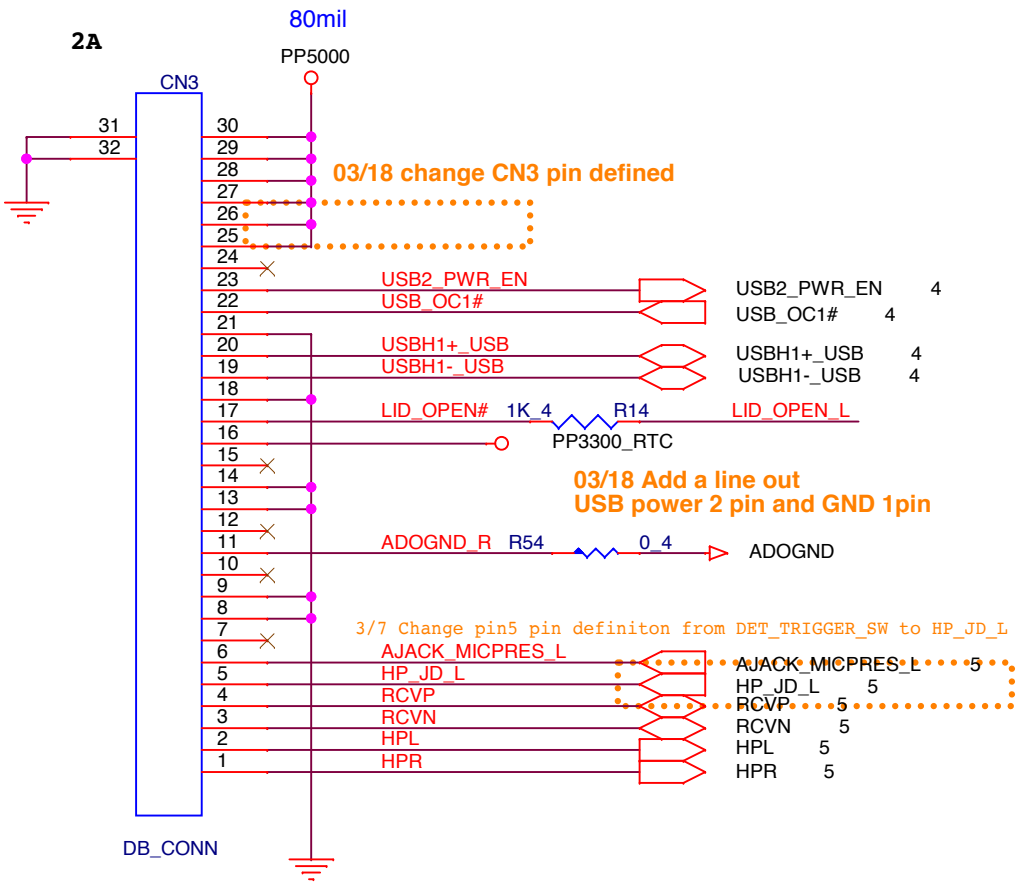
Reference	Description
*	do not stuff
/F	1% esistance

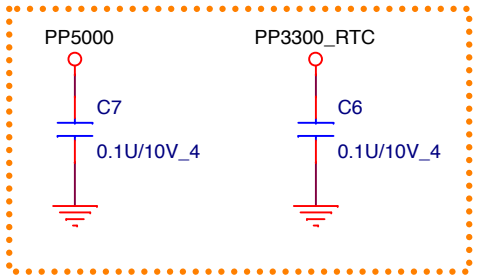
USB2.0: 500mA x1
Charger (DCP): 2A x1
Hall Sensor 3.3V x1

Quanta Computer Inc.
PROJECT : ZHQ_IO BOARD

Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, June 23, 2014	Sheet 2 of 5	

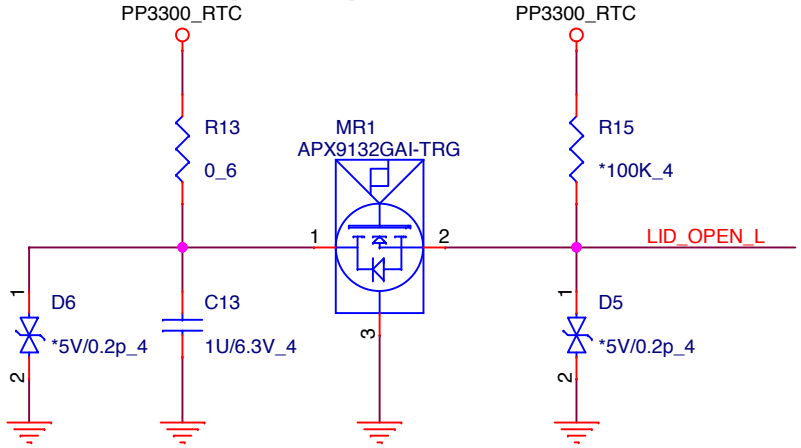
IO Board Connector



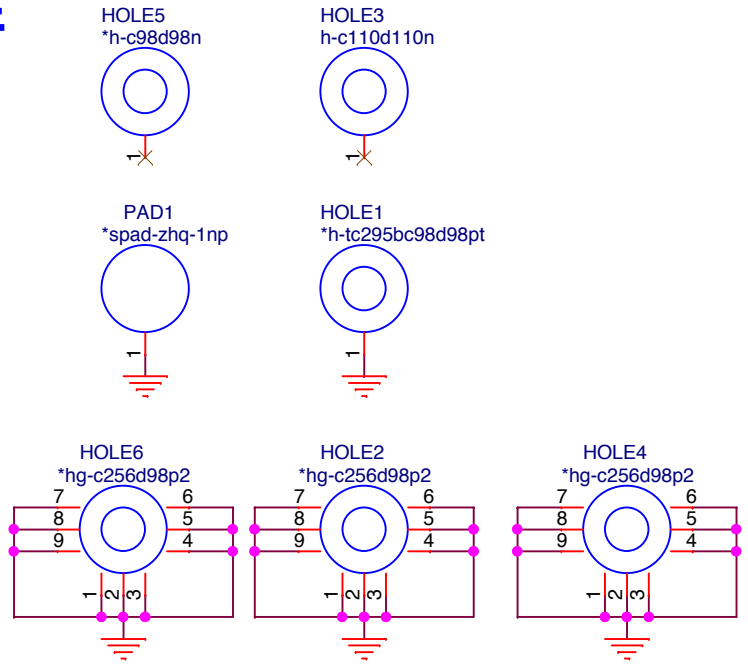


02/12 Add 0.1u on PP5000 & PP3300_RTC for EMI.

Lid Switch (HSR)



HOLE



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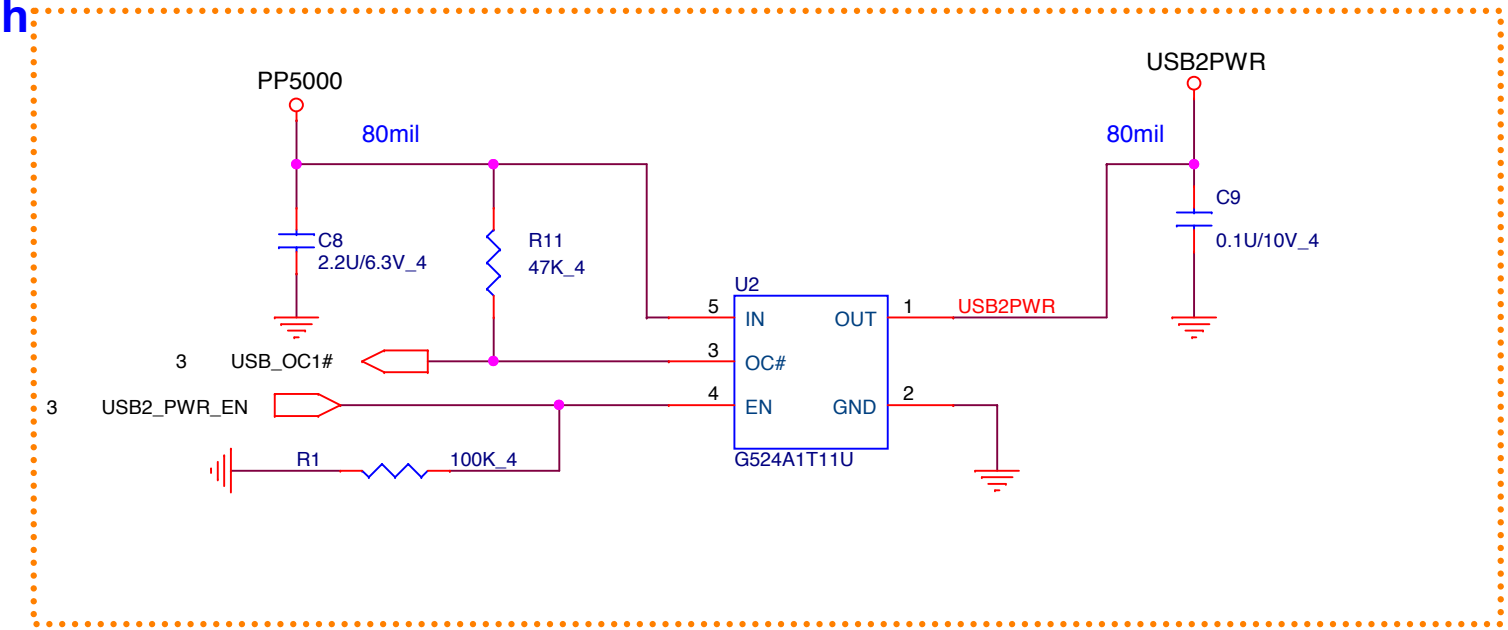
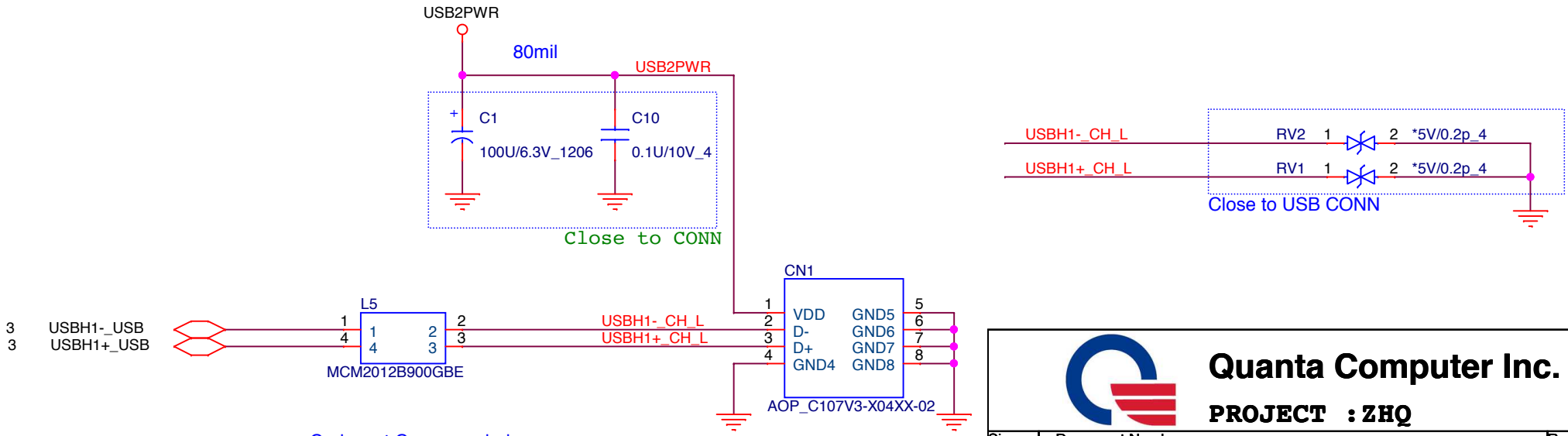
USB Switch



1/28 Change USB charger to USB switch
02/11 Change USB power switch (U1) from G547F1P81U to G524C1T11U.
Change C3 value from 1U to 2.2U.

USB 2.0



Co-layout Common choke
for A-test validation only.

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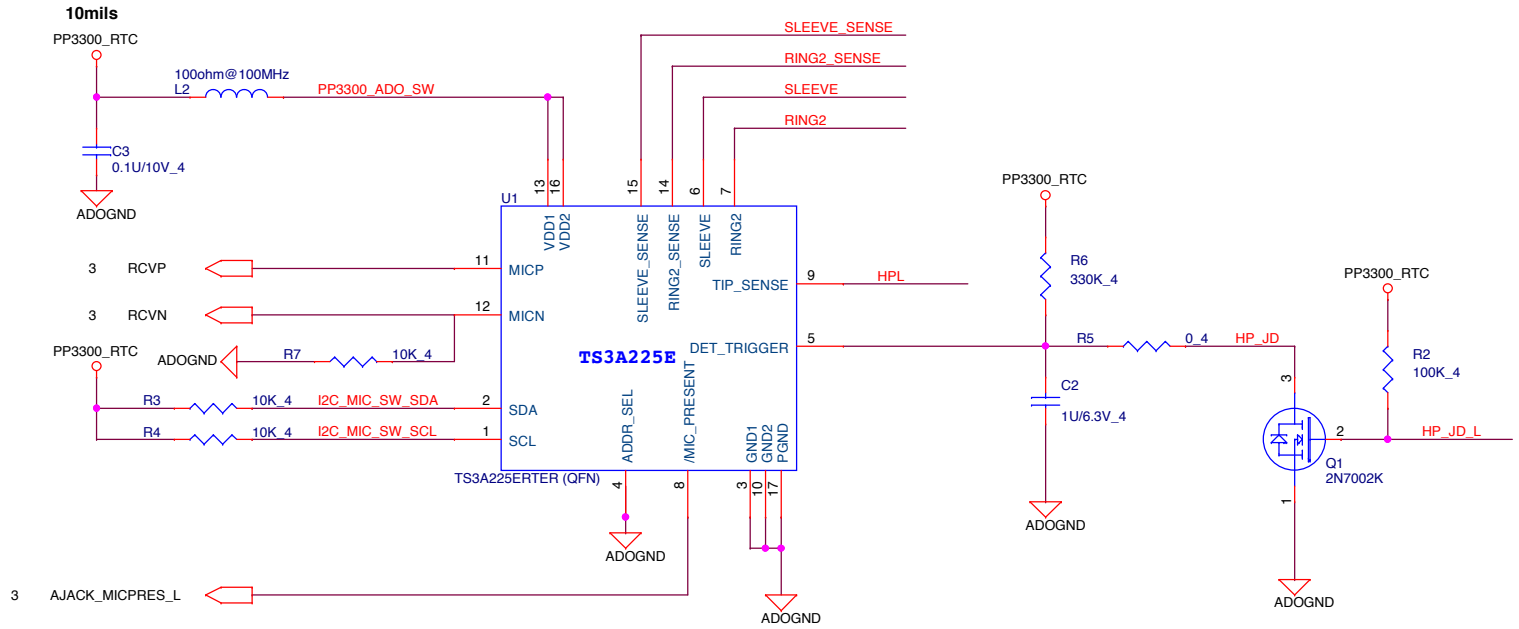
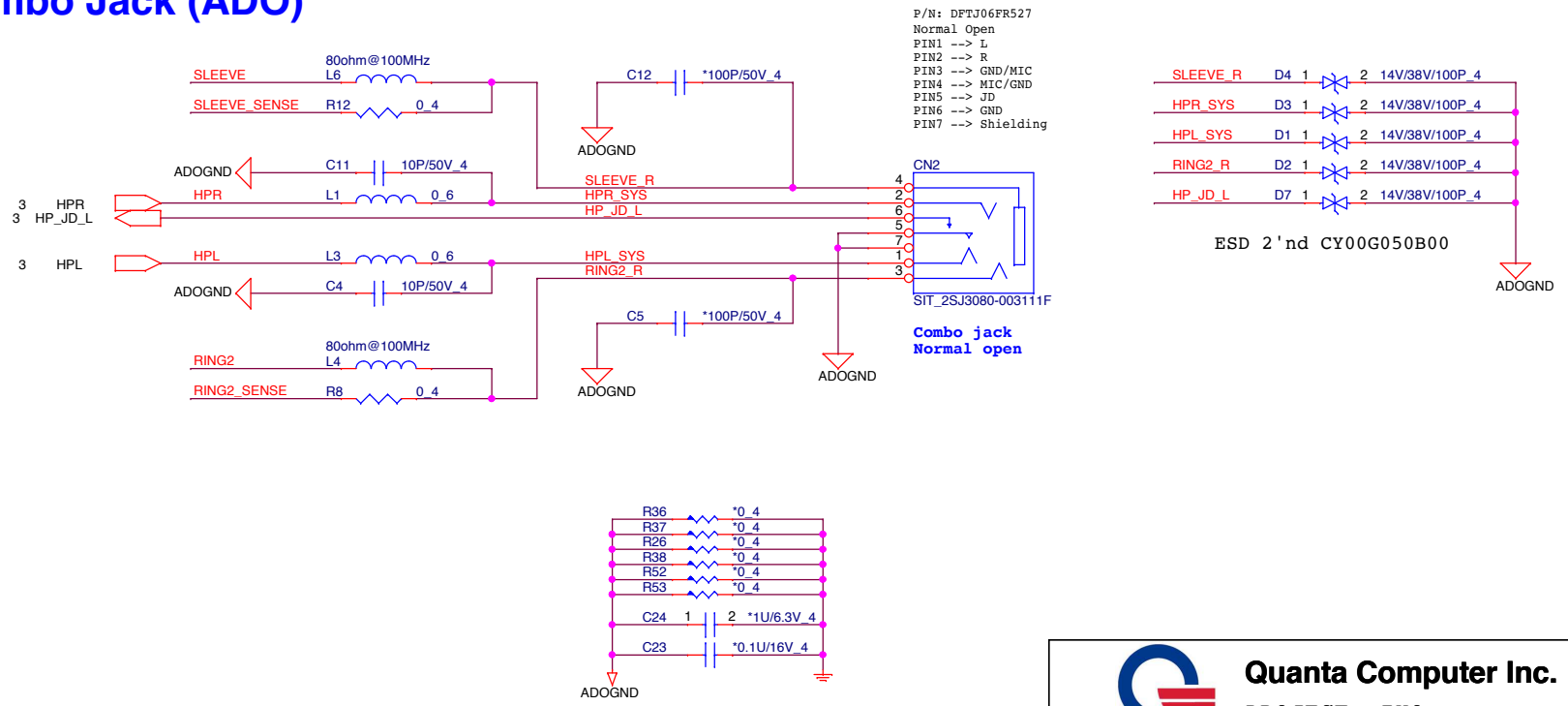
Audio Headset Switch (ADO)



Combo Jack (ADO)



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Size	Document Number: Audio Headset Switch/ Combo Jack	Rev: 1A
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