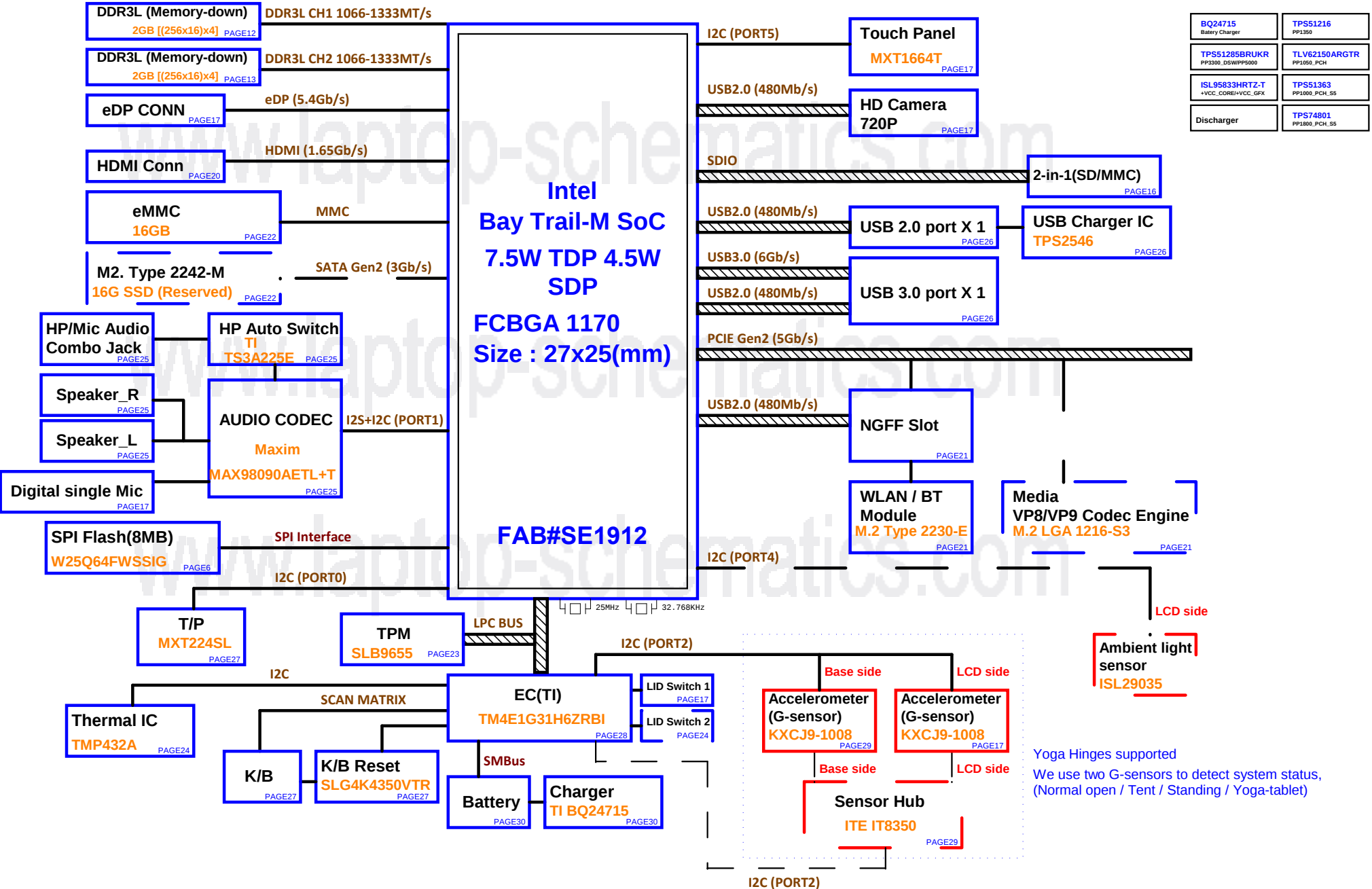
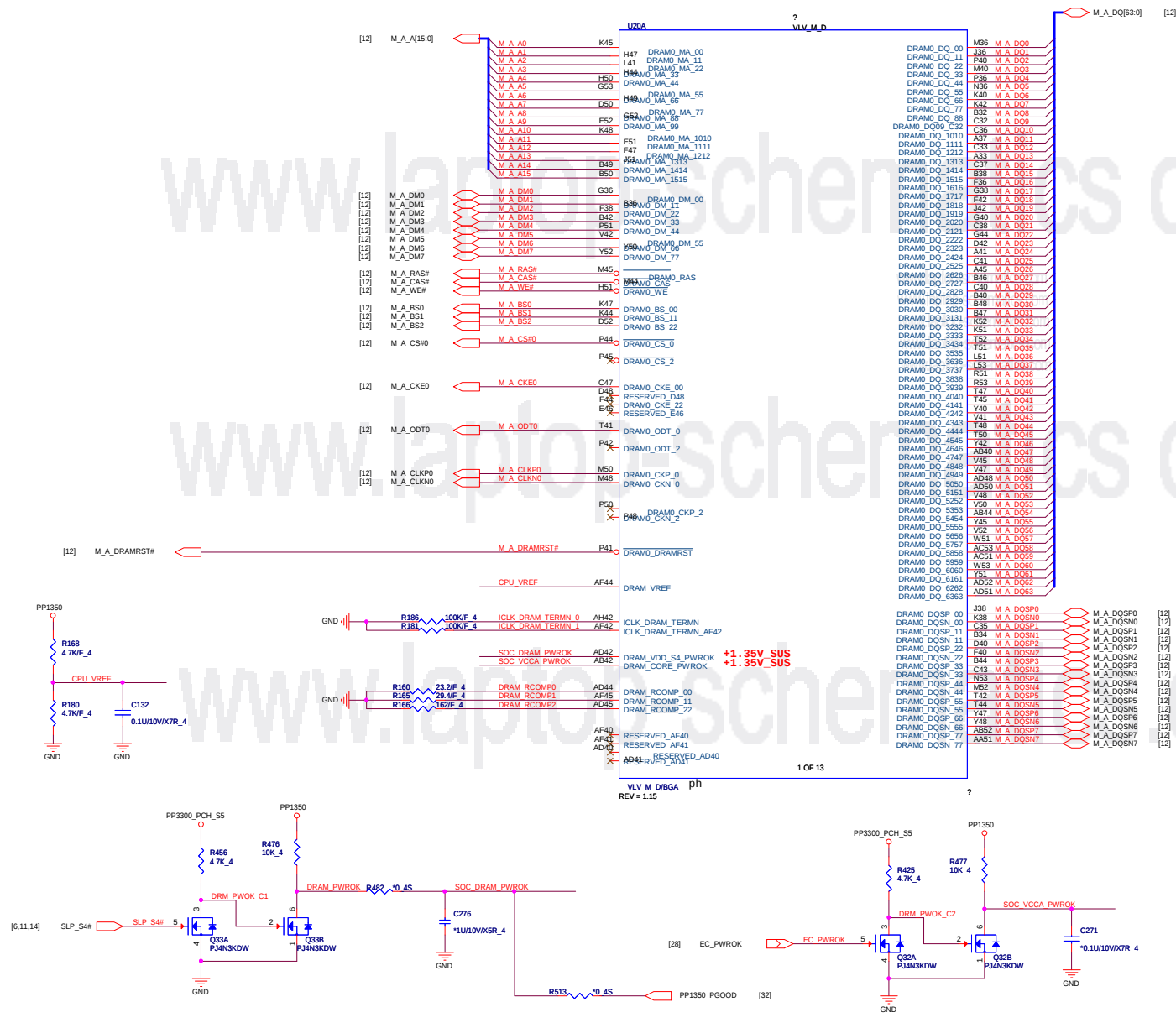
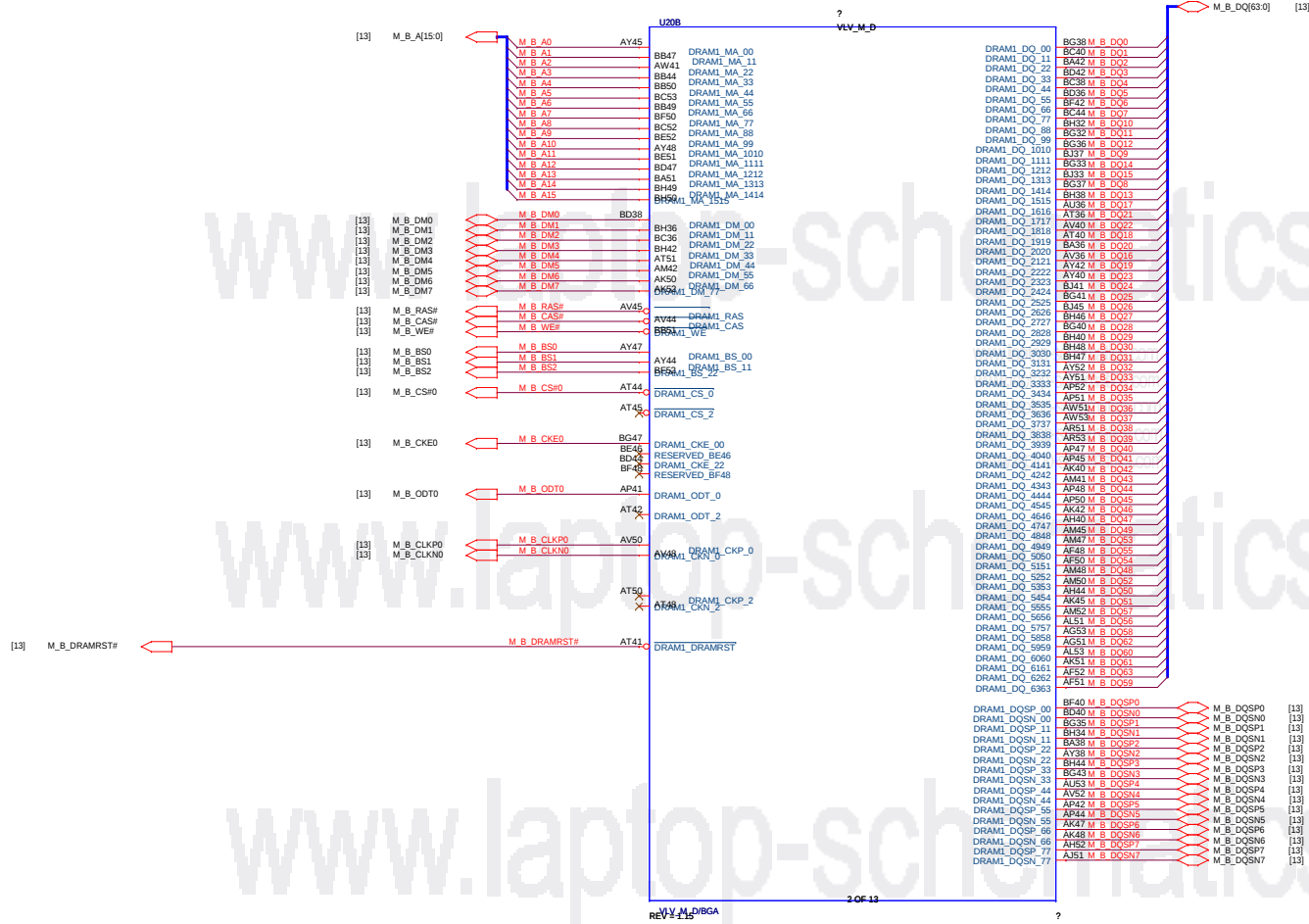
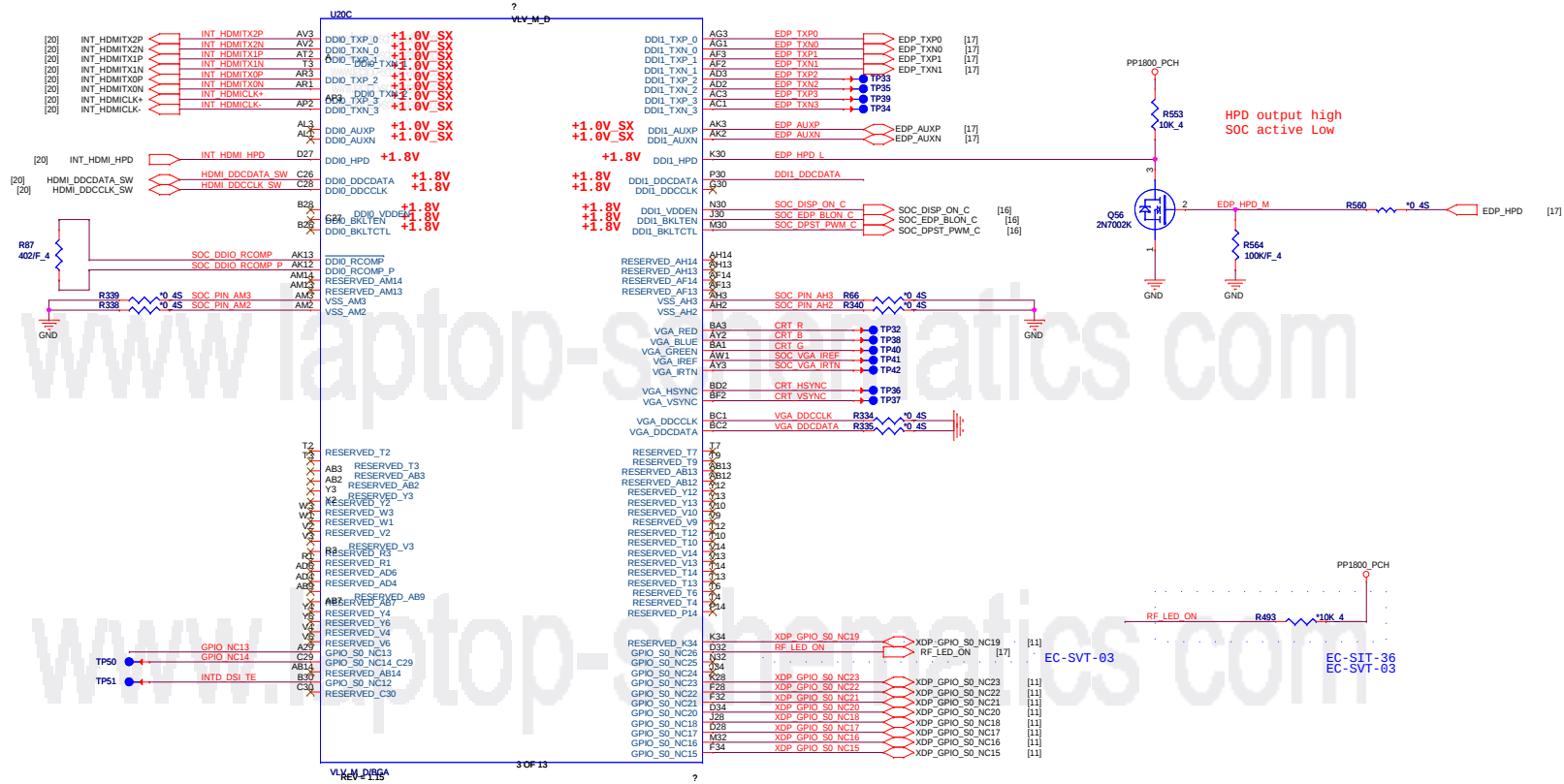


Lima5B UMA Block Diagram (Chrome)



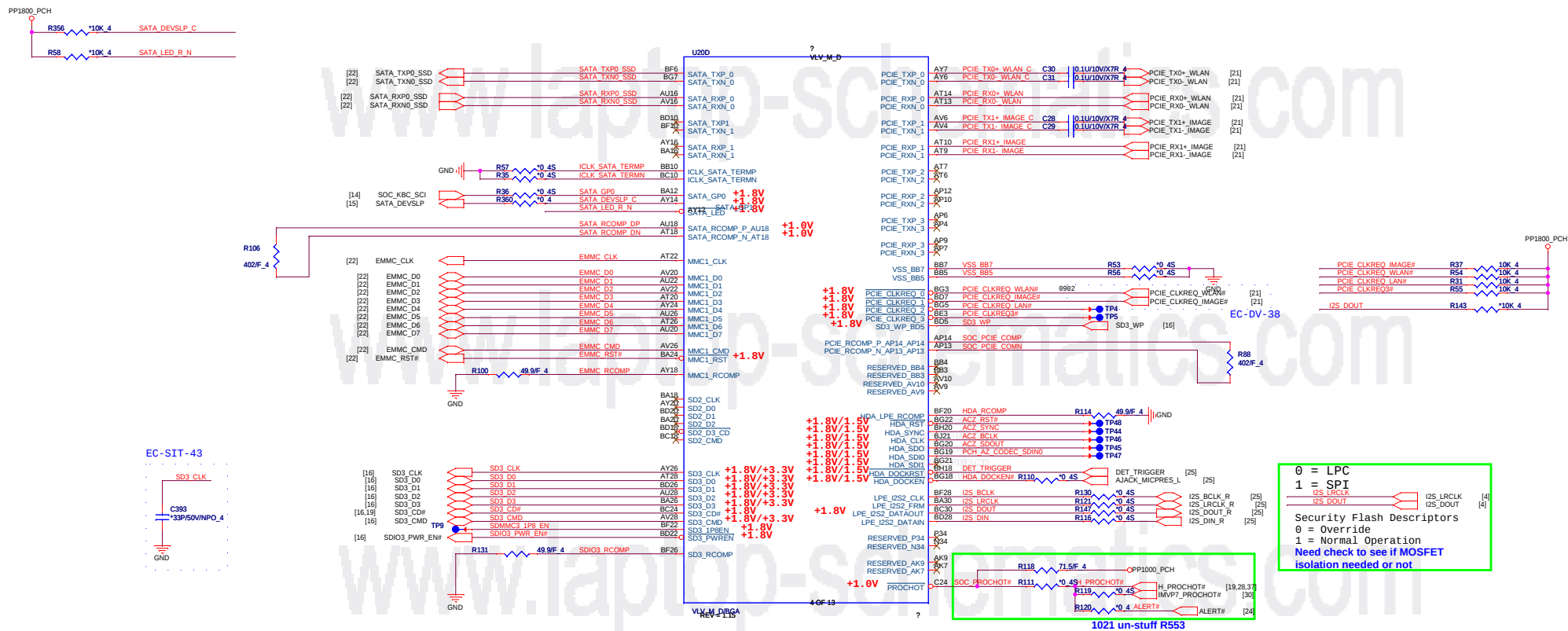






BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	[7] GPIO_SO_SC_56
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	[5] I2S_LRCLK
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	[5] I2S_DOUT
DDIO_DDCDATA	DDIO Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	[28] SOC_OVERRIDE#
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDIO not detected 1 = DDIO detected	[17] GPIO_NC13
GPIO_SO_NC_13				[11] GPIO_SO_NC13

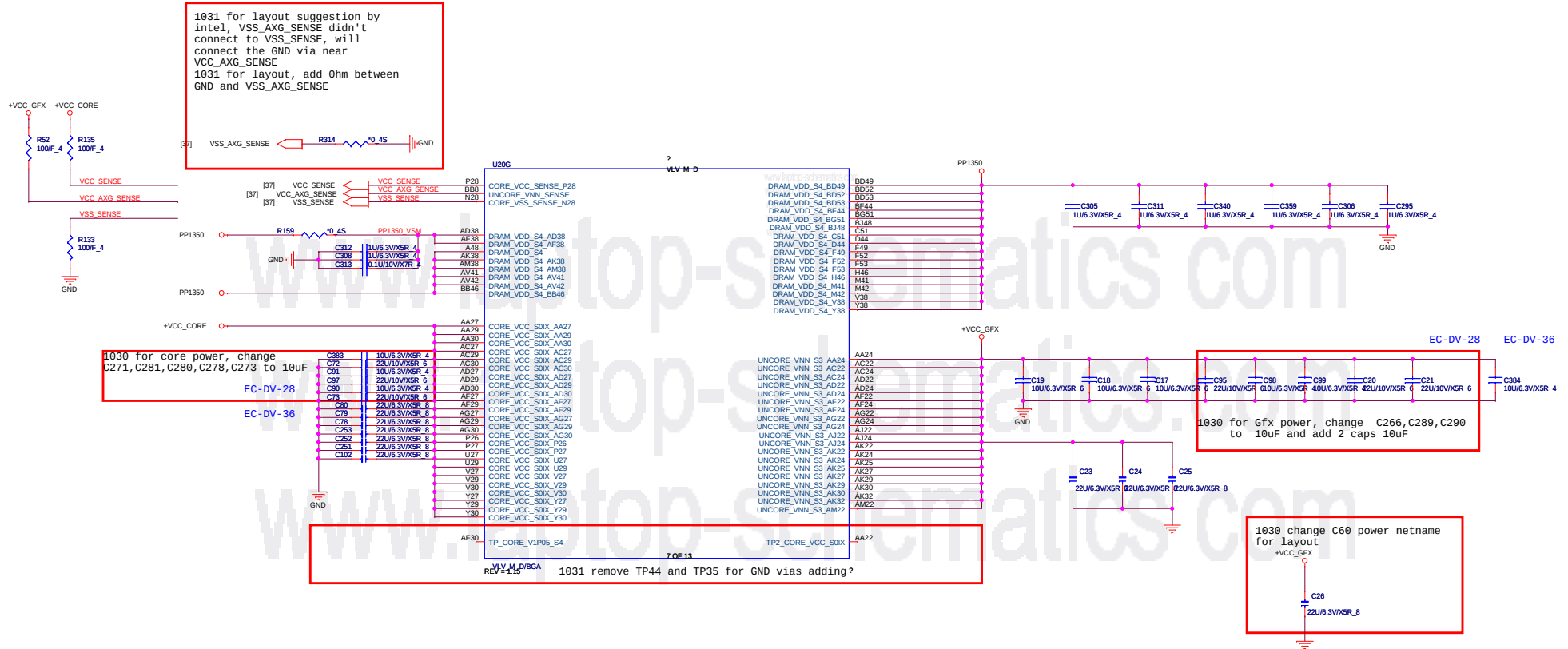


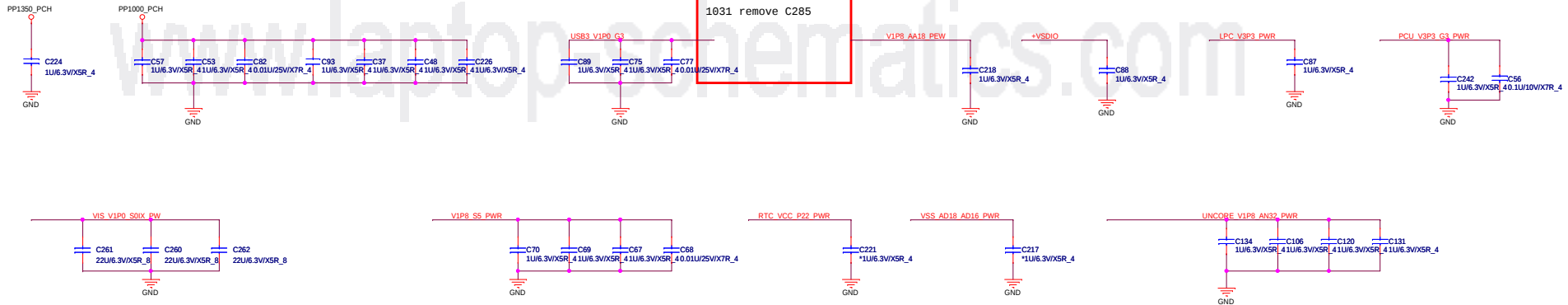


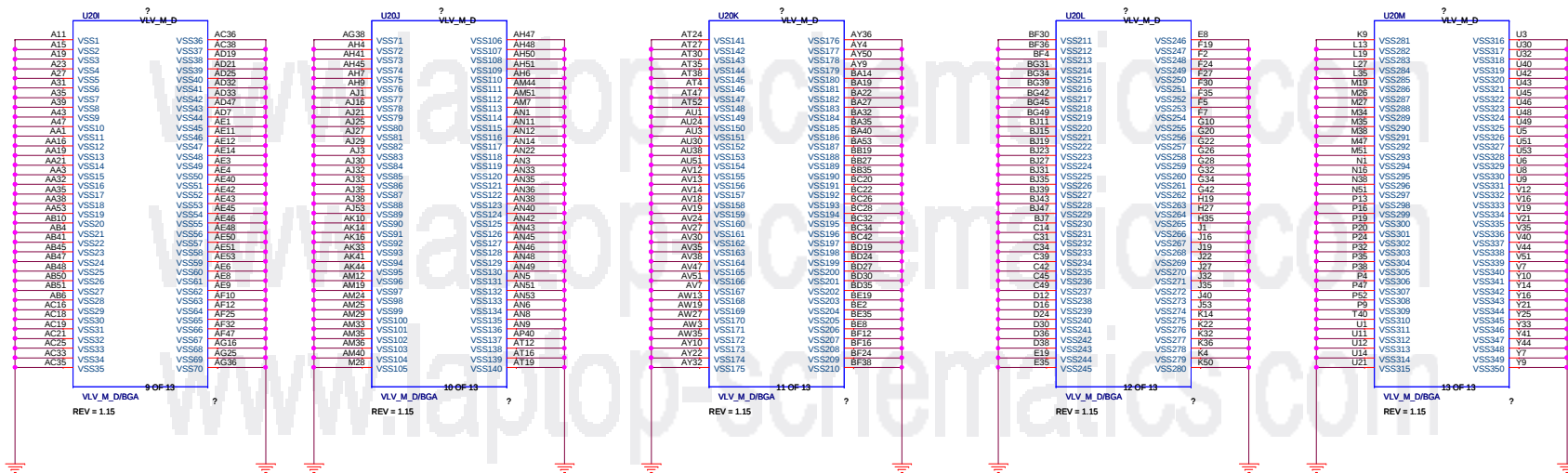
Vender	RAM ID	Q PN	MFR. PN	Freq.	Size	# ch	Total size
Micron	0000	AKD5JGSL02	MT41K256M16HA-125:E (V80A/4Gb/30nm)	1600MHz	4Gb	2 ch	4GB
Hynix	0001	AKD5JGTV00	HT4G63AFR-PBA (A/4Gb/29nm)	1600MHz	4Gb	2 ch	4GB
Micron	0010	AKD5DGS102	MT41K128M16JT-125:K (V89C/2Gb/30nm)	1600MHz	2Gb	2 ch	2GB
Hynix	0011	AKD5MG0TW02	H5TC2G63FFR-PBA (F/2Gb /29nm)	1600MHz	2Gb	2 ch	2GB
Samsung	0100	AKD5MG4T510	K4B2G1646Q-BYK0 (Q/2Gb/35nm)	1600MHz	2Gb	2 ch	2GB
Hynix	0101	AKD5JGTV00	H5TC4G63AFR-PBA (A/4Gb/29nm)	1600MHz	4Gb	1 ch	2GB
Samsung	0110	AKD5PGST500	K4B4G1646Q-HYK0 (D350/4Gb/35nm)	1600MHz	4Gb	2 ch	4GB
Elpida	0111	AKD5JGSL403	EDJ42J6EFG-GN-F (F/4Gb/30nm)	1600MHz	4Gb	2 ch	4GB
Micron	1000	AKD5JGSL02	MT41K256M16HA-125:E (V80A/4Gb/30nm)	1600MHz	4Gb	1 ch	2GB
Elpida	1001	AKD5JGSL403	EDJ42J6EFG-GN-F (F/4Gb/30nm)	1600MHz	4Gb	1 ch	2GB
Samsung	1010	AKD5PGST500	K4B4G1646Q-HYK0 (D350/4Gb/35nm)	1600MHz	4Gb	1 ch	2GB

EC-SIT-16

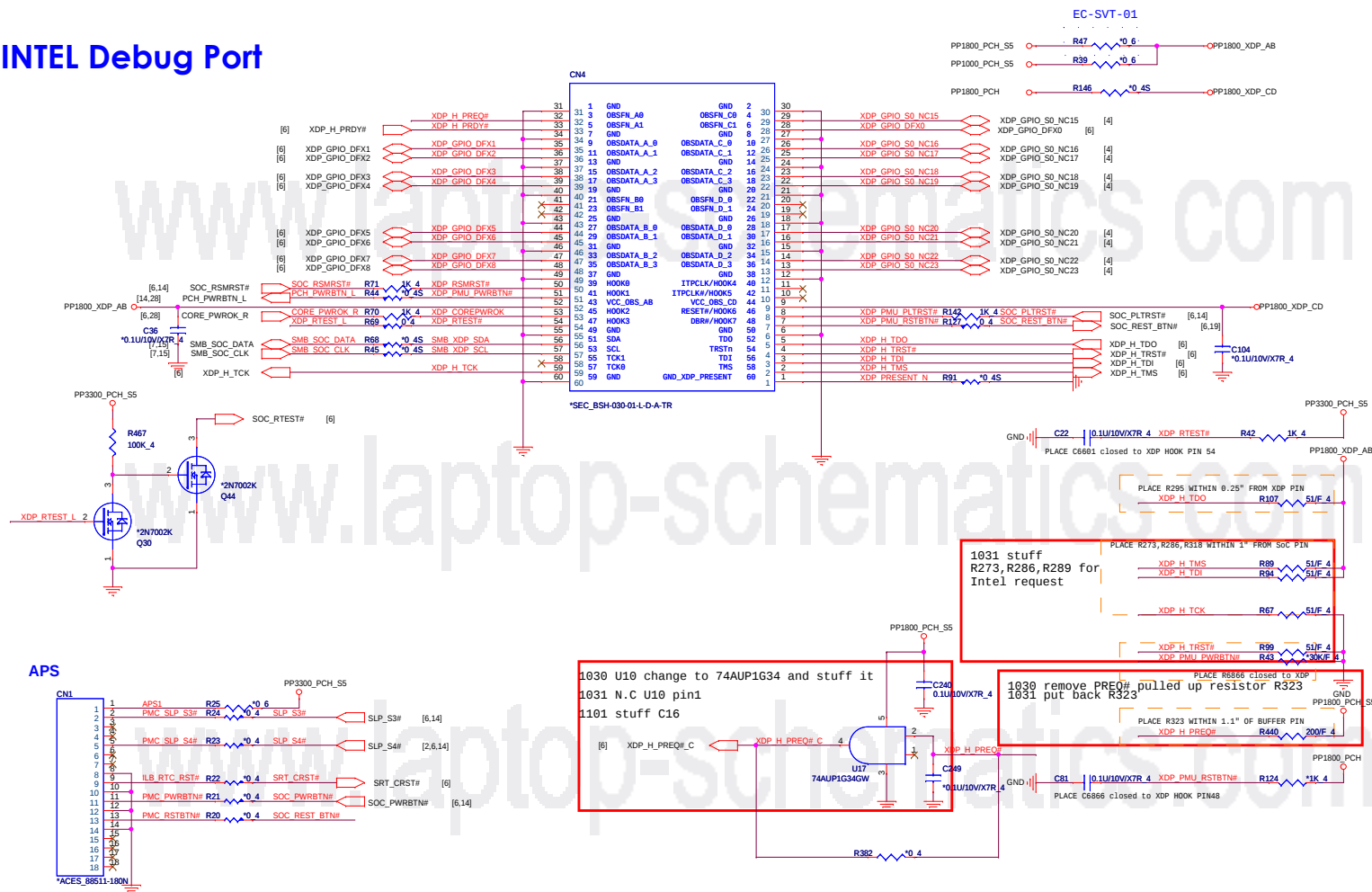
EC-SIT-47





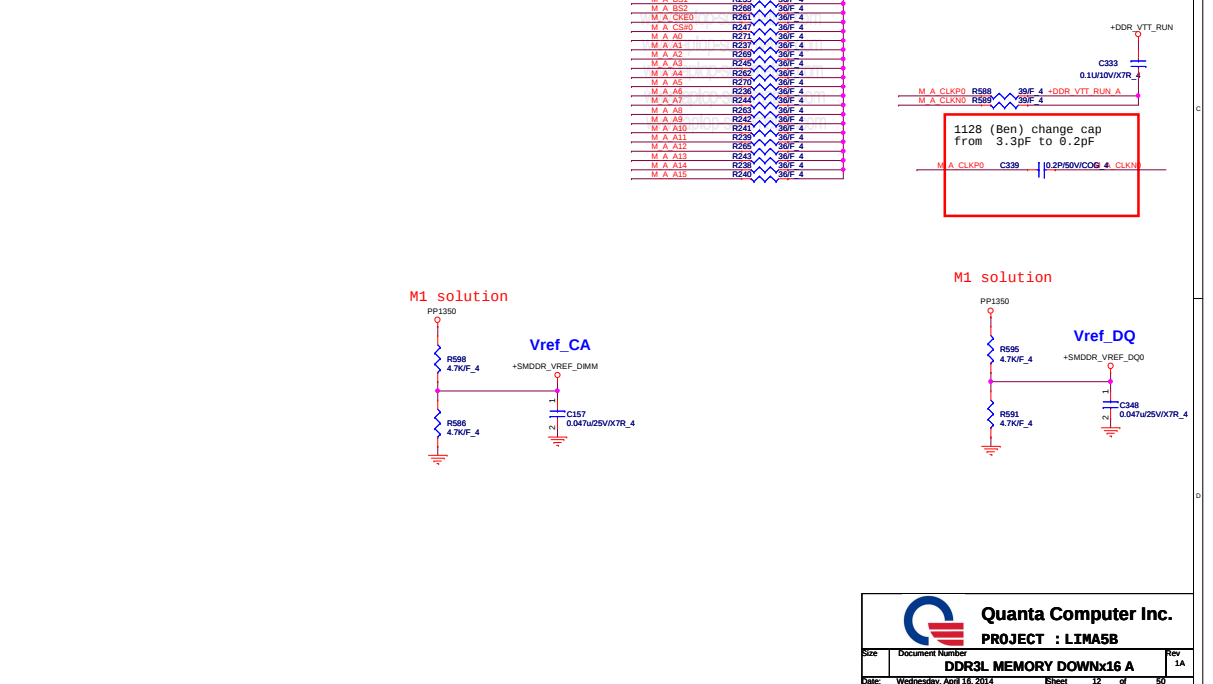
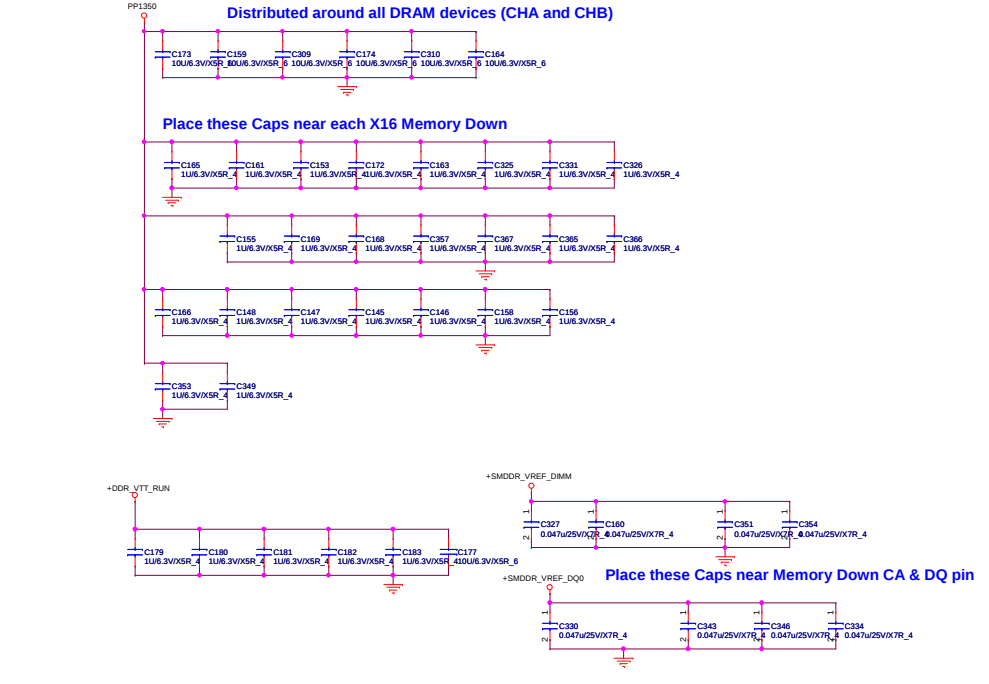


INTEL Debug Port





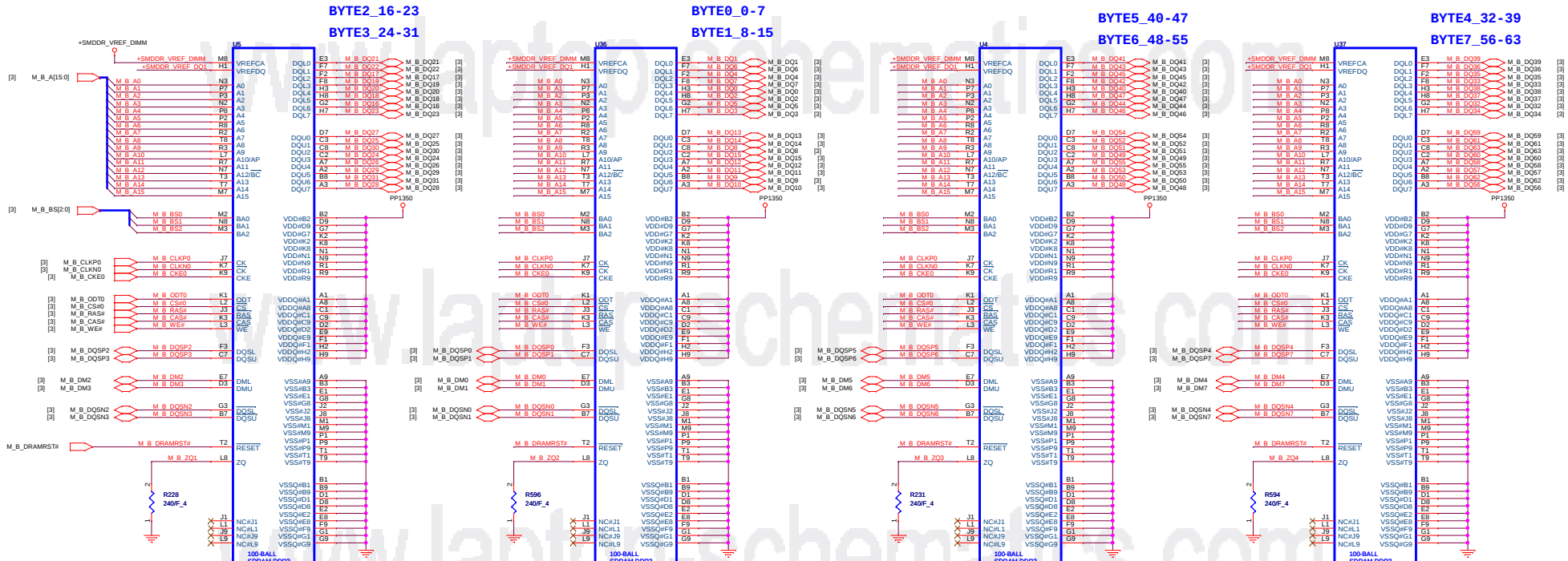
Vendor	P/N	
Hynix	AKD5JGST400	DDR3L 1333MHz 4Gb
Elpida	AKD5JGST404	DDR3L 1600MHz 4Gb



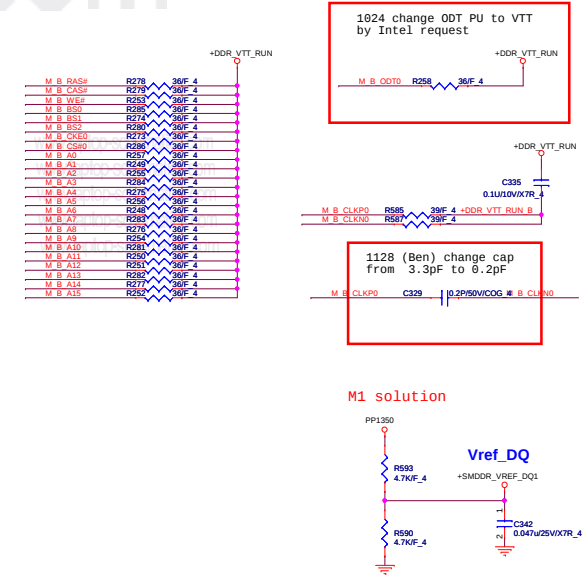
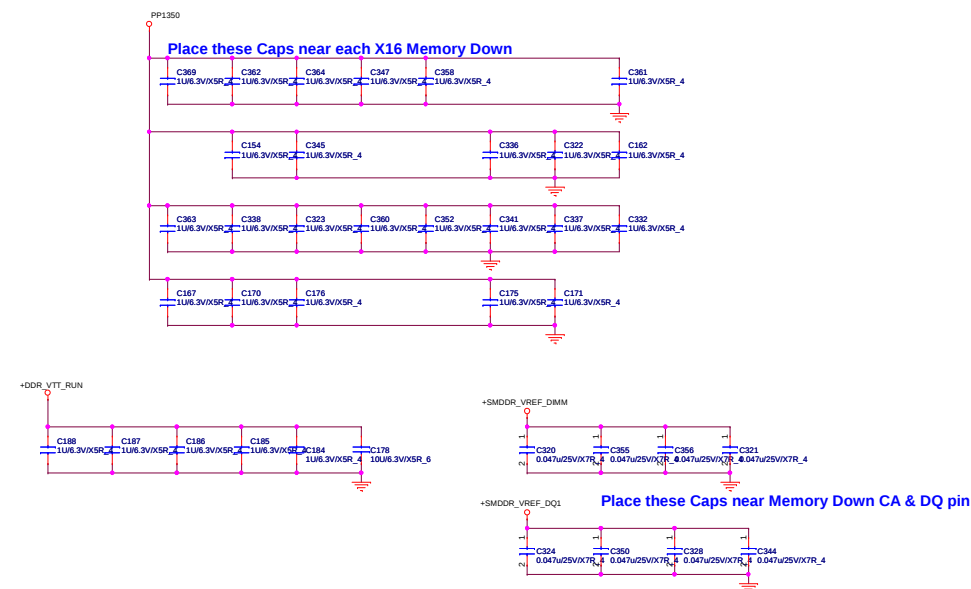
1024 change ODT PU to VTT by Intel request

1128 (Ben) change cap from 3.3pF to 0.2pF

<DDR>

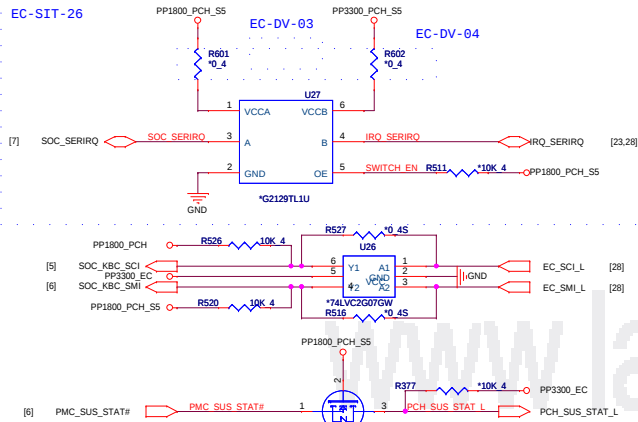


Vendor	P/N	
Micron	AKD5JGSTL02	MT41K256M16HA-125:E
Elpida	AKD5JGST400	
	AKD5JGST404	



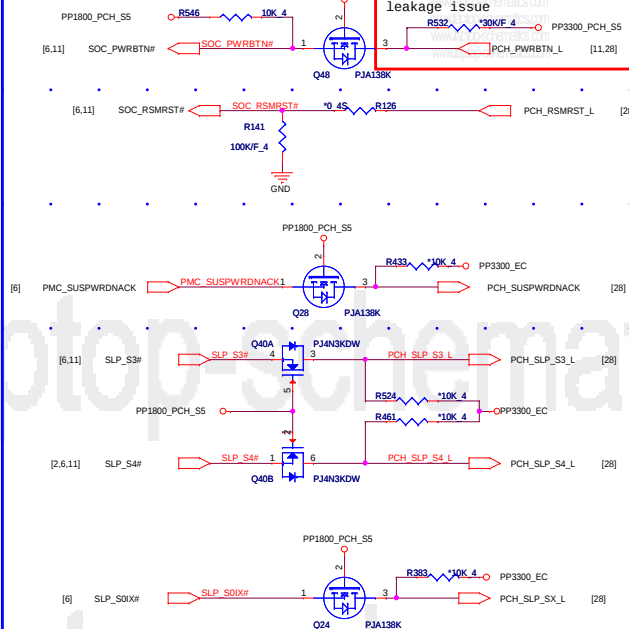
PWRON SEQUENCE

9/6 EC table says SERIRQ is OD pin,
reserve for debugging

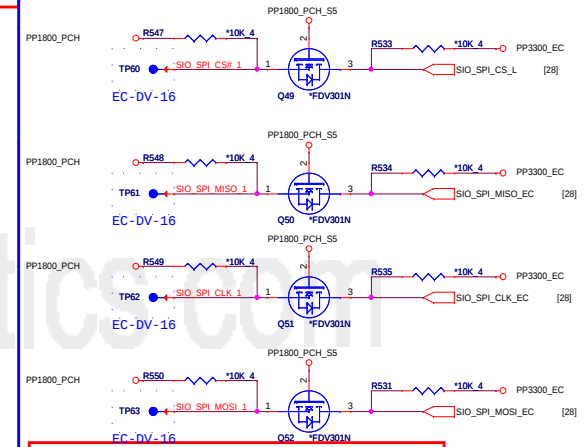


PWRON SEQUENCE

1022 un-stuff R182 for S5
leakage issue



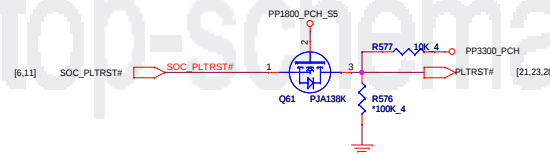
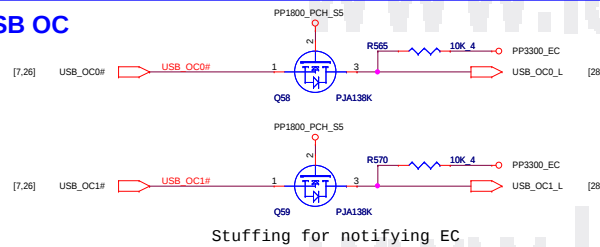
EC-DV-03



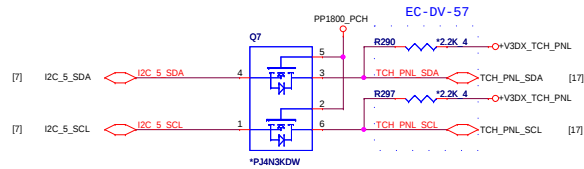
9/6 Need check MOSFET switching
speed>15MHz

EC-SIT-25

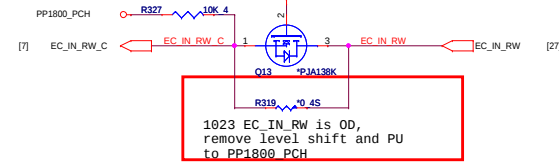
USB OC



Touch Panel

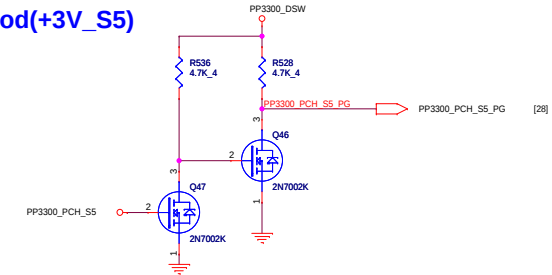


HW RESET



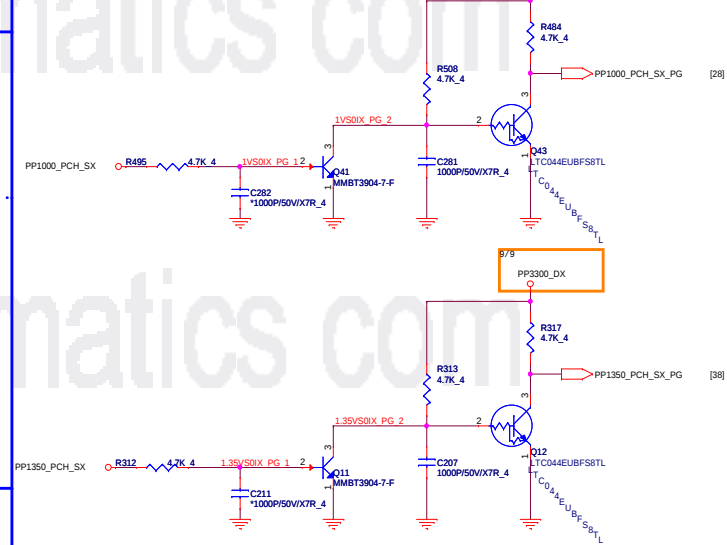
S5 Power Good(+3V_S5)

0839 A24

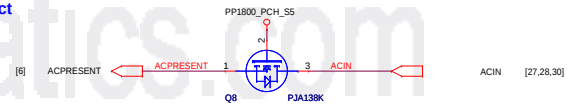


S0ix Power Good

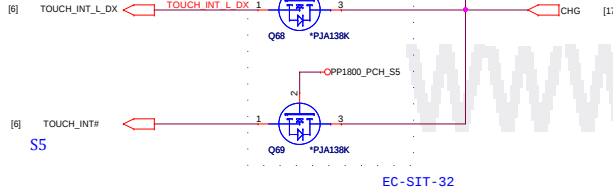
for proto type only, can remove at MP stage if S0ix is not needed



AC Detect

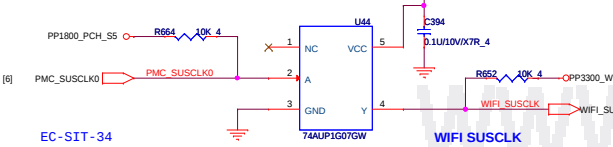


S0

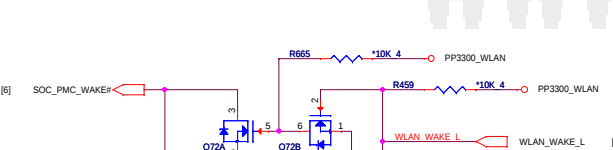


S5

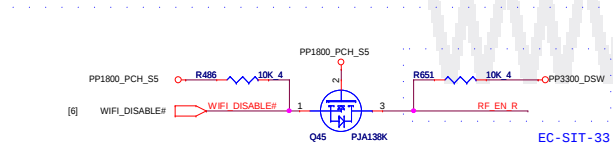
WIFI



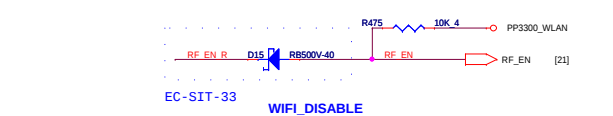
EC-SIT-34



EC-SVT-06

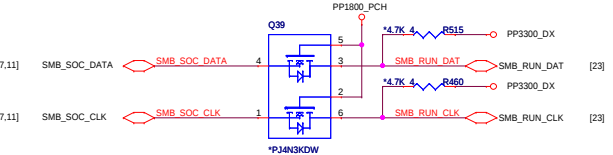


EC-SIT-33

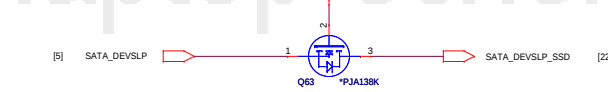


WIFI_DISABLE

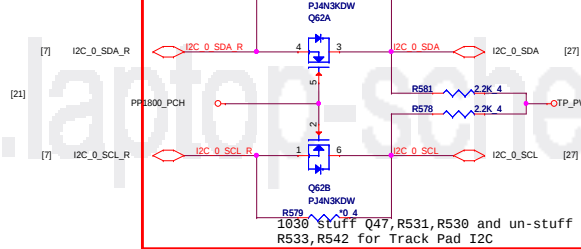
RFID



SATA



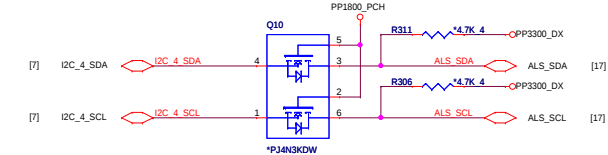
Track Pad



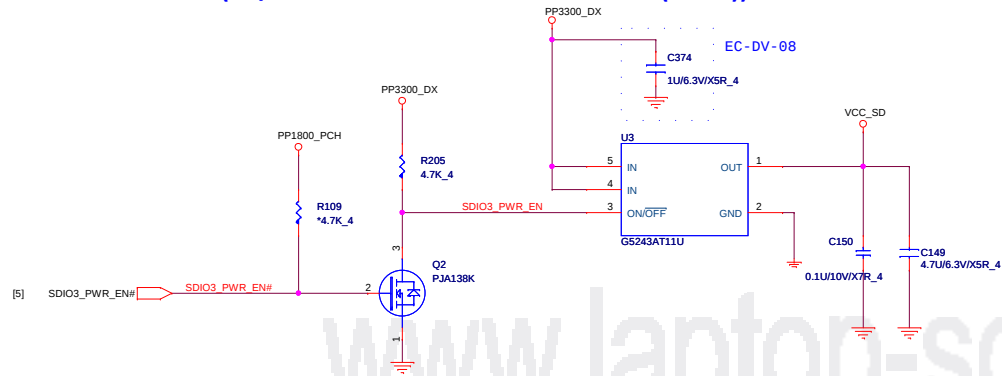
eDP control pin

1107 delete and add in page16

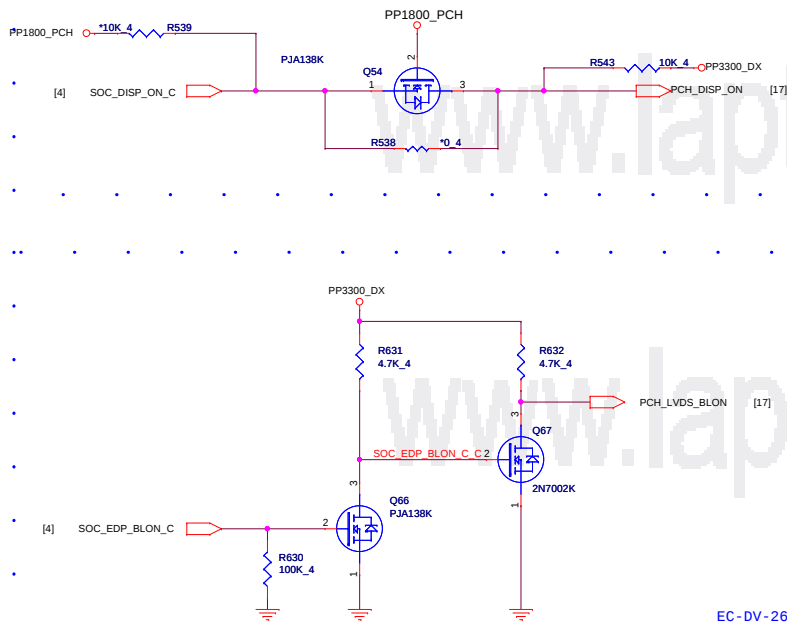
ALS



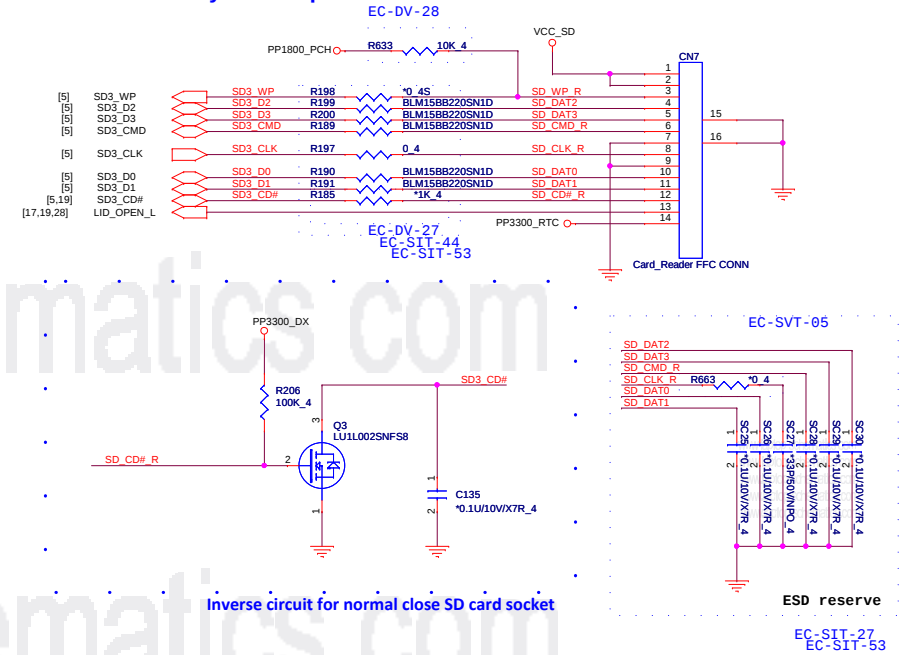
To Card Reader Board (SD/MMC CARD READER CONNECTOR (MMC))



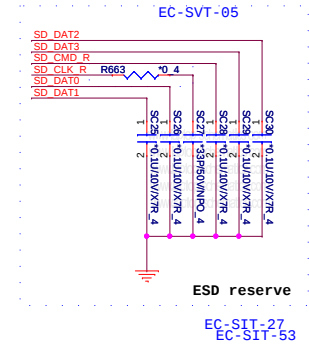
eDP level shifter



1025 the damping of SDIO change to 0 ohm by Intel request



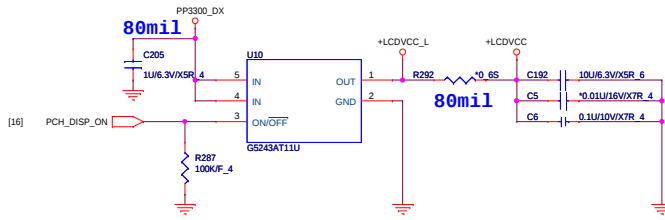
Inverse circuit for normal close SD card socket



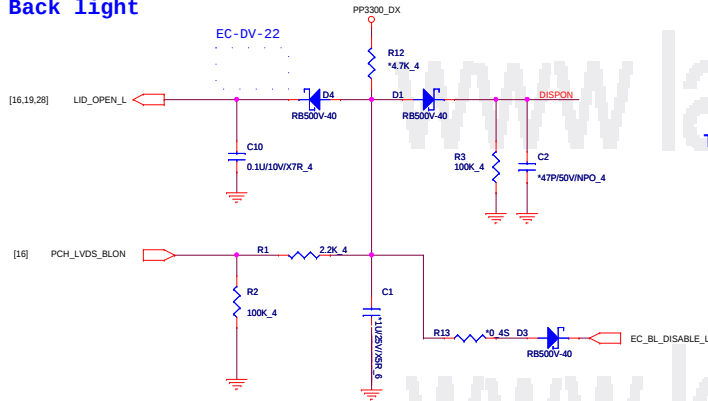
ESD reserve

EC-SIT-27
EC-SIT-53

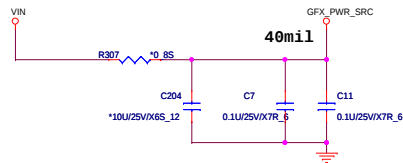
LCDVCC



Back light



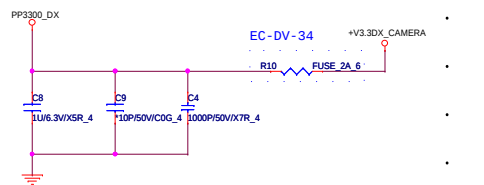
GFX_PWR_SRC



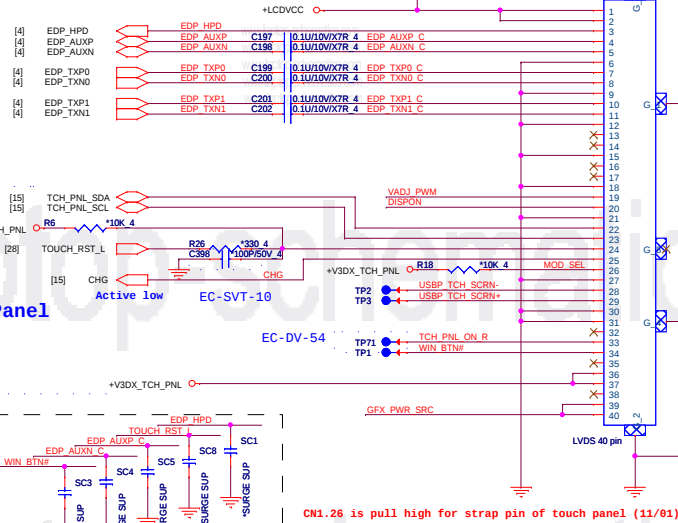
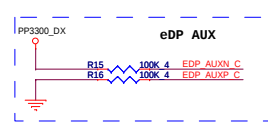
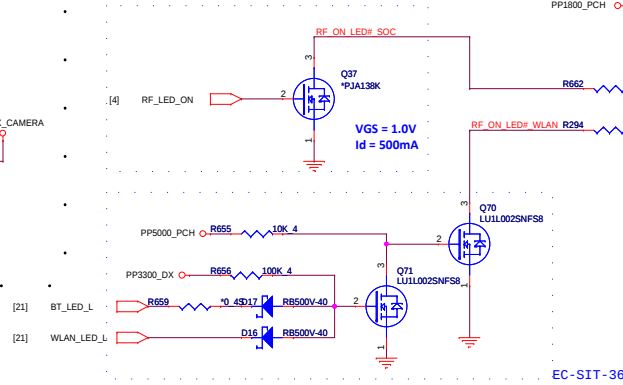
CCD+MIC+LOGO+WLAN LED+Sensor board CONN

CAMERA VCC

+CAM_VCC
Max Current : 800mA



EC-SVT-03

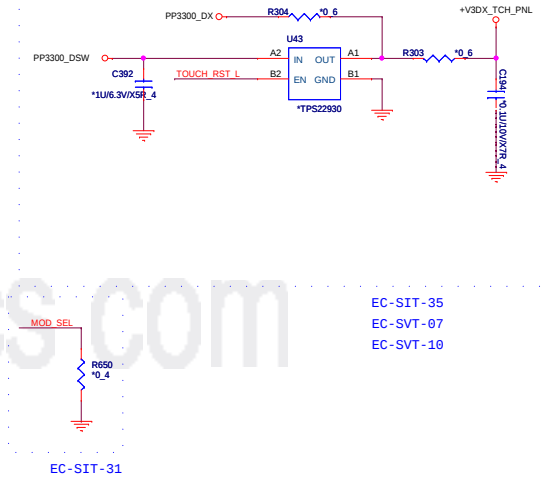


[15,16,20,21,22,23,24,28,29,30,37,38,39,40]
[6,16,24,25,27,28,30,31]
[30,31,32,33,34,37,41]

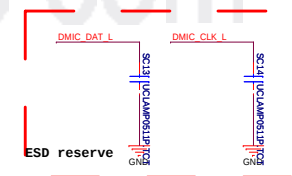
PP3300_DX
PP3300_RTC
VIN

18

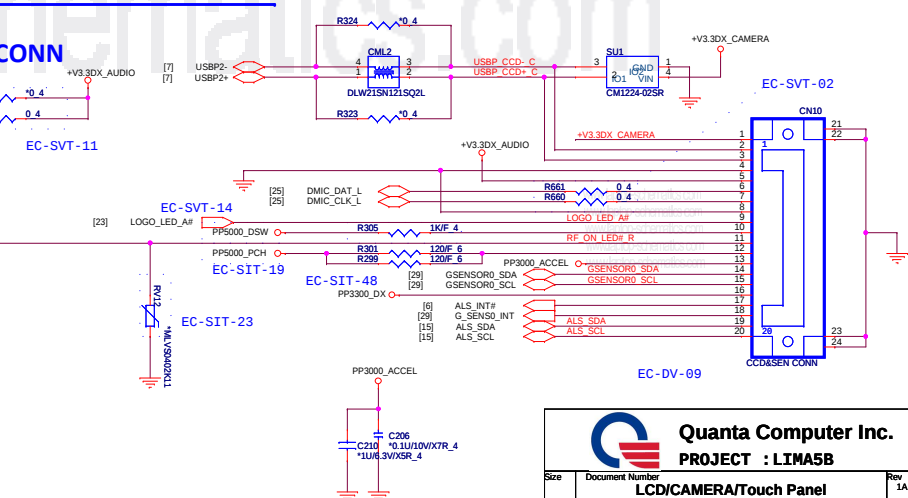
Touch Panel VCC

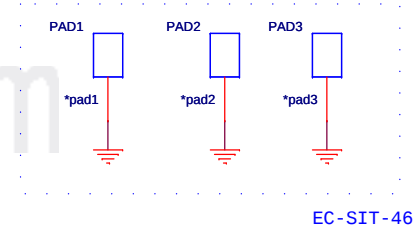
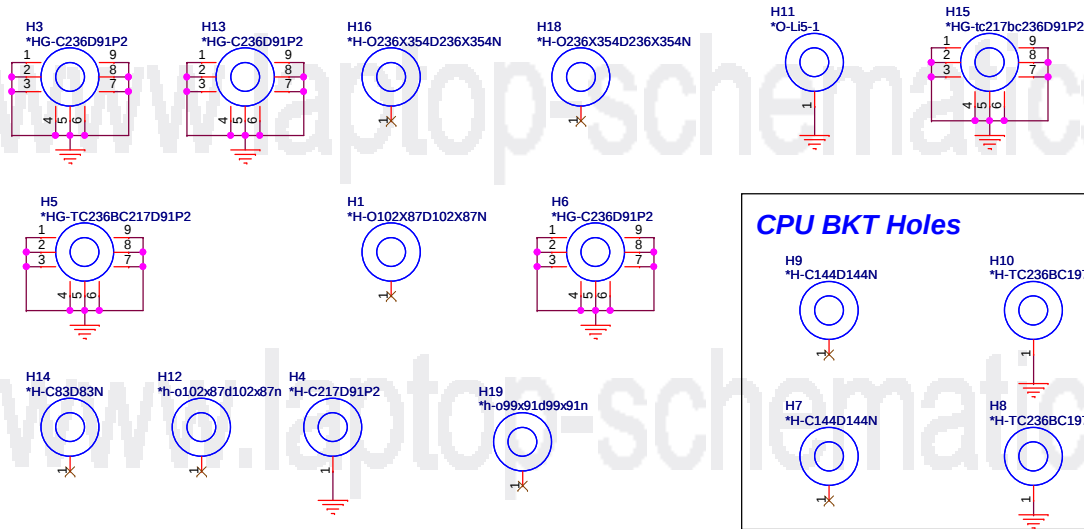


EC-SIT-35
EC-SVT-07
EC-SVT-10



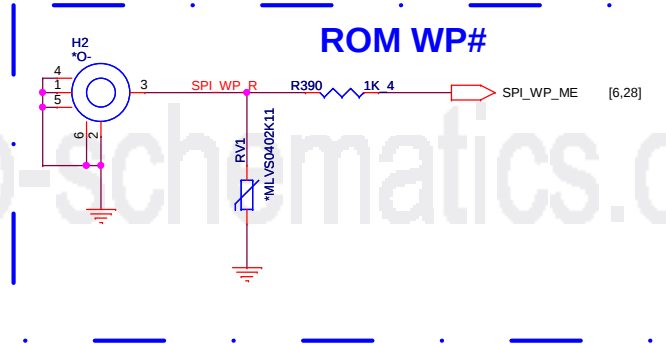
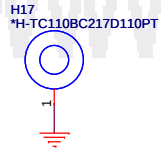
EMI reserved





Stuff NUT Location:

NGFF WLAN Nut



PROJECT : LI5
Quanta Computer Inc.

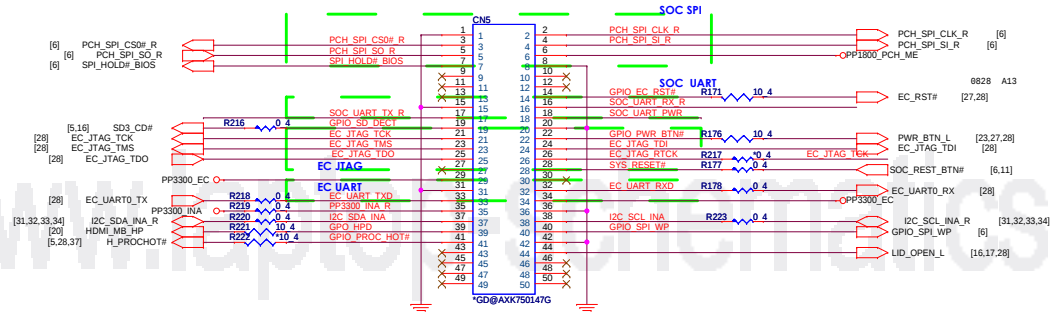
Size	Document Number	Rev
B		1A

Screw Hole

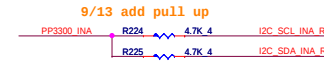
Date: Wednesday, April 16, 2014 Sheet 18 of 50

GOOGLE Debug Port(MPC) **50 pin BTB is MUST, don't use 42 pin** **Socket part number AXK750147G**

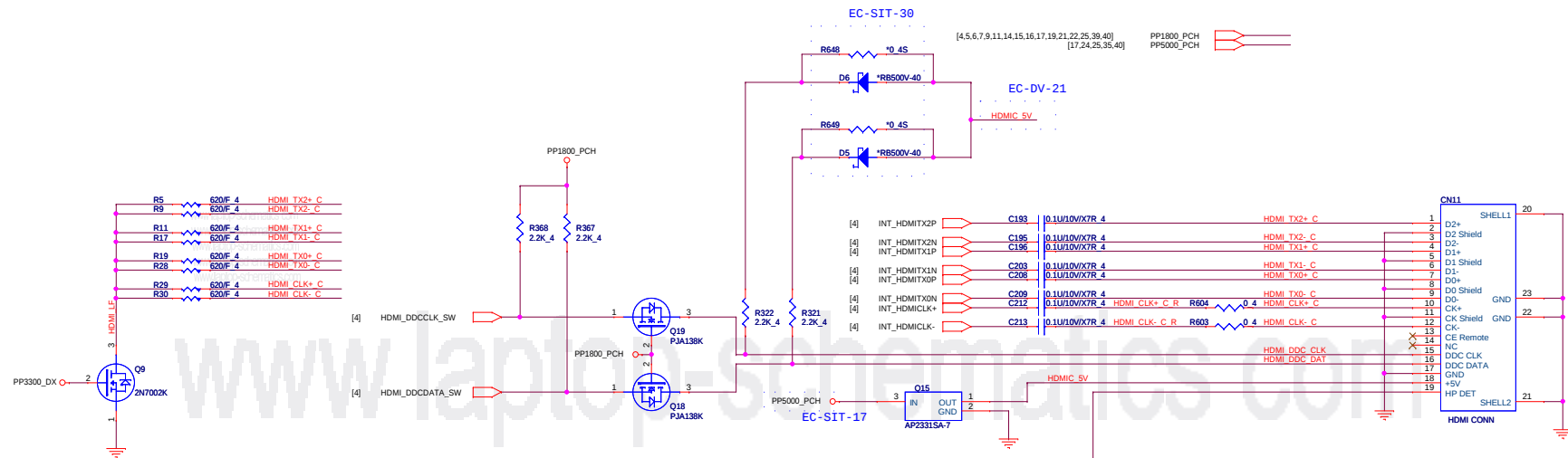
PIN7 OD PIN39 OD PIN49 OD
 PIN14 OD PIN41 OD PIN50 OD
 PIN19 OD PIN43 OD
 PIN22 OD PIN44 OD
 PIN28 OD PIN45 OD
 PIN30 OD PIN46 OD
 PIN37 OD PIN47 OD
 PIN38 OD PIN48 OD



1021 change footprint and PN



9/6 using optional instead of level shifted, default is from SoC

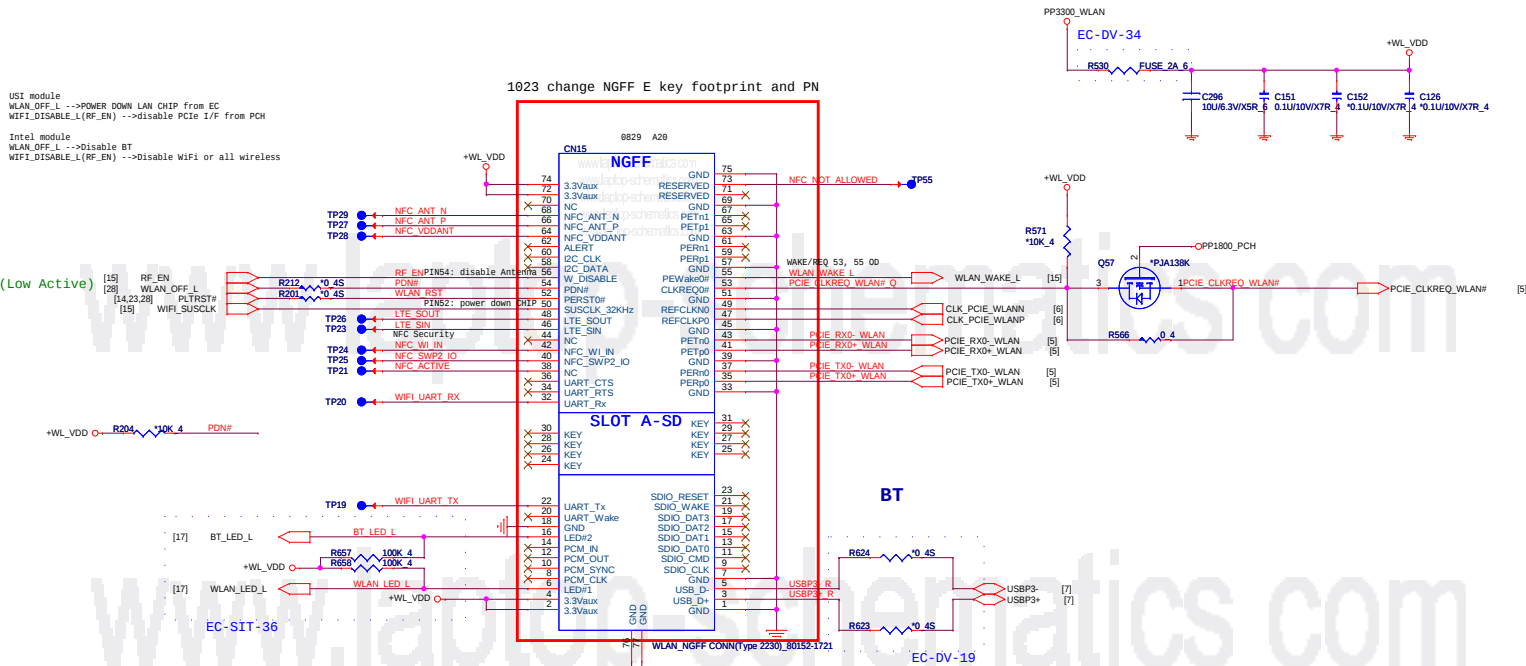


```

USI module
WLAN_OFF_L -->POWER DOWN LAN CHIP from EC
WIFI_DISABLE_L(RF_EN) -->disable PCIe I/F from PCH

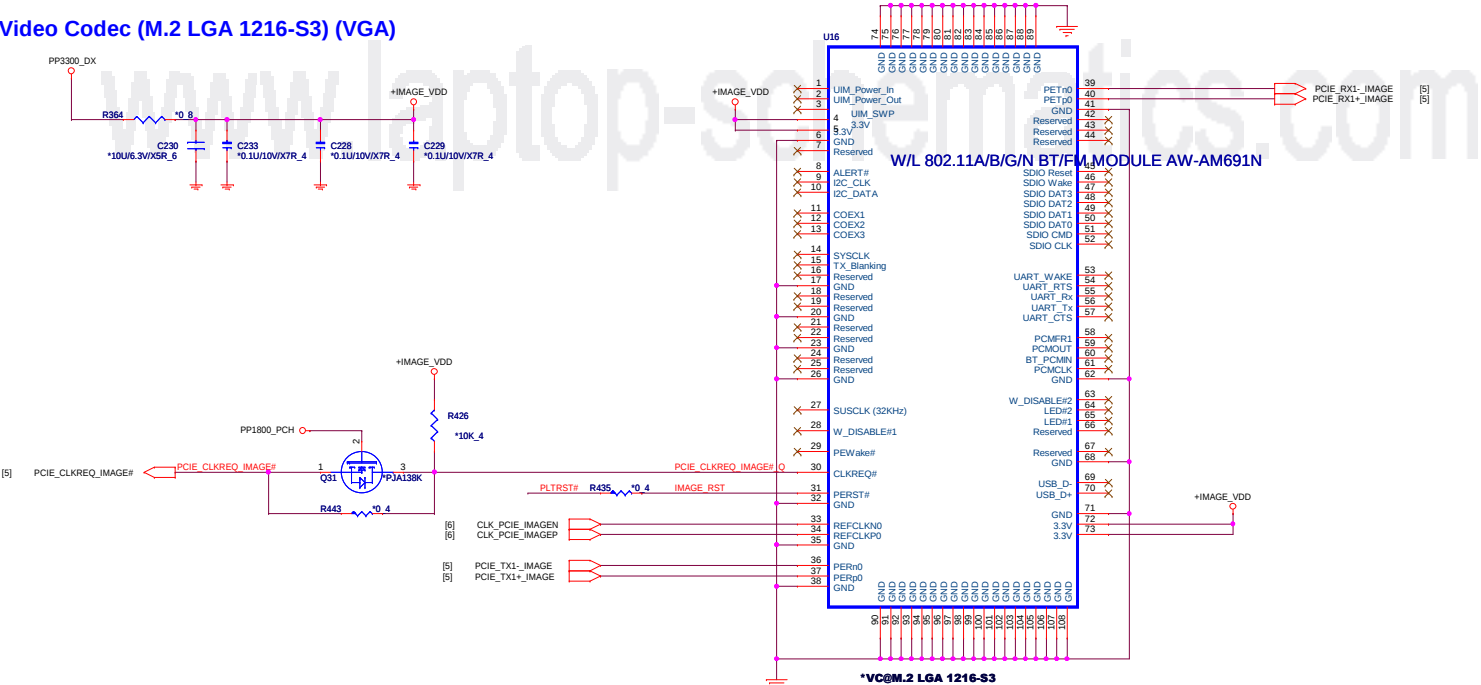
Intel module
WLAN_OFF_L -->Disable BT
WIFI_DISABLE_L(RF_EN) -->Disable WiFi or all wireless

```



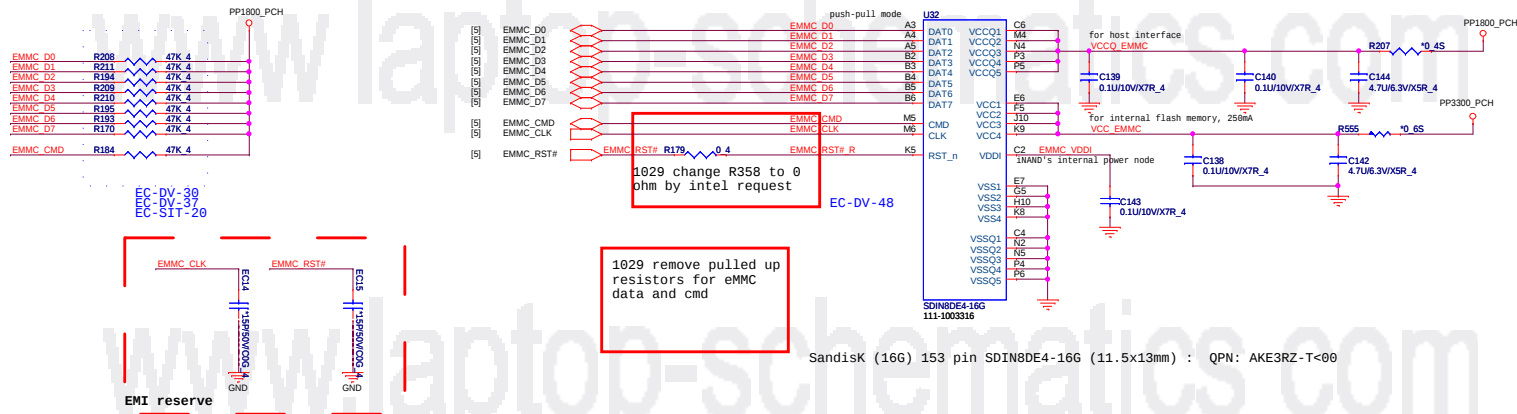
EC-DV-12
EC-SVT-19

Video Codec (M.2 LGA 1216-S3) (VGA)

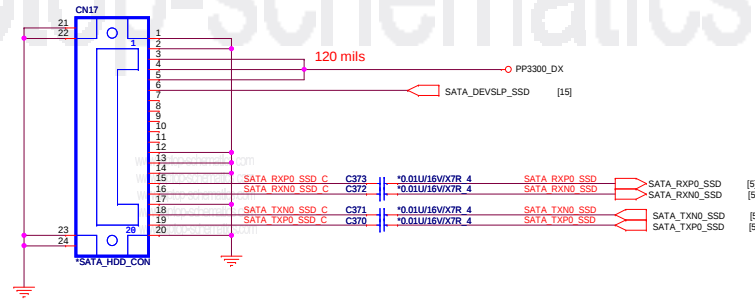


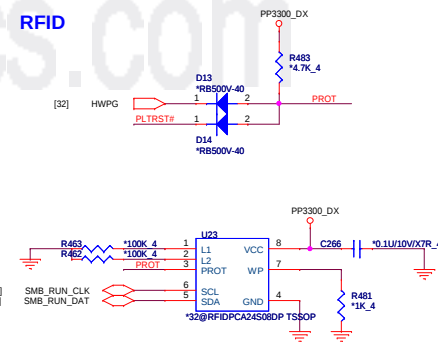
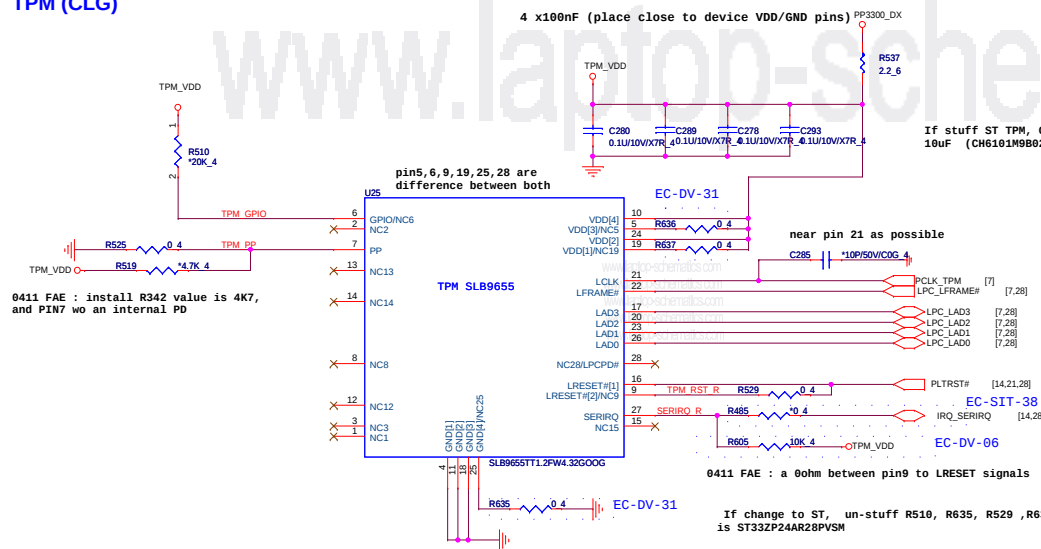
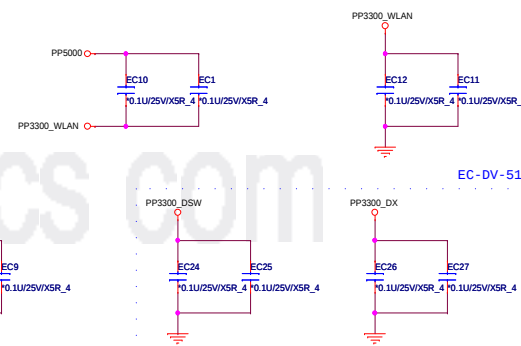
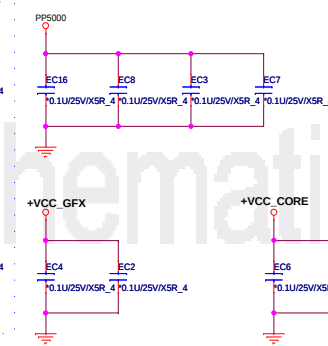
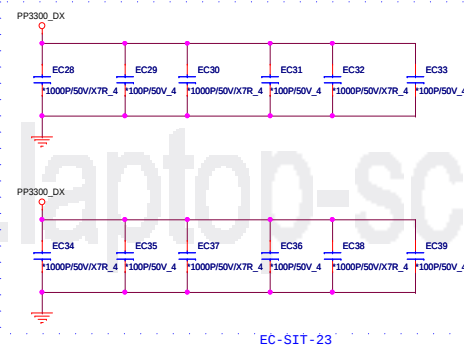
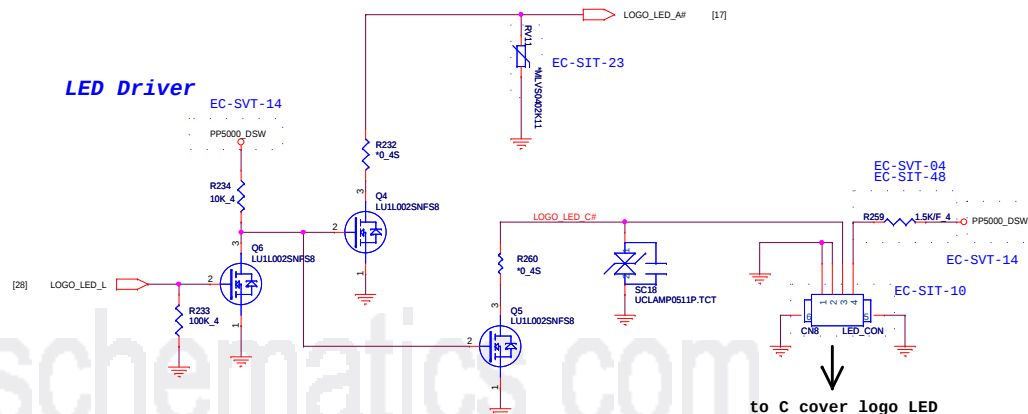
EMMC (CBS)

Add pulled up resistors for sandisk debugging

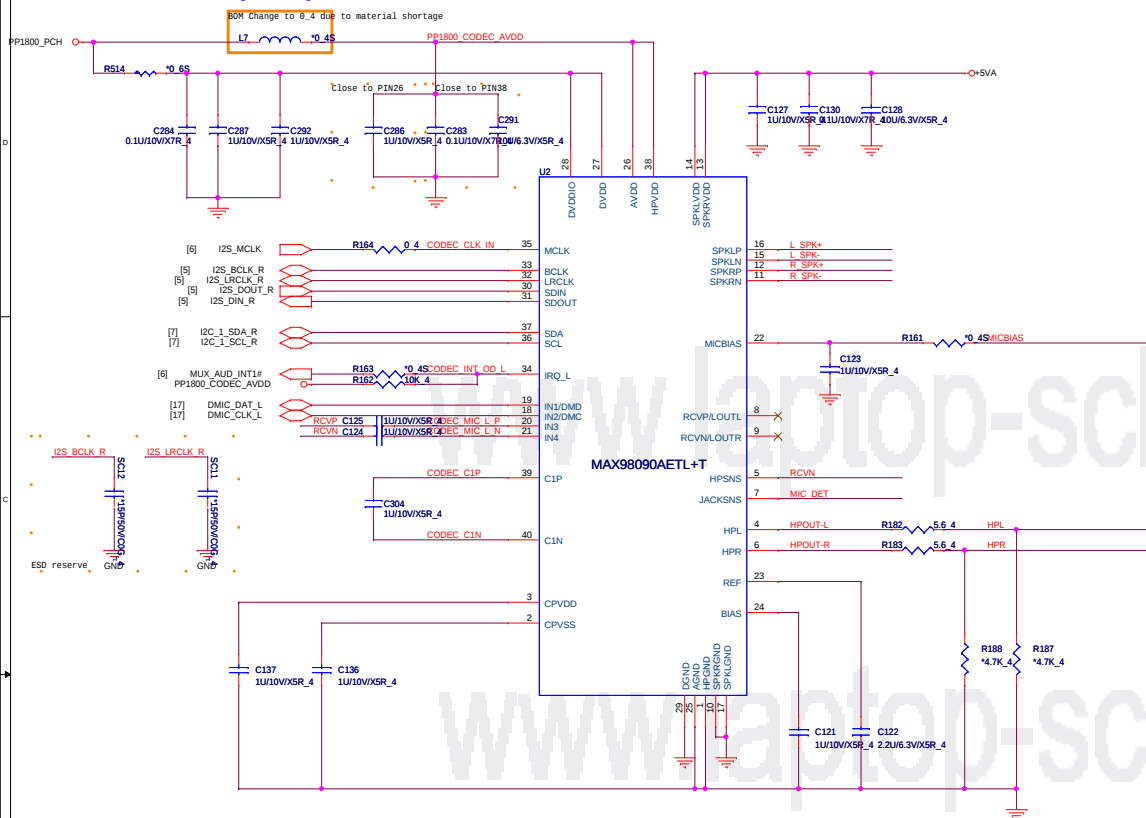


To SSD board

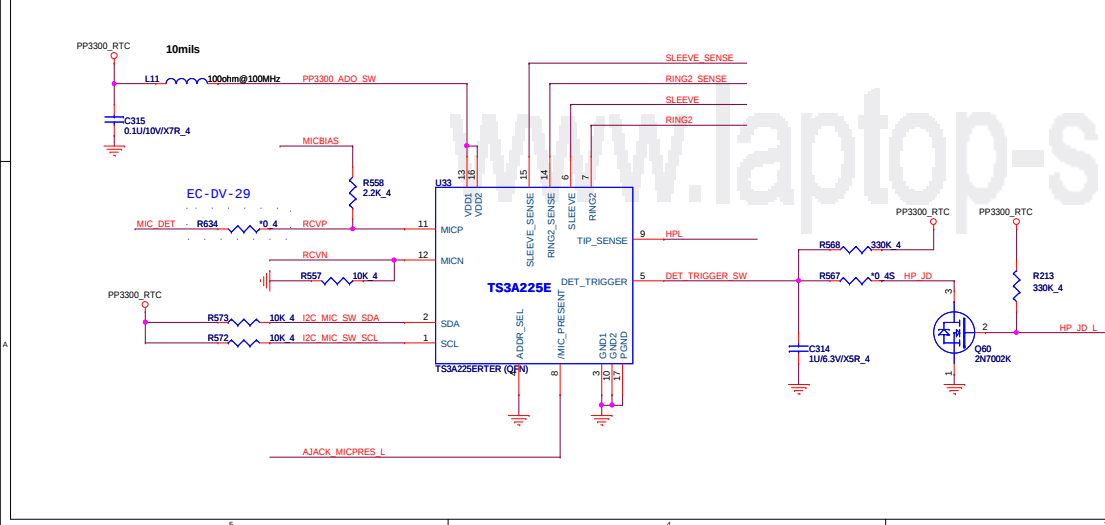




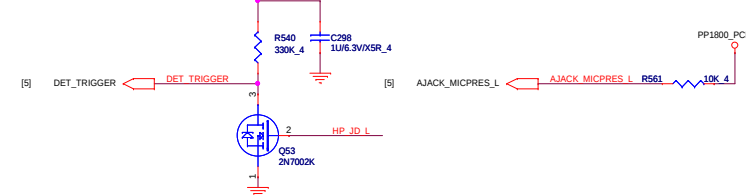
AUDIO CODEC (ADO)



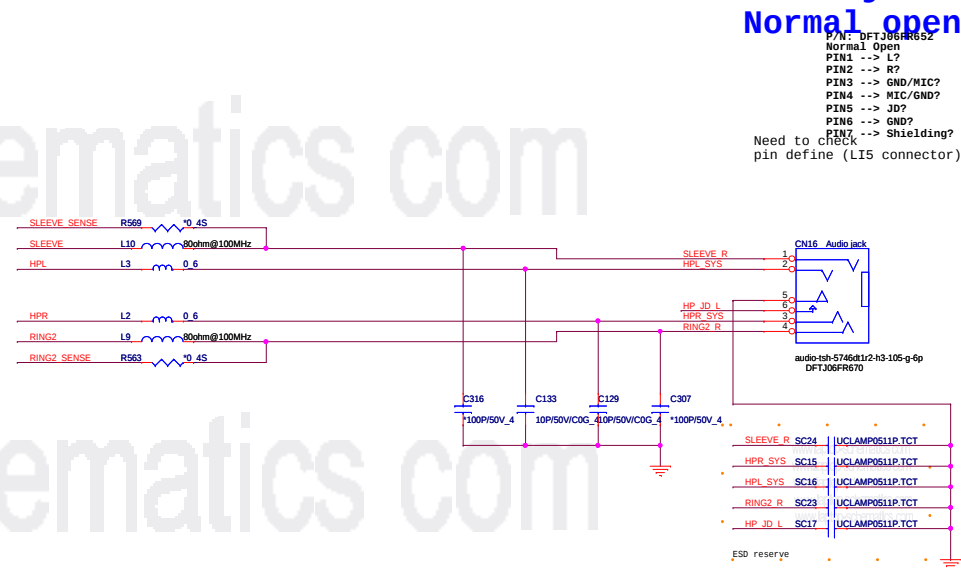
Audio Headset Switch



SOC DET



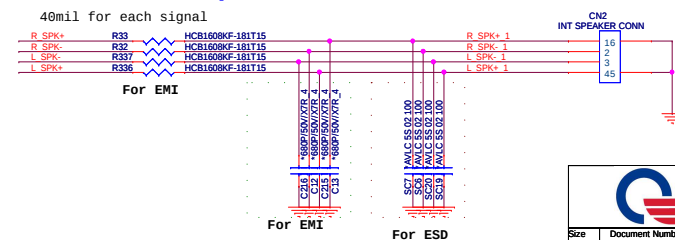
HEADPHONE/Mic combo(ADO)



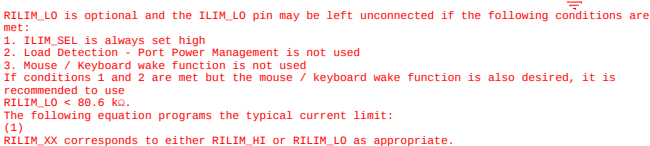
Codec PWR 5V(ADO)



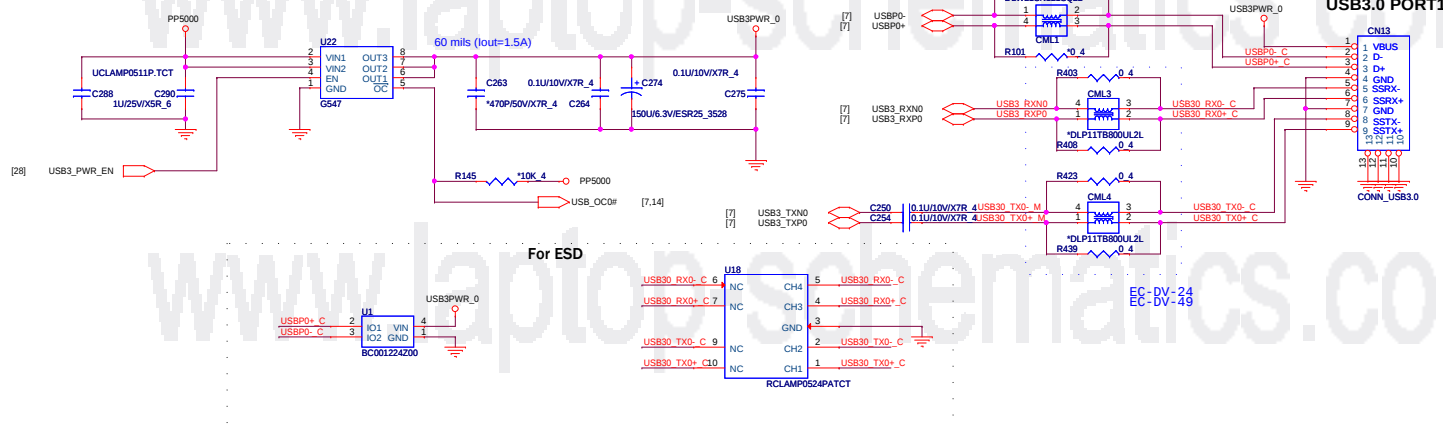
Internal Speaker



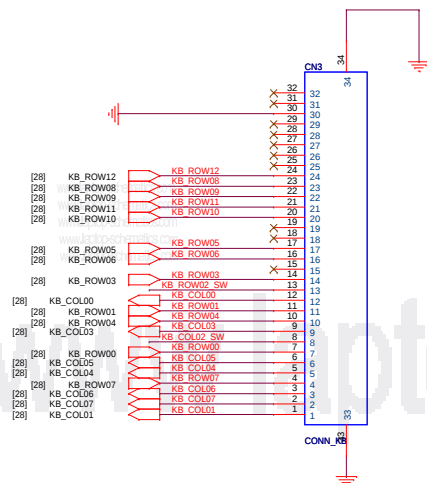
USB2.0 Port1



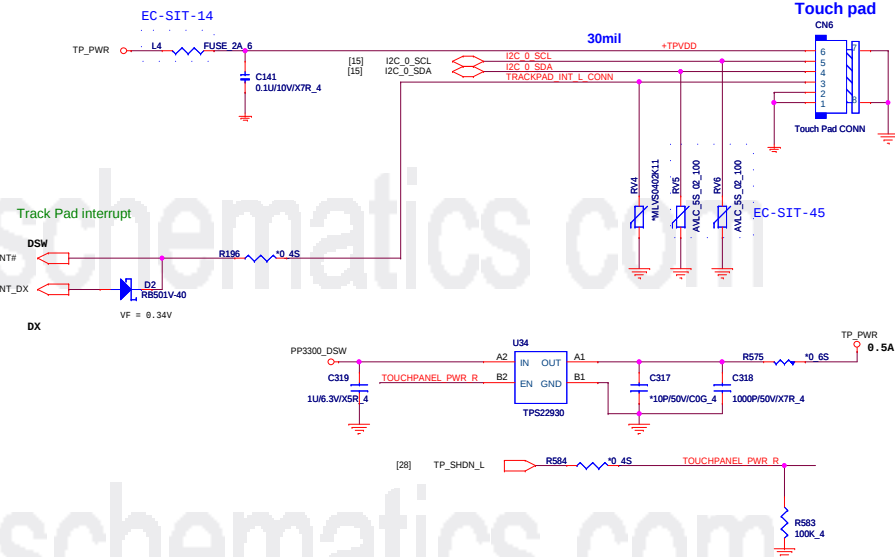
For ESD suggestion



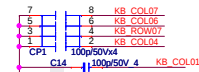
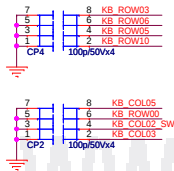
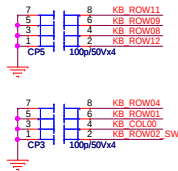
K/B (KBC)



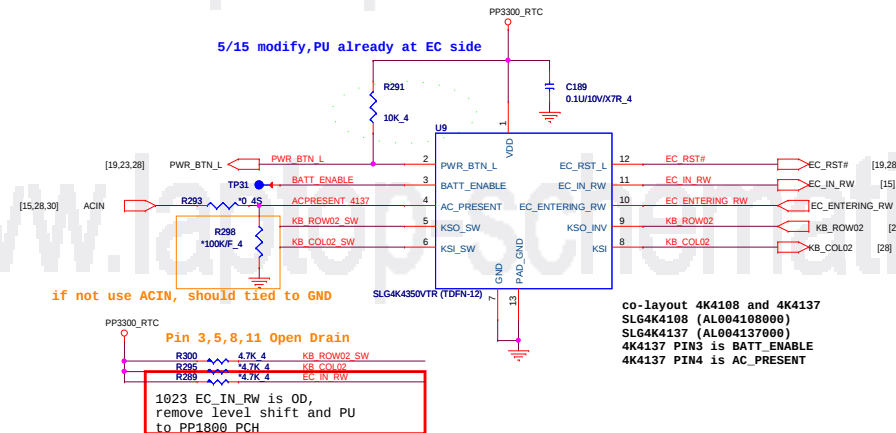
Track PAD BOARD CONN (TPD)



EC-DV-17

HOLELESS RESET
2-CHIP(KBC)

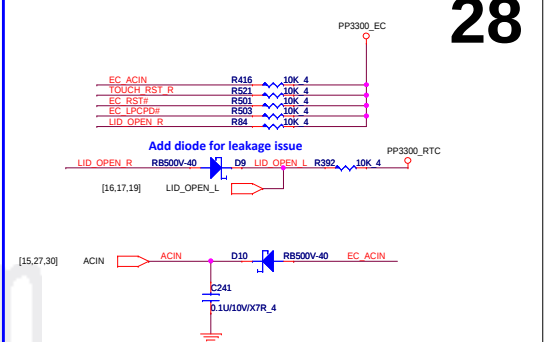
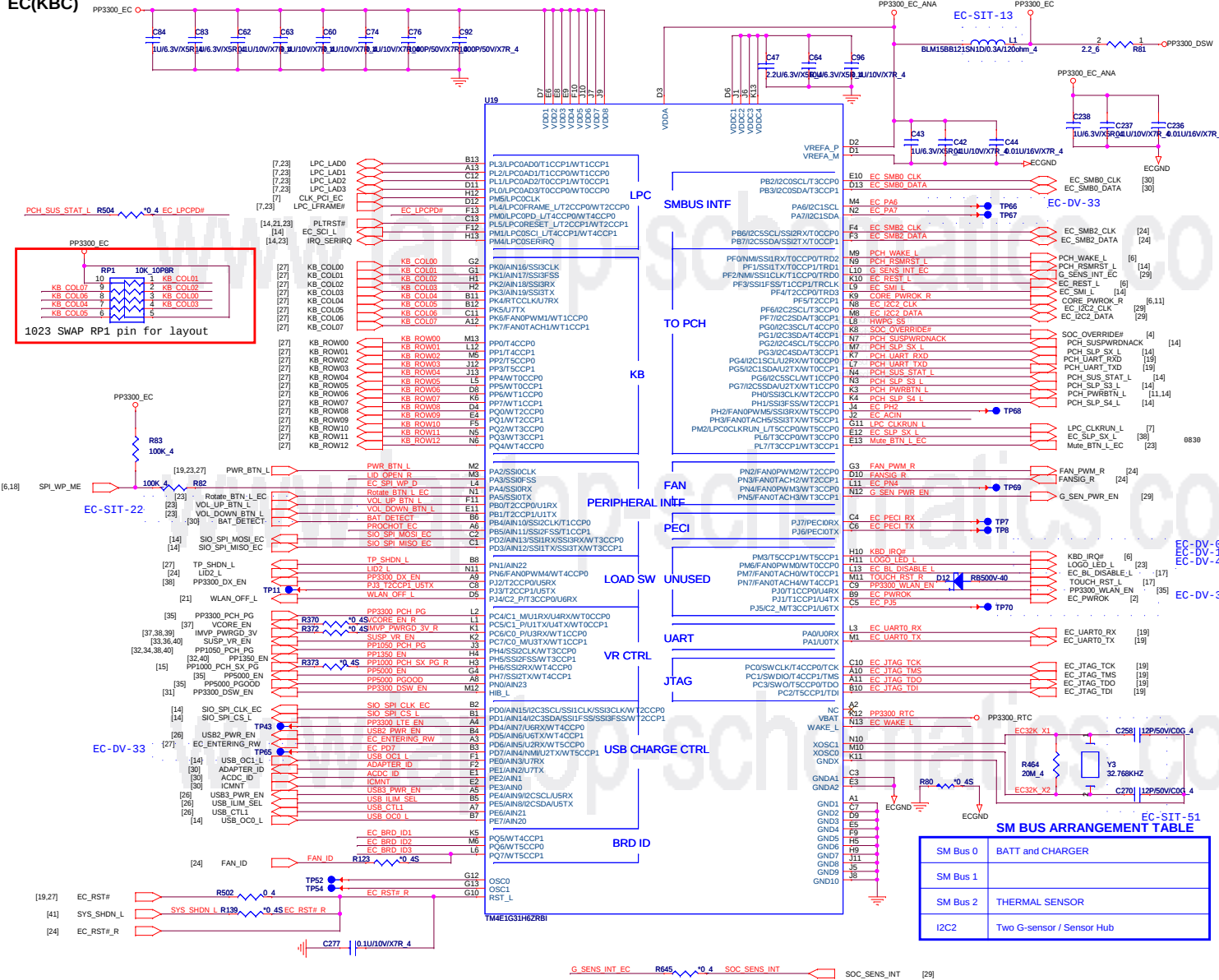
5/15 modify, PU already at EC side



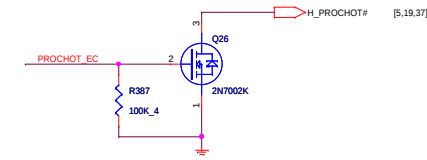
Connect to EC reset pin

Connect to GPIO on CPU
with PU to GPIO power
wellConnect to EC pin C5 (must
be low when EC IN RESET)

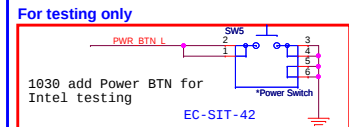
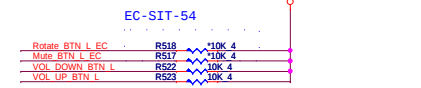
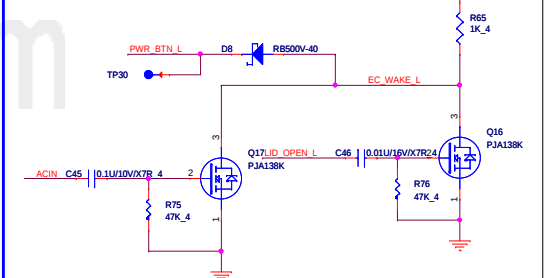
co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT



SM BUS/I2C PU(KBC)

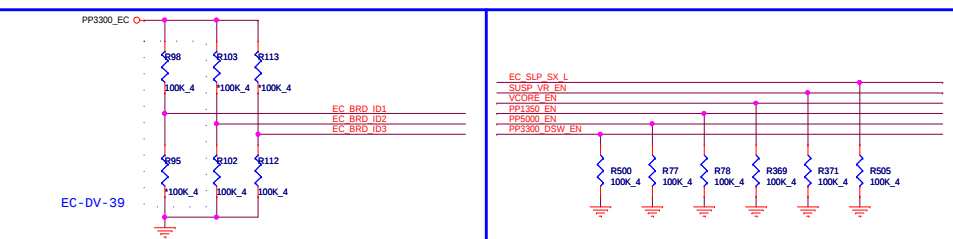


EC HIB WAKE SOURCES



 **Quanta Computer Inc.**
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Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1A
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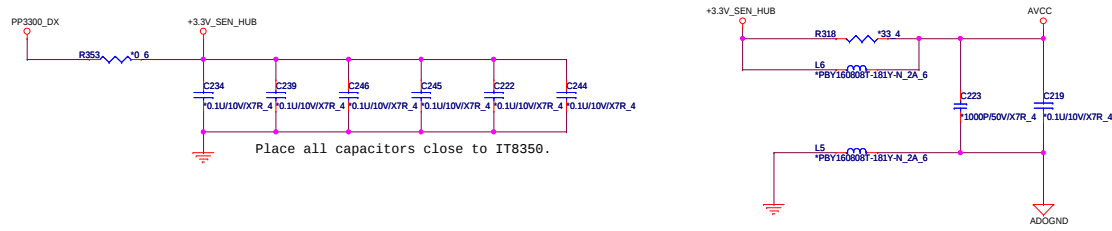
HWPG(KBC)



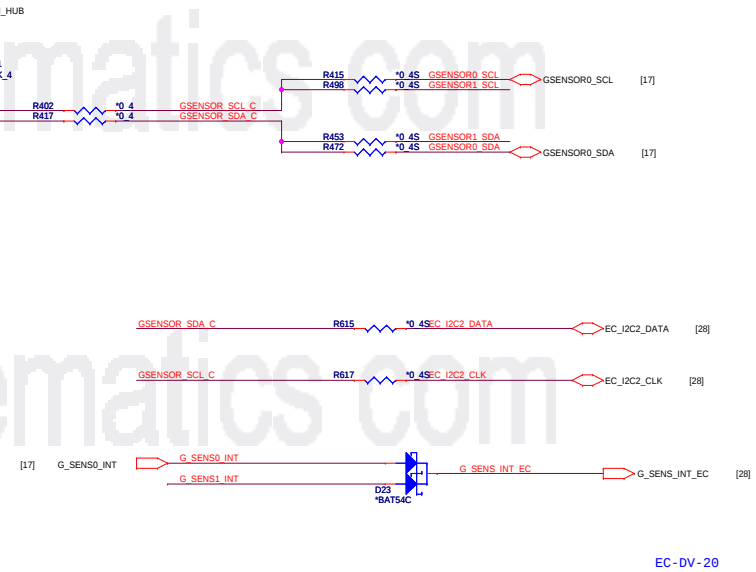
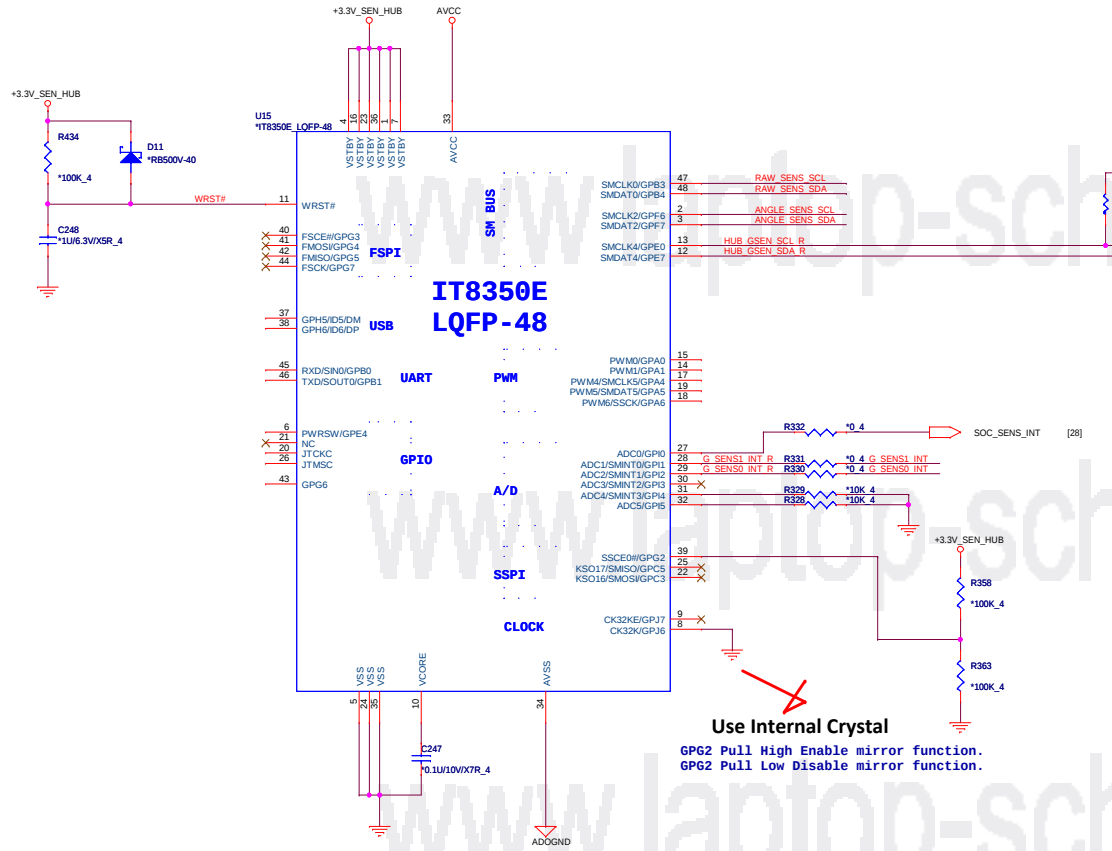
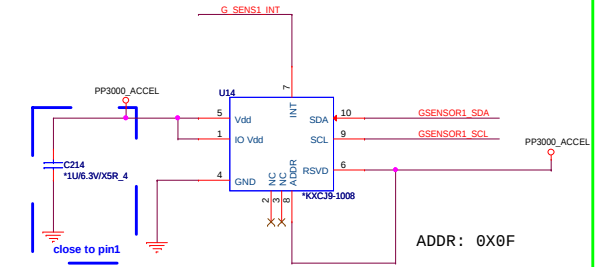
OD pin list

```
EC_REST_L
BAT_LED0
BAT_LED1

SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L
```

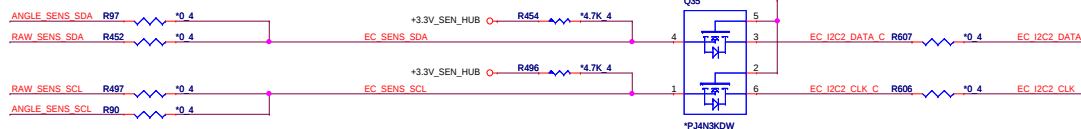


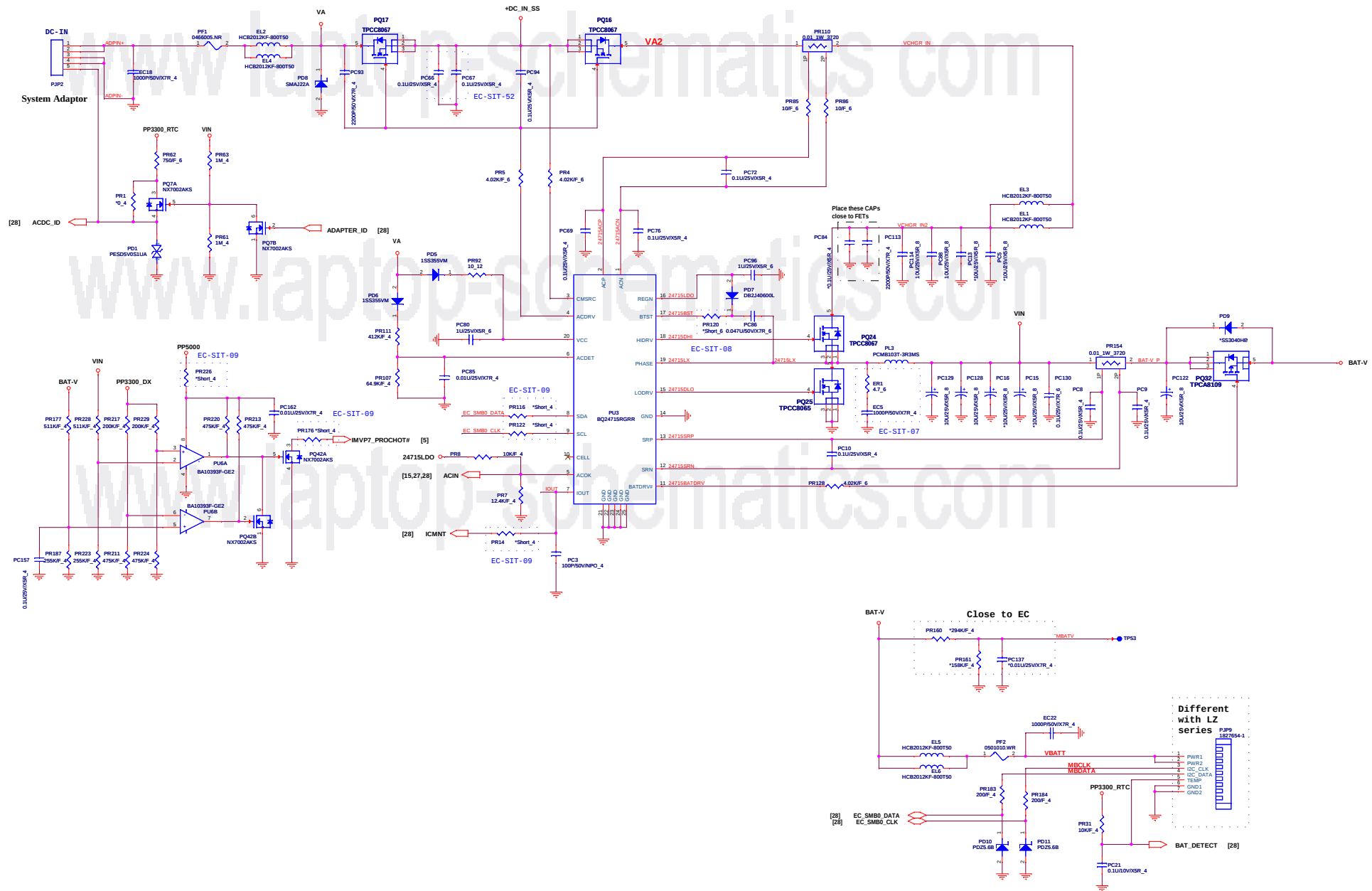
G-SENSOR on MB

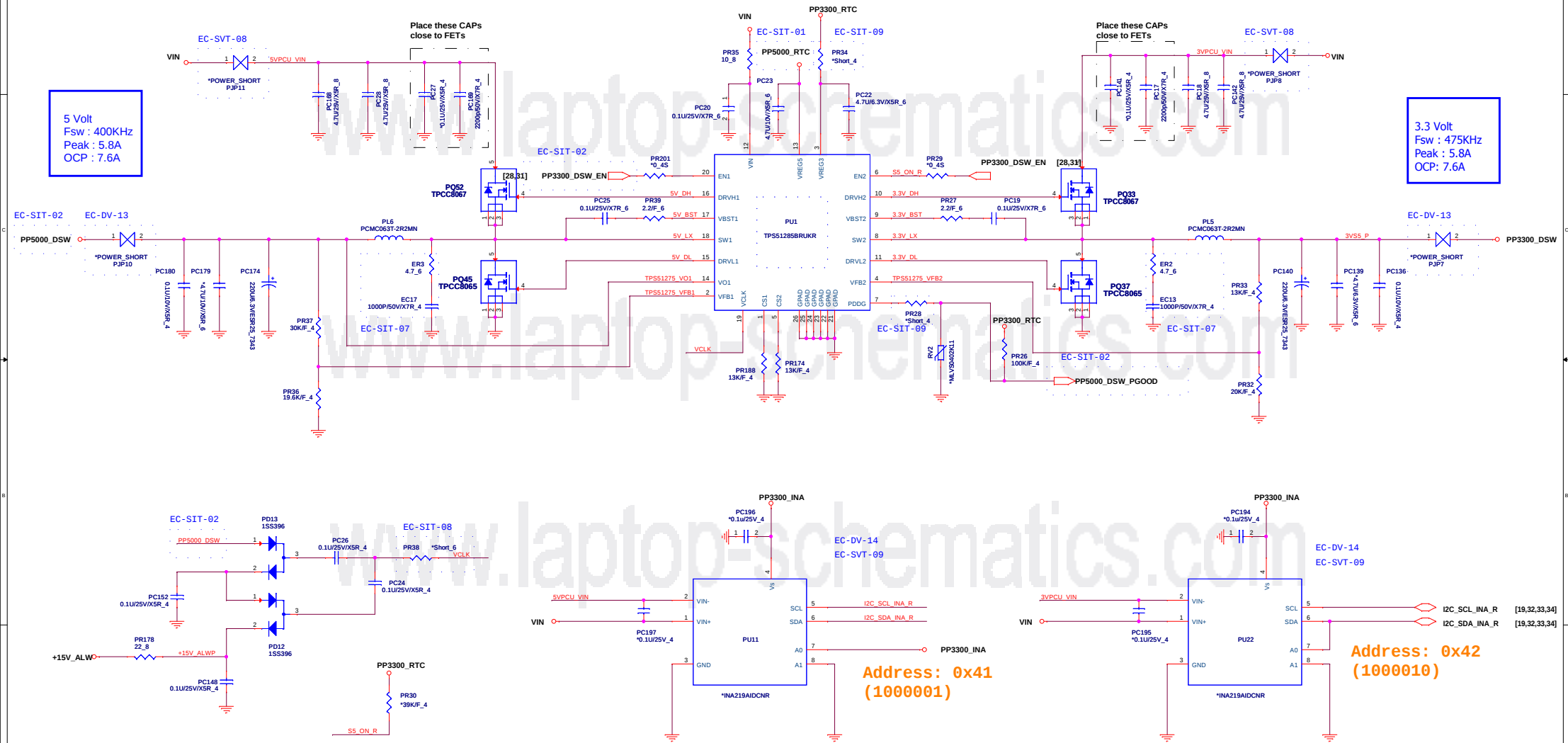


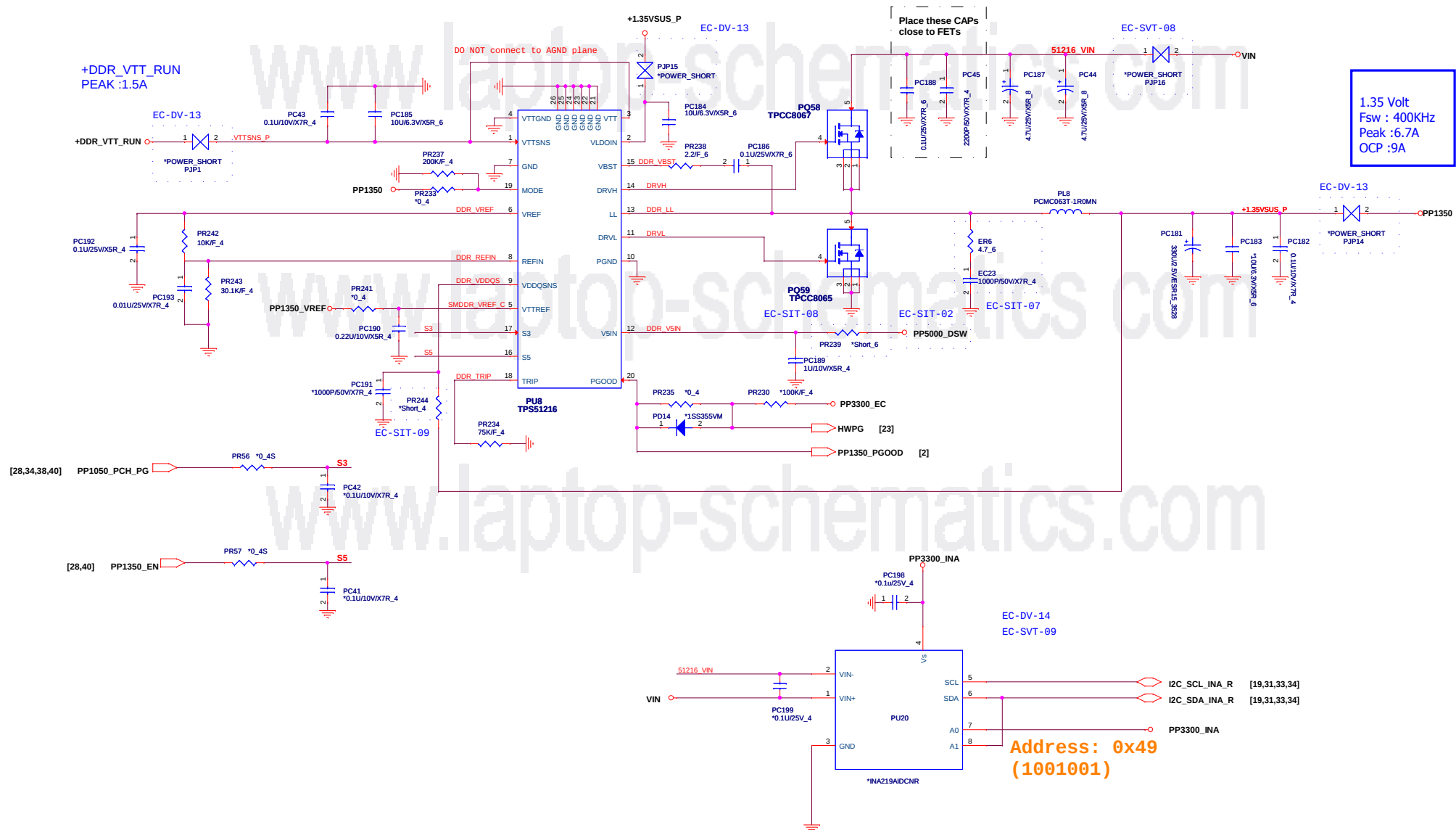
leakage

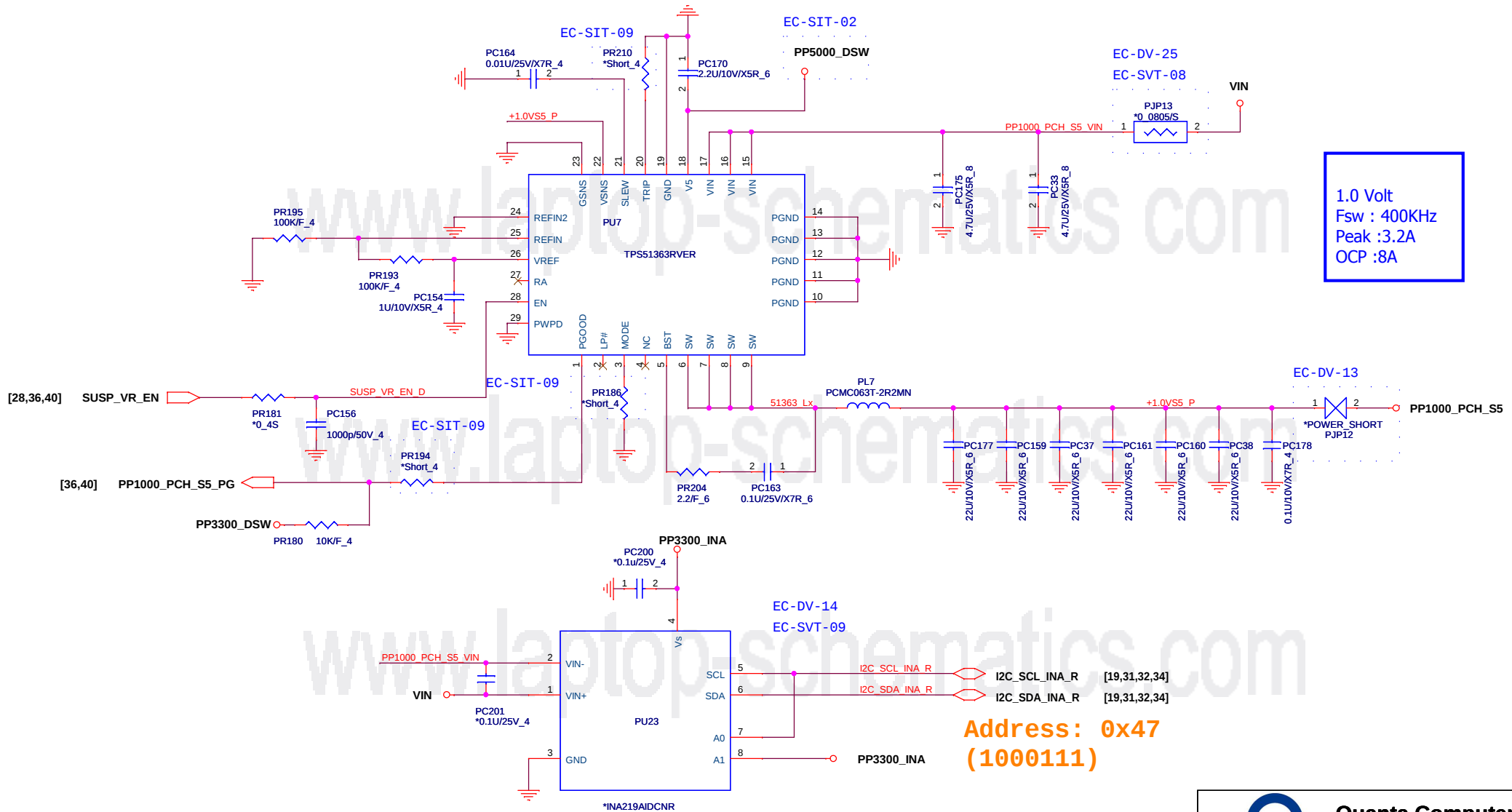
To EC I2C2





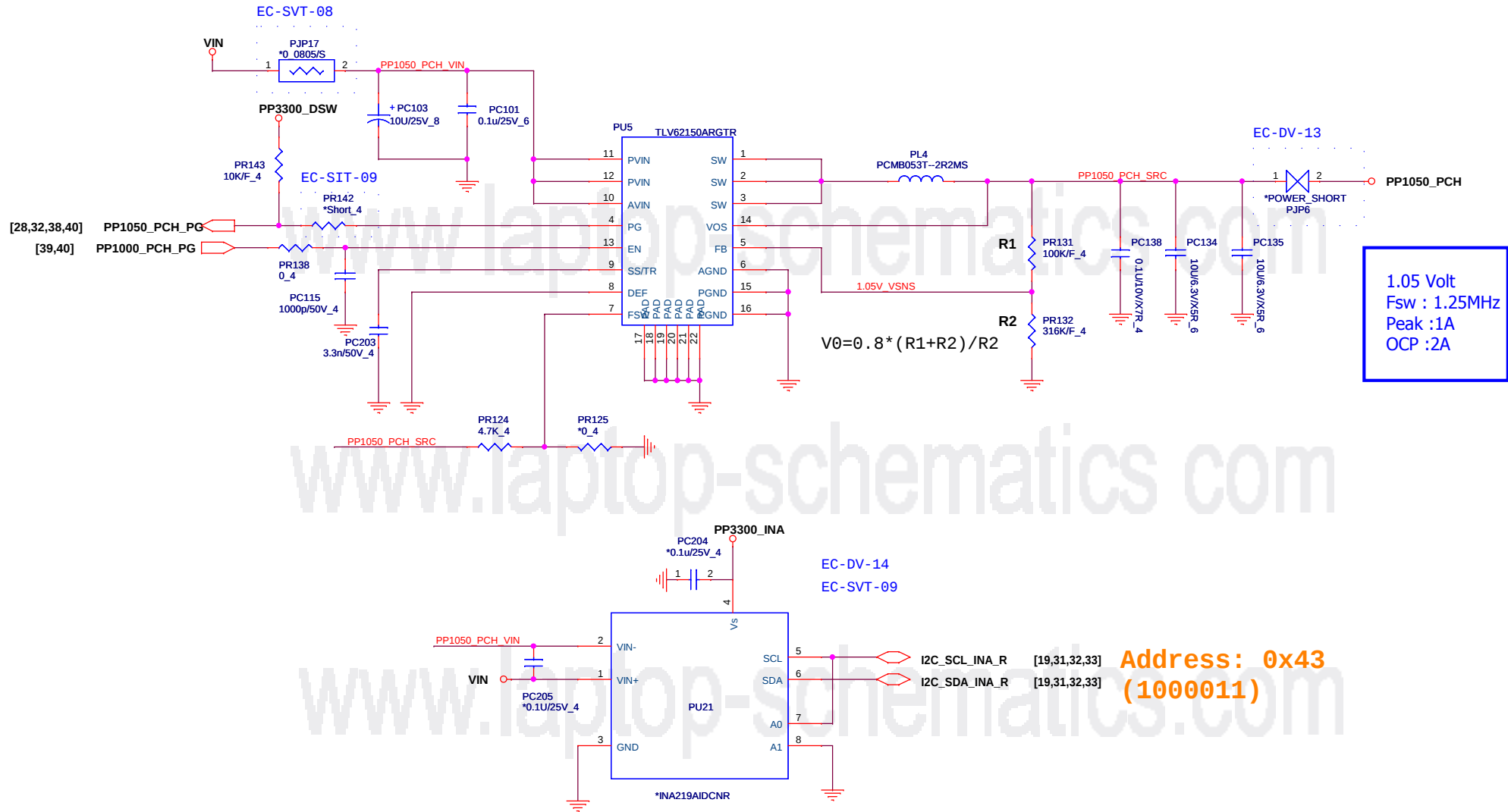






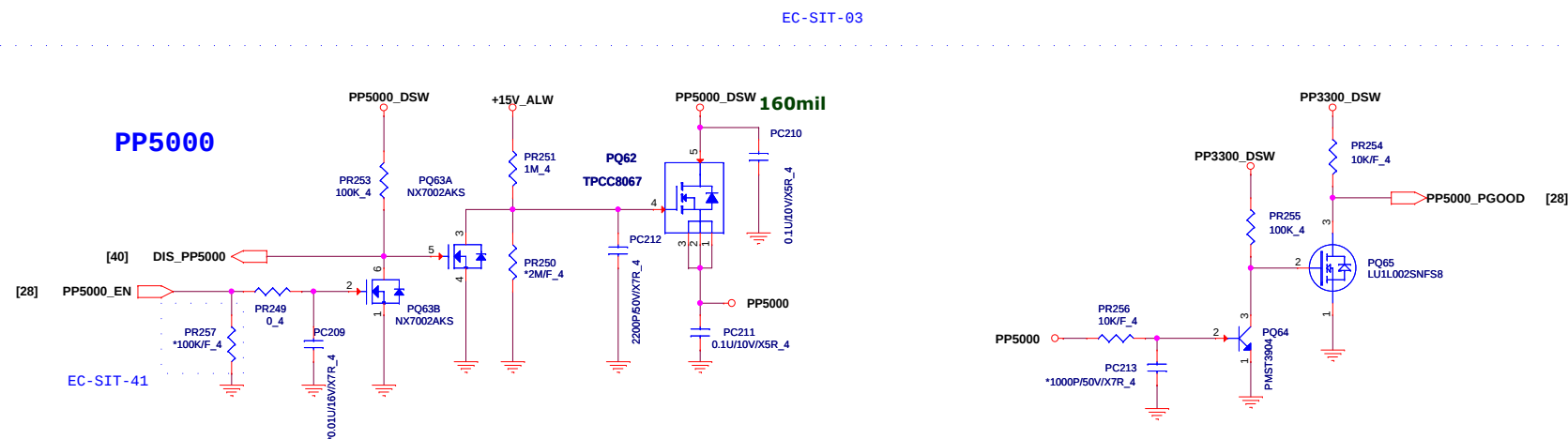
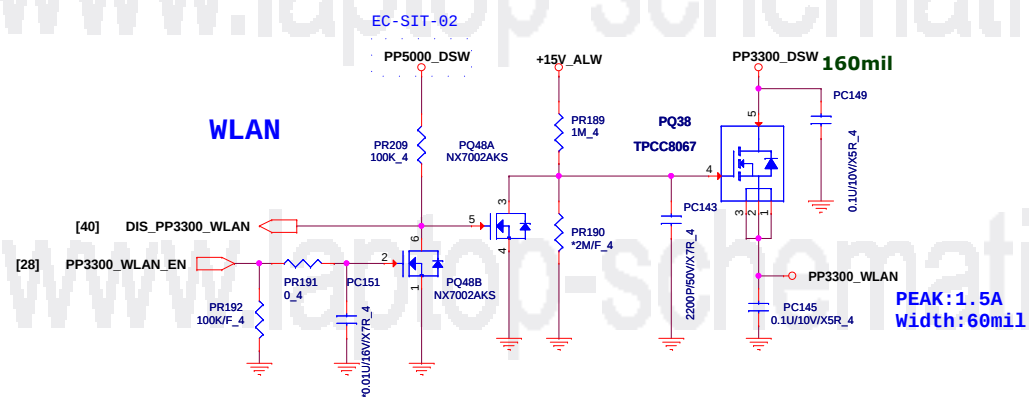
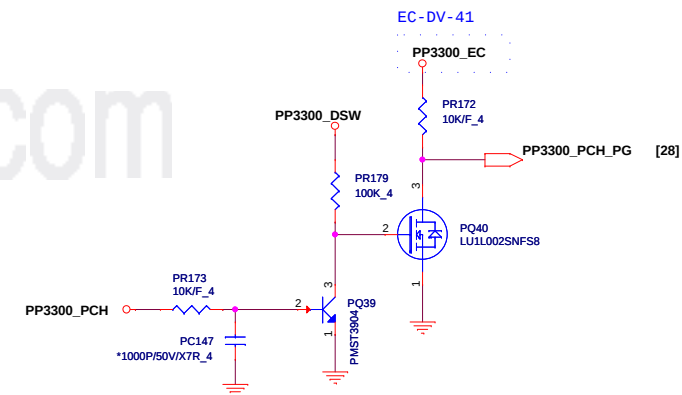
Quanta Computer Inc.
PROJECT : LIMA5B

Size	Document Number	Rev
	+1.0VS5(TPS51363)	1A
Date:	Wednesday, April 16, 2014	Sheet 33 of 50



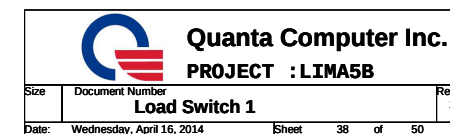
Quanta Computer Inc.
PROJECT : LIMA5B

Size	Document Number	Rev
	+1.05V (TLV62150ARGTR)	1A
Date:	Wednesday, April 16, 2014	Sheet 34 of 50

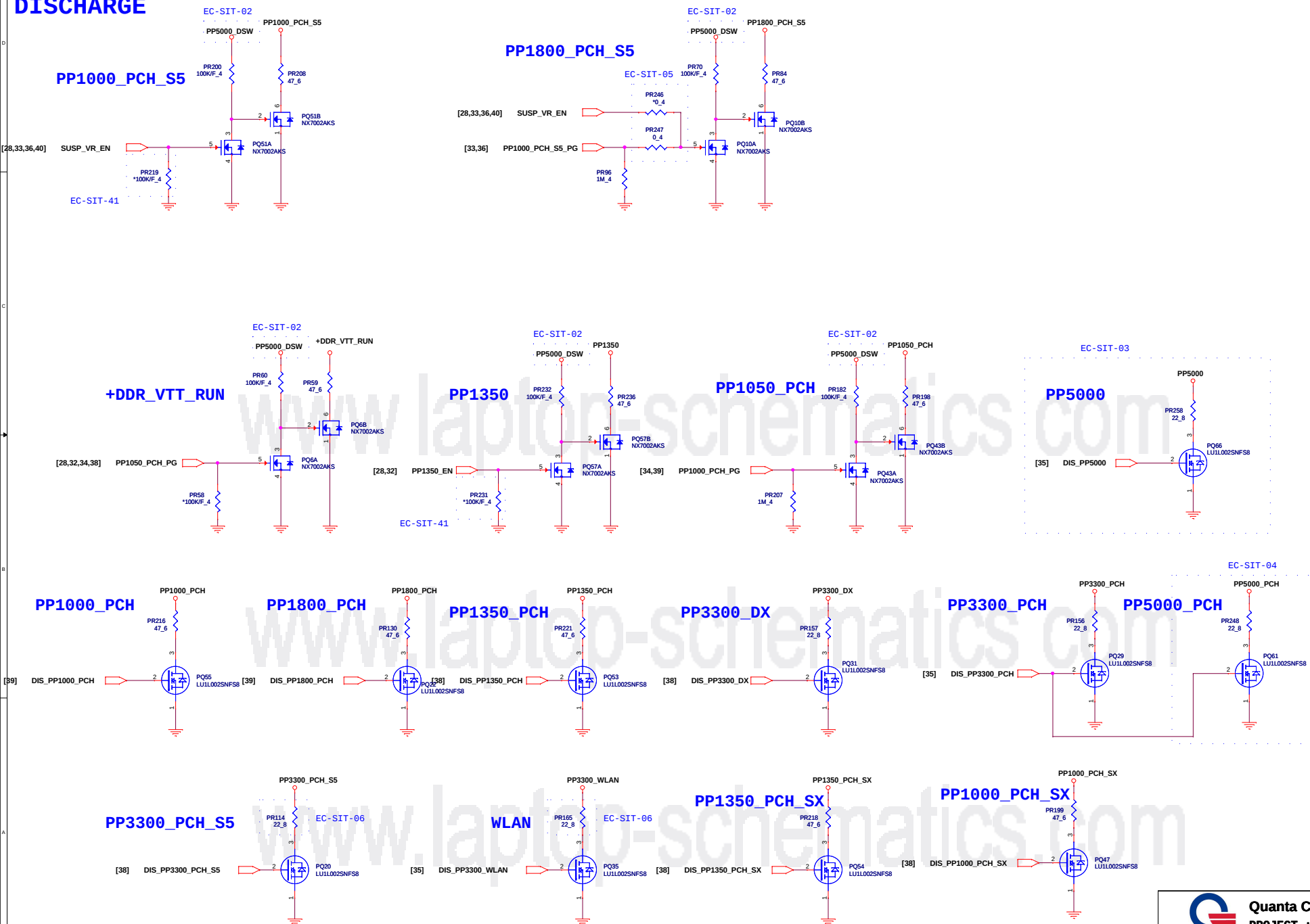


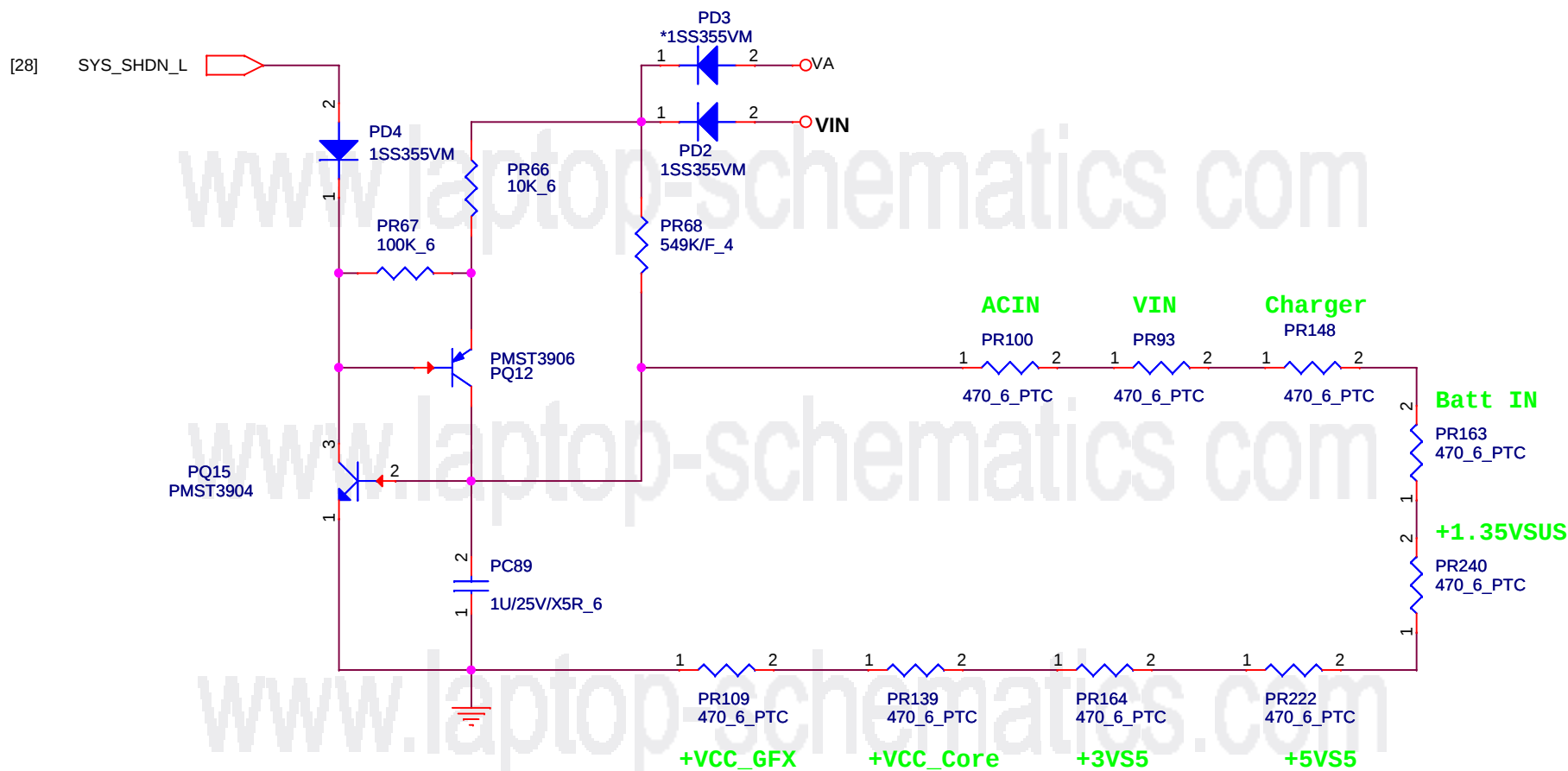


38



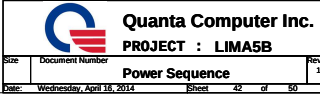
DISCHARGE





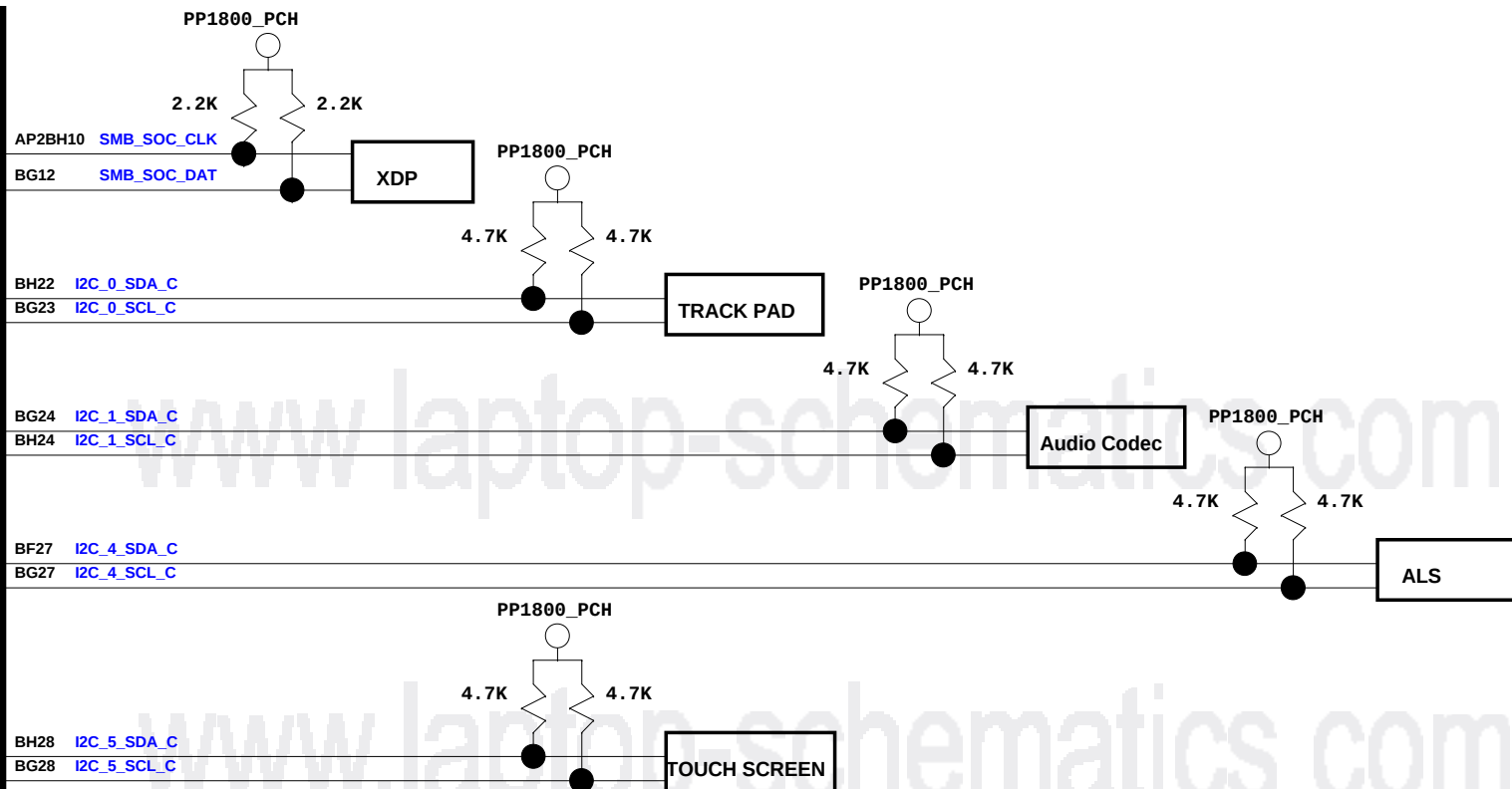
Quanta Computer Inc.
PROJECT : LIMA5B

Size	Document Number	Rev
	PTC	1A
Date:	Wednesday, April 16, 2014	Sheet 41 of 50

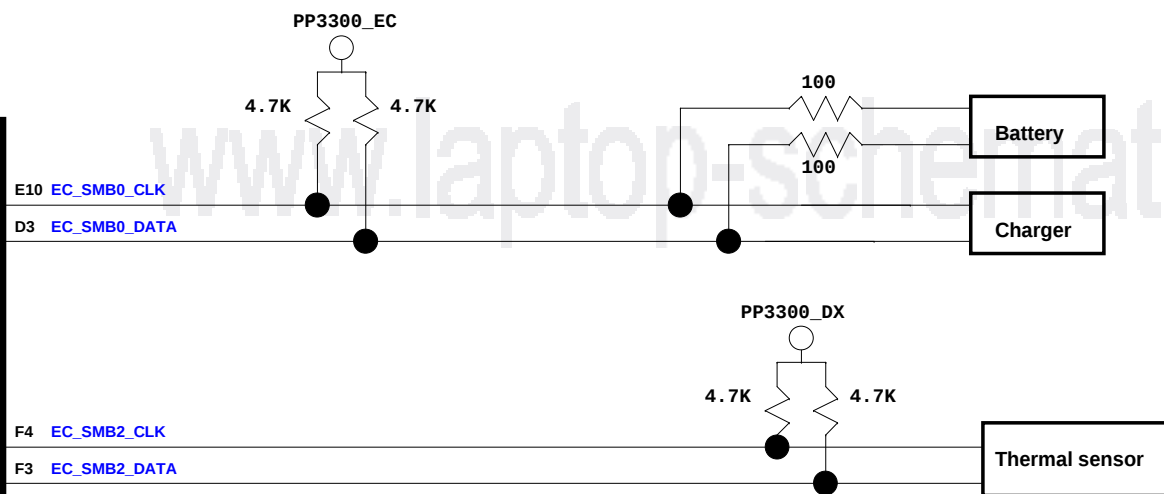


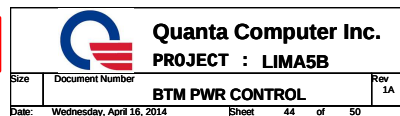
SMBUS
Bay-trail M

I2C

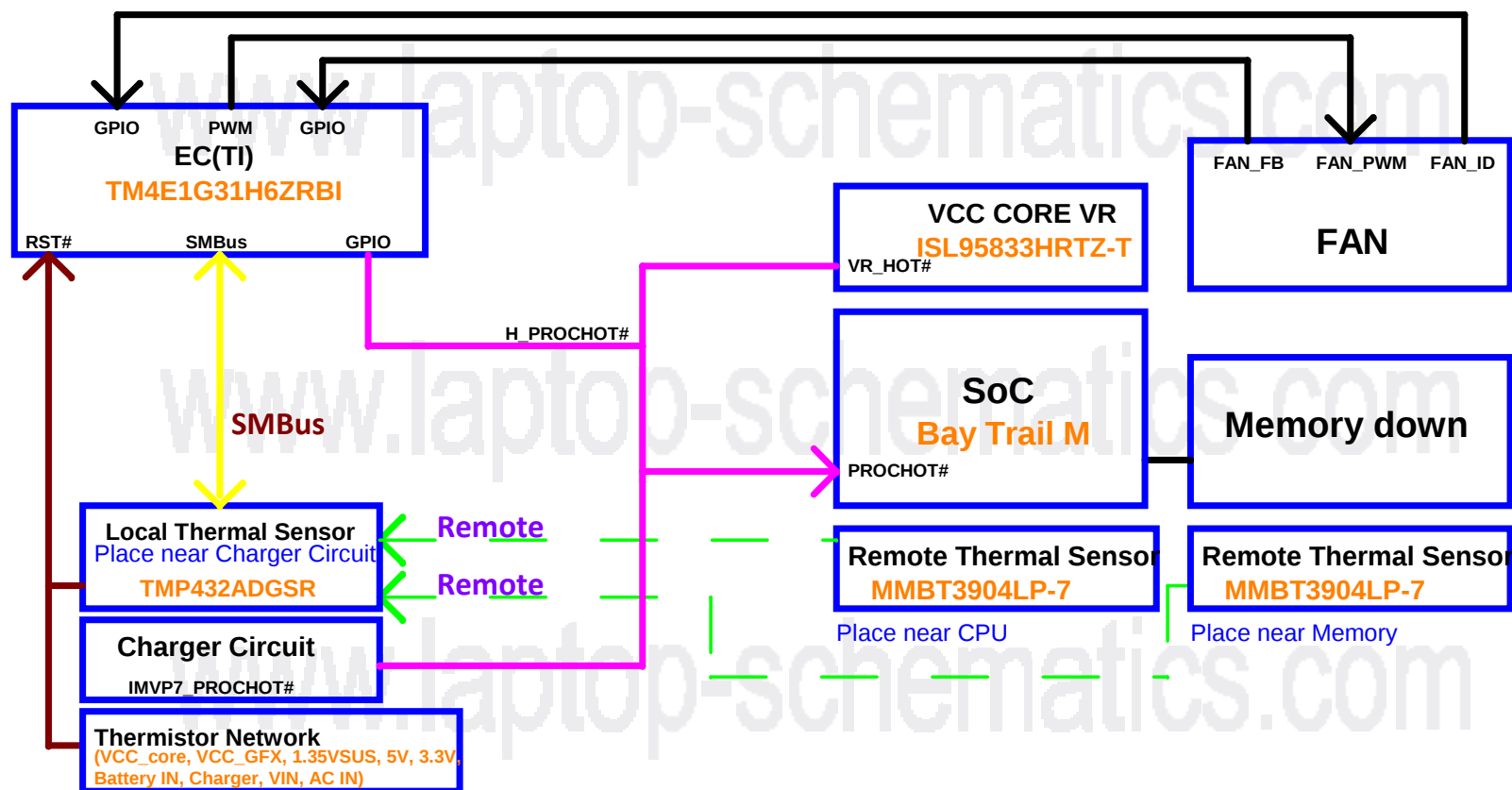


KBC
TI
SMBUS





Thermal Block Diagram



LI□A5B Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-DV-01	6	Pull up according to page 34 of Intel check list	R599
EC-DV-02	6,28	Add Net: KBD_IRQ# and R600 for following Rambi.	R600 and Net
EC-DV-03	14	Remove R512, because SERIRQ of TPM needs 3V (Follow Rambi).	R512
EC-DV-04	14	Add 0 ohm, R601 and R602, on VCCA and VCCB for debugging (Follow Rambi).	R601 and R602
EC-DV-05	20	Add R603 and R604 and reserve L12 (Follow Rambi).	R603, R604, and L12
EC-DV-06	23	Add R605 to pull up on SERIRQ_R to TPM_VDD (Follow Rambi).	R605
EC-DV-07	42,44	Update power sequence and power tree (Follow Rambi).	
EC-DV-08	16	Add C374 for U3 input inrush current (Follow Rambi).	C374
EC-DV-09	17	Change connecting CN10.13 from GND to PP3300_DSW for supporting G-sensor on S3/S5.	CN10.13
EC-DV-10	28	VOL_UP_BTN_L change connecting from U19.F11 to U19.B9, and VOL_DOWN_BTN_L change connecting from U19.E11 to U19.C5 for Google suggestion.	U19.F11, U19.B9, U19.E11, and U19.C5
EC-DV-11	28	G_SENS1_INT_EC connect to U19.F11, and G_SENS2_INT_EC connect to U19.E11 for Google suggestion.	U19.F11 and U19.E11
EC-DV-12	21	Add PCIE re-driver because of layout problem.	U41, C375~C382, and R608~R614
EC-DV-13	31,32,33,34,36,37	PJP1, PJP3, PJP4, PJP5, PJP6, PJP7, PJP10, PJP12, PJP14, and PJP15 change to short pad.	PJP1, PJP3, PJP4, PJP5, PJP6, PJP7, PJP10, PJP12, PJP14, and PJP15
EC-DV-14	31,32,33,34	Add PU11, PU20, PU21, PU22, and PU23 current sense IC.	PU11, PU20, PU21, PU22, and PU23
EC-DV-15	34	Change PWM IC from TPS51312 to TLV62150.	
EC-DV-16	6,14	Delete SPI net from SOC to level shifter, and add test point.	TP56~TP63
EC-DV-17	27	Stuff CP1~CP5 and C14 for ESD suggestion.	CP1~CP5 and C14
EC-DV-18	23,28	Rotate_BTN_L_EC connect to U19.H11.	
EC-DV-19	21	Add CML6, R623, and R624 for Intel suggestion.	CML6, R623, and R624
EC-DV-20	29	Change structure of Yoga mode connection (two G-sensor).	
EC-DV-21	20	HDMI_DDC_DATA and HDMI_DDC_CLK change to pull up to HDMIC_5V.	D6 and D5
EC-DV-22	17	Remove R14 because LID_OPEN_L have R392 to pull up	R14
EC-DV-23	20	HDMI_HPD change to HDMI_MB_HP for connecting to HDMI connector.	Net name change
EC-DV-24	26	Stuff R403, R408, R423, and R439, and un-stuff CML3 and CML4 for EA test.	R403, R408, R423, R439, CML3, and CML4
EC-DV-25	33	Change footprint of PJP13 for power suggestion.	PJP13
EC-DV-26	16	Add a pull down on SoC_EDP_BLON_C and using double inverting OD FETs structure (Follow Rambi) Delete R554, R574, and Q55.	R630, R631, R632, Q66, Q67, R554, R574, and Q55
EC-DV-27	16	R185 changes to 1K to isolate SD socket and servo/SoC (Follow Rambi)	R185
EC-DV-28	16	Add R633 pull up to PP1800_PCH (Follow Rambi)	R633
EC-DV-28	8	Change C95, C20, C21, C72, C97, and C73 to 0603 22uF for ACLL issue (Follow Rambi)	C95, C20, C21, C72, C97, and C73

LI□A5B Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-DV-29	25	Reserve R634 connection from RCVP to MIC_DET as back up in case driver needs to be through codec using JACKSNS pin (Follow Rambi).	R634
EC-DV-30	22	Change value of pulled up resistors for eMMC I/F (Follow Rambi)	R208, R211, R194, R209, R210, R195, R193, R170, and R184
EC-DV-31	23	Co-layout ST and Infineon TPM (Follow Rambi)	R635, R636, and R637
EC-DV-32	28	Move EC_PWROK from PH2 to PJ1, and VOL_UP_BTN_L from PJ1 to PH2 (Follow Rambi)	U19.J4 and U19.B9
EC-DV-33	28	Add test point, TP65~TP67, on unused pins of EC.	TP65, TP66, and TP67
EC-DV-34	17,21	Change R10 and R530 to 2A fuse (0603)	R10 and R530
EC-DV-35	6,7, 28,29	Change structure of Yoga mode connection (two G-sensor) and EC pinout define.	
EC-DV-36	8	Add C383 and C384 for ACLL issue.	C383 and C384
EC-DV-37	22	All Pulled up resistors of eMMC data/cmd to be un-stuffed,and R184 change to 47K ohm as well (Follow Rambi)	R170, R184, R193, R194, R195, R208, R209, R210, and R211
EC-DV-38	5	Swap CLKREQ_WLAN and CLKREQ_IMAGE for CLKREQ and CLK pins are aligned (Follow Rambi)	
EC-DV-39	28	Board ID of proto2 change to 001 (Follow Rambi).	R98 and R95
EC-DV-40	29	Add R639 and R640 for layout problems of length.	R639 and R640
EC-DV-41	35	Change pull up power of PP3300_PCH_PG to PP3300_EC (Follow Rambi).	
EC-DV-42	38	Change pull up power of PP1350_PCH_PG to PP3300_PCH_S5 (Follow Rambi).	
EC-DV-43	39	Change pull up power of PP1000_PCH_PG to PP3300_PCH_S5 (Follow Rambi).	
EC-DV-44	12,13	C329 and C339 change from 0.2pF to 3.3pF for Intel suggestion.	C329 and C339
EC-DV-45	24	Change thermal sensor design for following Rambi.	
EC-DV-46	28	Change connection of LOGO_LED_L from U19.L11 to U19.H11, and Rotate_BTN_L_EC from U19.H11 to U19.N1.	
EC-DV-47	28	Connect SOC_SENS_INT to U19.L10.	
EC-DV-48	22	Remove R167 on eMMC CLK (Follow Rambi).	R167
EC-DV-49	26	Change CML3 and CML4 to DLP11TB800UL2 for Intel suggestion.	CML3 and CML4
EC-DV-50	2	Add decoupling caps (0.1uF), C385~C390, for Intel suggestion.	C385~C390
EC-DV-51	23	Add decoupling caps (0.1uF), EC24~EC27, for EMI suggestion.	EC24~EC27
EC-DV-52	4	Connect RF_LED_ON to U20.D32 (GPIO26) for Google suggestion.	
EC-DV-53	17	Power of touch panel select to PP3300_DSW for Google suggestion.	R303 and R304
EC-DV-54	17	Delete TCH_PNL_ON and add test point (TP71) for Google suggestion.	TP71
EC-DV-55	24	Change Hall sensor IC of U8.	U8
EC-DV-56	38	Un stuff PR54 and stuff PR51 (Follow Rambi)	PR54 and PR51
EC-DV-57	15	Un stuff R290, R297, and R310 for Touch panel detect issue.	R290, R297, and R310

LI□A5B Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-SIT-01	35	PP5000_DSW net rename to PP5000_RTC	
EC-SIT-02	31~40	PP5000 net rename to PP5000_DSW	
EC-SIT-03	35,40	Add PP5000 load switch and discharge schematic	PQ60,PQ66, PR258, PC206~PC208
EC-SIT-04	35,40	Add PP5000_PCH load switch and discharge schematic	PQ61~PQ65, PR248~PR257, PC209~PC213
EC-SIT-05	36,40	Reserved SUSP_VR_EN for PP1800_PCH_S5 power rail EN	PR245, PR246, PR247
EC-SIT-06	40	Change PR114 and PR165 value and footprint	PR114, PR165
EC-SIT-07	30~32,37	Stuff for ESD solution	ER1~ER6,EC5,EC13,EC17,EC20,EC21,EC23
EC-SIT-08	30~32,36	Change 0 ohm to 0603 short pad for cost saving.	PR120,PR38,PR239,PR82
EC-SIT-09	30~37	Change 0 ohm to 0402 short pad for cost saving.	PR14,PR116,PR122,PR176,PR226,PR28,PR34,PR244,PR186,PR210,PR194,PR142,PR91,PR147,PR149,PR65,PR72,PR123,PR9,PR12
EC-SIT-10	23	Change Pin define of CN8.	CN8
EC-SIT-11	24	Change Pin define of CN12.	CN12
EC-SIT-12	17	Change footprint and Quanta PN of CN9.	CN9
EC-SIT-13	28	Change footprint and Quanta PN of L1.	L1
EC-SIT-14	27	Change L4 from 0 ohm to 2A fuse.	L4
EC-SIT-15	7	Add RAM_ID3 on GPIO_S5_40 (U20.J3).	R646 and R647
EC-SIT-16	7	Modify RAM ID table.	
EC-SIT-17	20	Change HDMI power from PP5000 to PP5000_PCH.	
EC-SIT-18	25	Change Audio 5V power from PP5000 to PP5000_PCH.	
EC-SIT-19	17	Change RF LED power from PP5000 to PP5000_PCH.	
EC-SIT-20	22	Stuff R170, R184, R193, R194, R195, R208, R209, R210, and R211 for eMMC debug.	R170, R184, R193, R194, R195, R208, R209, R210, and R211
EC-SIT-21	1~29	Update function code.	
EC-SIT-22	23,28	Swap Net of Volume UP and Volume DOWN.	
EC-SIT-23	17,23	Reserve RV11, RV12, and EC29~EC39 for ESD and EMI suggestion.	RV11, RV12, and EC29~EC39
EC-SIT-24	26	R448 change from 25.5K ohm to 20K ohm because of changing charge current.	R448
EC-SIT-25	14	Un-staff Q49~Q52, R547~R550, R531, and R533~R535 because Google does not support them.	Q49~Q52, R547~R550, R531, and R533~R535
EC-SIT-26	14	Un-staff U27, R601, R602, and R511 for leakage issue.	U27, R601, R602, and R511
EC-SIT-27	16	Reserve SC25~SC30 for ESD suggestion.	SC25~SC30
EC-SIT-28	17	Stuff R304, and un-stuff R303 for changing power of Touch panel from S5 to S0.	R303 and R304
EC-SIT-29	24	Change FANSIG_R and FAN_ID pull high power rail from PP3300_DX to PP3300_DSW, because Fan power rail is PP5000.	
EC-SIT-30	20	Un-stuff D5 and D6, and add R648 and R649 for cost saving.	D5, D6, R648 and R649
EC-SIT-31	17	Reserve R650 because Touch control board will change design.	R650

LI□A5B Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-SIT-32	15	Delete Q14, and add Q68 and Q69 for leakage current issue.	Q14, Q68, and Q69
EC-SIT-33	15	Add R651 and D15 for leakage current issue.	R651 and D15
EC-SIT-34	15	Q38 change to U42 for leakage current issue.	Q38 and U42
EC-SIT-35	17	Change Touch panel power rail to S3 state.	U43, C392, R653, R303, R304, and C194
EC-SIT-36	4,17,21	Change RF LED design from SOC GPIO to WLAN module.	
EC-SIT-37	24	Change Fan power rail from S3 state to S0 state.	
EC-SIT-38	23	Un-stuff R485 for leakage current issue (follow Rambi).	R485
EC-SIT-39		R115,R122,R123,R126,R13,R132,R137,R140,R157,R159,R169,R189,R190,R191,R196,R197,R198,R199,R200,R201,R207,R212,R294,R314,R325,R326,R333,R334,R335,R338,R339,R340,R35,R36,R370,R372,R373,R384,R4,R404,R41,R413,R48,R482,R513,R53,R56,R560,R562,R57,R584,R63,R66,R74,R80,R138,R152,R292,R309,R34,R354,R40,R455,R470,R474,R555,R575,R144,R153,R307 change from 0 ohm to short pad.	
EC-SIT-40	24	Un-stuff U8, C391, C190, and R288 because LID2 is not necessary.	U8, C391, C190, and R288
EC-SIT-41	35,38,40	Un-stuff PR257, PR231, PR219, and PR55 because EC side has pull-down resisters.	PR257, PR231, PR219, and PR55
EC-SIT-42	28	Un-stuff SW5 because power button is on MB.	SW5
EC-SIT-43	5	Reserve C393 for EMC suggestion.	C393
EC-SIT-44	16	Change R189, R199, R200, R190, R191, and R197 from short pad to 22 ohm bead for EMC suggestion.	R189, R199, R200, R190, R191, and R197
EC-SIT-45	20,23,27	Stuff R296, R302, R308, R315, RV5, RV6, RV3, RV7, RV8, and RV9 for EMC suggestion.	R296, R302, R308, and R315
EC-SIT-46	17,18	Add PAD1, PAD2, and PAD3, and let CN9.45 float.	
EC-SIT-47	7	Modify RAM ID table, add three config.	
EC-SIT-48	17,23	Change R305 and R259 to 1k ohm for meeting spec.	R305 and R259
EC-SIT-49	38	Un-stuff PC64 for power up sequence time.	PC64
EC-SIT-50	06	Change C231 and C232 from 15 pF to 8.2 pF for Xtal vendor suggestion.	C231 and C232
EC-SIT-51	28	Change C258 and C270 from 18 pF to 12 pF for Xtal vendor suggestion.	C258 and C270
EC-SIT-52	30	Stuff PC66 and PC67 for EMC suggestion.	PC66 and PC67
EC-SIT-53	16	R197 change from 75 ohm to 0 ohm and un-stuff SC27 because SD card signal EA has not been tested.	R197 and SC27
EC-SIT-54	6,23,28	Un-stuff SW1, R203, RV3, R357, R517, and R518 because of function dropping.	SW1, R203, RV3, R357, R517, and R518

LI□A5B Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-SVT-01	11	Un-stuff R47 for leakage current issue.	R47
EC-SVT-02	17	Reserve R660 and R661 for following Rambi design.	R660 and R661
EC-SVT-03	4,17	Reserve R493, Q37, and R662 for RF LED controlling by SOC GPIO.	R493, Q37, and R662
EC-SVT-04	23	Change R259 to 1.5k ohm for meeting spec.	R259
EC-SVT-05	16	Reserve R663 for EMC suggestion.	R663
EC-SVT-06	15	Delete U42 and Q34, and add U44, C394, R664, Q72, and R665 for following Rambi to solve leakage current issue.	U42, U44, R665, C394, Q72, and R664
EC-SVT-07	17	Reserve R666 for following Rambi design (reserve TOUCH_RST_L as LDO enable pin).	R666
EC-SVT-08	31~34	Change current sense resistor to short pad for cost saving.	PJP8, PJP11, PJP16, PJP13, PJP17
EC-SVT-09	31~34	Un-stuff current sense IC and capacitor for cost saving.	PU11, PU22, PU20, PU23, PU21, PC196~PC201, PC204 and PC205
EC-SVT-10	17	Delete R653, R666, R654, and R27, and add C398 for changing touch panel power control pin.	C398, R653, R666, R654, and R27
EC-SVT-11	17	Change R309 to 0402 package and add R672 for DMIC noise issue.	R309 and R672
EC-SVT-12	6,7,17, 28,29	Add D23, U45, C395 ,C397, C396, R670, R671, R669 and delete R626, R627, R616, R618, R619, R620, R621, R622, R639, R640, R320, R625, R316, and R638 for changing G-sensor connection.	D23, U45, C395 ,C397, C396, R670, R671, R669, R626, R627, R616, R618, R619, R620, R621, R622, R639, R640, R320, R625, R316, and R638
EC-SVT-13	7	Reserve R673 for following Rambi design.	R673
EC-SVT-14	17,23	Change R305, R259, and R234 to connect to PP5000_DSW for supporting in S5 state.	R305, R259, and R234
EC-SVT-15	21	Add U41.21, U41.22, U41.23, U41.24, and U41.25 and connect to GND for IC design.	U41.21, U41.22, U41.23, and U41.24
EC-SVT-16		Change L7,R671,R615,R617,R415,R453,R472,R498,R352,R146,R293,R567,R527,R198,R294,R662, R659,R623,R624,R642,R643,R641,R644,R139,R563,R569,R161,R163,R648,R649,PR56,PR201, PR181,PR127,PR29,R91,R44,R45,R68,R319,PR57,R110,R111,R116,R119,R121,R130,R147,R381, R514,PR13,R516 to shortpad, and delete CML6 to shortpad, and delete CML6 for cost saving.	
EC-SVT-17		Un -stuff R493,Q7,Q68,Q69,Q39,R515,R460,Q10,R311,R306,R6,R26,C398,R18,U43,C392,R303, C194,Q37,R364,C230,C233,R443,R435,C234,C239,C246,C245,C222,C244,L6,L5,C223,C219, D11,R434,C248,C247,R363,R328,R329,R386,R411,C214,U14,D23,U45,C395,C396,R670,R669, Q35,R454, and R496 for non-touch sku.	
EC-SVT-18	1	Update Block Diagram.	
EC-SVT-19	21	Remove R610,R611,R612,R613,R614,C380,C379,C378,C377,R609,TP64,U41, C382,R608,C375,C376,and C381 for battery life issue.	R610,R611,R612,R613,R614,C380,C379,C378,C377,R609,TP64,U41, C382,R608,C375,C376,and C381
EC-SVT-20	29	Change R670 from 0 ohm to 2A fuse for Lenovo suggestion.	R670

