1. Schematic Page Description :

ZRU/Vichy Schematic Ver : 1.0

I2C table

Function	Channel	Read	Write
Touch pad	I2C0	0x67	
Audio codec	I2C1	0x21	0x20
Light sensor	I2C4		

SMBus table

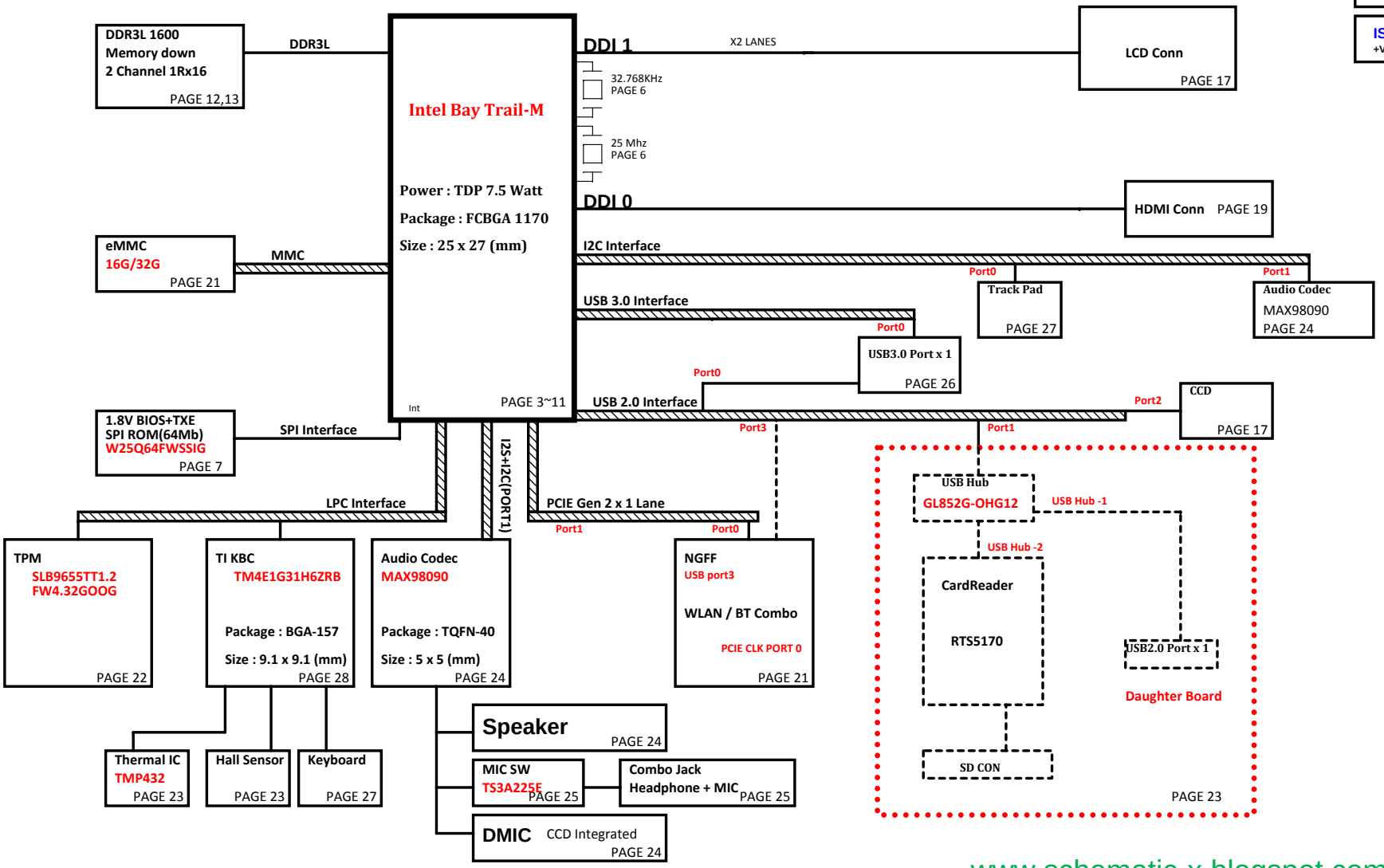
Function	Channel	Address
Battery	SMB0	
Thermal	SMB2	0x4C

Function	Channel
PP3300_DSW	0x42
PP5000	0x41
PP1350	0x49
PP1050_PCH	0x43
PP1000_PCH	0x47

ZRU/Vichy
Intel Bay Trail-M Platform Block Diagram

SKUA DC N2830
AJSR1W4UT02 --CPU(1170P)N2830 2.16G SR1W4(FCBGA)STNBSQ

BQ24717RGRR Batery Charger	TPS51216 PP1350
TPS51225 PP3300_DSW/PP5000	NB671GQ-Z PP1000_PCH
ISL95833HRTZ-T +VCC_CORE/+VCC_GFX	Thermal Protection Discharger

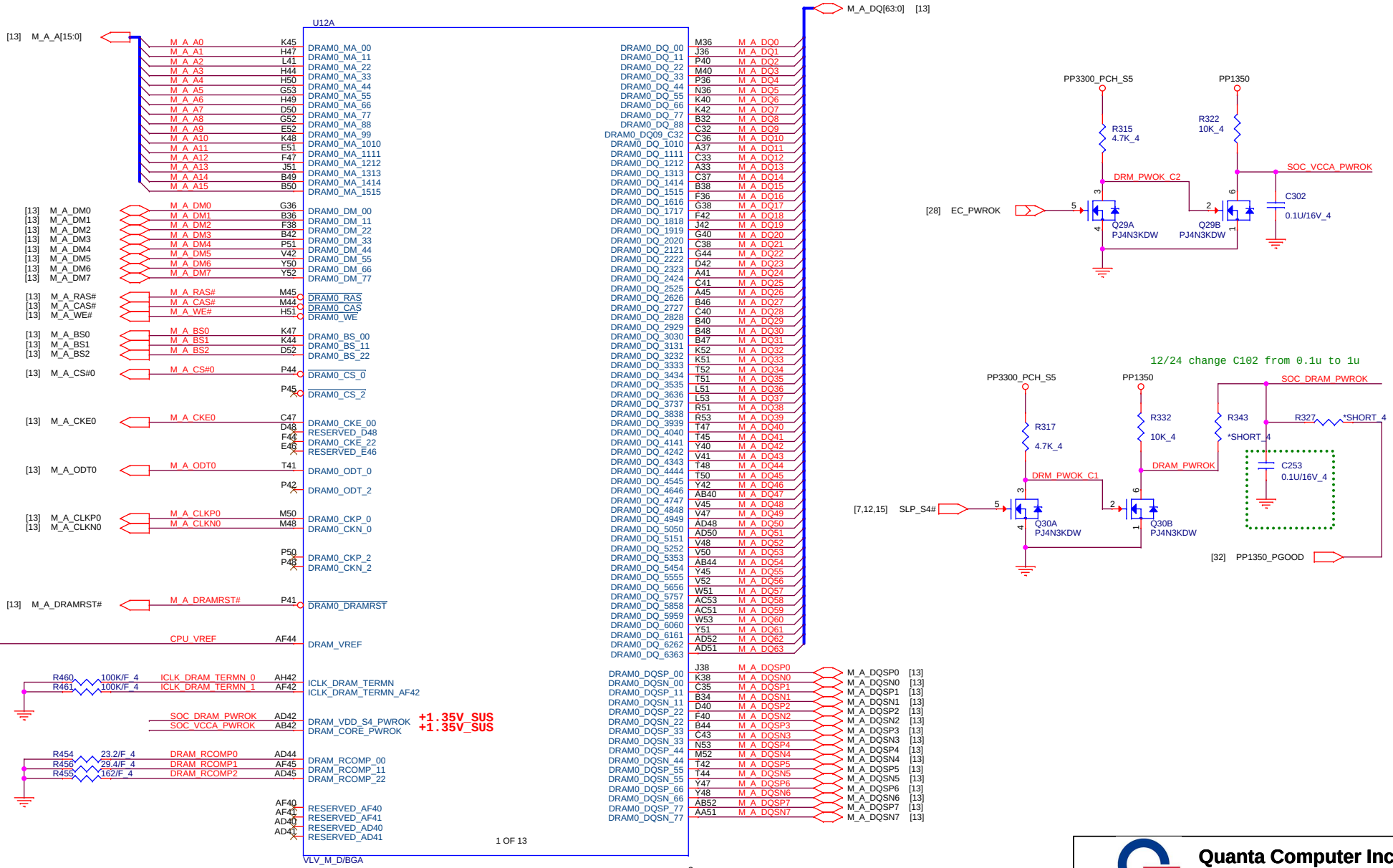


BOM value option:
SX@ => SOiX
NSX@=>none SOiX
HUB@=>USB HUB
3G@ => LTE
GD@ =>Google debug

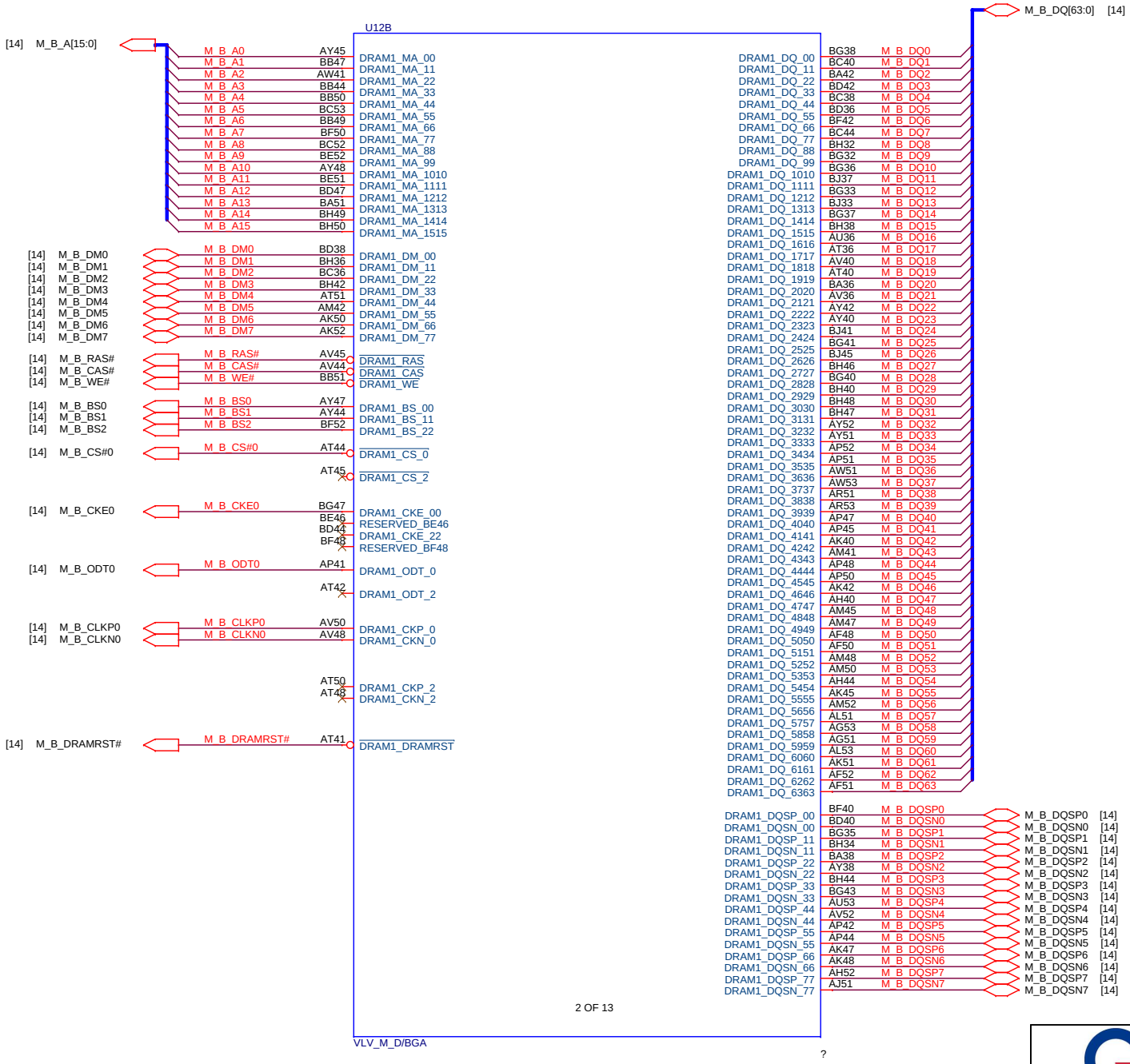
Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	Block Diagram	1A

Date: Tuesday, March 31, 2015 Sheet 2 of 41



Quanta Computer Inc.			
PROJECT : ZRU			
Size	Document Number		Rev
	Valley 1/9 (DDRA)		1A
Date: Tuesday, March 31, 2015		Sheet 3 of 41	



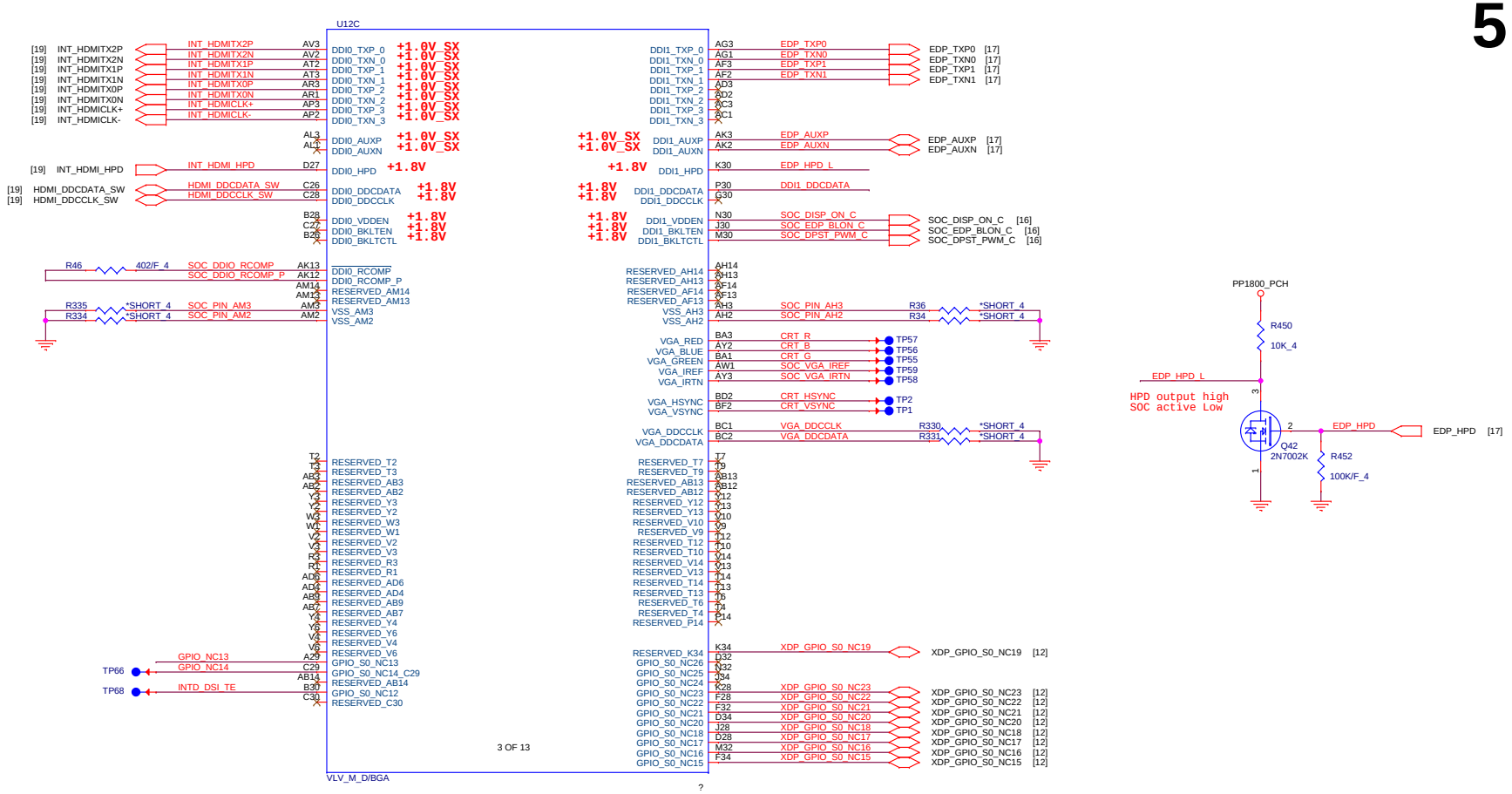
4

Quanta Computer Inc.

PROJECT : ZRU

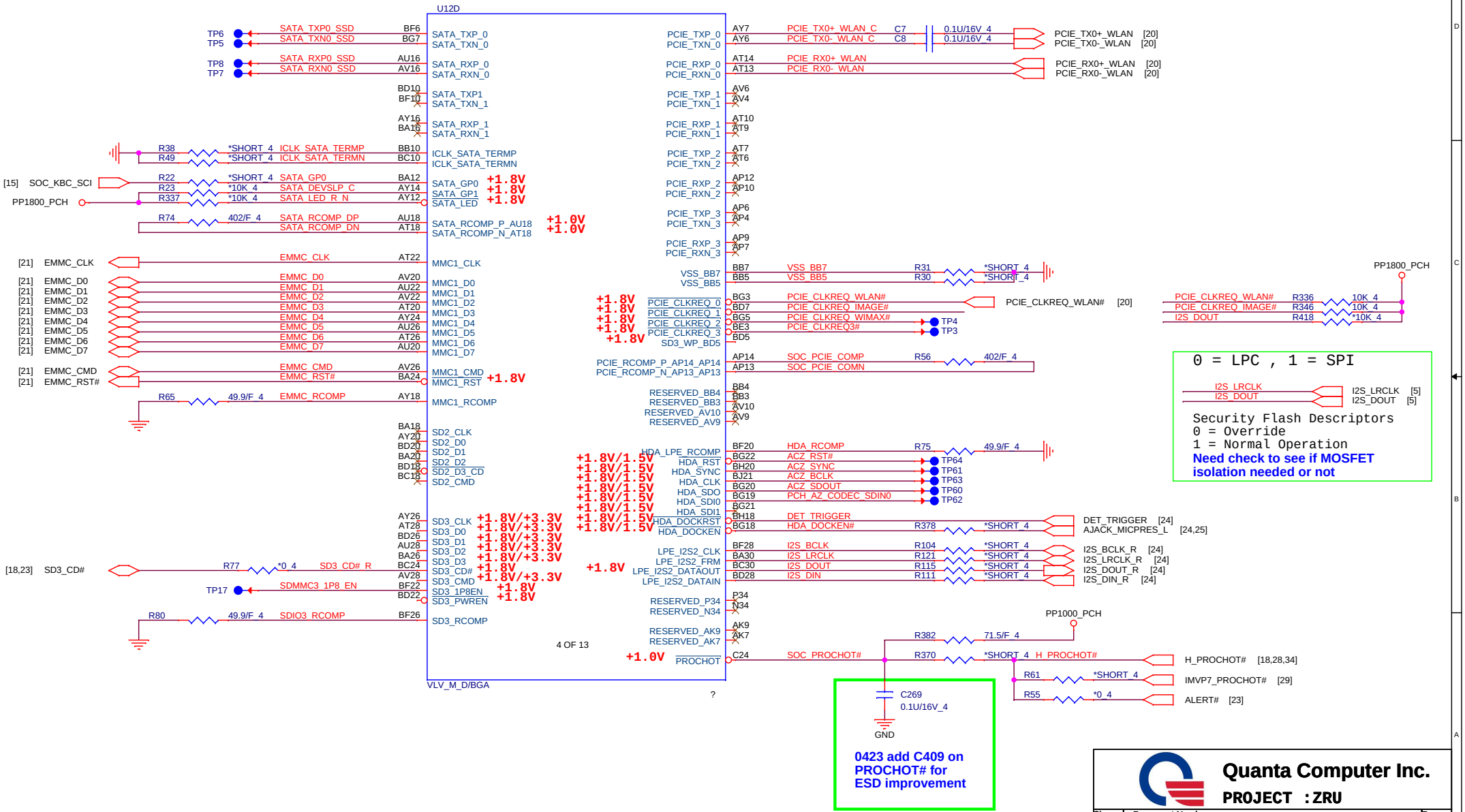
Size	Document Number	Rev
	Valley 2/9 (DDRB)	1A

Date: Tuesday, March 31, 2015 Sheet 4 of 41



BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged **1 = Top address bit is inverted**	using SoC internal PU
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC **1 = SPI**	using SoC internal PU
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override **1 = Normal operation**	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	Pull up +1.8V at HDMI side
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	using SoC internal PU
GPIO_SO_NC_13				

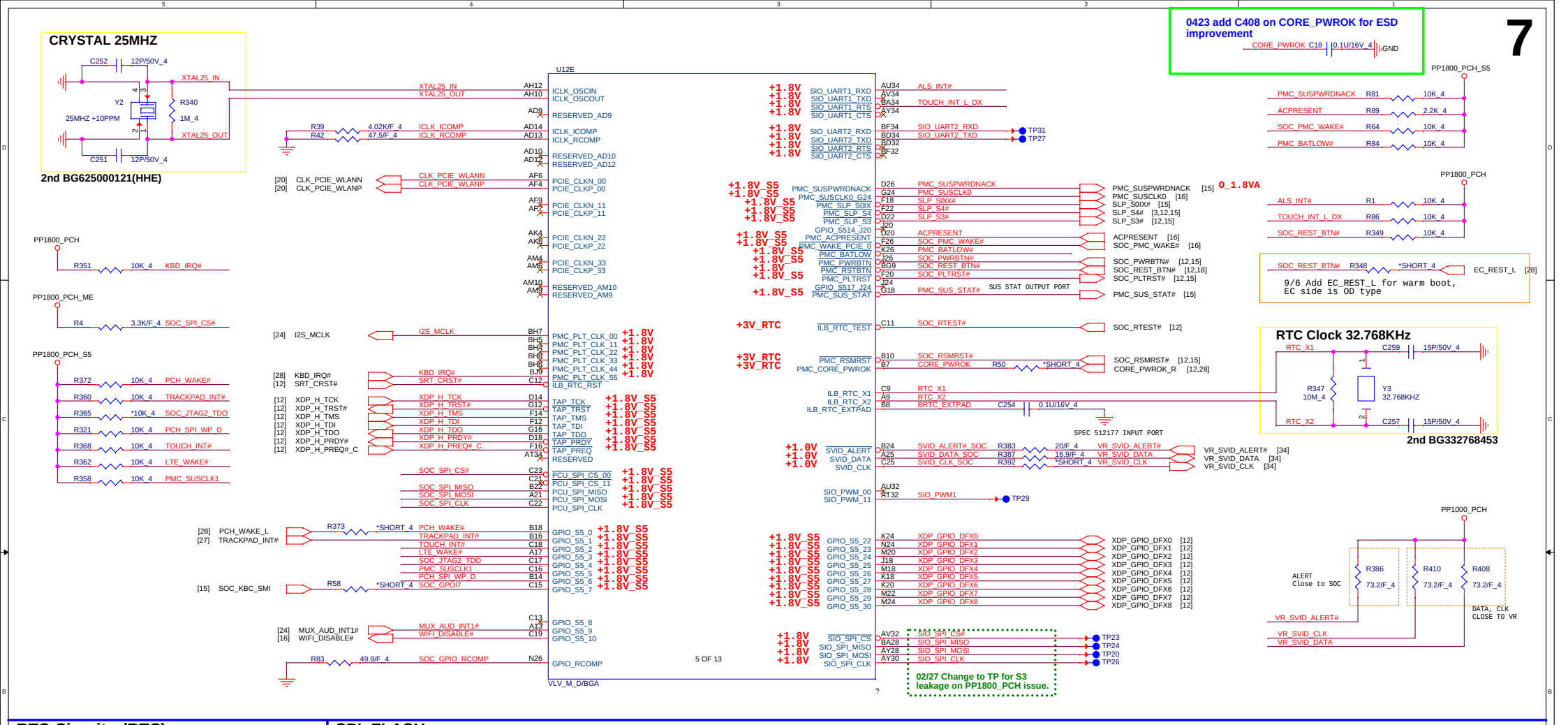


Quanta Computer Inc.

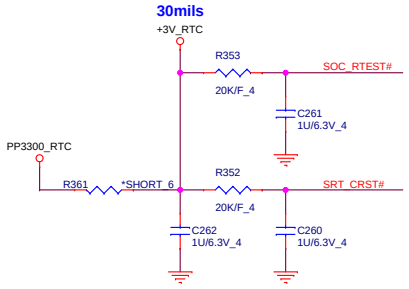
PROJECT : ZRU

Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	1A

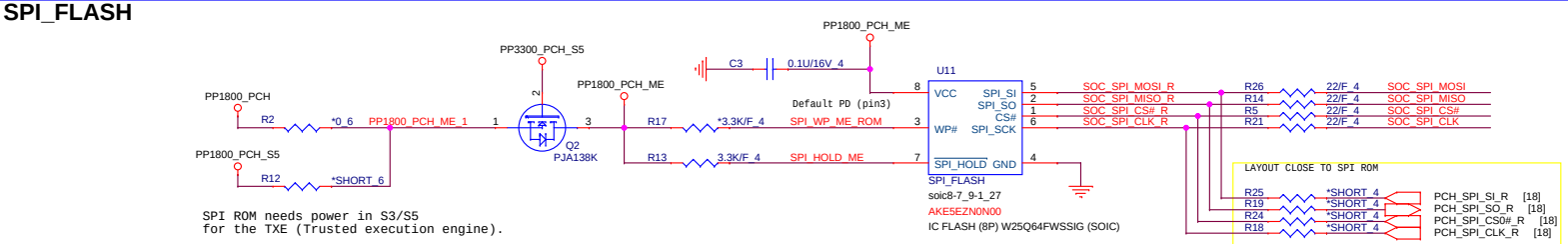
Date: Tuesday, March 31, 2015 Sheet 6 of 41

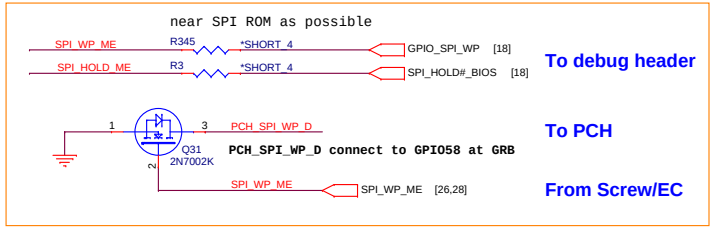


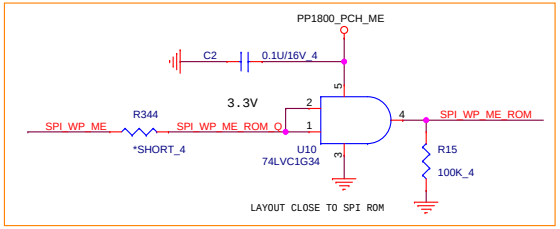
RTC Circuitry(RTC)



SPI_FLASH







Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	Valley 5/9 (SPI/GPIO/CLK)	1A
Date: Tuesday, March 31, 2015	Sheet 7 of 41	

Stage	Vender	RAM_ID 3210	Q P/N	Mfr. PN	Freq.	Size	Pice
C-2	Samsang	0x0000	AKD5PGST514	K4B4G1646Q-HYK0	1600MHz	2GB	4
A-1	Hynix	0x0001	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz	4GB	8
	Hynix	0x0010	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz	2GB	4
	Samsang	0x0011	AKD5PGST514	K4B4G1646Q-HYK0	1600MHz	4GB	8
C-1	Hynix	0x0100	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	2GB	4
	Hynix	0x0101	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	4GB	8

02/14 Change RMID to 001.

RAM ID

PP1800_PCH_S5

R323 *1K_4 RAM_ID0 R319 1K_4
R324 1K_4 RAM_ID1 R320 *1K_4
R329 *1K_4 RAM_ID2 R318 1K_4
R341 *1K_4 RAM_ID3 R328 *1K_4

02/27 Reserve RAM_ID3 for memory BOM option.

PP1800_PCH_S5
R342 10K_4 LTE_DISABLE#

U12F

LTE_DISABLE#
RAM_ID0
RAM_ID1
RAM_ID2
RAM_ID3

GPIO_S5_31
GPIO_S5_32
GPIO_S5_33
GPIO_S5_34
GPIO_S5_35
GPIO_S5_36
GPIO_S5_37
GPIO_S5_38
GPIO_S5_39
GPIO_S5_40
GPIO_S5_41
GPIO_S5_42
GPIO_S5_43

RESERVED_M10
RESERVED_M9
RESERVED_P7
RESERVED_P6
RESERVED_M7
USB3_REXT0
RESERVED_P10
RESERVED_P12
RESERVED_M4
RESERVED_M6

USB3_REXT0 R43 1.24K/F_4

USB3_RXP0 USB3_RXP0 USB3_RXP0 [26]
USB3_RXN0 USB3_RXN0 USB3_RXN0 [26]
USB3_TXP0 USB3_TXP0 USB3_TXP0 [26]
USB3_TXN0 USB3_TXN0 USB3_TXN0 [26]

PORT 1 USB CONN
PORT 2 Cardreader
PORT 3 NA
PORT 4 NA

MB USB3.0
HUB1
CCD
BT

[26] USBP0+ [26] USBP0- USB_DP0 USB_DN0
[23] USBP1+ [23] USBP1- USB_DP1 USB_DN1
[17] USBP2+ [17] USBP2- USB_DP2 USB_DN2
[20] USBP3+ [20] USBP3- USB_DP3 USB_DN3

R53 1K/F_4 ICLK_USB_TERMN_0
R59 1K/F_4 ICLK_USB_TERMN_1
ICLK_USB_TERMN_D10
ICLK_USB_TERMN

RESERVED_H8
RESERVED_H7
RESERVED_H5
RESERVED_H4

R62 SOC_UART_TX SOC_UART_RX *0_4
Un-Stuff for Test Only

[15,26] USB_OC0#
PP1800_PCH_S5
[15,23] USB_OC1#
R379 10K_4 USB_OC0#
R339 10K_4 USB_OC1#
USB_OC_00
USB_OC_11
+1.8V_S5
+1.8V_S5

R41 45.3/F_4 USB_RCOMP
USB_RCOMPO
USB_RCOMPI

R47 *0_4 USB_PLL_MON
USB_PLL_MON

USB_HSIC0_DATA
USB_HSIC0_STROBE
USB_HSIC1_DATA
USB_HSIC1_STROBE

R338 45.3/F_4 USB_HSIC_RCOMP
R67 49.9/F_4 LPC_RCOMP
USB_HSIC_RCOMP

GPIO_S0_SC_55
GPIO_S0_SC_56
GPIO_S0_SC_57
GPIO_S0_SC_58
GPIO_S0_SC_59
GPIO_S0_SC_60
GPIO_S0_SC_61
+1.8V

TRACKPAD_INT_DX
GPIO_S0_SC_56
SOC_UART_TX
SIM_DET_C
EC_IN_RW_C
SOC_UART_RX

TRACKPAD_INT_DX [27]
GPIO_S0_SC_56 [5]
SOC_UART_TX [18]
EC_IN_RW_C [16]
SOC_UART_RX [18]

PP1800_PCH
TRACKPAD_INT_DX R60 10K_4
SIM_DET_C R63 10K_4

ILB_8254_SPKR

PP1800_PCH
I2C_0_SDA_R R389 4.7K_4
I2C_0_SCL_R R394 4.7K_4
I2C_1_SDA_R R401 4.7K_4
I2C_1_SCL_R R406 4.7K_4

SIO_I2C0_DATA
SIO_I2C0_CLK
I2C_0_SDA_C R388 22/F_4
I2C_0_SCL_C R393 22/F_4
I2C_0_SDA_R [16]
I2C_0_SCL_R [16]
Touch pad

SIO_I2C1_DATA
SIO_I2C1_CLK
I2C_1_SDA_C R400 22/F_4
I2C_1_SCL_C R405 22/F_4
I2C_1_SDA_R [24]
I2C_1_SCL_R [24]
Audio Codec

SIO_I2C2_DATA
SIO_I2C2_CLK
SIO_I2C3_DATA
SIO_I2C3_CLK
SIO_I2C4_DATA
SIO_I2C4_CLK
SIO_I2C5_DATA
SIO_I2C5_CLK
SIO_I2C6_DATA
SIO_I2C6_CLK

[22] PCLK_TPM
R366 *0_4
[28] CLK_PCI_EC
[28] LPC_CLKRUN_L
R367 *SHORT_4 CLK_PCI_EC_R
LPC_CLKRUN_L R377 *SHORT_4 SOC_CLKRUN#

[22,28] LPC_LAD0
[22,28] LPC_LAD1
[22,28] LPC_LAD2
[22,28] LPC_LAD3
[22,28] LPC_LFRAME#
R364 22/F_4 SOC_CLKOUT_0
R359 22/F_4 SOC_CLKOUT_1
SOC_SERIRQ
[15] SOC_SERIRQ

LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME#
LPC_RCOMP
ILB_LPC_AD_00
ILB_LPC_AD_11
ILB_LPC_AD_22
ILB_LPC_AD_33
ILB_LPC_FRAME
ILB_LPC_CLK_00
ILB_LPC_CLK_11
ILB_LPC_CLKRUN
ILB_LPC_SERIRQ
+1.8V/+3.3V
+1.8V

PP1800_PCH
R356 2.2K_4 SMB_SOC_DATA
R355 2.2K_4 SMB_SOC_CLK
R350 2.2K_4 SMB_SOC_ALERTB

[12] SMB_SOC_DATA
[12] SMB_SOC_CLK
SMB_SOC_DATA
SMB_SOC_CLK
SMB_SOC_ALERTB
PCU_SMB_DATA
PCU_SMB_CLK
PCU_SMB_ALERT
+1.8V

0424 reserve R483 for CLKRUN# disable

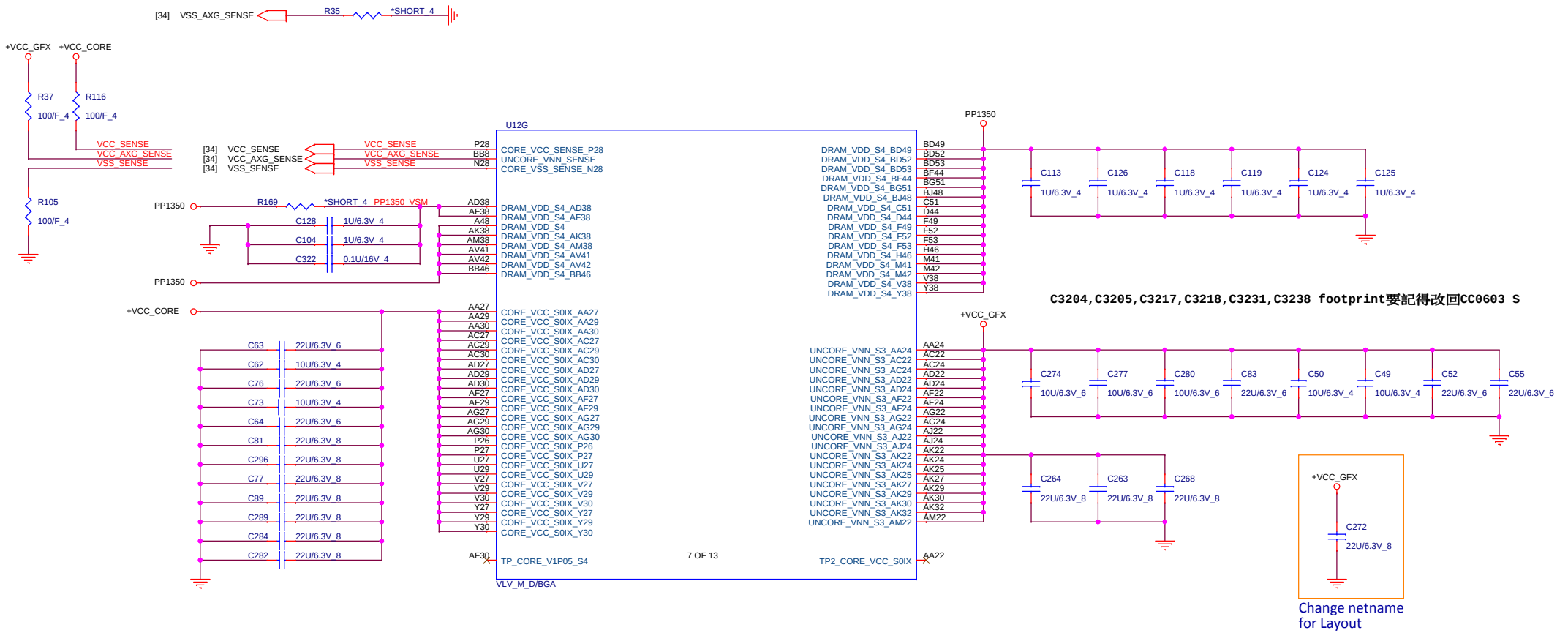
GND R369 *0_4 SOC_CLKRUN#

6 OF 13

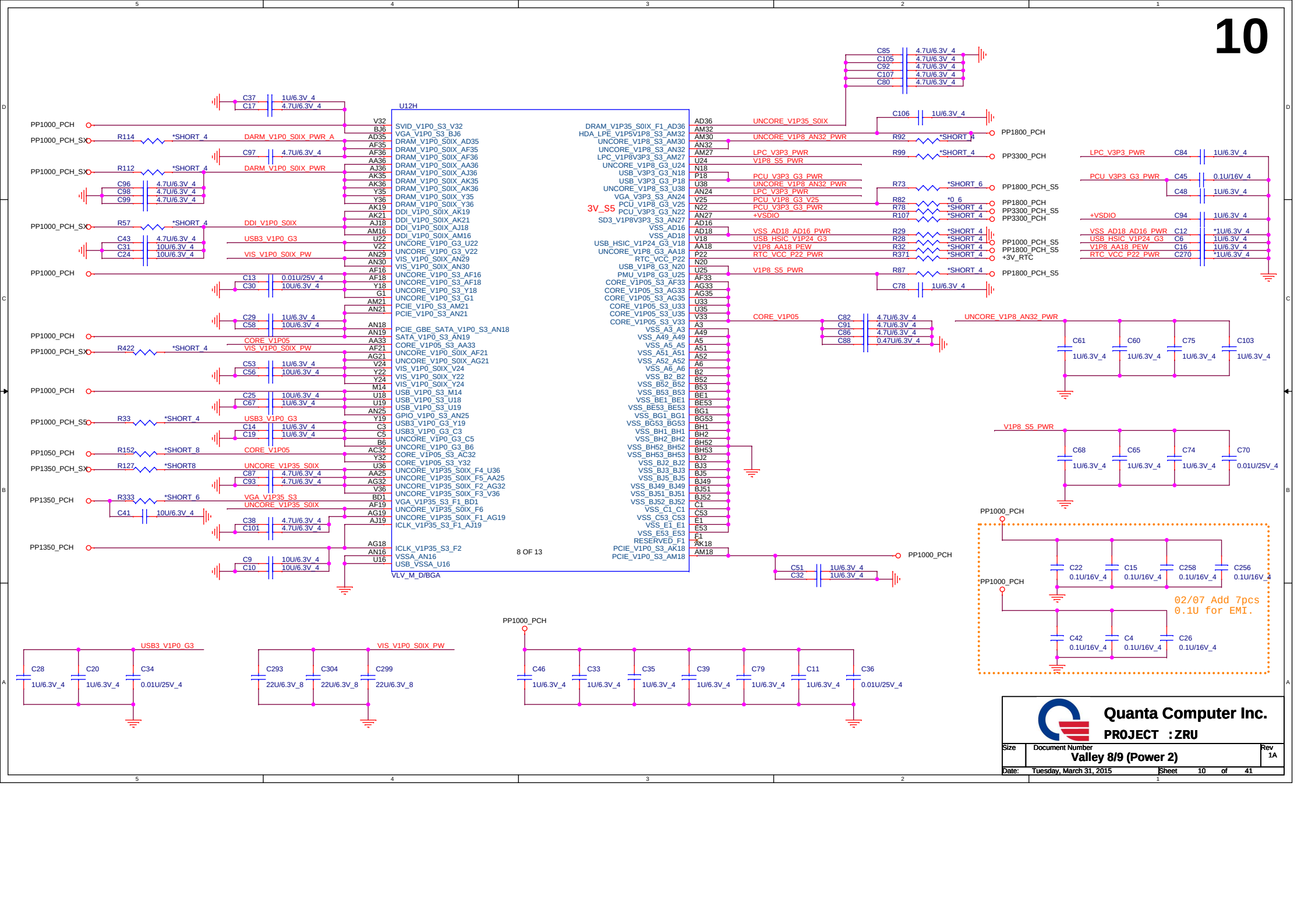
VLV_M_D/BGA

1031 for layout suggestion by intel,
VSS_AXG_SENSE didn't connect to VSS_SENSE,
will connect the GND via near VCC_AXG_SENSE

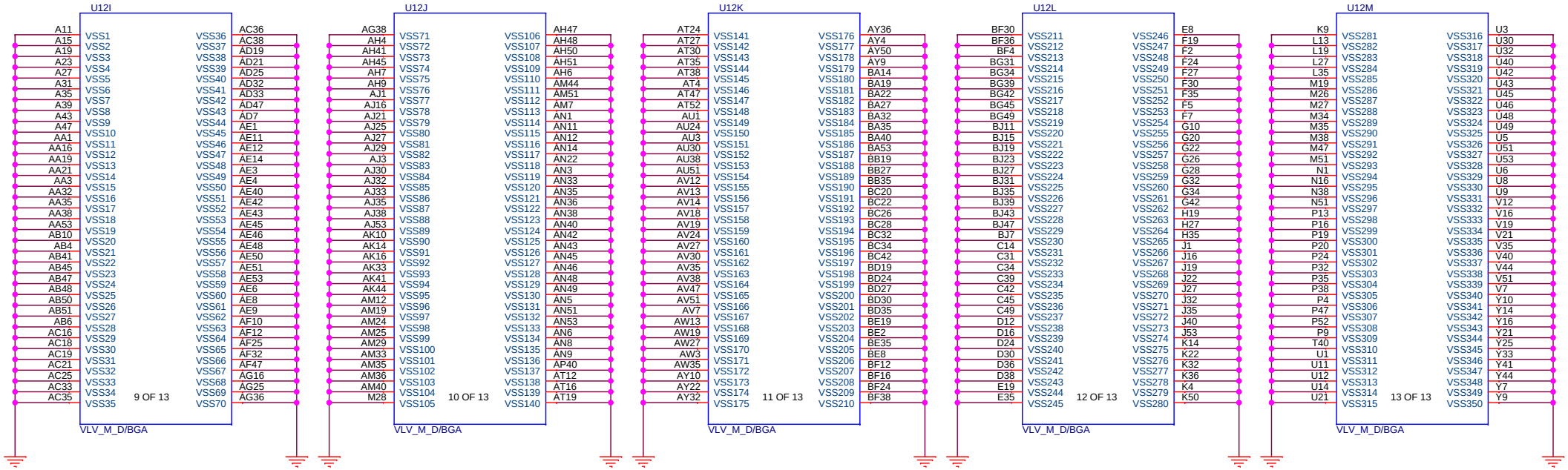
1031 for layout, add 0hm between
GND and VSS_AXG_SENSE



Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: Valley 7/9 (Power 1)	Rev: 1A
Date: Tuesday, March 31, 2015	Sheet 9 of 41	



Quanta Computer Inc.			
PROJECT : ZRU			
Size	Document Number		Rev
	Valley 8/9 (Power 2)		1A
Date: Tuesday, March 31, 2015	Sheet 10 of 41		



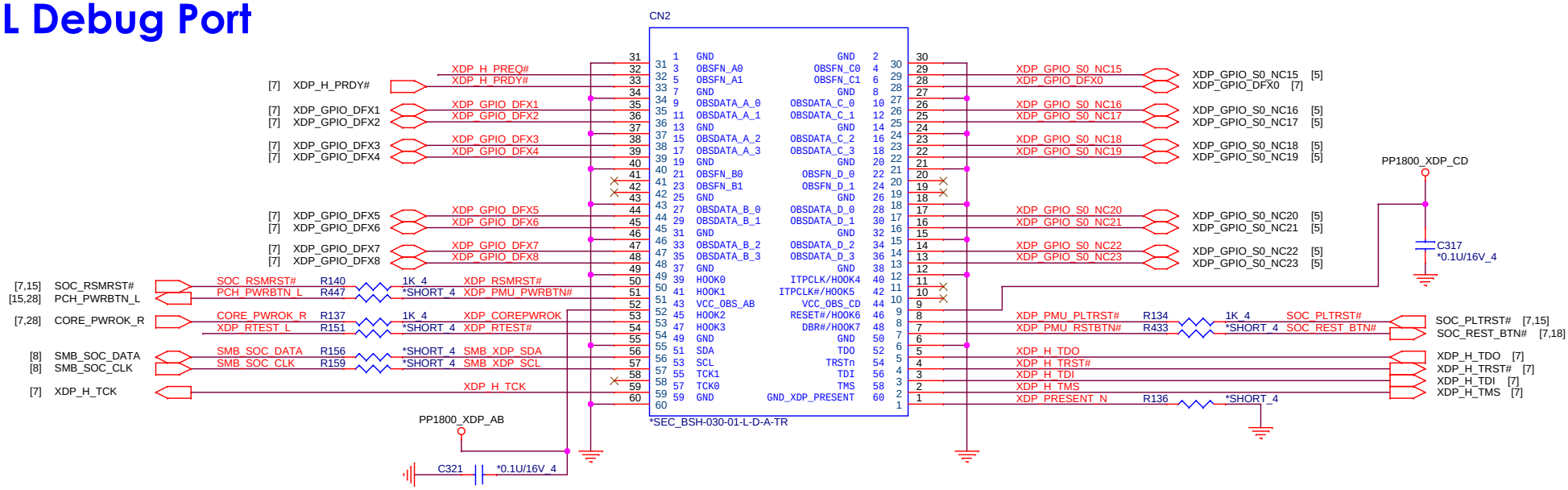
Quanta Computer Inc.

PROJECT : ZRU

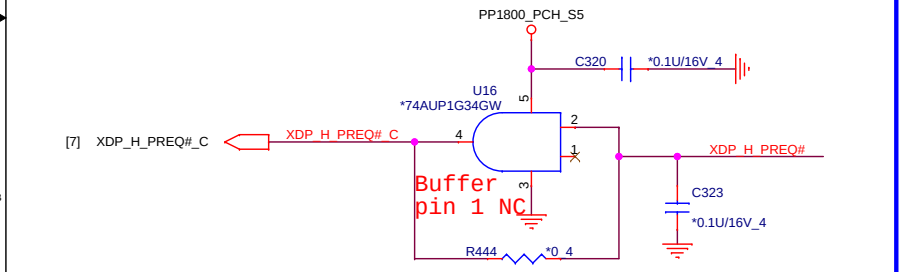
Size	Document Number	Rev
	Valley 9/9 (GND)	1A
Date: Tuesday, March 31, 2015	Sheet 11 of 41	

INTEL Debug Port

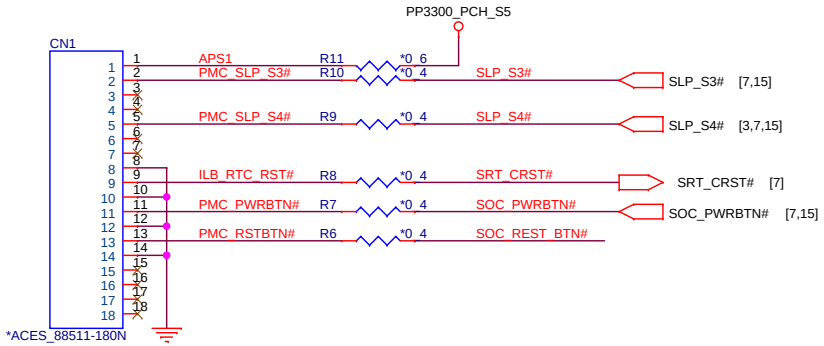
12



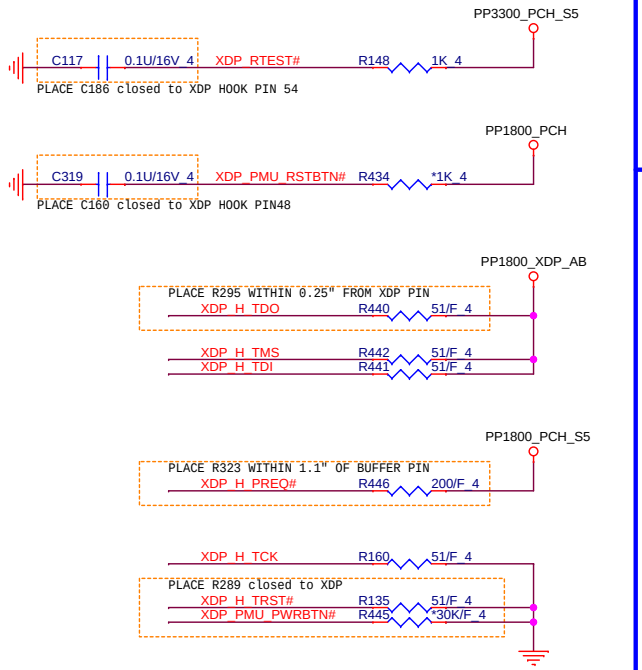
XDP



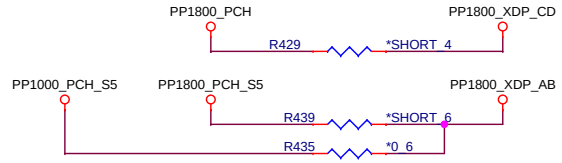
APS



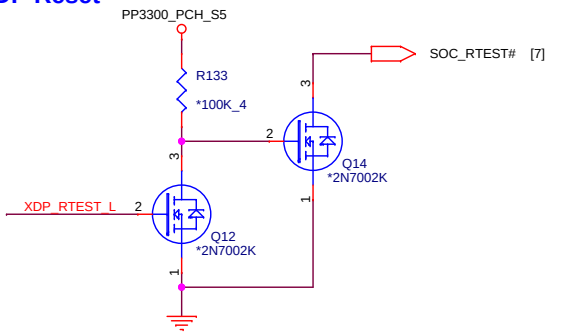
XDP



INTEL Debug Port Power



XDP Reset



Quanta Computer Inc.

PROJECT : ZRU

Size	Document Number	Rev
	CPU XDP / APS	1A

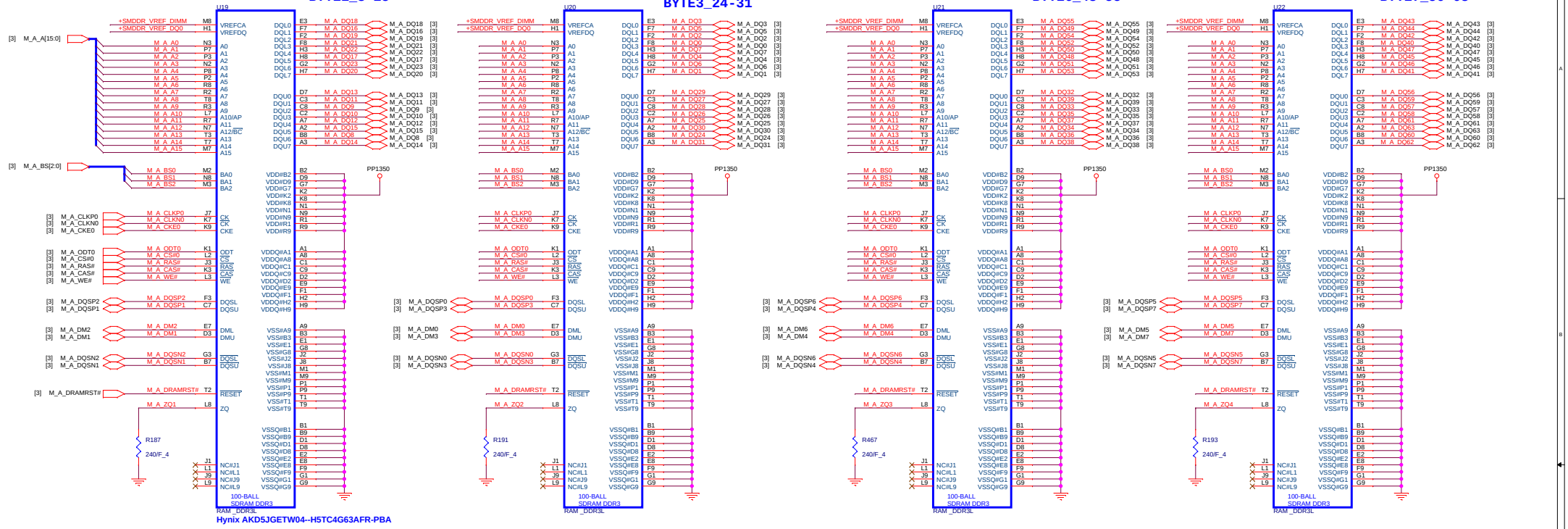
Date: Tuesday, March 31, 2015 Sheet 12 of 41

BYTE2_16-23
BYTE1_8-15

BYTE0_0-7
BYTE3_24-31

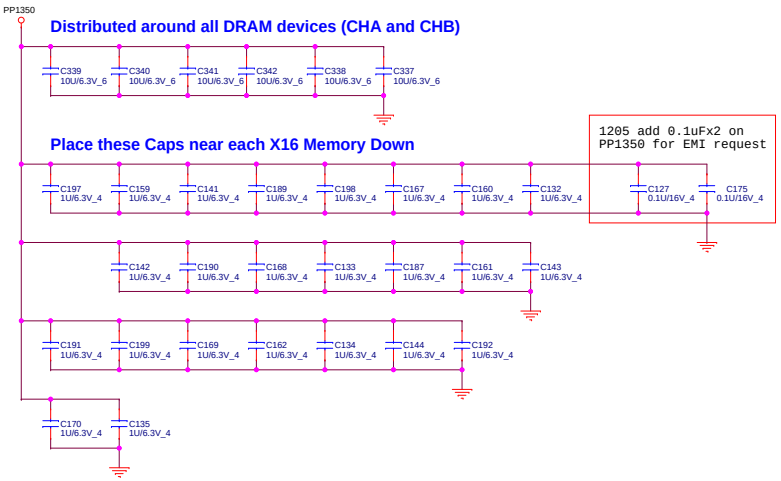
BYTE4_32-39
BYTE6_48-55

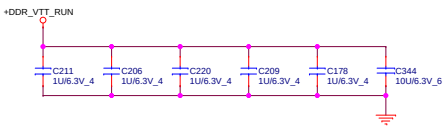
BYTE5_40-47
BYTE7_56-63

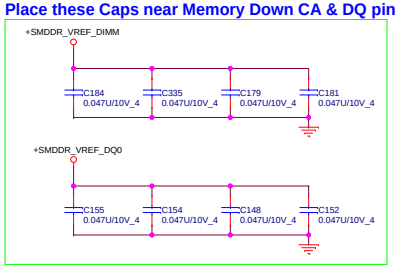


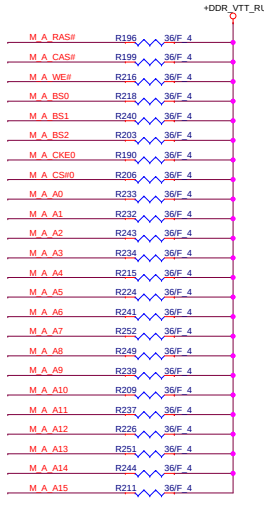
Hynix AKD5JGETW04--H5TC4G63AFR-PBA

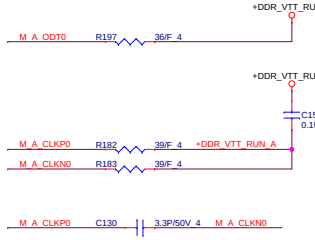
Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

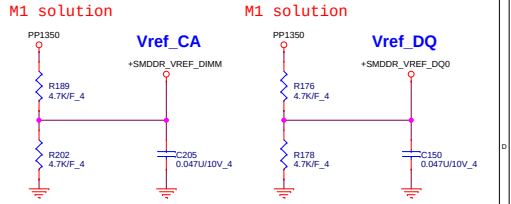












Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 A	1A

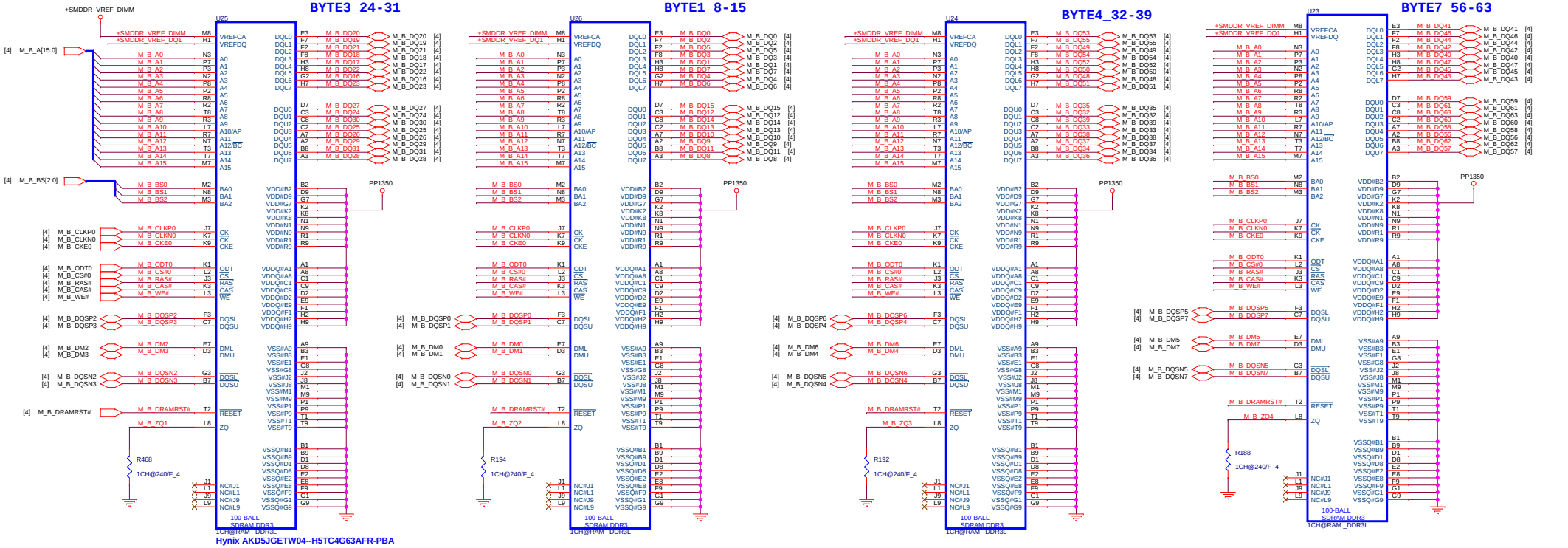
Date: Tuesday, March 31, 2015 Sheet 13 of 41

BYTE2_16-23
BYTE3_24-31

BYTE0_0-7
BYTE1_8-15

BYTE6_48-55
BYTE4_32-39

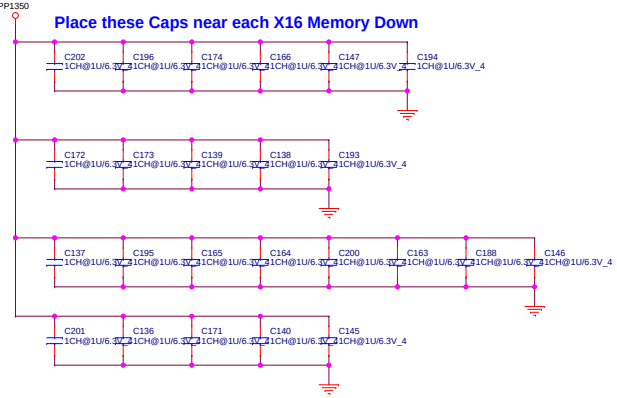
BYTE5_40-47
BYTE7_56-63

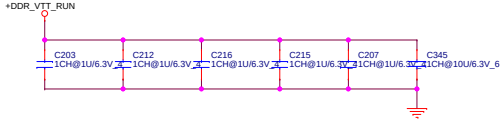


Hynix AKD5JGETW04--H5TC4G63AFR-PBA

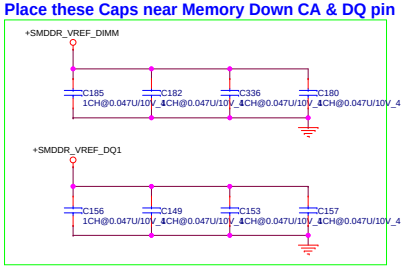
Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1333Mhz 4Gb

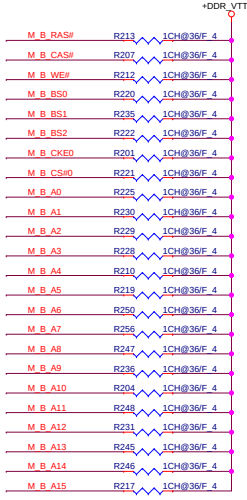
Place these Caps near each X16 Memory Down

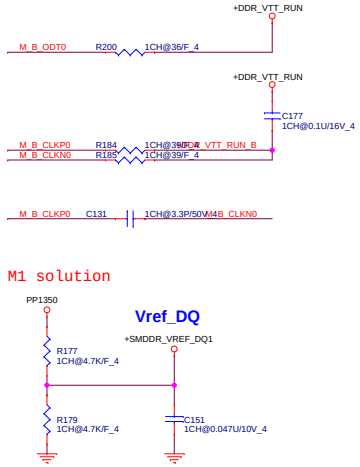




Place these Caps near Memory Down CA & DQ pin







Quanta Computer Inc. PROJECT : ZRU			
Size	Document Number	DDR3L MEMORY DOWNx16 CH-B	Rev 1A
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PWRON SEQUENCE

unstuff U20/R391/R592/R156 @3/18

PP1800_PCH_S5 — R416 *0_4 — U14 VCCA / VCCB — R437 *0_4 — PP3300_PCH_S5

[8] SOC_SERIRQ — SOC_SERIRQ — A / B — IRQ_SERIRQ — IRQ_SERIRQ [22,28]

GND / OE — SWITCH_EN — R438 *10K_4 — PP1800_PCH_S5

*G2129TL1U

PP1800_PCH — R421 10K_4 — R417 0_4 — EC_SCI_L [28]

[6] SOC_KBC_SCI

U13 Y1 A1 VCC GND Y2 A2 — PP3300_EC

[7] SOC_KBC_SMI

PP1800_PCH_S5 — R428 10K_4 — R427 0_4 — EC_SMI_L [28]

*74LVC2G07GW

PP1800_PCH_S5 — R399 *10K_4 — PP3300_EC

[7] PMC_SUS_STAT# — PMC_SUS_STAT# — Q38 *PJA138K — PCH_SUS_STAT_L — PCH_SUS_STAT_L [28]

PP1800_PCH_S5 — R311 10K_4

[7,12] SOC_PWRBTN# — SOC_PWRBTN# — Q26 PJA138K — R308 *30K/F_4 — PP3300_PCH_S5 — PCH_PWRBTN_L [12,28]

PP1800_PCH_S5

[7,12] SOC_RSMRST# — SOC_RSMRST# — R96 *SHORT_4 — PCH_RSMRST_L [28]

R91 100K/F_4

PP1800_PCH_S5 — R325 *10K_4 — PP3300_EC

[7] PMC_SUSPWRDNACK — PMC_SUSPWRDNACK — Q32 PJA138K — PCH_SUSPWRDNACK [28]

USB OC

PP1800_PCH_S5 — R120 10K_4 — PP3300_EC

[8,26] USB_OC0# — USB_OC0# — Q10 PJA138K — USB_OC0_L [28]

PP1800_PCH_S5 — R48 10K_4 — PP3300_EC

[8,23] USB_OC1# — USB_OC1# — Q3 PJA138K — USB_OC1_L [28]

PWRON SEQUENCE

[7,12] SLP_S3# — SLP_S3# — Q27A PJ4N3KDW — PCH_SLP_S3_L — PCH_SLP_S3_L [28]

PP1800_PCH_S5 — R307 *10K_4 — PP3300_EC

Q27B PJ4N3KDW — R310 *10K_4

[3,7,12] SLP_S4# — SLP_S4# — PCH_SLP_S4_L — PCH_SLP_S4_L [28]

PP1800_PCH_S5 — R326 *10K_4 — PP3300_EC

[7] SLP_S0IX# — SLP_S0IX# — Q33 PJA138K — PCH_SLP_SX_L [28]

PP1800_PCH_S5 — R186 10K_4 — PP3300_PCH

[7,12] SOC_PLTRST# — SOC_PLTRST# — Q19 PJA138K — PLTRST# [20,22,28]

R180 *100K_4

02/27 Cancel level shift for S3 leakage on PP1800_PCH issue.

Quanta Computer Inc.

PROJECT : ZRU

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	Level Shifter (SOC_EC)	1A
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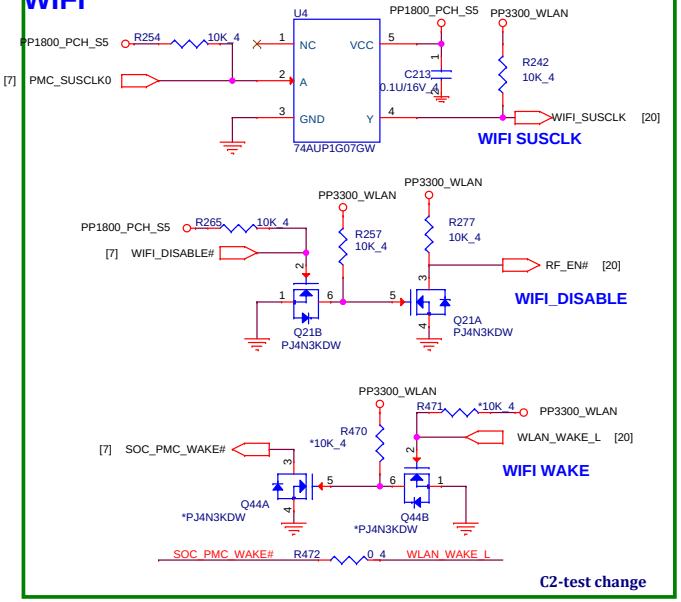
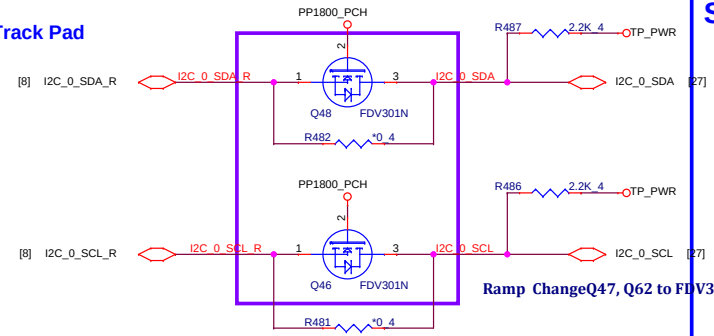
Touch Panel level shift(TPS)

WIFI

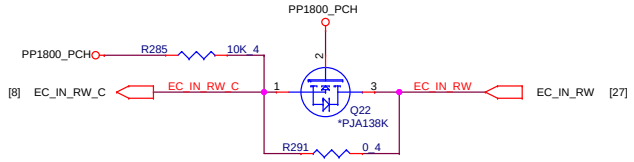


Track Pad

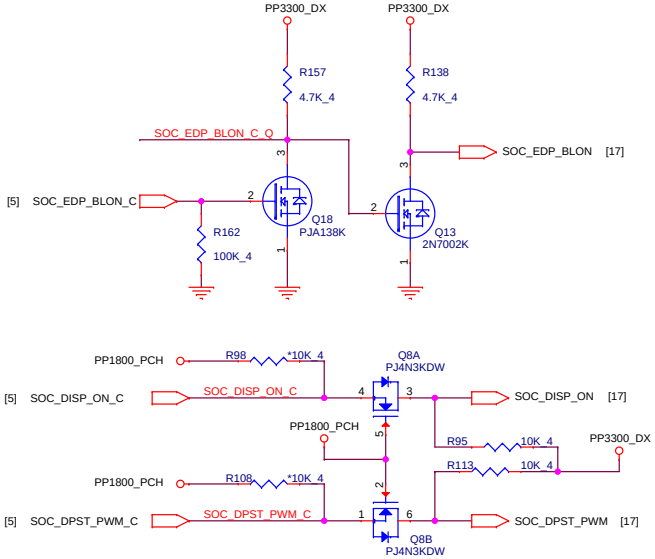


Ramp ChangeQ47, Q62 to FDV301N 22u--0326

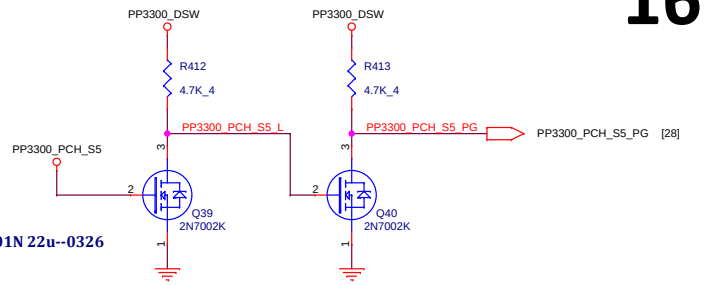
HW RESET



eDP control pin

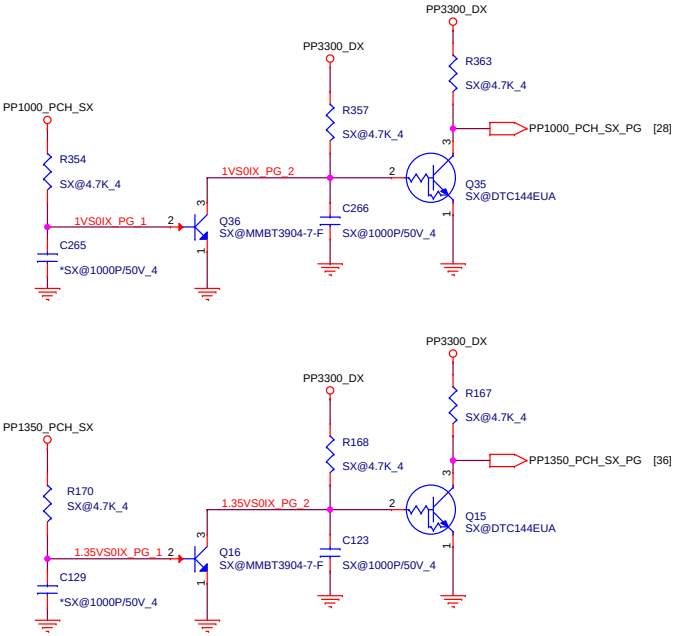


S5 Power Good(+3V_S5)

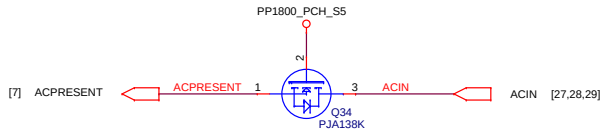


S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed



AC Detect



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Quanta Computer Inc.

PROJECT : ZRU

Size	Document Number	Rev
	Level Shifter (SOC_DEV)	1A

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LCD CONN

VIN
F1
KMC5S150RY24
C318 4.7U/25V_8
C307 1000P/50V_4
LCD_VIN
Max 1.5A
LCDVCC
Max 1.5A
CN3

02/06 Reserve TP for AUO panel pin 14(LCD Panel Self Test Enable).

TP71
LCD_Self_Test
EC_BL_PWM_CONN
EC_BL_EN_CONN
EDP_HPD_CONN

eDP (VGA)

[5] EDP_AUXN
[5] EDP_AUXP
C310 0.1U/16V_4
C311 0.1U/16V_4
EDP_AUXN_C
EDP_AUXP_C

[5] EDP_TXP0
[5] EDP_TXN0
C312 0.1U/16V_4
C313 0.1U/16V_4
EDP_TXP0_C
EDP_TXN0_C

[5] EDP_TXP1
[5] EDP_TXN1
C314 0.1U/16V_4
C315 0.1U/16V_4
EDP_TXP1_C
EDP_TXN1_C

DMIC_DAT C110 *10P/50V_4
DMIC_CLK C111 *10P/50V_4

[24] DMIC_DAT
DMIC_DAT

DIMC

150mA
CCD_PWR
[24] DMIC_CLK
DMIC_CLK

CCD USB (CCD)

USBP2+_R
USBP2-_R

C316 *1U/6.3V_4
PP1800_PCH
R432 *SHORT_4
DMIC_VCC

Touch Screen (TPS)

[5] EDP_HPD
R109 33_4
EDP_HPD_CONN
C95 *10P/50V_4

ACS DFHS40FS104
CLX DFHS40FS106

EDP_50406-04071-001

CCD Power(CCD)

0.5A
150224: Change R97 to short pad
PP3300_DX
CCD_PWR
R97 *SHORT_6
C66 1U/6.3V_4
C57 *10P/50V_4
C59 1000P/50V_4

CCD USB(CCD)

150224: Remove L6 and change R430,R431 to short pad

[8] USBP2+
[8] USBP2-
R430 *SHORT_4
R431 *SHORT_4
USBP2+_R
USBP2-_R

eDP panel control(LDS)

[16] SOC_DPST_PWM
R119 10/F_4
EC_BL_PWM_CONN
R118 *100K_4
C102 *0.1U/16V_4

150310: Change R119 to 10ohm

[16] SOC_EDP_BLON
R131 2.2K_4
EC_BL_EN_CONN

[28] EC_BL_DISABLE_L
D6 RB500V-40
EC_BL_DISABLE#
R125 *SHORT_4
R129 *100K_4

eDP Power(LDS)

PP3300_DX
C47 1U/6.3V_4
U1
IN
IN
ON/OFF
OUT
GND
GND
G5243AT11U
sot23-5

[16] SOC_DISP_ON
R85 *SHORT_4
EDP_ON
R88 100K_4

150224: Change R90 to short pad
LCDVCC_1
R90 *SHORT_8
C44 *0.1U/16V_4
C54 *2.2U/6.3V_6
C72 0.1U/16V_4
C71 0.01U/25V_4
C69 22U/6.3V_8
LCDVCC

Quanta Computer Inc.
PROJECT : ZRU

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	LVDS/CCD/DMIC	1A
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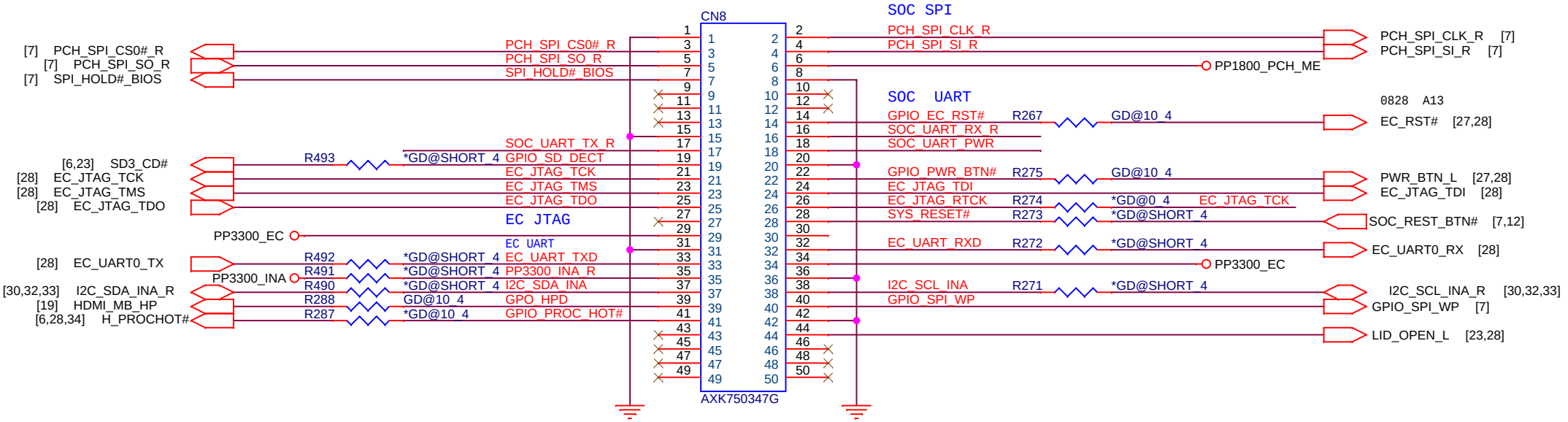
GOOGLE Debug Port(MPC)

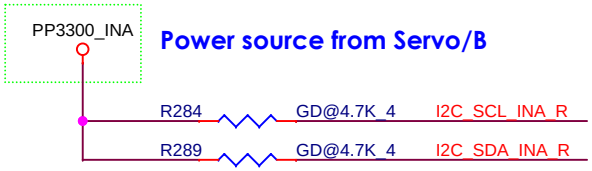
PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD

50 pin BTB is MUST, don't use 42 pin

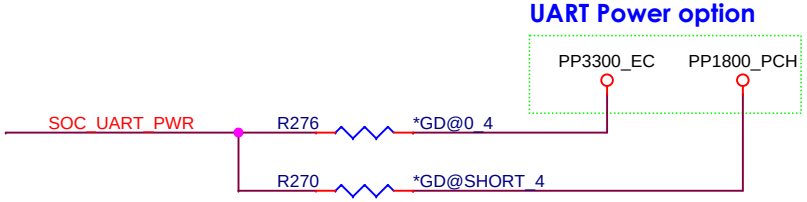
Socket part number AXK750147G



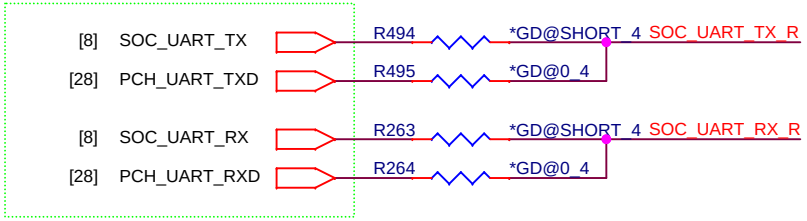
Servo/B I2C Power(MPC)



UART Power(MPC)



UART(MPC)



Quanta Computer Inc.

PROJECT : ZRU

Size	Document Number	Rev
	Google Debug	1A
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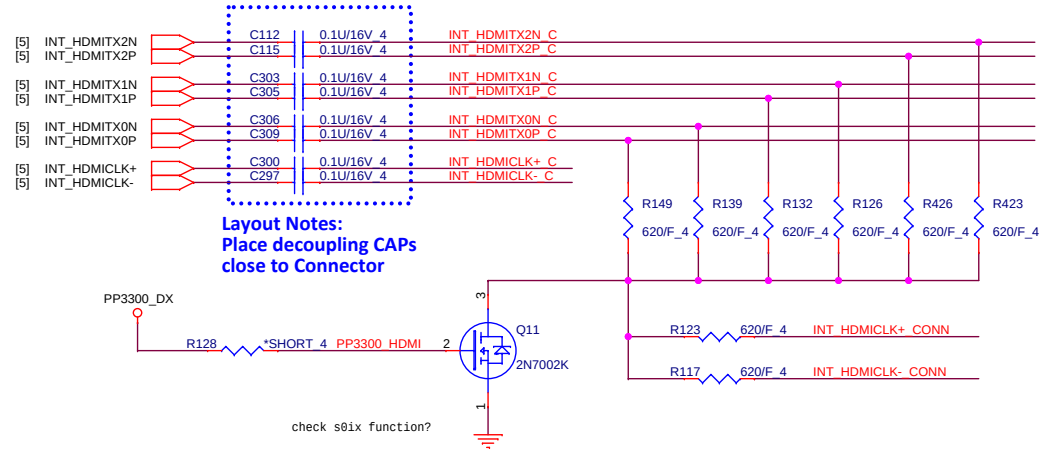
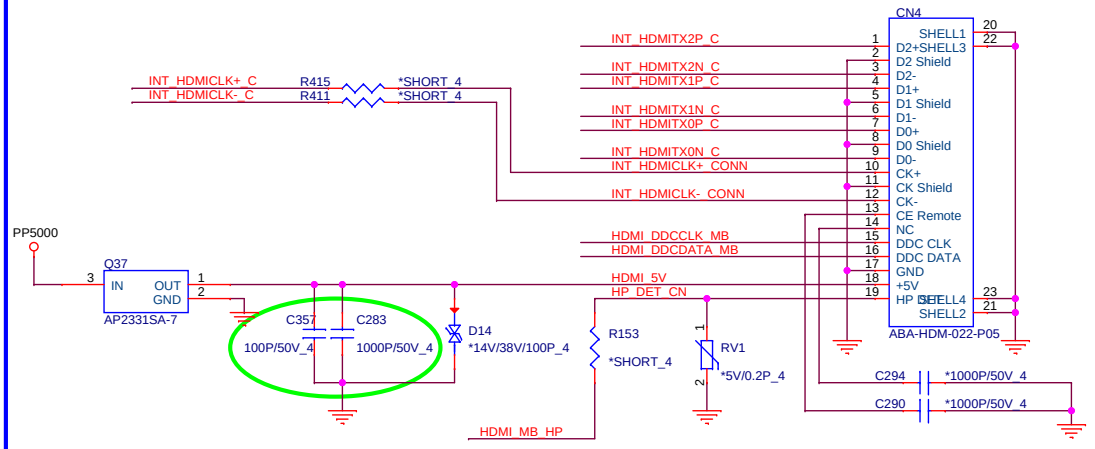
HDMI Cost Reduced level shift (HDM)

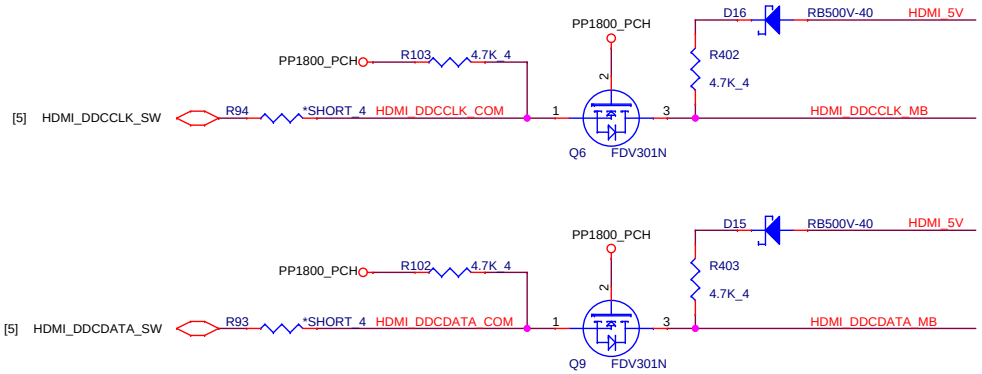


HDMI connector (HDM)



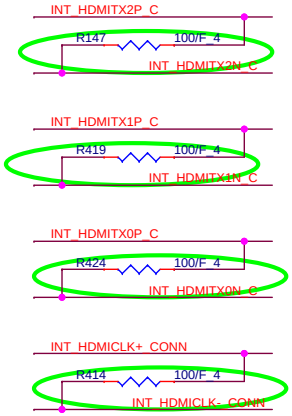
150224: Change C283 to 1000pF and Add C357 for EMI

HDMI DDC (HDM)

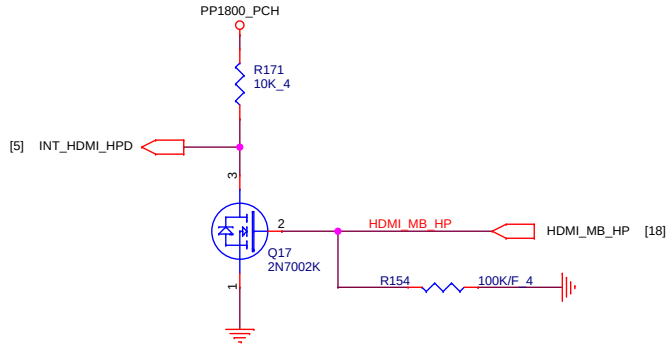


EMI

150224: Stuff R147,R419,R424,R414



HDMI-detect (HDM)



Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	HDMI	1A
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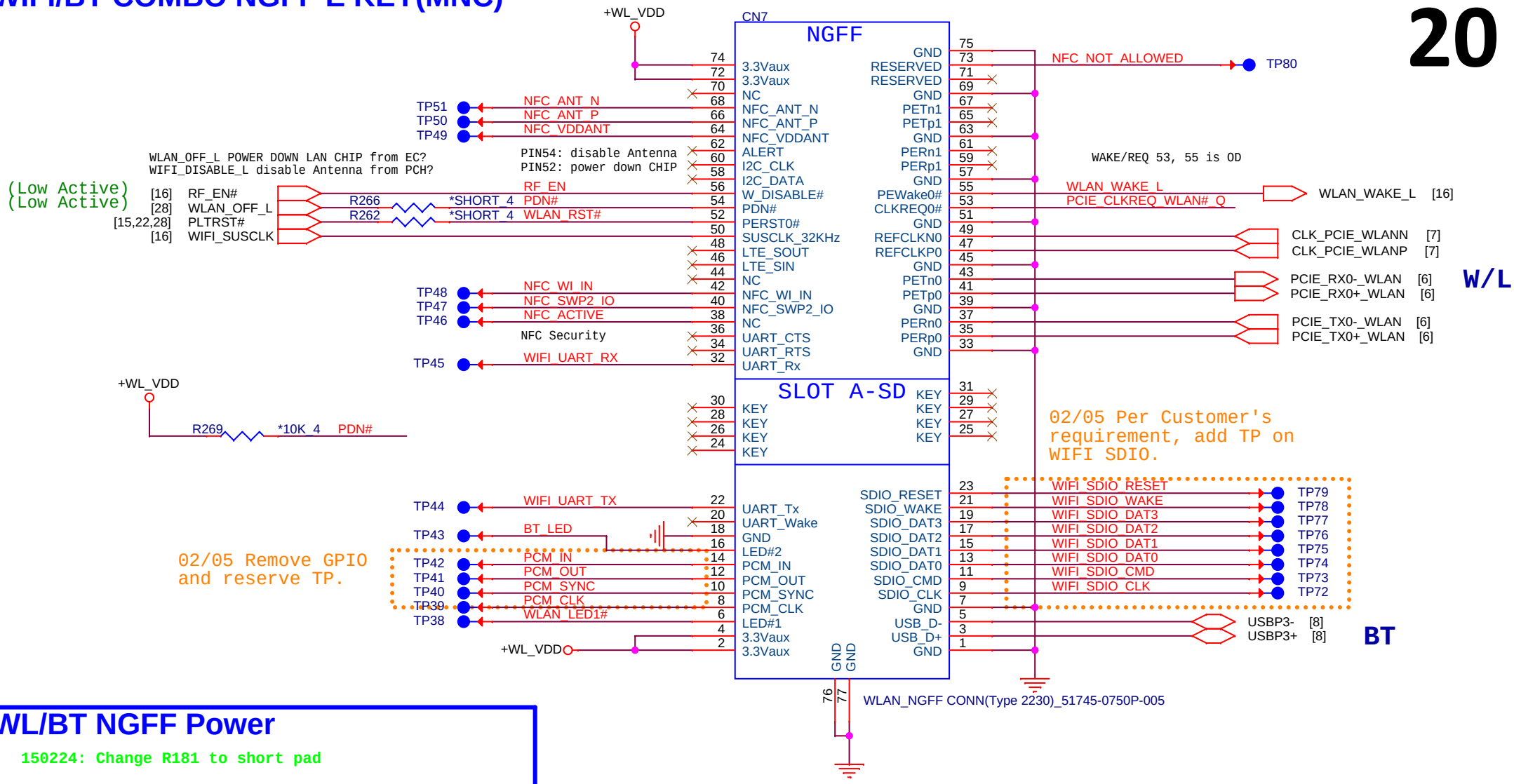
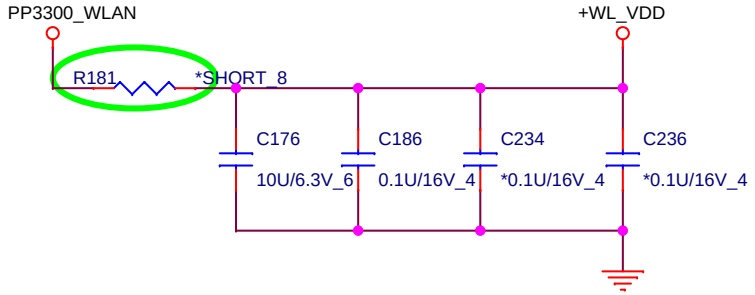
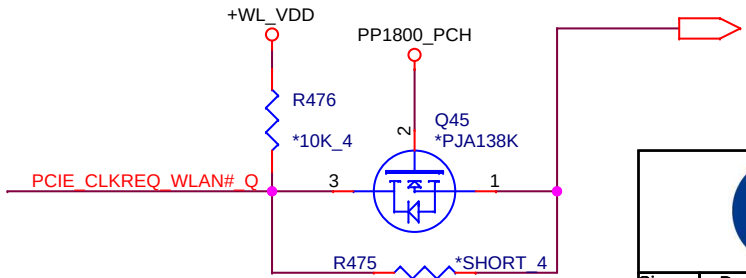
WIFI/BT COMBO NGFF E KEY(MNC)



WL/BT NGFF Power

150224: Change R181 to short pad





Quanta Computer Inc.

PROJECT : ZRU

Size	Document Number	Rev
	WIFI / BT	1A

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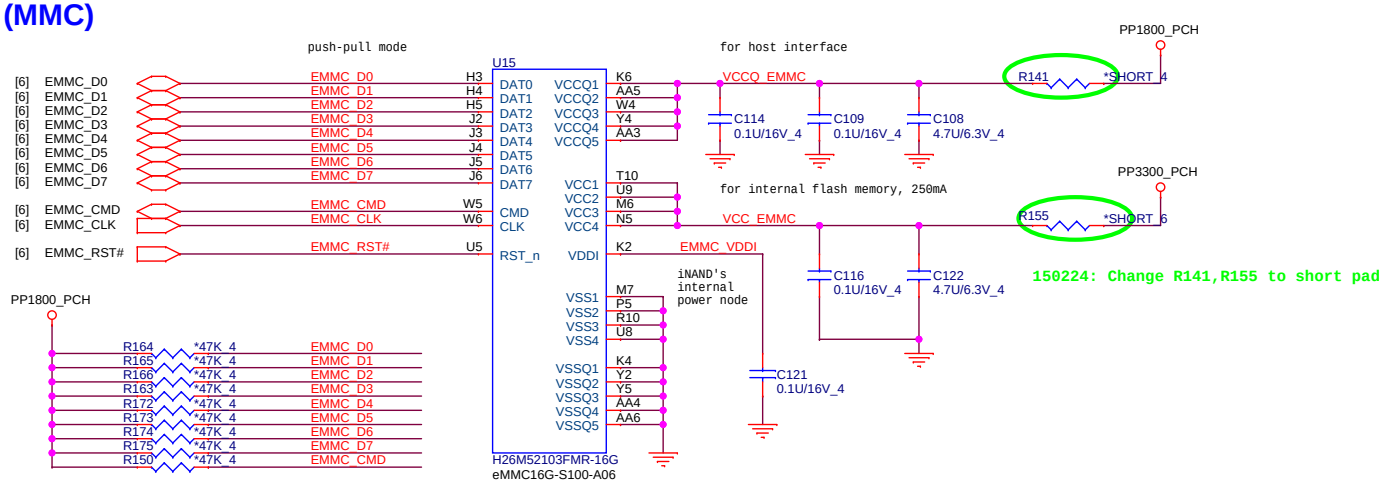
EMMC (MMC)



150224: Change R141,R155 to short pad

Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: EMMC / LTE NGFF	Rev: 1A
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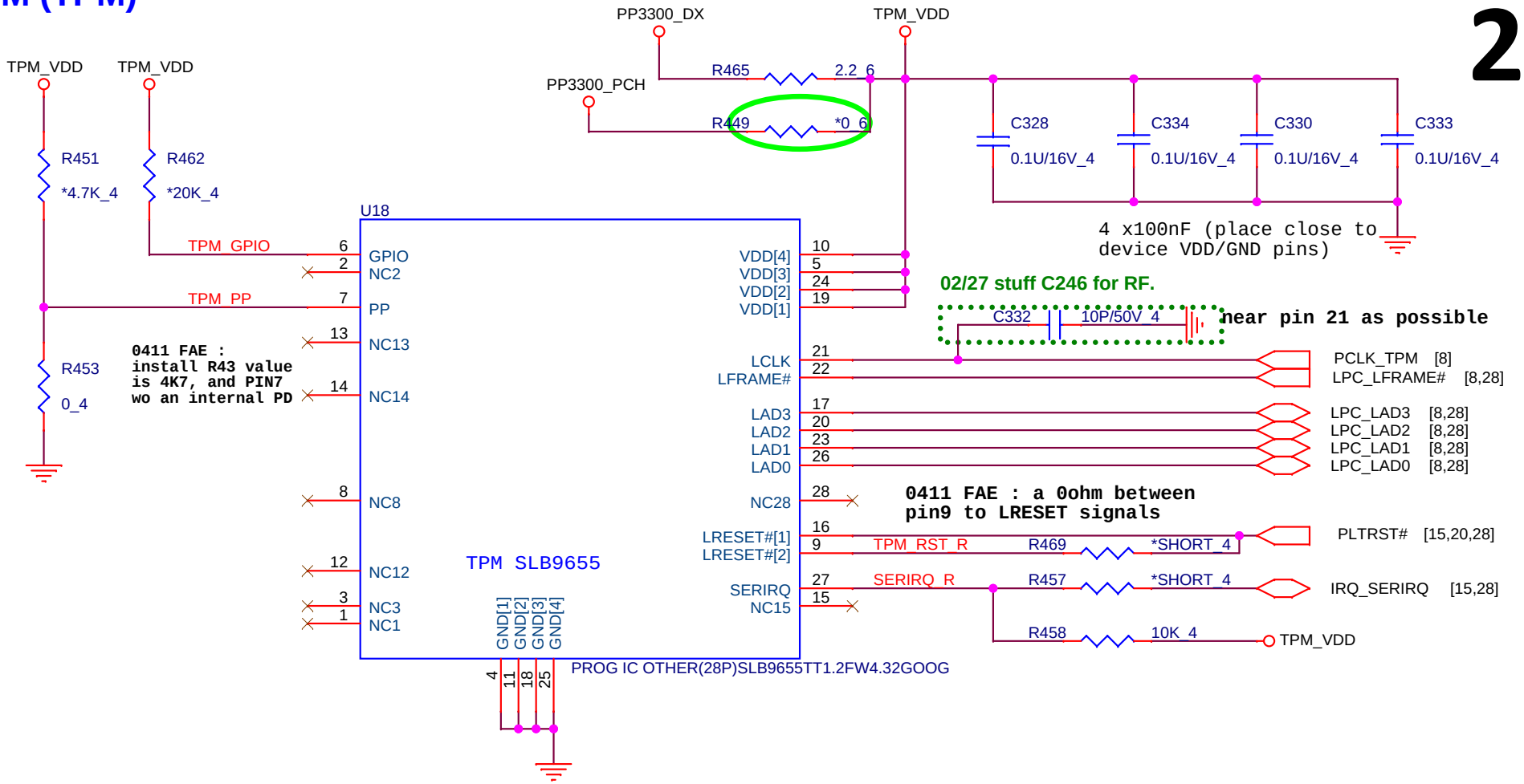
TPM (TPM)



Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: TPM SLB9655 / LED	Rev 1A
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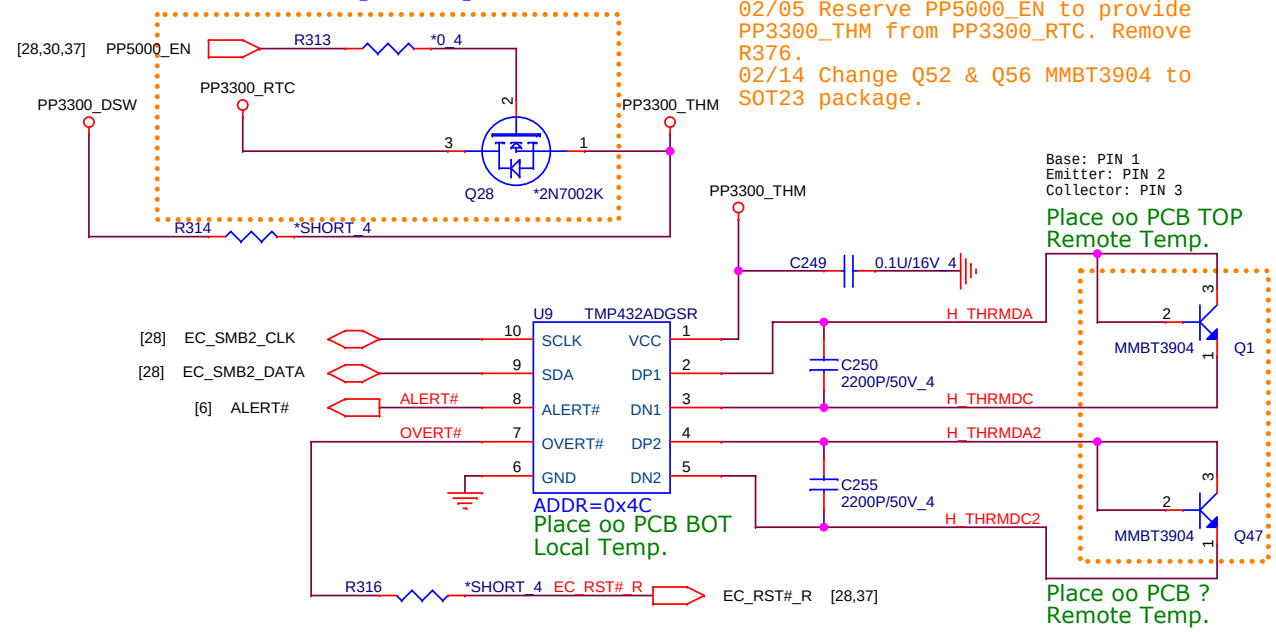
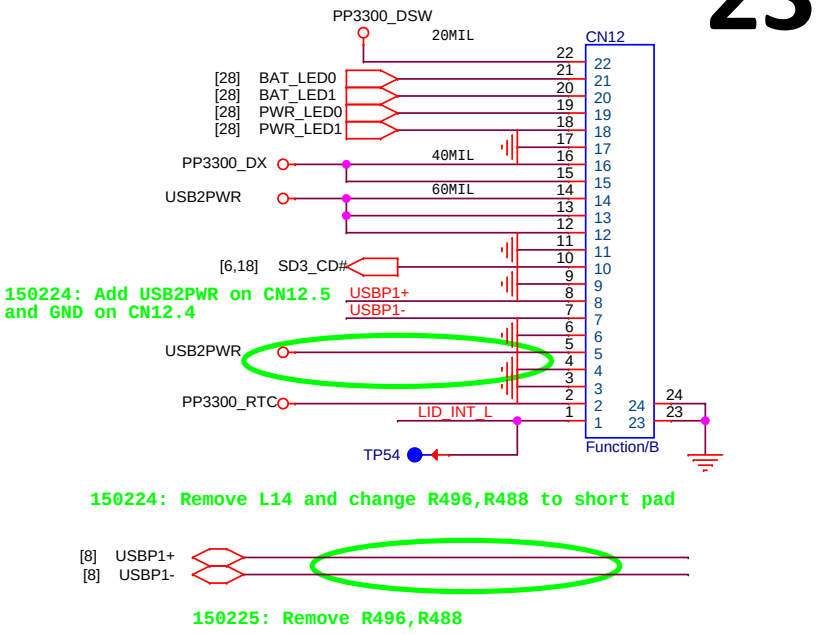
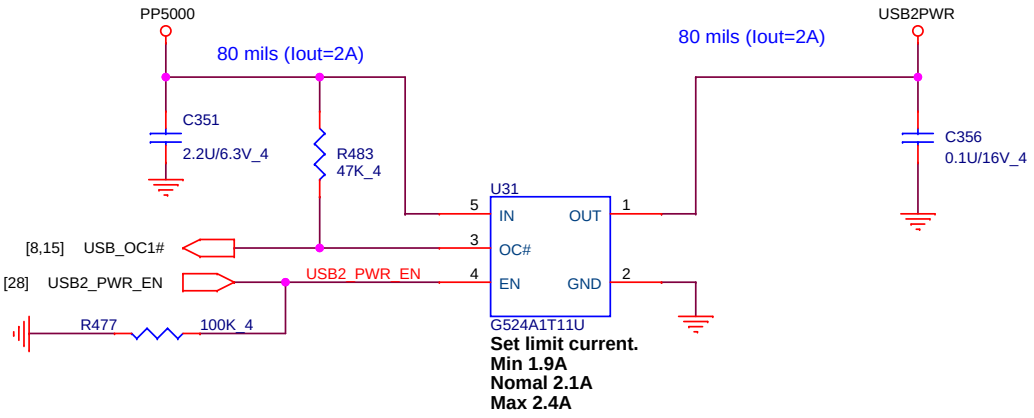
Thermal Sensor(THM)



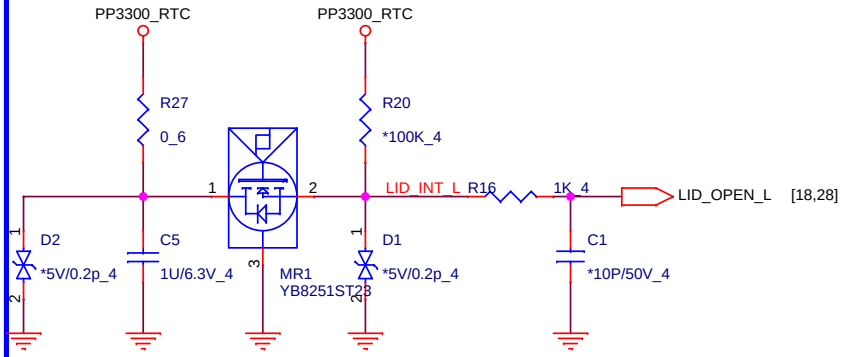
DB FFC conn 30P





change USB power SW from G524C1T11U to G524A1T11U 3/18

Lid Switch (HSR)



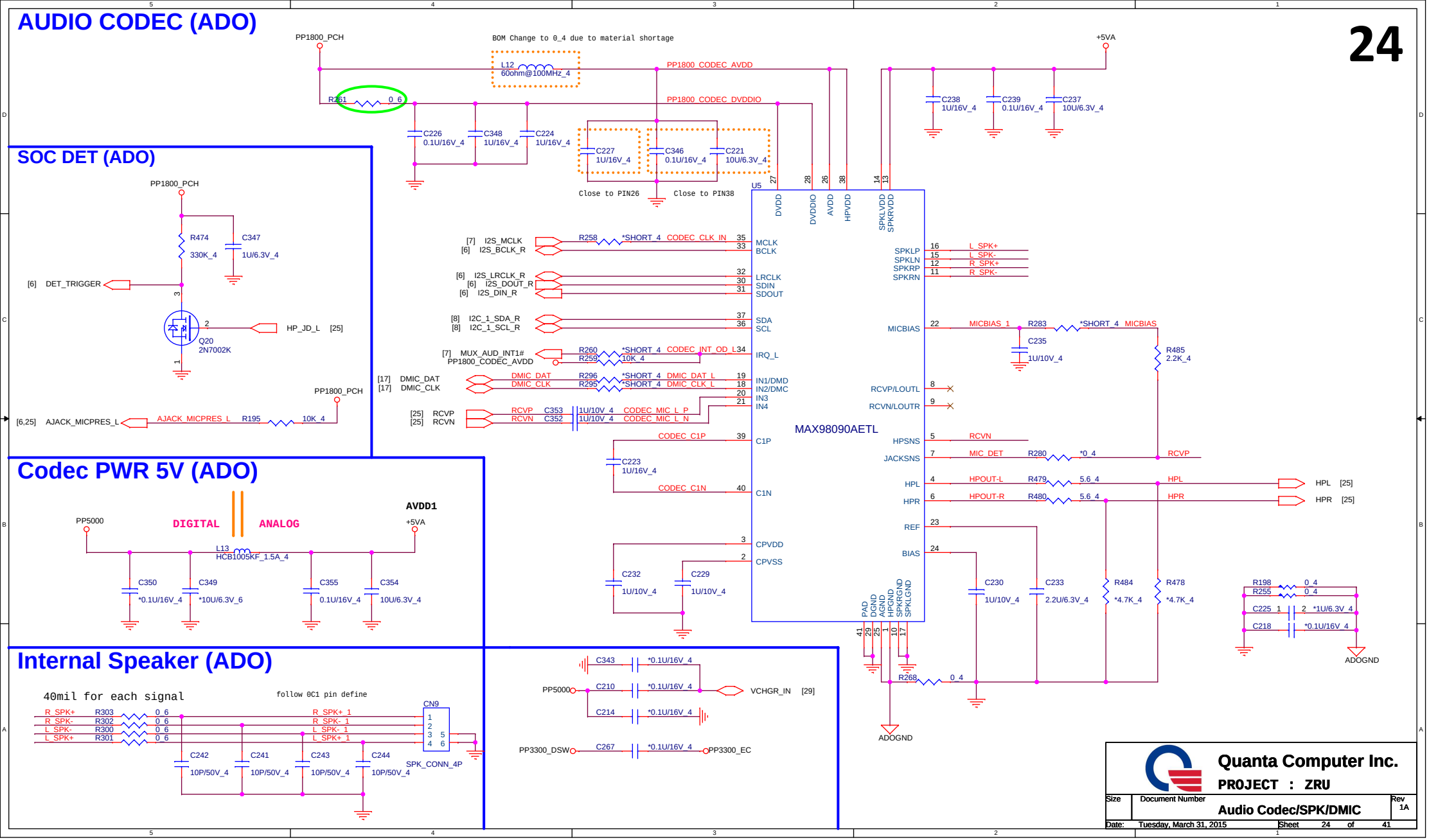
Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: DB/Thermal sensor/LID	Rev: 1A
Date: Tuesday, March 31, 2015	Sheet 23 of 41	

AUDIO CODEC (ADO)

SOC DET (ADO)

Codec PWR 5V (ADO)

Internal Speaker (ADO)



Quanta Computer Inc.			
PROJECT : ZRU			
Size	Document Number	Audio Codec/SPK/DMIC	Rev 1A
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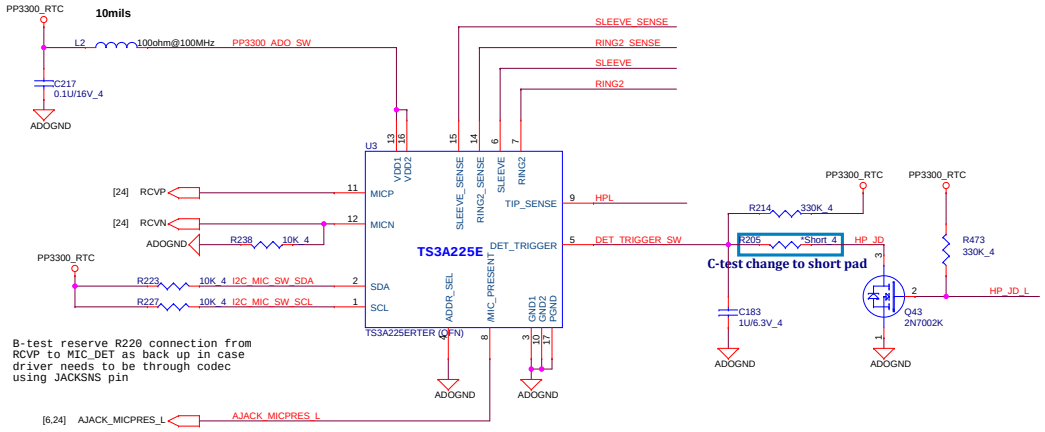
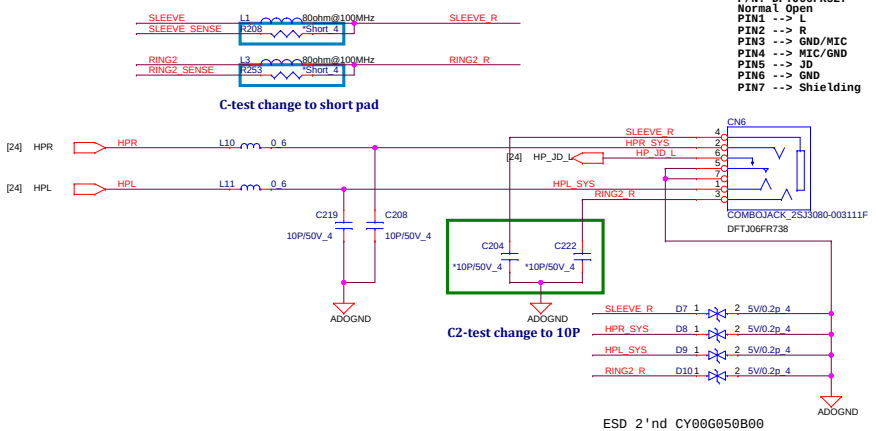
Audio Headset Switch



combo jack
Normal open

P/N: DFTJ06FR527
Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC
PIN4 --> MIC/GND
PIN5 --> JD
PIN6 --> GND
PIN7 --> Shielding



Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: Audio Headset Switch/HP	Rev: 1A
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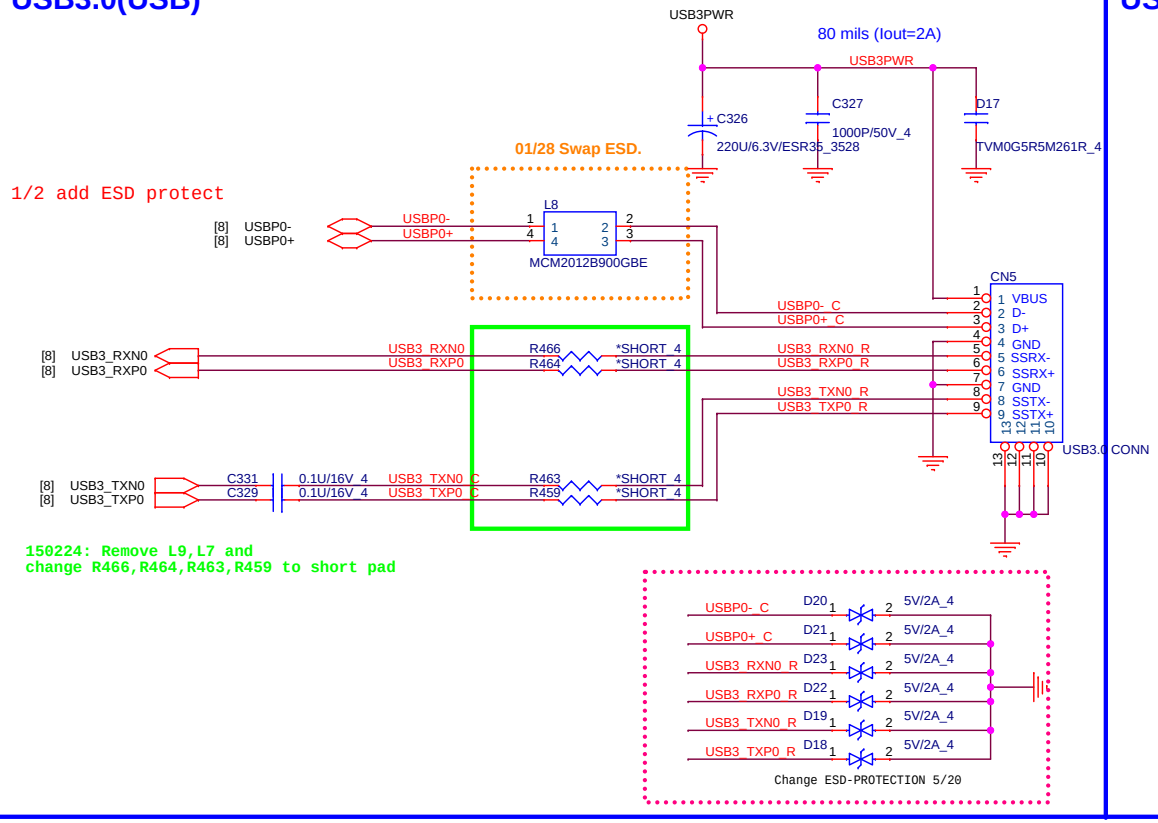
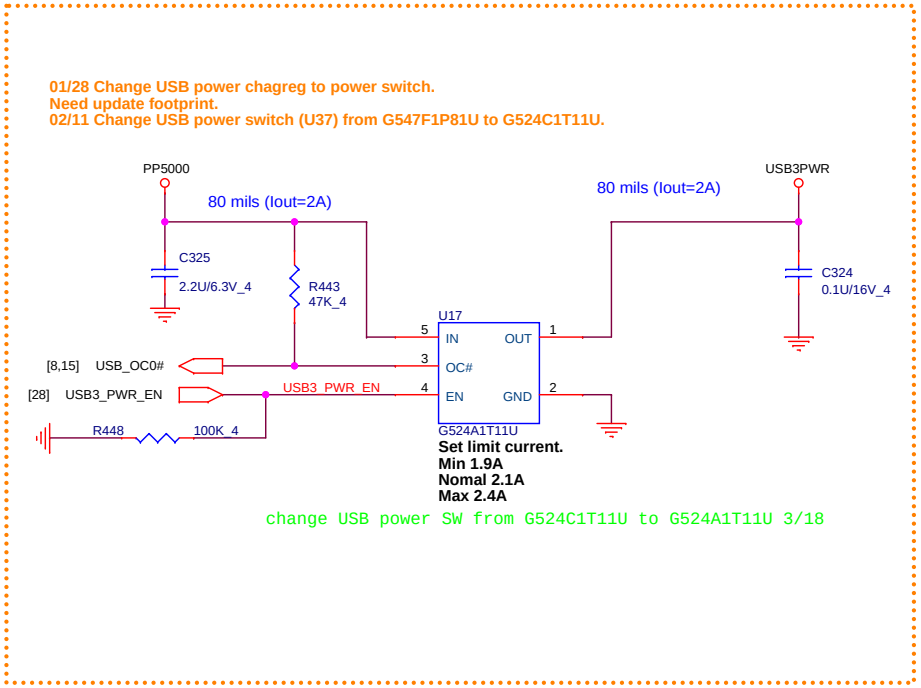
USB3.0(USB)



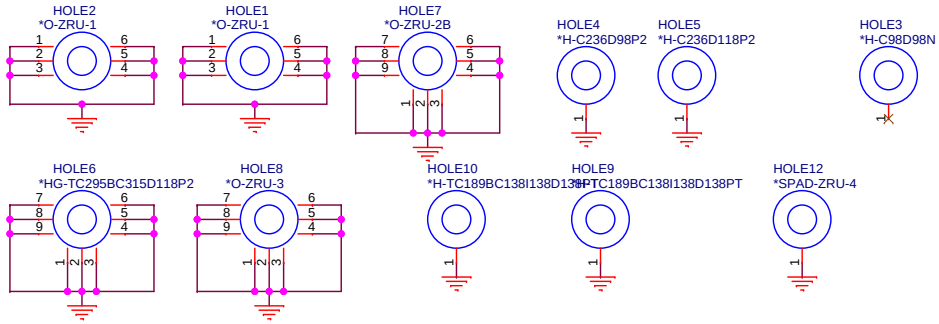
USB Switch



26

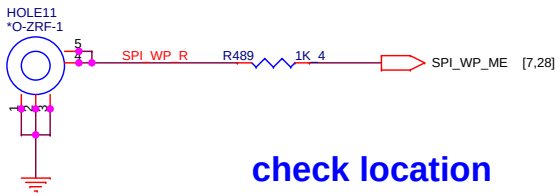
HOLE(OTH)

02/13 Update hole footprint.



CPU

ROM WP#



check location

Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: USB3/Hole	Rev: 1A
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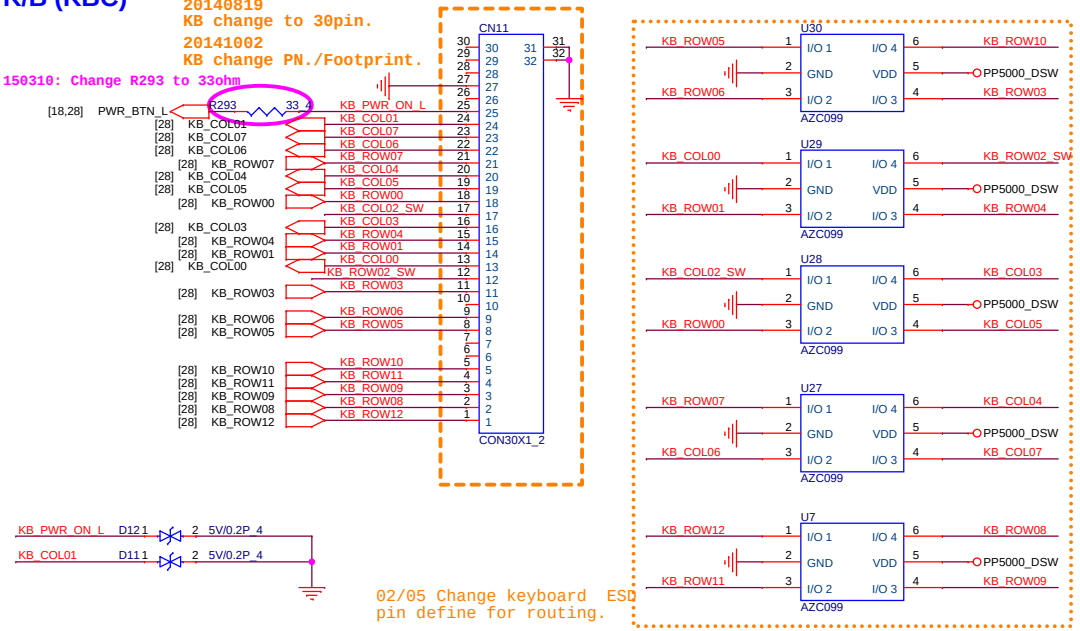
K/B (KBC)

20140819
KB change to 30pin.
20141002
KB change PN./Footprint.

150310: Change R293 to 33ohm

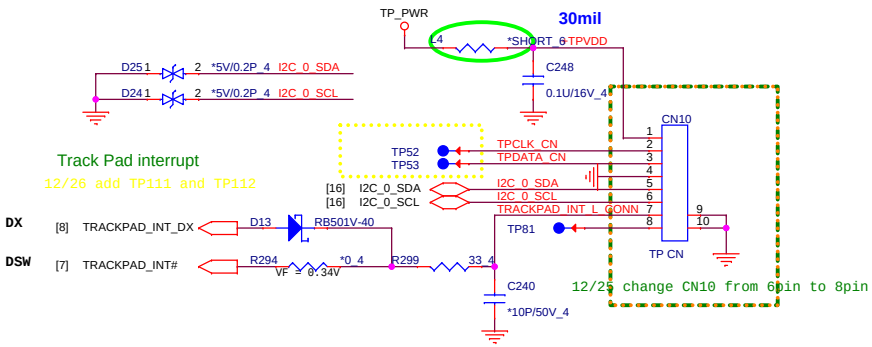


KB_PWR_ON_L D121 2 5V/0.2P_4
KB_COL01 D111 2 5V/0.2P_4

02/05 Change keyboard ESD pin define for routing.

Track PAD BOARD CONN (TPD)

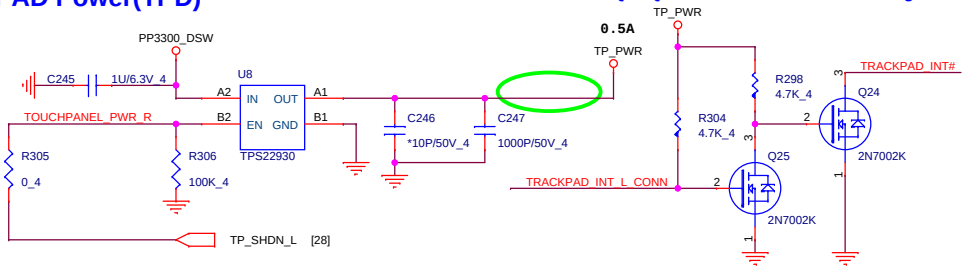
150224: Change L4 to short pad



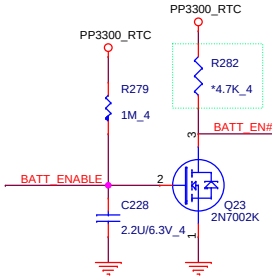
12/25 change CN10 from 6pin to 8pin

Track PAD Power(TPD)

0423 add Q44/Q65 on Track Pad INT# for leakage issue



HOLELESS RESET 2-CHIP(KBC)



BATT_EN# [29]

B/I shutdown function

The first time Power On needs the AC adapter.

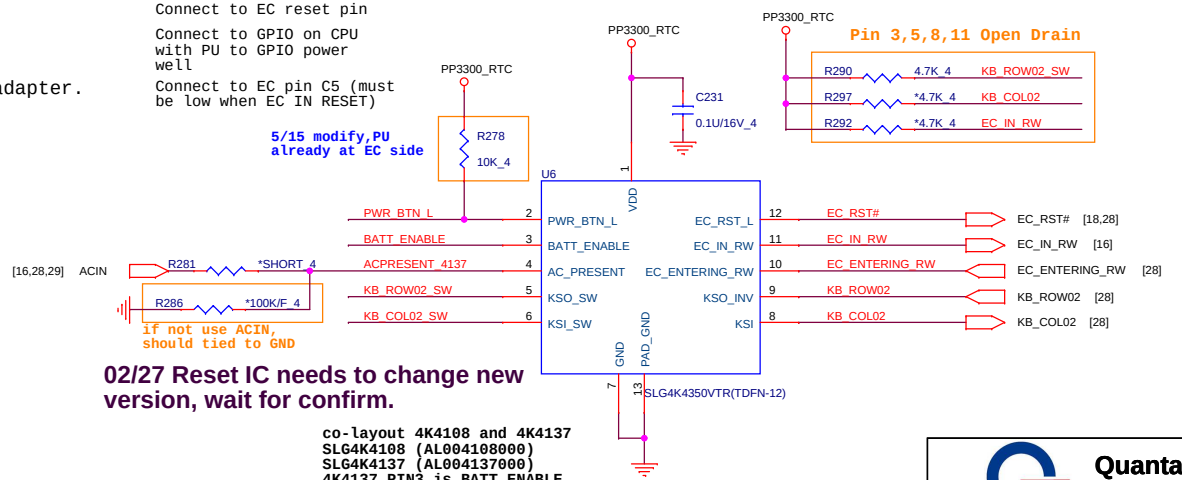
0318 unstuff R454 for auto power on issue when insert battery first time,follow OC2A

Connect to EC reset pin

Connect to GPIO on CPU with PU to GPIO power well

Connect to EC pin C5 (must be low when EC IN RESET)

5/15 modify,PU already at EC side



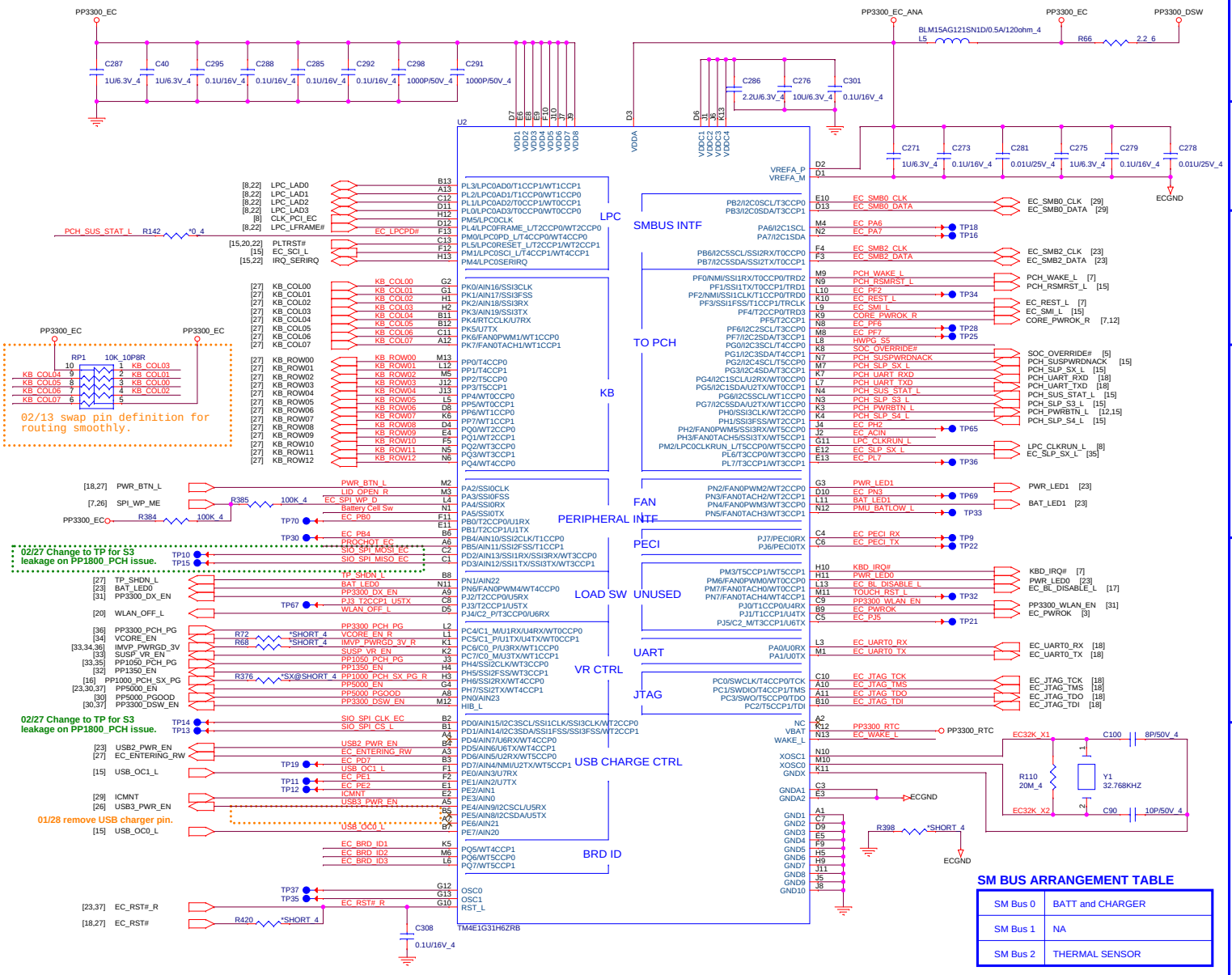
02/27 Reset IC needs to change new version, wait for confirm.

co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

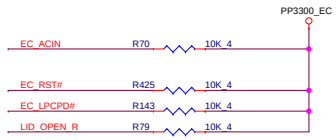
Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	KB/TP/HW Reset	1A
Date: Tuesday, March 31, 2015	Sheet 27 of 41	

EC(KBC)

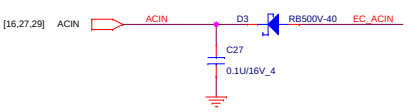


Pull-up(KBC)

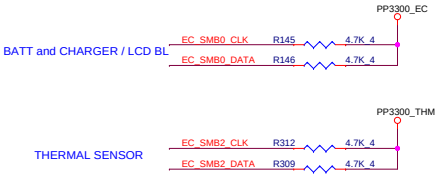


LID_OPEN(KBC)

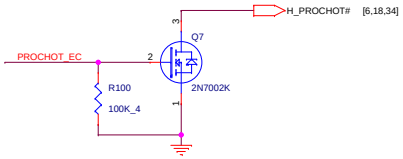
ACIN_EC(KBC)



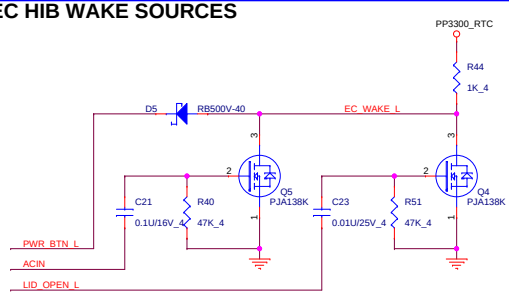
SM BUS/I2C PU(KBC)



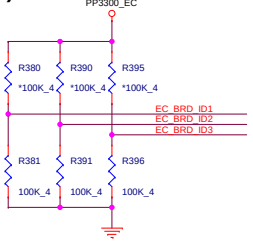
PROCHOT_EC(KBC)



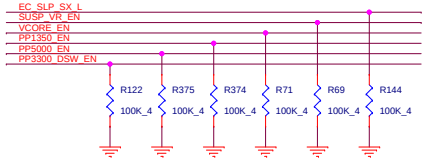
EC HIB WAKE SOURCES



Board_ID(KBC)

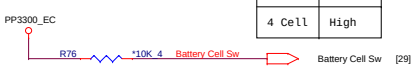


Pull-down(KBC)



HWPG(KBC)

Battery cell select

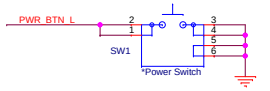


3 Cell	float
4 Cell	High

OD pin list

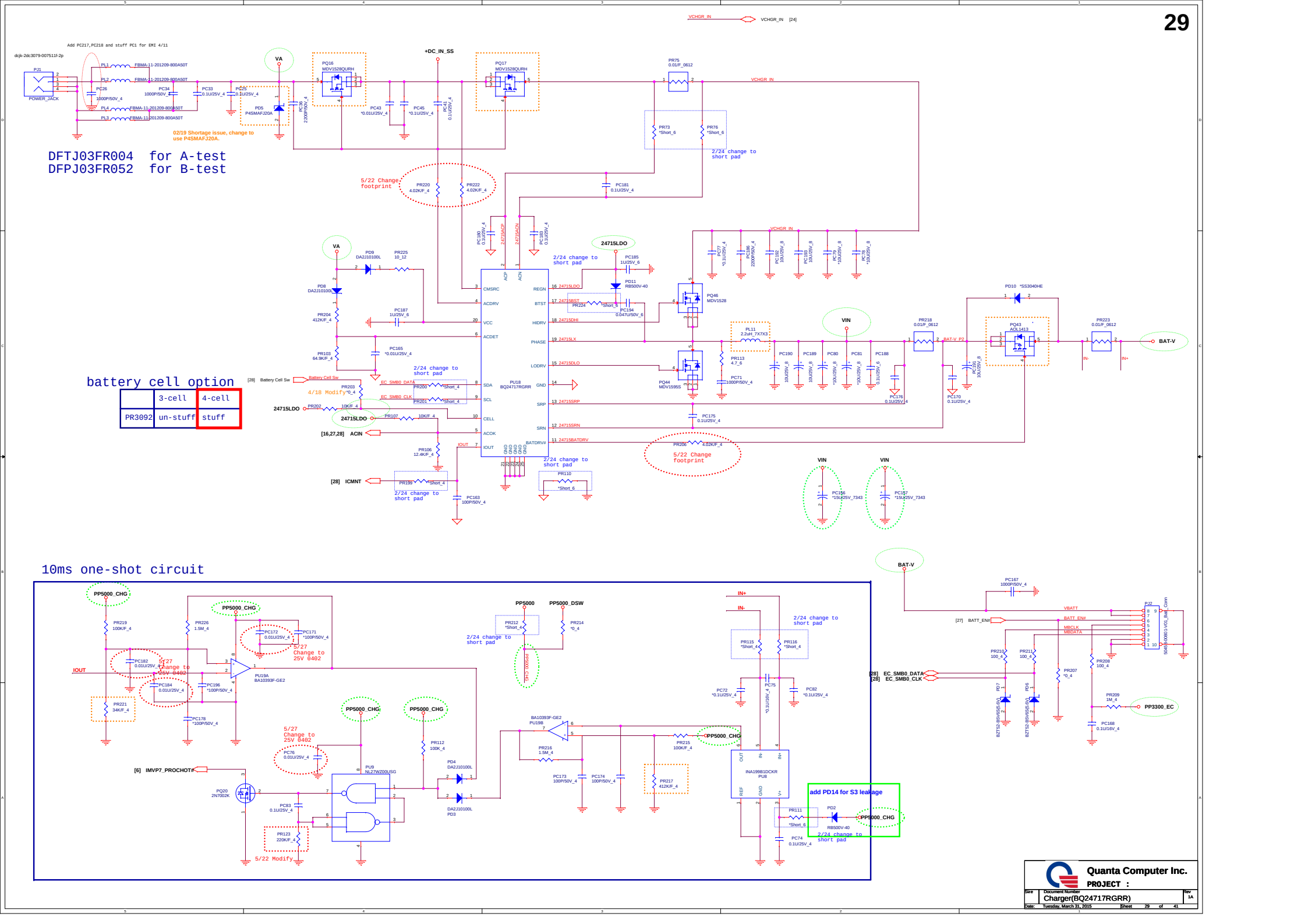
EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

For testing only



Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1A
Date: Tuesday, March 31, 2015	Sheet 28 of 41	

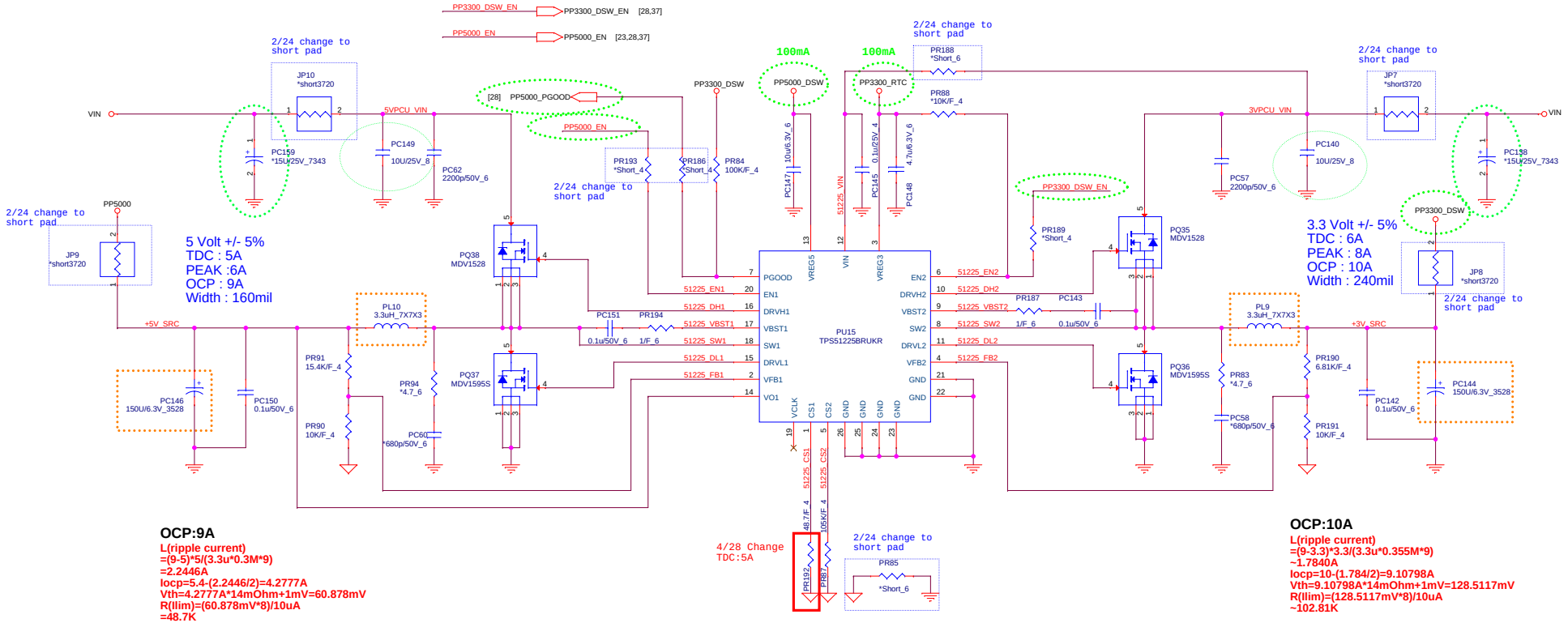


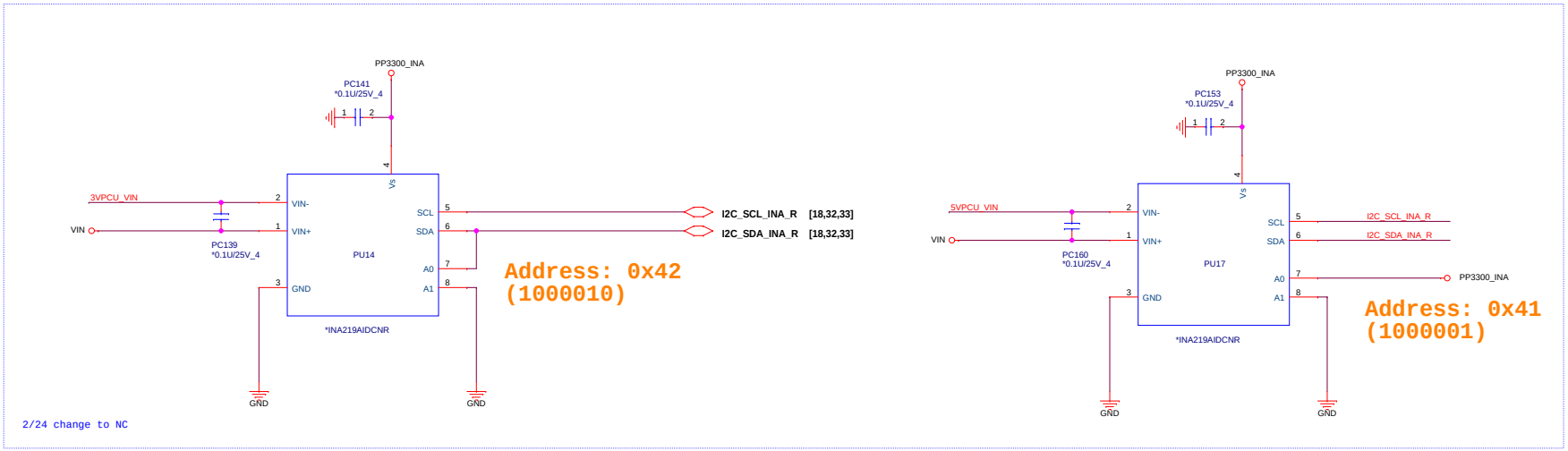
battery cell option

	3-cell	4-cell
PR3092	un-stuff	stuff

10ms one-shot circuit

Quanta Computer Inc.
PROJECT :
Size | Document Number | Rev
Charger(BQ24717RGRR) | 1A
Date: Tuesday, March 31, 2015 | Sheet 29 of 41





Quanta Computer Inc.		
PROJECT :		
Size	Document Number: SYSTEM 5V/3V (TPS51225BRUKR)	Rev 1A
Date: Tuesday, March 31, 2015	Sheet 30 of 41	

[36] PP1800_PCH_S5_PG
[28] PP3300_DX_EN

PP1800_PCH_S5_PG
PP3300_DX_EN

2/24 change to short pad

PP3300_DSW
PR92 *Short_8
PC59 1U/10V_4

[28] PP3300_WLAN_EN
PP3300_WLAN_EN
PR93 *Short_4
2/24 change to short pad
PP3300_WLAN_EN_R
PR89 100K/F_4
PC61 *0.1U/50V_6

PR86 *0_8
PU6
PP3300_WLAN_R
A2 IN OUT A1
EN GND B1
TPS22930
PP3300_WLAN

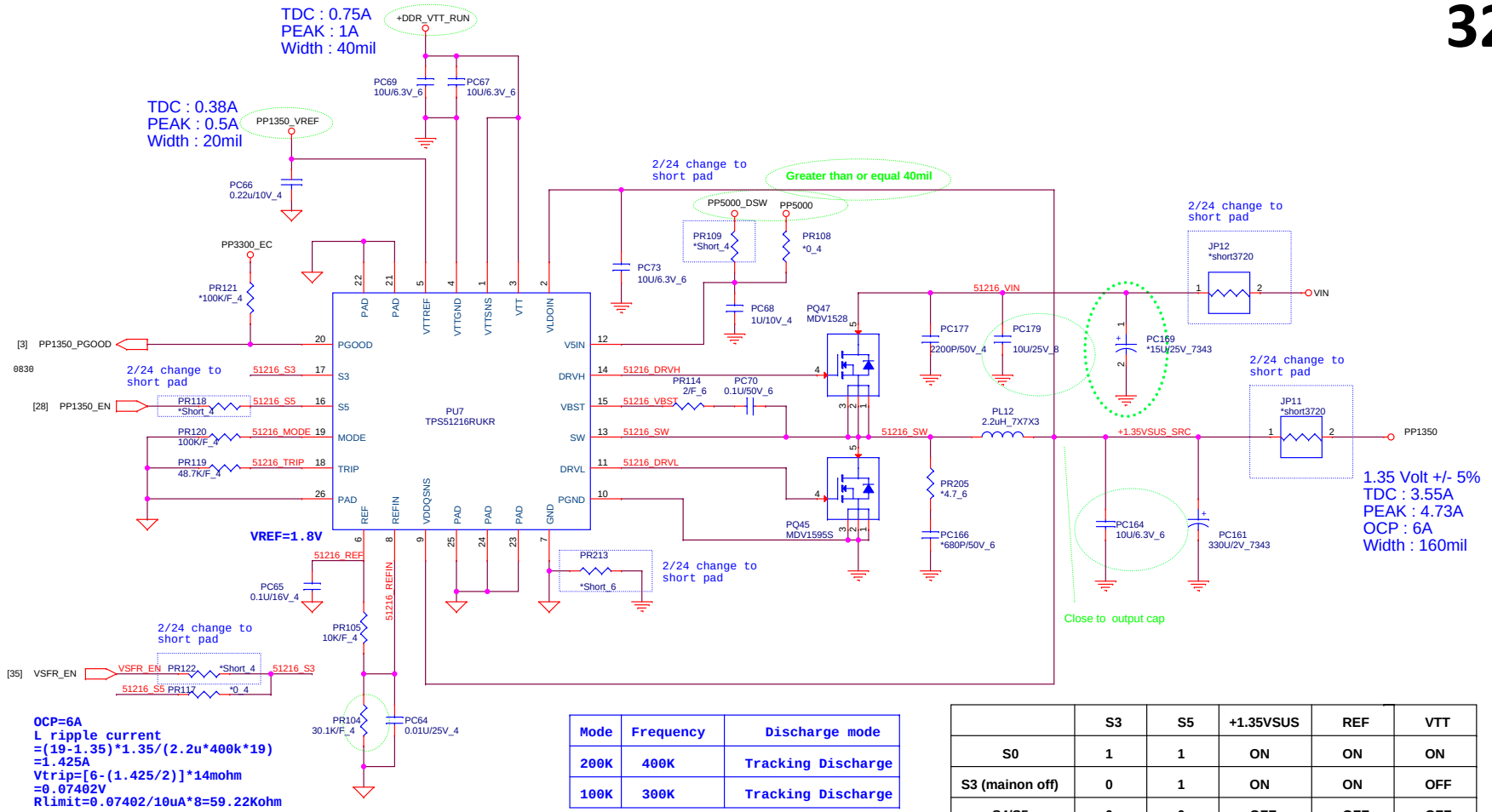
PP3300_PCH_S5_R
PU2
PP3300_DSW
A2 IN OUT A1
B2 EN GND B1
TPS22930
PR8 *Short_6
PP3300_PCH_S5
PC6 1U/10V_4
PP1800_PCH_S5_PG
PR3 *Short_4
PR4 *100K/F_4
PC2 *0.1U/50V_6
2/24 change to short pad
2/24 change to short pad

DX should be earlier than VREN by EC.

PP3300_DSW
PC56 1U/10V_4
PU5
A2 IN1 OUT1 A1
B2 IN2 OUT2 B1
EN GND C1
TPS22964CYZPR
PP3300_DX_EN
PR81 *Short_4
PP3300_DX_EN_R
PR82 100K/F_4
PP3300_DX_R
PR80 *Short_6
PP3300_DX
2/24 change to short pad
2/24 change to short pad

Quanta Computer Inc.
PROJECT :

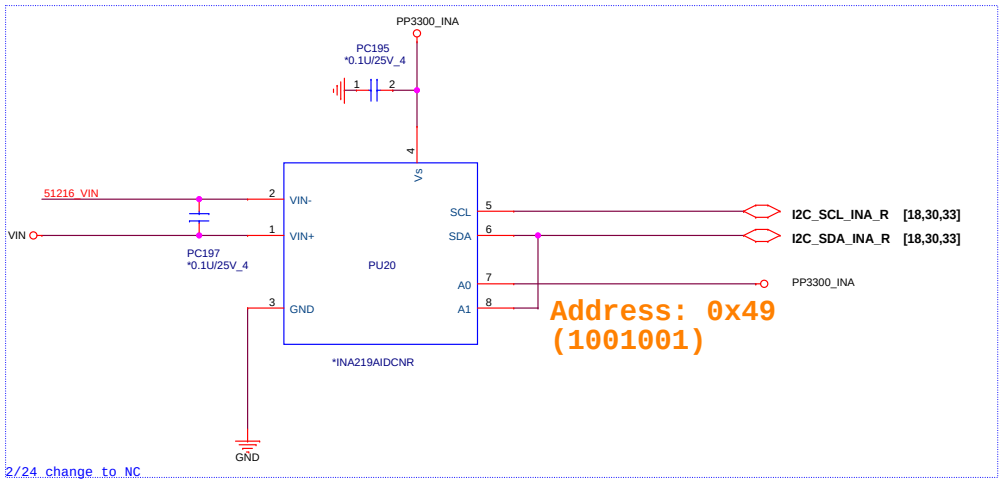
Size	Document Number	Rev
	Load Switch	1A
Date: Tuesday, March 31, 2015	Sheet 31 of 41	



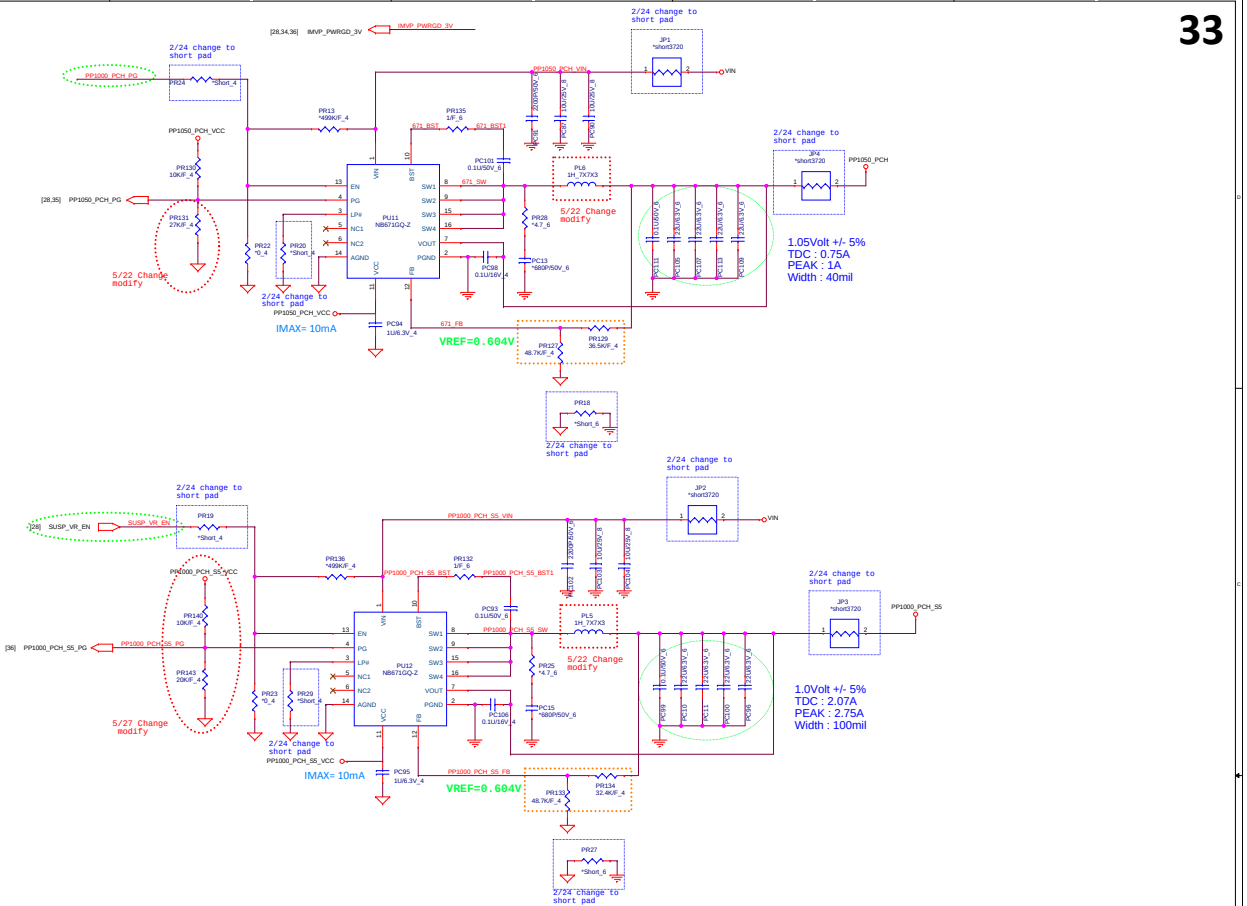
OCP=6A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=[6-(1.425/2)]*14mohm
=0.07402V
Rlimit=0.07402/10uA*8=59.22Kohm

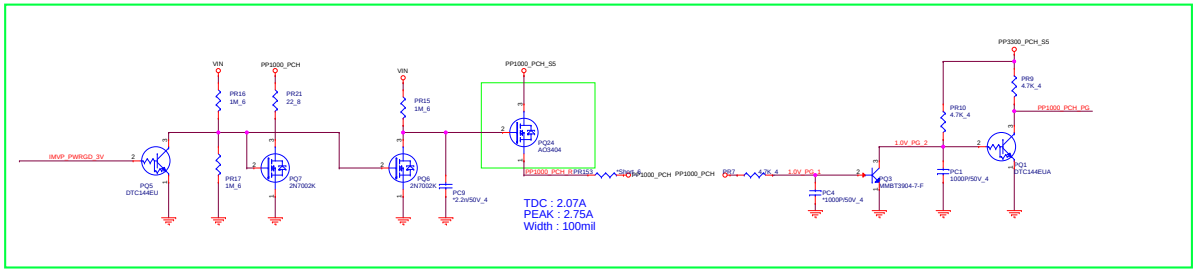
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

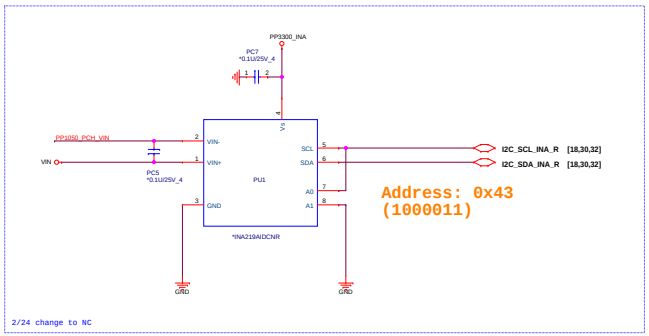
	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

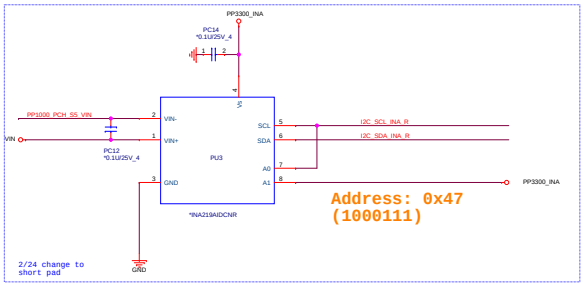


Quanta Computer Inc.	PROJECT :	
Size	Document Number: DDR 1.35V(TPS51216)	Rev 1A
Date: Tuesday, March 31, 2015	Sheet 32 of 41	





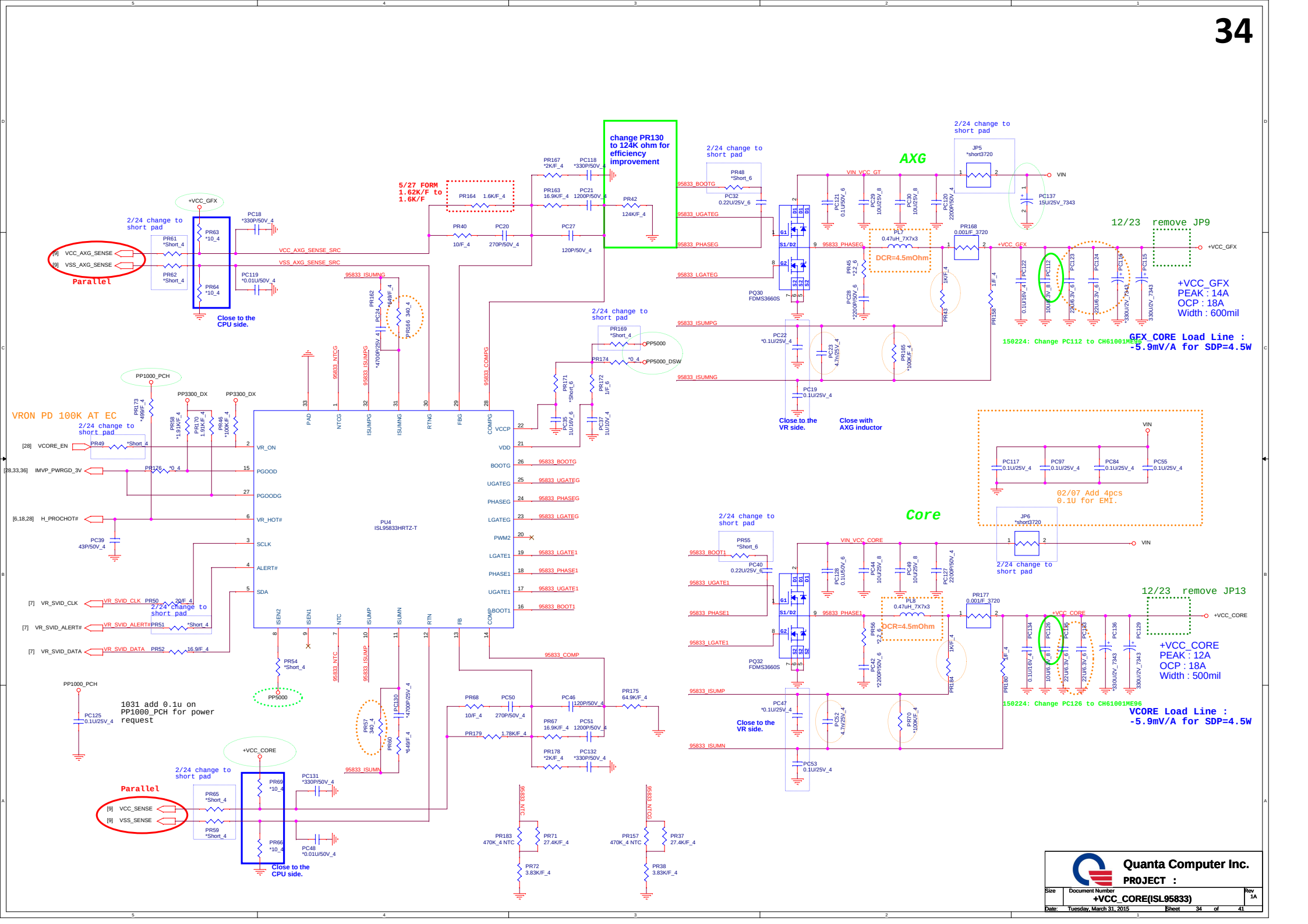




Quanta Computer Inc.

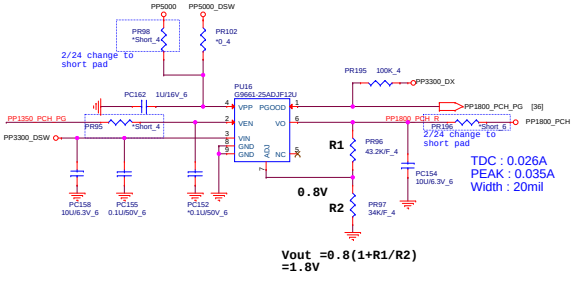
PROJECT :

Size	Document Number	Rev
	+1.05V/+1V(NB671LGQ-Z)	1A
Date:	Tuesday, March 31, 2015	Sheet 33 of 41

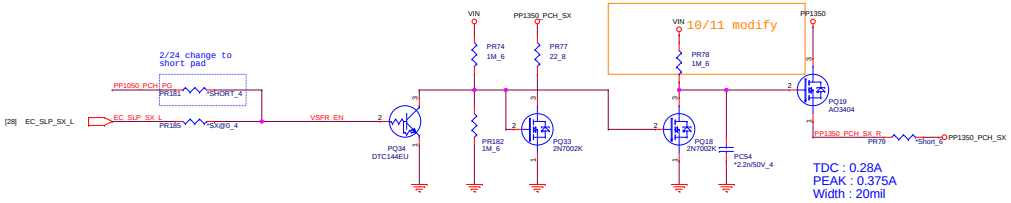


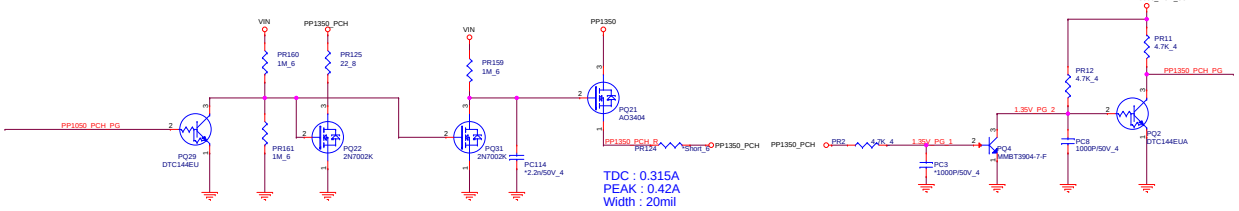
Quanta Computer Inc.	PROJECT :		
Size	Document Number		Rev
	+VCC_CORE(ISL95833)		1A
Date: Tuesday, March 31, 2015	Sheet 34 of 41		

[32] VSFR_EN → VSFR_EN
[28,33] SUSP_VR_EN
[28,33] PP1050_PCH_PG



Vout =0.8(1+R1/R2)
=1.8V



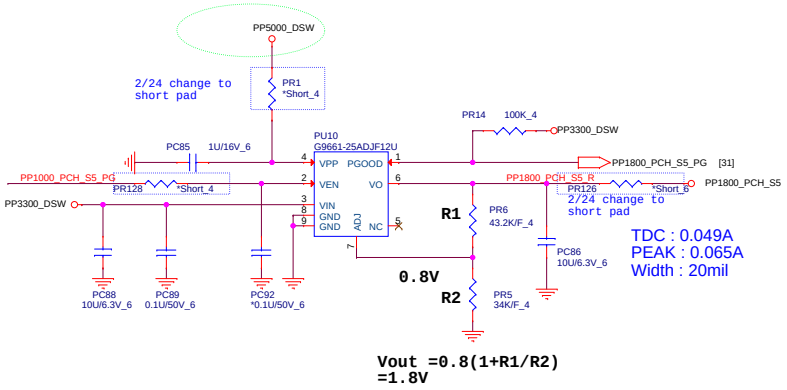


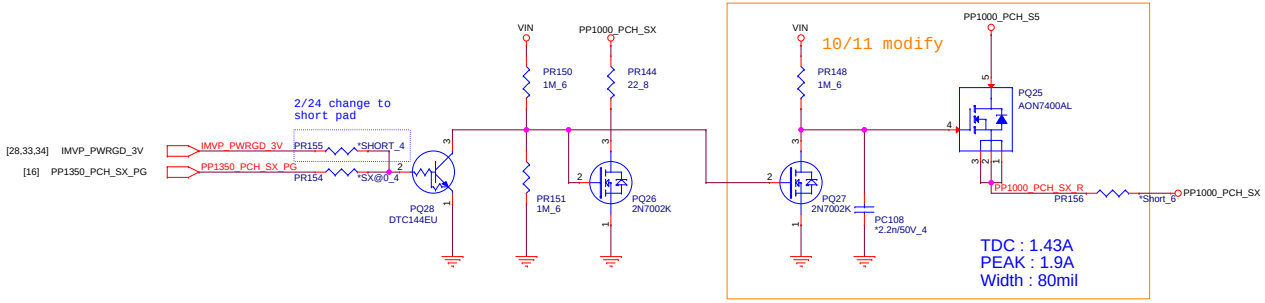
Quanta Computer Inc.
PROJECT :

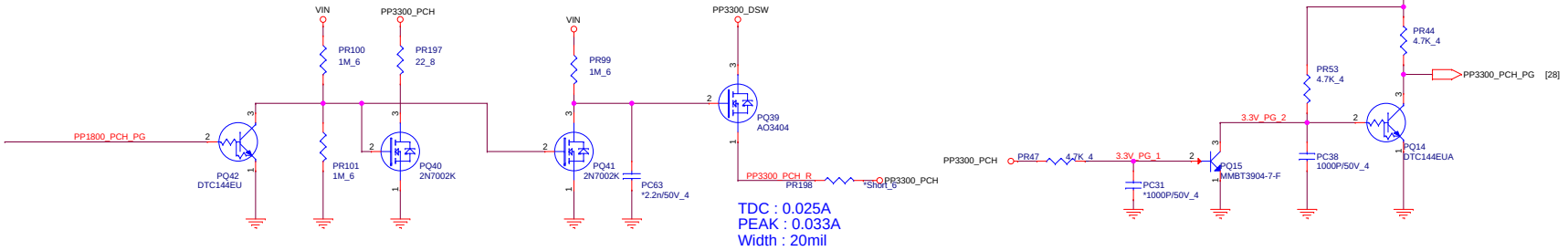
Size	Document Number	Rev
	LDO (1V/1.35V/1.5V/1.8V)	1A
Date: Tuesday, March 31, 2015	Sheet 35 of 41	

[35] PP1800_PCH_PG

[33] PP1000_PCH_S5_PG







Quanta Computer Inc.

PROJECT :

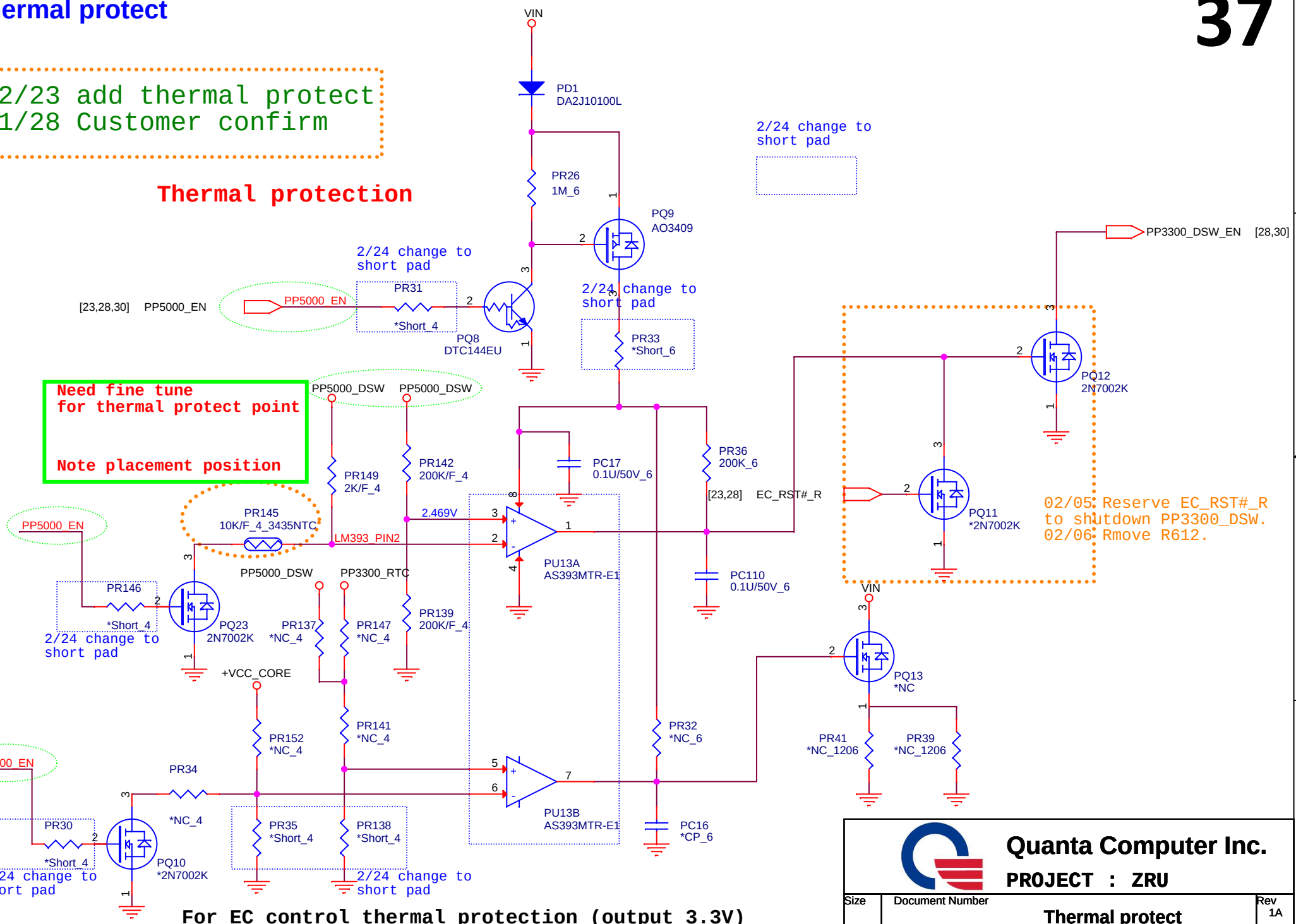
Size	Document Number	Rev
	LDO(1.2V/3.3V/1.8V)	1A

Date: Tuesday, March 31, 2015 Sheet 36 of 41

Thermal protect

12/23 add thermal protect
01/28 Customer confirm

Thermal protection



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZRU		
Size	Document Number: Thermal protect	Rev 1A
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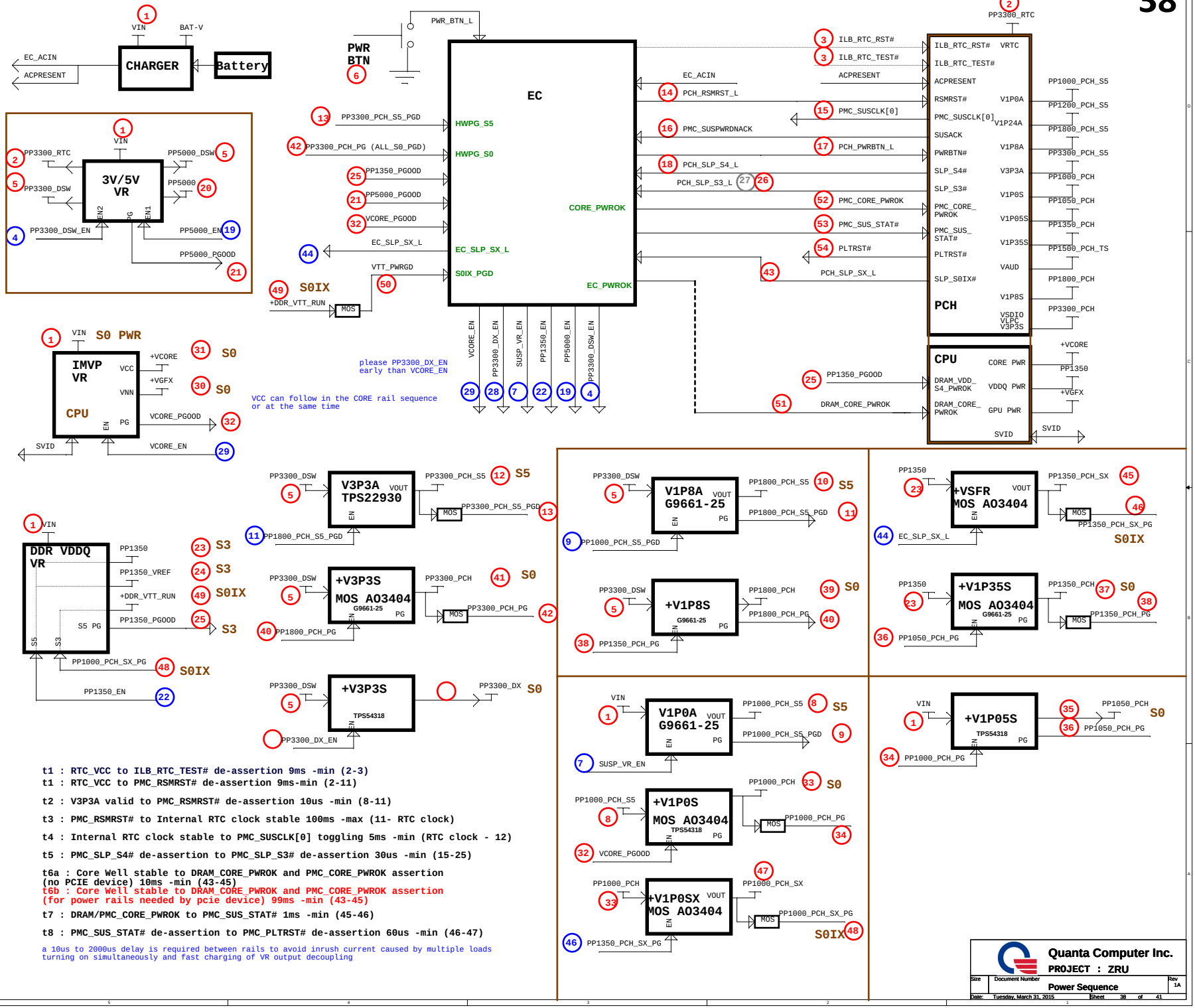
Support S0iX



t1 : RTC_VCC to ILB_RTC_TEST# de-assertion 9ms -min (2-3)
t1 : RTC_VCC to PMC_RSMRST# de-assertion 9ms-min (2-11)

t2 : V3P3A valid to PMC_RSMRST# de-assertion 10us -min (8-11)

t3 : PMC_RSMRST# to Internal RTC clock stable 100ms -max (11- RTC clock)

t4 : Internal RTC clock stable to PMC_SUSCLK[0] toggling 5ms -min (RTC clock - 12)

t5 : PMC_SLP_S4# de-assertion to PMC_SLP_S3# de-assertion 30us -min (15-25)

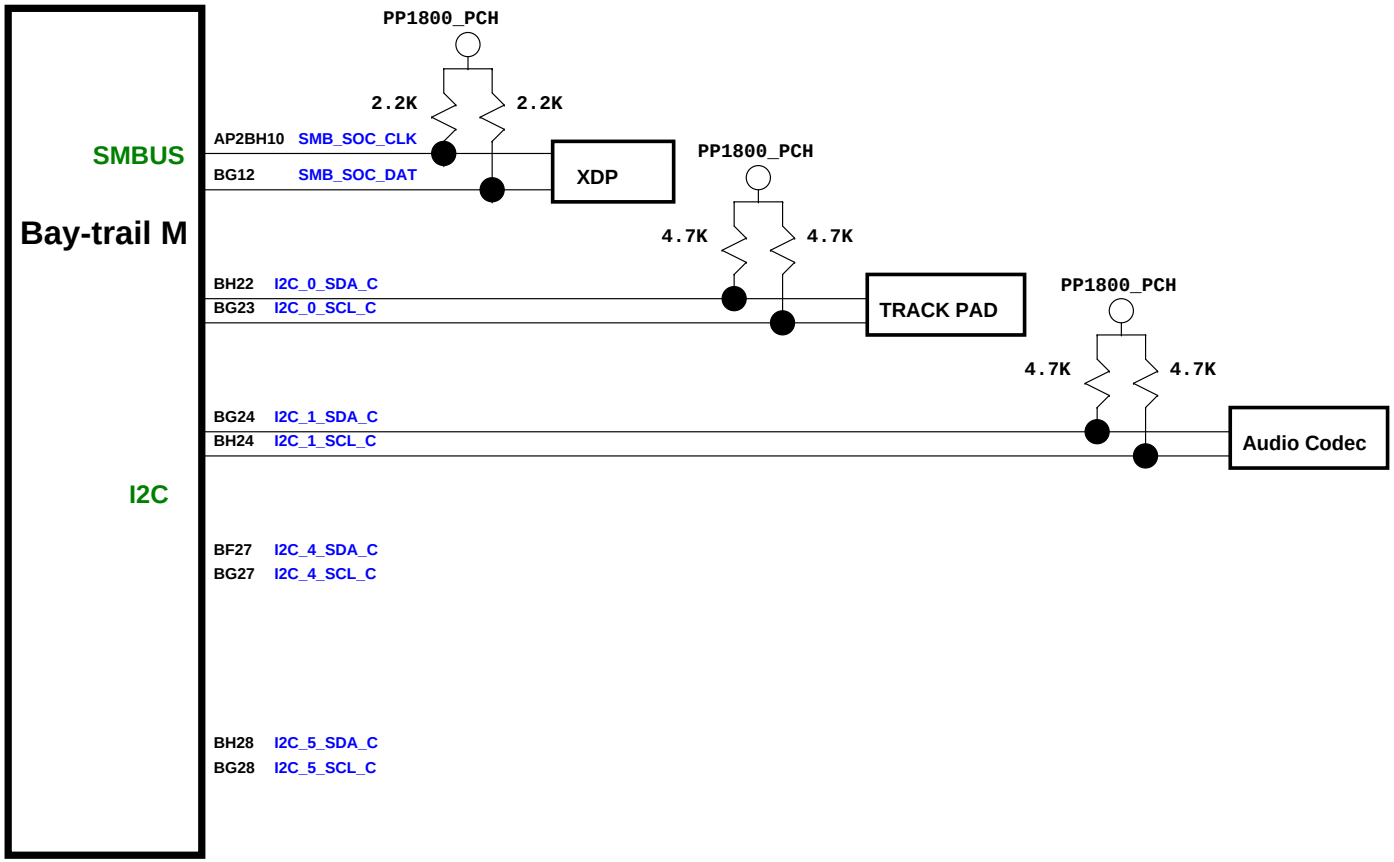
t6a : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (no PCIE device) 10ms -min (43-45)
t6b : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by pcie device) 99ms -min (43-45)

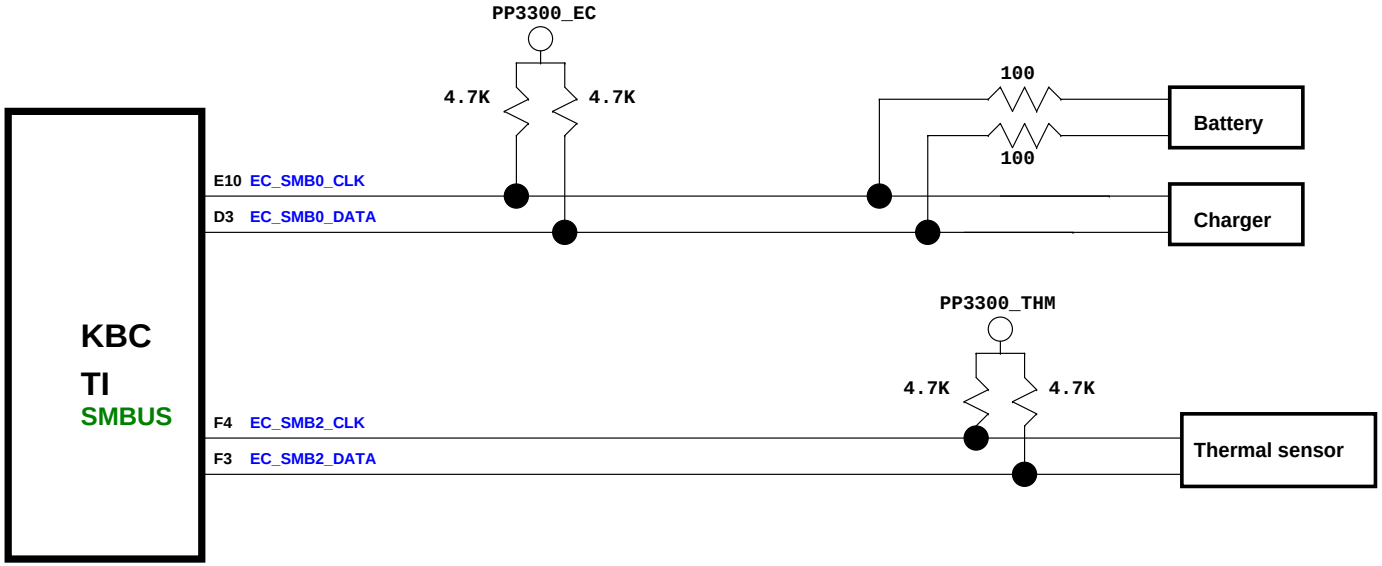
t7 : DRAM/PMC_CORE_PWROK to PMC_SUS_STAT# 1ms -min (45-46)

t8 : PMC_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion 60us -min (46-47)

a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling

Quanta Computer Inc.			
PROJECT : ZRU			
Size	Document Number	Power Sequence	Rev 1A
Date: Tuesday, March 31, 2015		Sheet 38 of 41	





Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	SMBUS_I2C	1A

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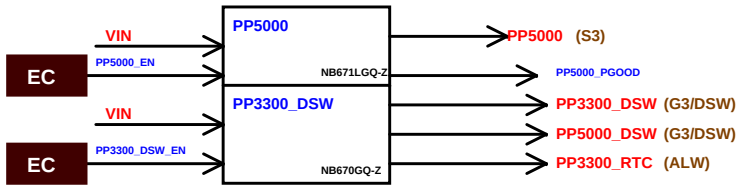
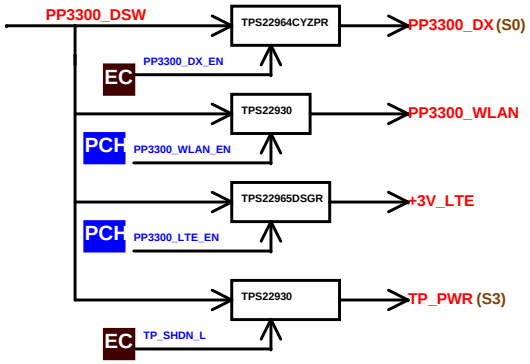
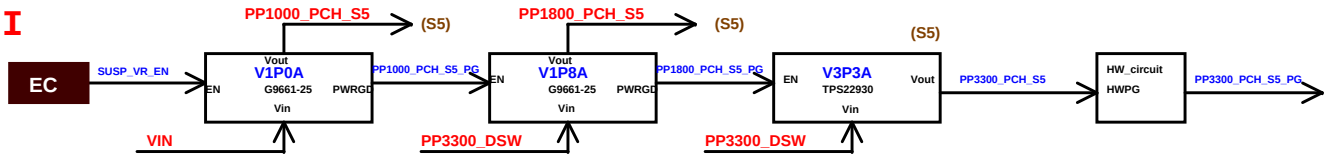
I

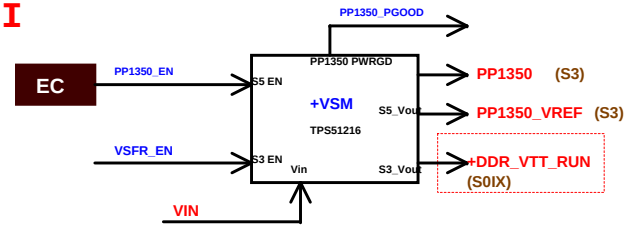


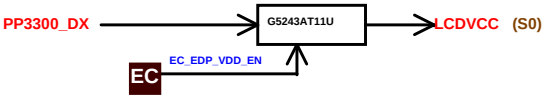


II

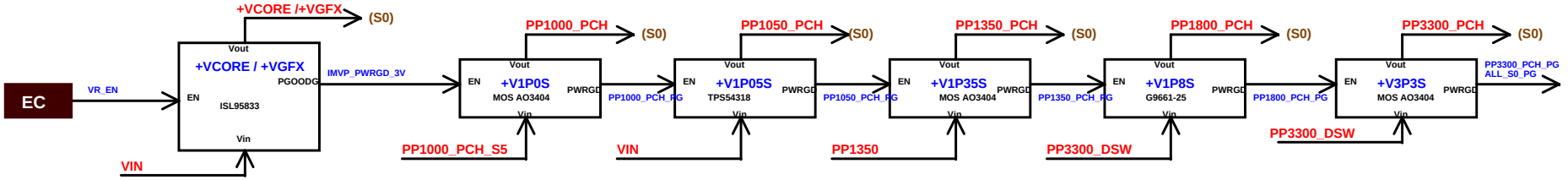


III

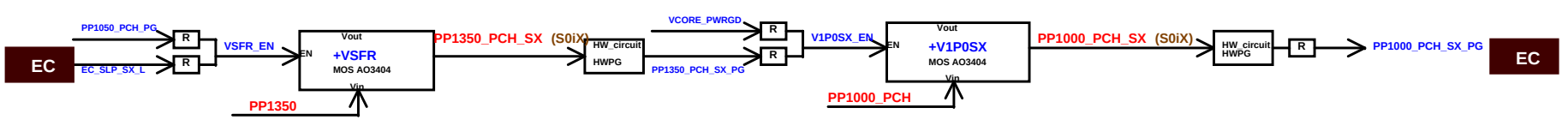


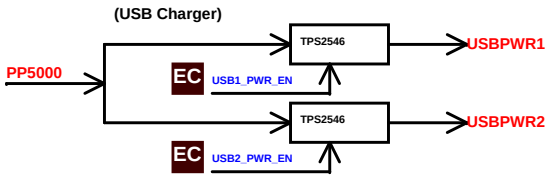


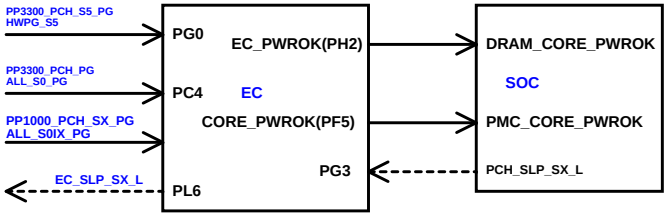
IV



V







Quanta Computer Inc.
PROJECT : ZRU

Size	Document Number	Rev
	BTM PWR CONTROL	1A

Date: Tuesday, March 31, 2015 Sheet 40 of 41

Model	Version	CHANGE LIST 41
	1A	
	3A	150224: Add USB2PWR on CN12.5 and add GND on CN12.4--page23 150224: Stuff R147,R419,R424,R414 for EMI--page19 150224: Change R97,R90 to short pad--page17 150224: Change R181 to short pad--page20 150224: Change R141,R155 to short pad--page21 150224: Change C283 to 1000pF and Add C357 for EMI--page19 150224: Change L4 to short pad--page27 150224: Remove L14 and change R496,R488 to short pad--page23 150224: Remove L6 and change R430,R431 to short pad--page17 150224: Remove L9,L7 and change R466,R464,R463,R459 to short pad--page26 150225: Change PR1,PR3,PR19,PR20,PR24,PR29,PR30,PR31,PR35,PR49,PR51,PR54,PR59,PR61,PR62,PR65,PR81,PR93,PR95,PR98,PR109,PR115,PR116,PR118, PR122,PR128,PR138,PR146,PR169,PR186,PR189,PR193,PR199,PR200,PR201,PR212,PR155,PR181 to short pad 150225: Change PR8,PR18,PR27,PR33,PR48,PR55,PR73,PR76,PR79,PR80,PR85,PR110,PR111,PR124,PR126,PR153,PR156,PR171,PR188,PR196,PR198,PR213,PR224 to short pad 150225: Change PR92 to short pad 150225: Change JP1,JP2,JP3,JP4,JP5,JP6,JP7,JP8,JP9,JP10,JP11,JP12 to short pad 150225: Un-Stuff PU1,PU3,PU14,PU17,PU20 150225: Un-Stuff PC5,PC7,PC12,PC14,PC139,PC141,PC153,PC160,PC195,PC197 150225: Remove R496,R488--page23 150226: Change PC112,PC126 to CH61001ME96--page34 150226: Update HOLE9,HOLE10,HOLE7 footprint--page26
	3A	150310: Chnage R119 to 10ohm by ESD --page17 150310: Chnage R293 to 33ohm by ESD--page27 150310: ChnageC17,C43,C87,C93,C96,C97,C98,C99,C101 to 4.7uF--page10 150324: Add Hole12 by ME add ESD pad.--page26 150324:Change D18,D19,D20,D21,D22,D23 to P/N BCPJSD05Z06 by ESD issue. --page26

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	Quanta Computer Inc. PROJECT : ZIIU
	PART NUMBER:		DRAWING BY:		REVISON:	Change list-1 1A