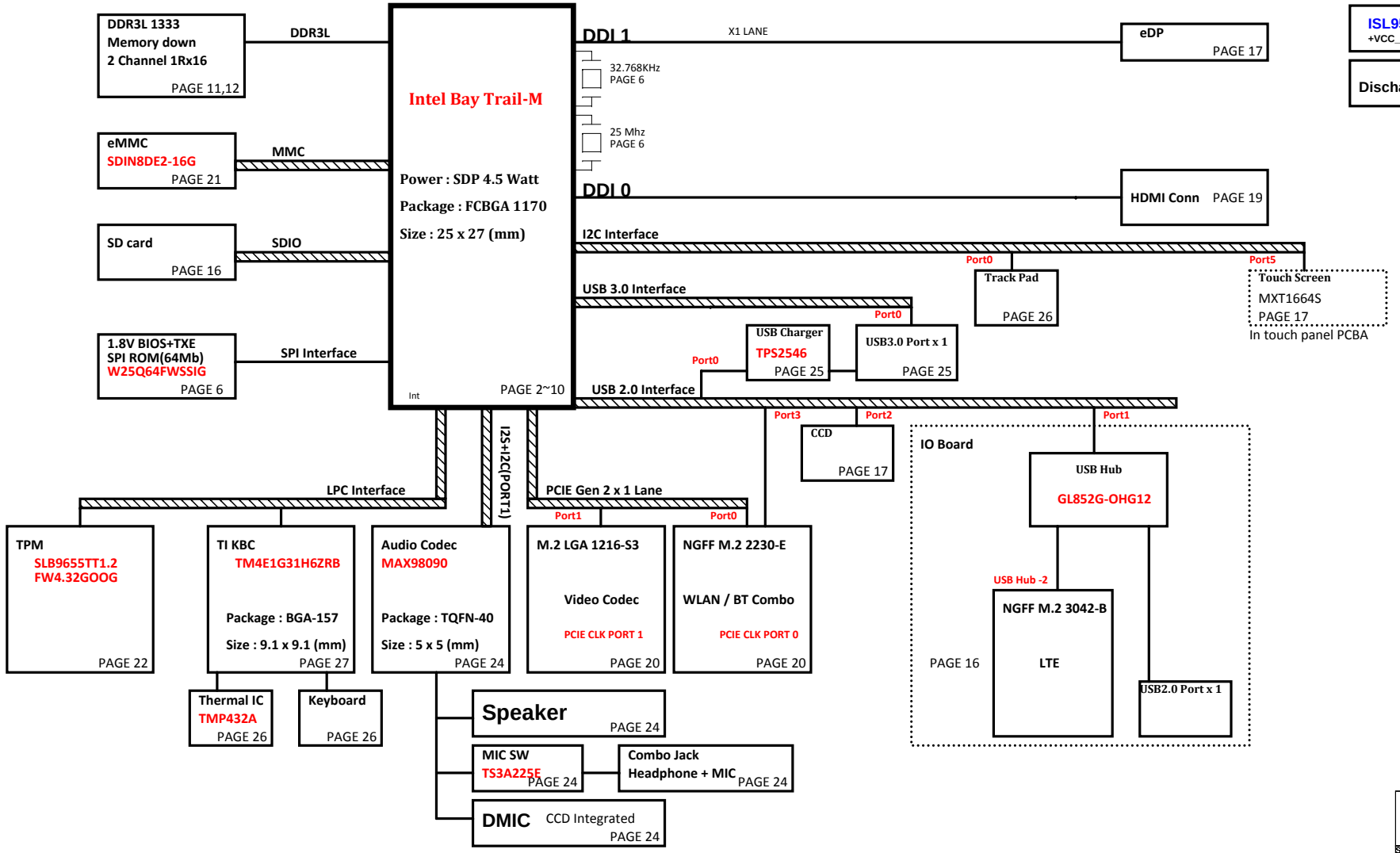
ZM8/Candy
Intel Bay Trail-M Platform Block Diagram

01

EVT
AJSR1YJUT07--CPU(1170P)N2840 2.16G SR1YJ(FCBGA)WINBSQ



BQ24715 Batery Charger	TPS51216 PP1350
NB670/NB671 PP3300_DSW/PP5000	TLV62150ARGTR PP1050_PCH
ISL95833HRTZ-T +VCC_CORE/+VCC_GFX	TLV62130ARGTR PP1000_PCH_S5
Discharger	

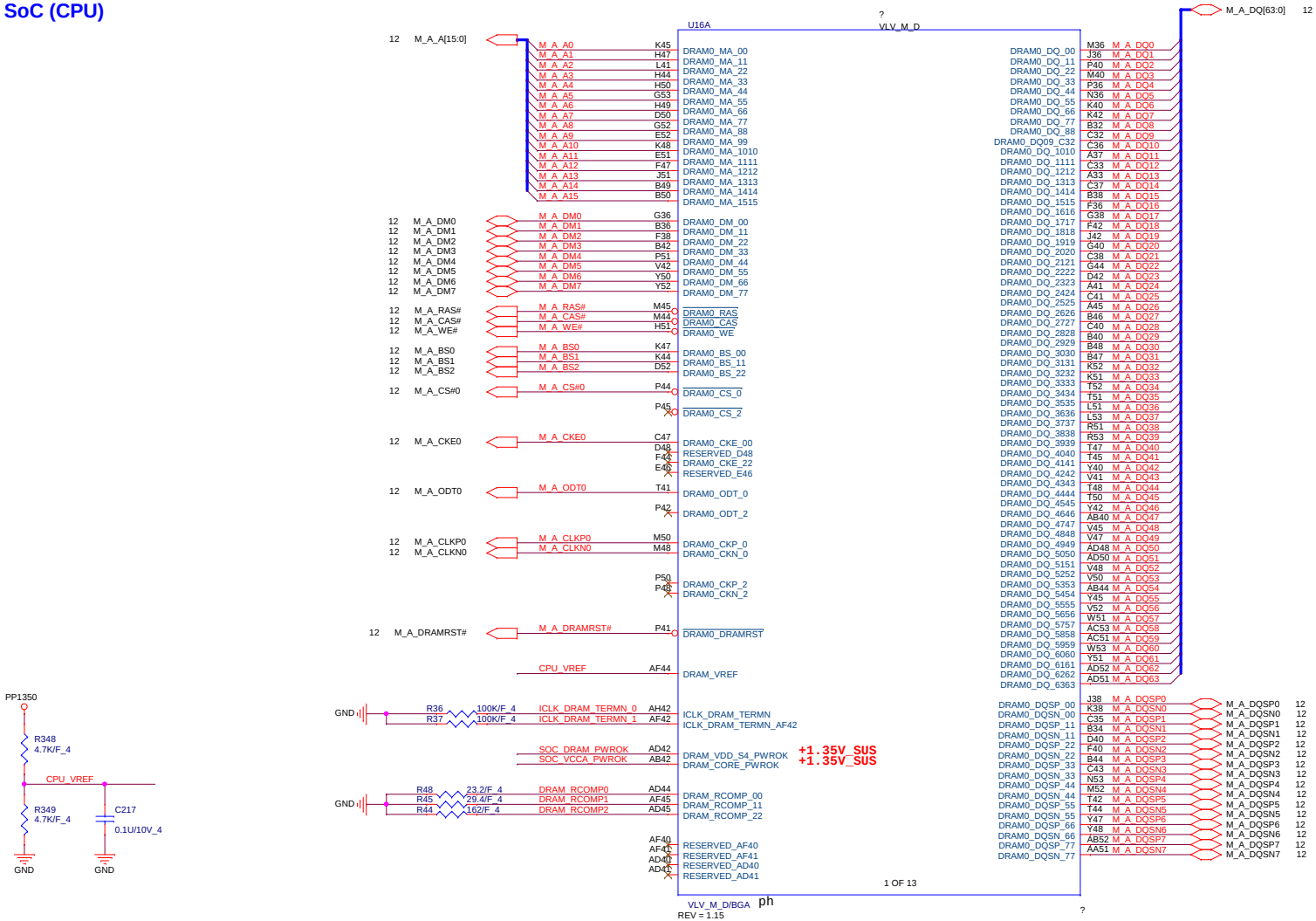
BOM value option:
CHB@-==>DDR Single channel or dual channel
EDP@ =>4 Lane eDP
TS@ =>Touch screen
SX@ => S0IX
NSX@=> Non S0ix
VC@ =>Video codec
LTE@ => LTE
GD@ =>Google debug

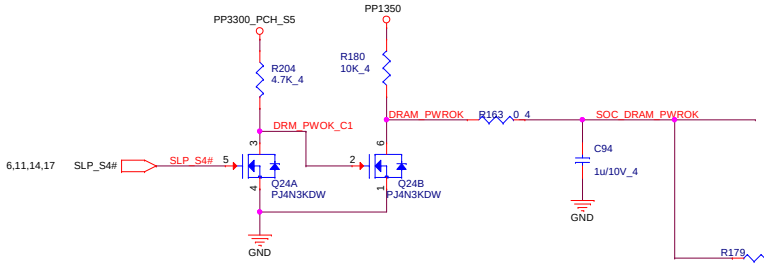
Quanta Computer Inc.
PROJECT : ZM8

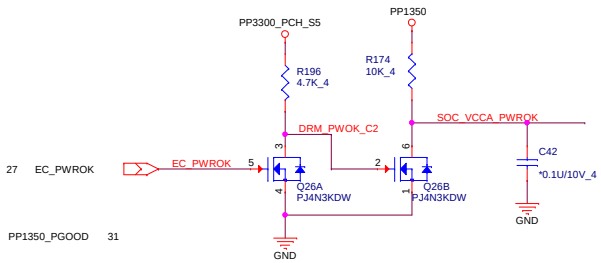
Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Thursday, September 25, 2014 Sheet 1 of 39

SoC (CPU)



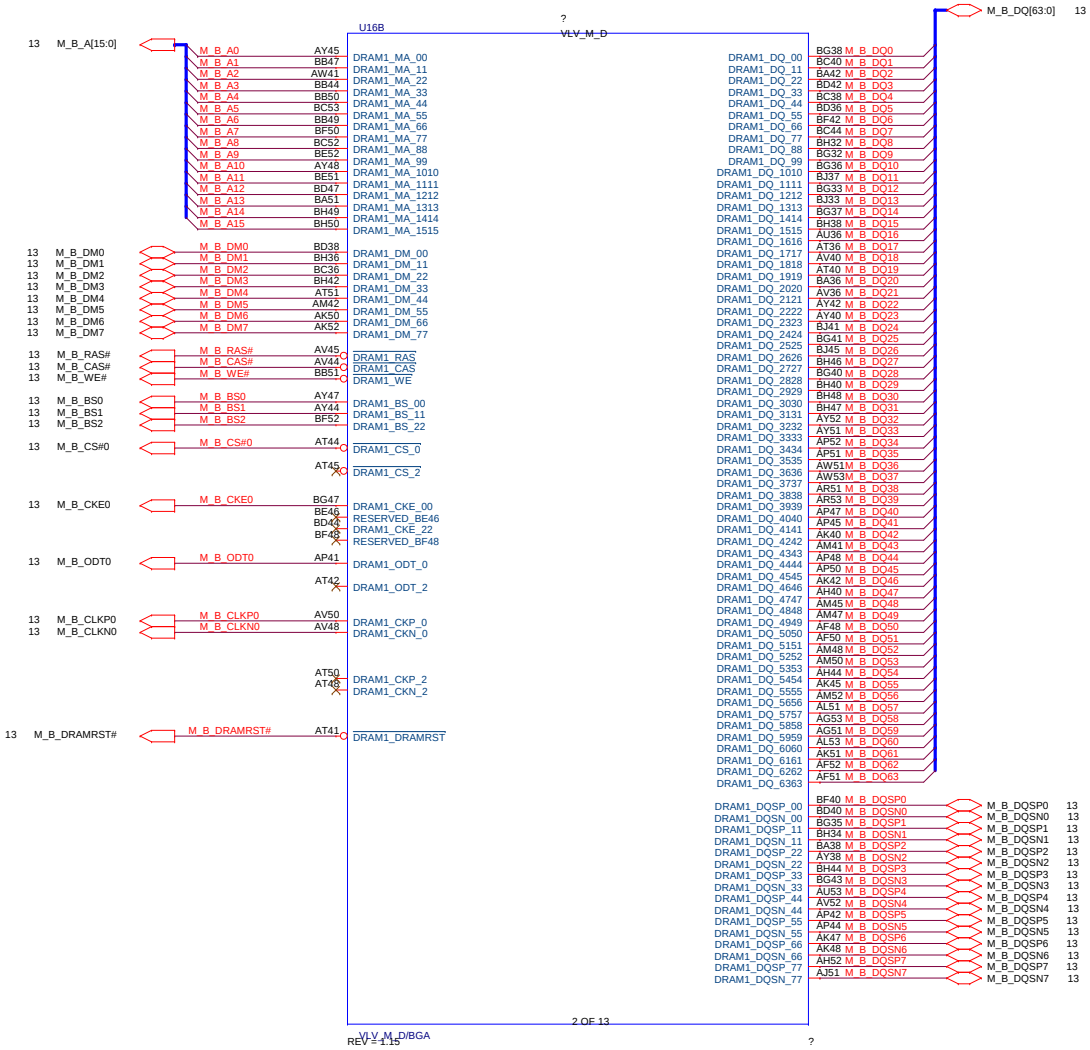




Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A
Date: Thursday, September 25, 2014	Sheet 2 of 39	

SoC (CPU)

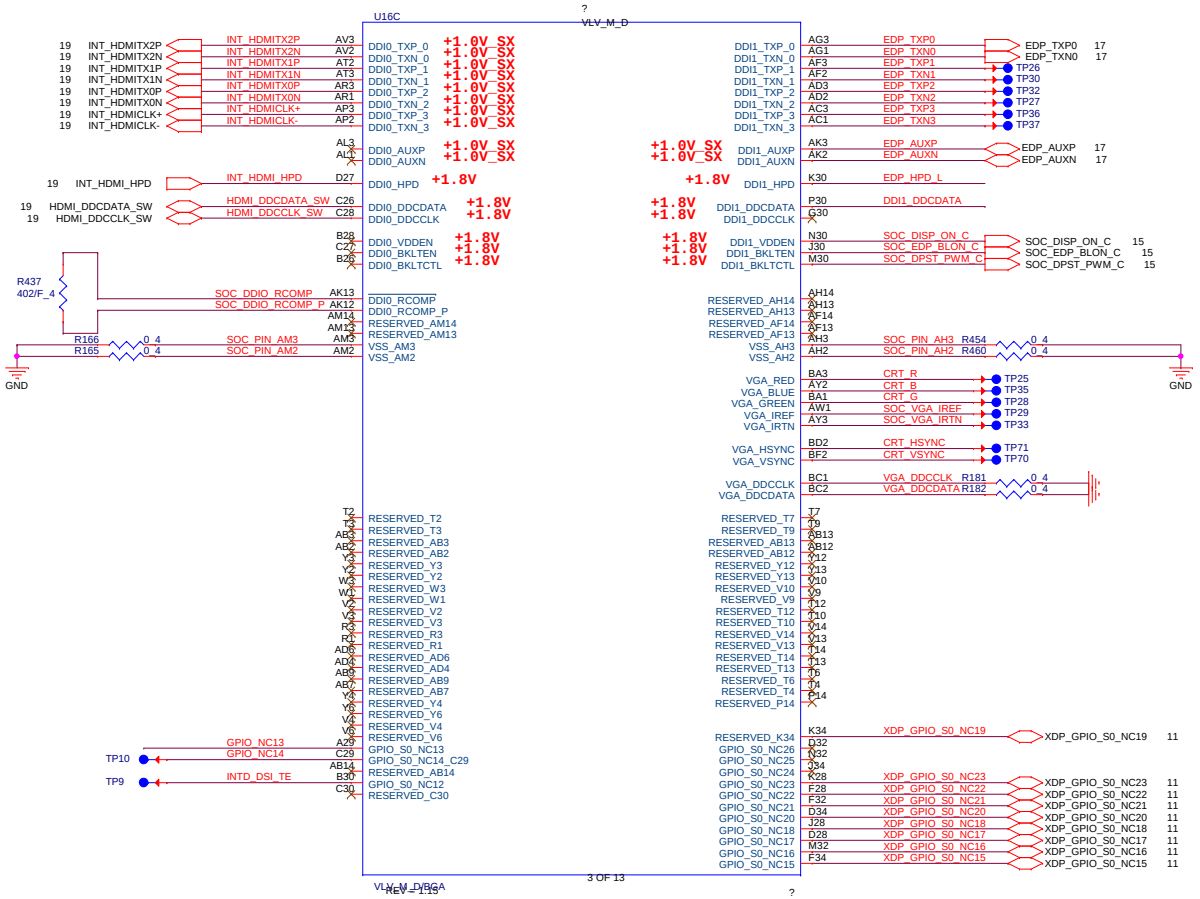


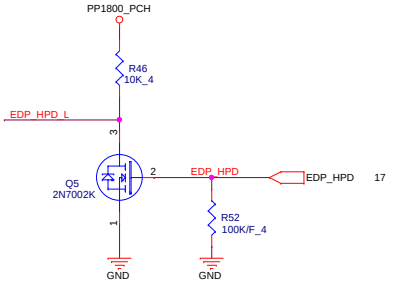
Quanta Computer Inc.

PROJECT : ZM8

Size	Document Number	Rev
	Valley 2/9 (DDRB)	1A

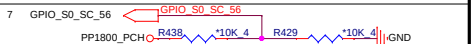
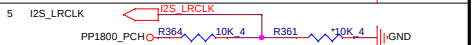
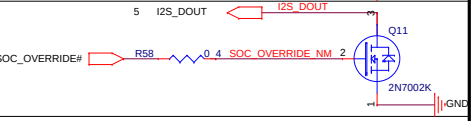
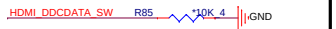
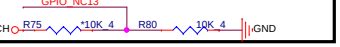
Date: Thursday, September 25, 2014 Sheet 3 of 39



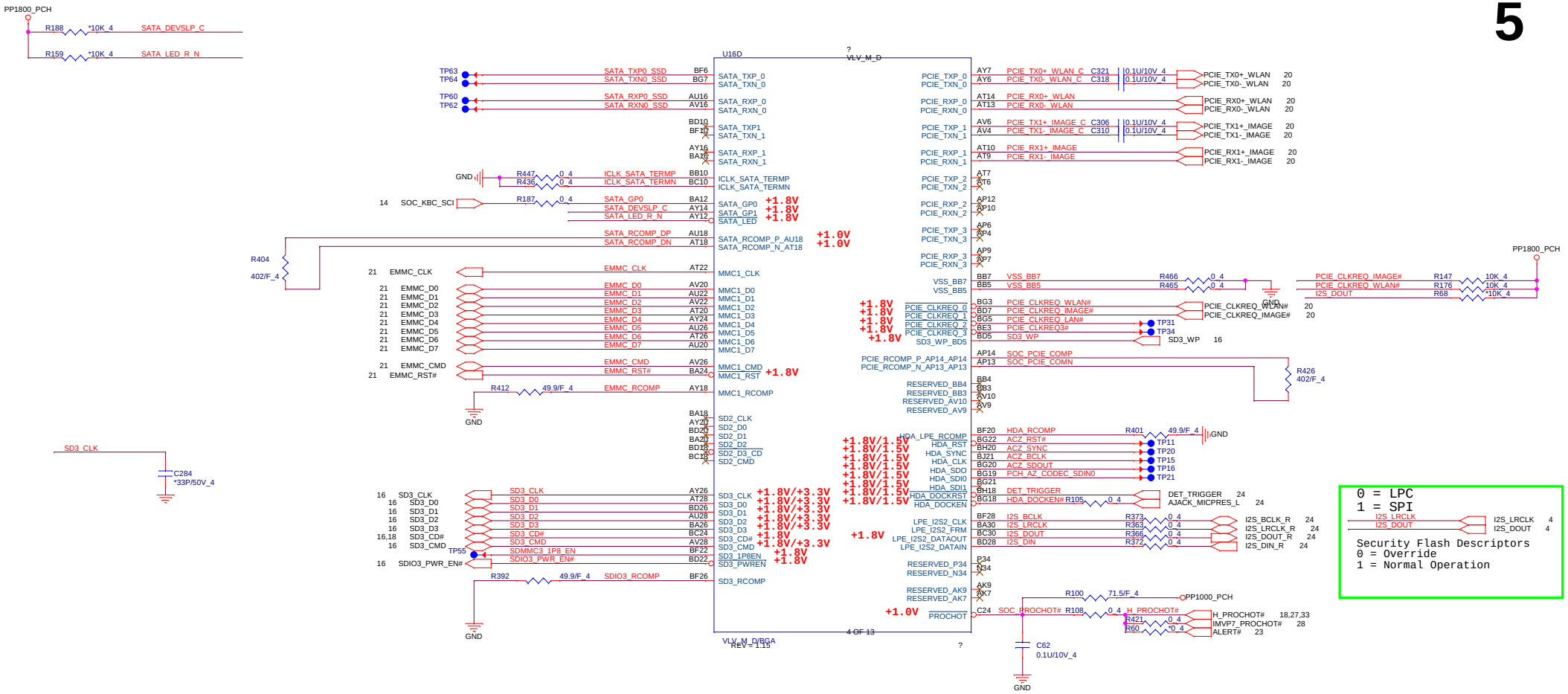


HPD output high
SOC active Low

BTM Strapping Table

Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is inverted 1 = Top address bit is unchanged	
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC **1 = SPI**	
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override **1 = Normal operation**	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	Pull up +1.8V at HDMI side 
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected **1 = DDI0 detected**	
GPIO_SO_NC_13				

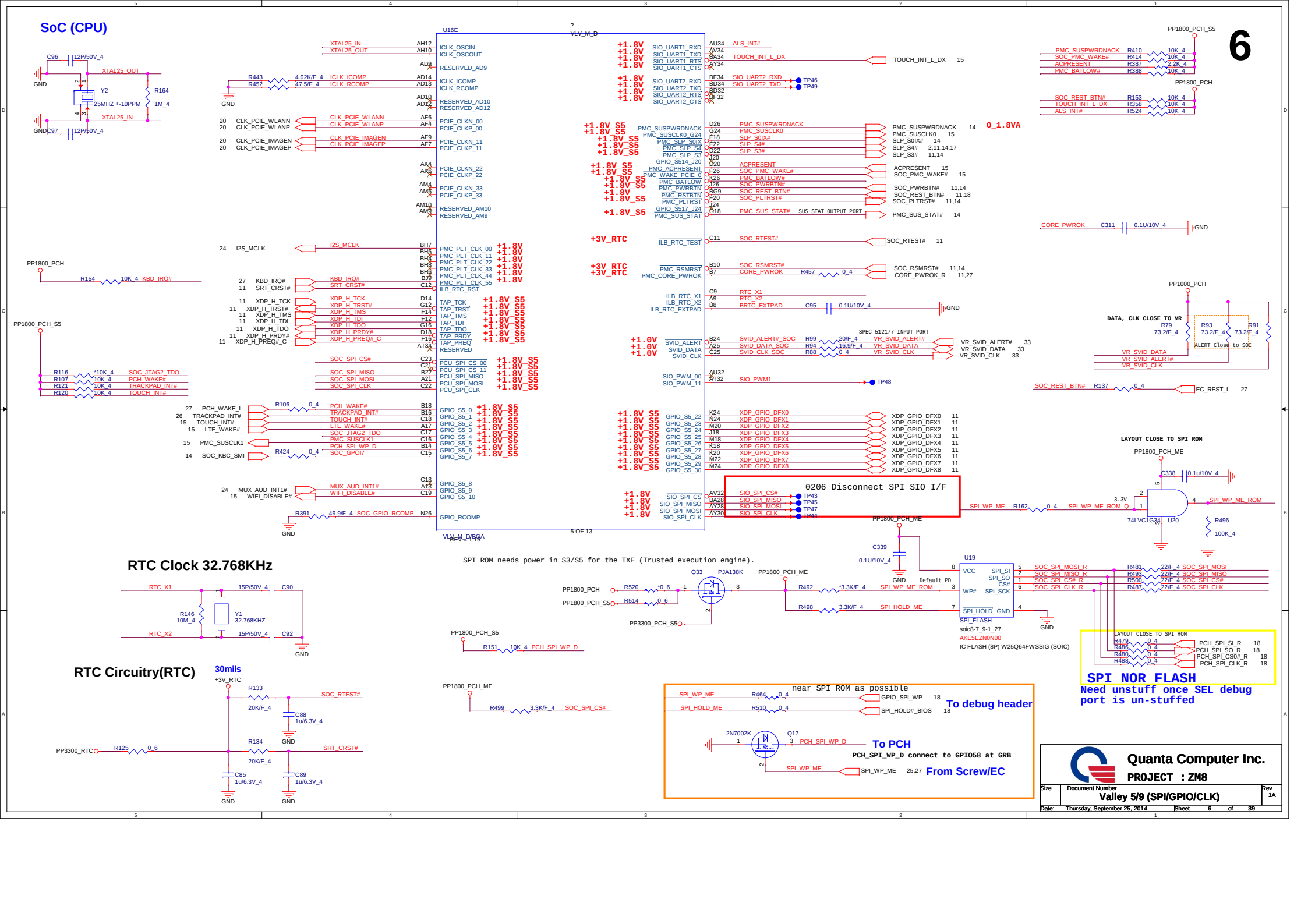
SoC (CPU)



5

Quanta Computer Inc.	
PROJECT : ZM8	
Size	Document Number: Valley 4/9 (SD/PCIE/SATA)
Rev	1A
Date: Thursday, September 25, 2014	Sheet 5 of 39

SoC (CPU)



RTC Clock 32.768KHz

RTC Circuitry(RTC)

SPI ROM needs power in S3/S5 for the TXE (Trusted execution engine).

SPI NOR FLASH

Need unstuff once SEL debug port is un-stuffed

0206 Disconnect SPI SIO I/F

DATA, CLK CLOSE TO VR

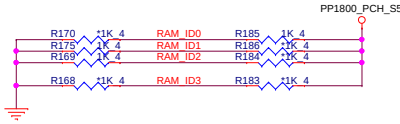
SPEC 512177 INPUT PORT

LAYOUT CLOSE TO SPI ROM

Quanta Computer Inc.	
PROJECT : ZM8	
Size	Document Number: Valley 5/9 (SPI/GPIO/CLK) — Rev: 1A
Date: Thursday, September 25, 2014	Sheet 6 of 39

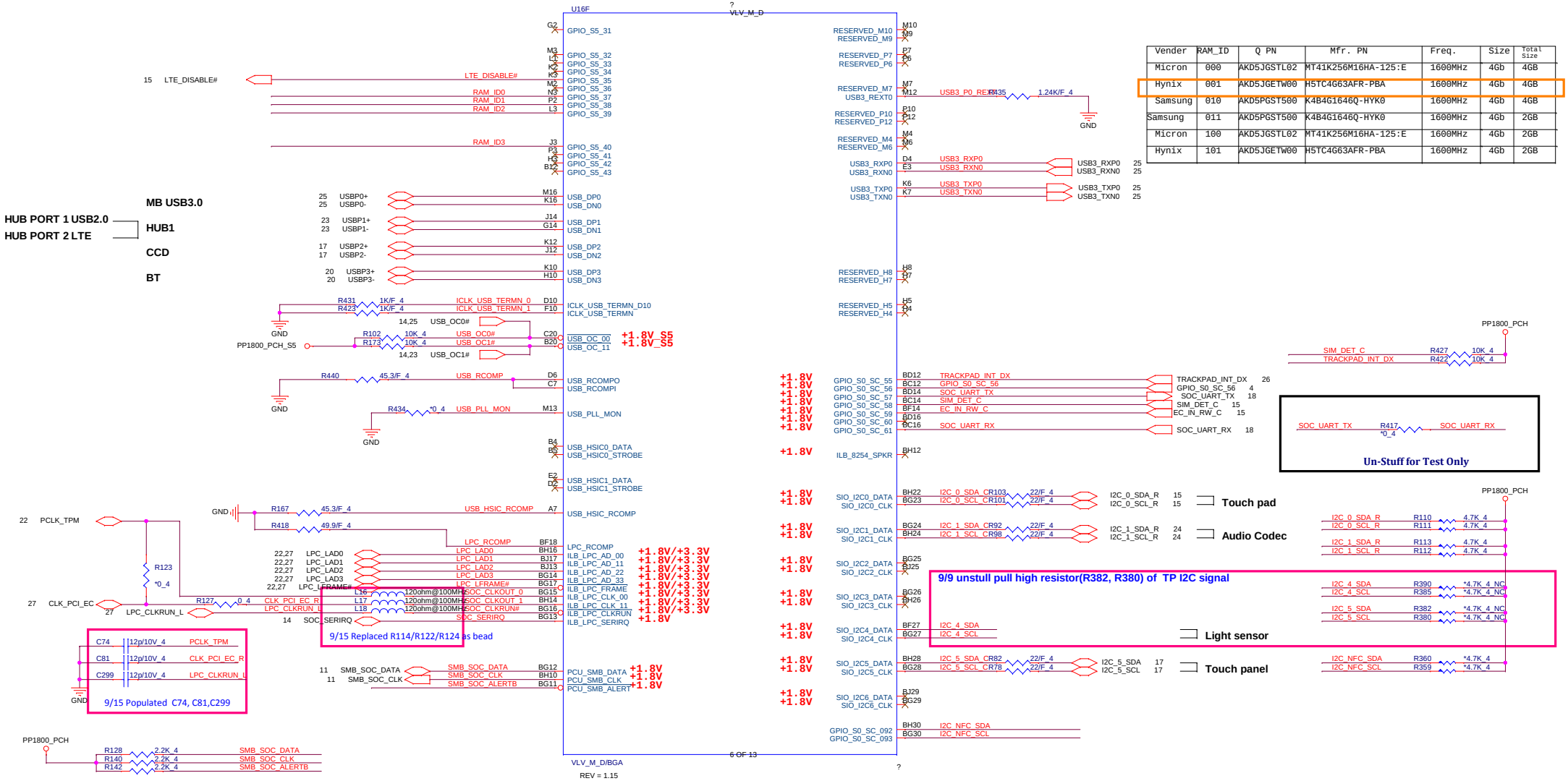
SoC (CPU)

RAM ID



7

Vender	RAM_ID	Q PN	Mfr. PN	Freq.	Size	Total Size
Micron	000	AKD5JGSTL02	MT41K256M16HA-125:E	1600MHz	4Gb	4GB
Hynix	001	AKD5JGETW00	H5TC4G63AFR-PBA	1600MHz	4Gb	4GB
Samsung	010	AKD5PGST500	K4B4G1646Q-HYK0	1600MHz	4Gb	4GB
Samsung	011	AKD5PGST500	K4B4G1646Q-HYK0	1600MHz	4Gb	2GB
Micron	100	AKD5JGSTL02	MT41K256M16HA-125:E	1600MHz	4Gb	2GB
Hynix	101	AKD5JGETW00	H5TC4G63AFR-PBA	1600MHz	4Gb	2GB



Touch pad

Audio Codec

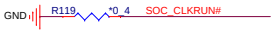
9/9 unstull pull high resistor(R382, R380) of TP I2C signal

Light sensor

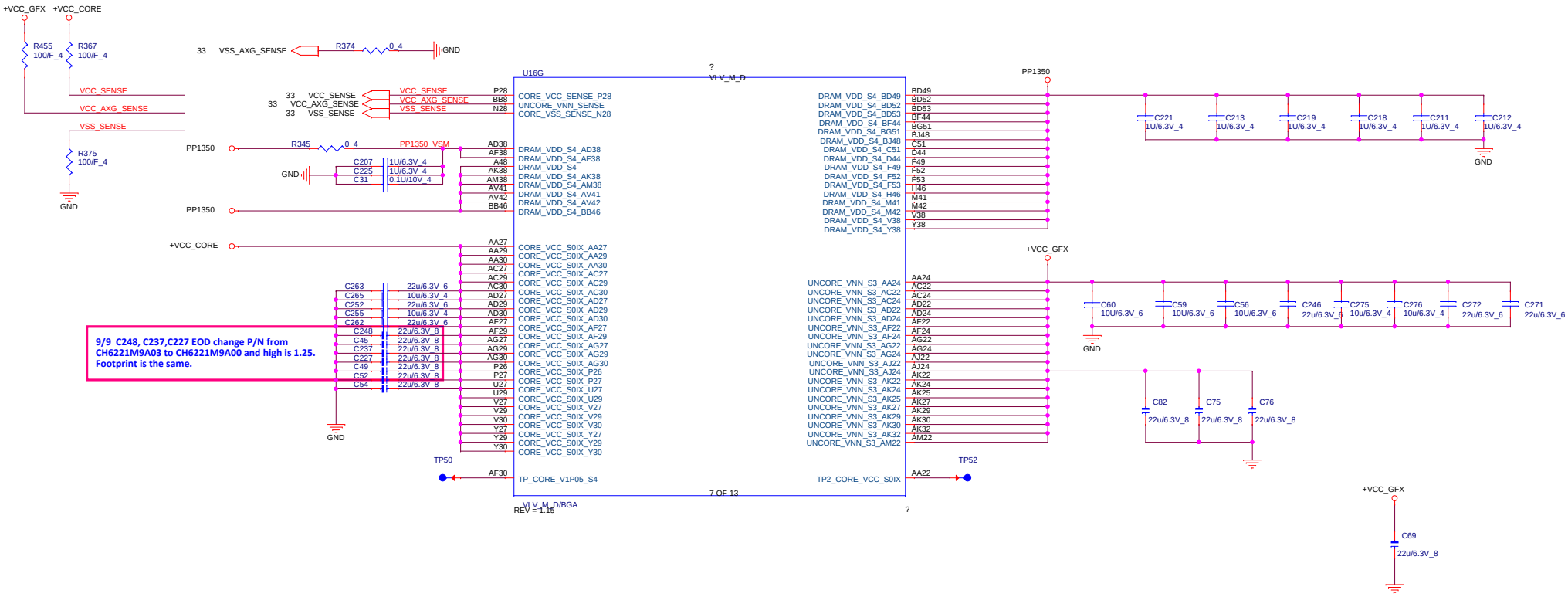
Touch panel

9/15 Replaced R114/R122/R124 as bead

9/15 Populated C74, C81,C299

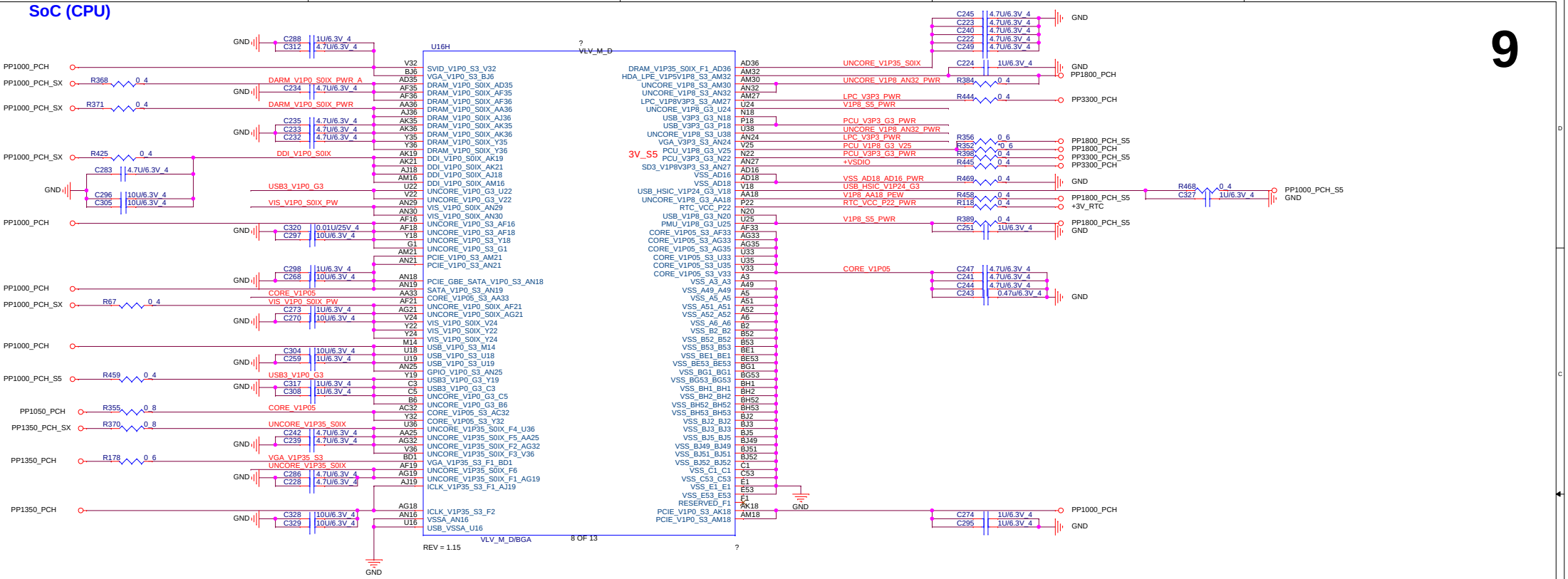


Quanta Computer Inc.			
PROJECT : ZM8			
Size	Document Number		Rev
	Valley 6/9 (USB/LPC/I2C)		1A
Date: Thursday, September 25, 2014		Sheet 7 of 39	

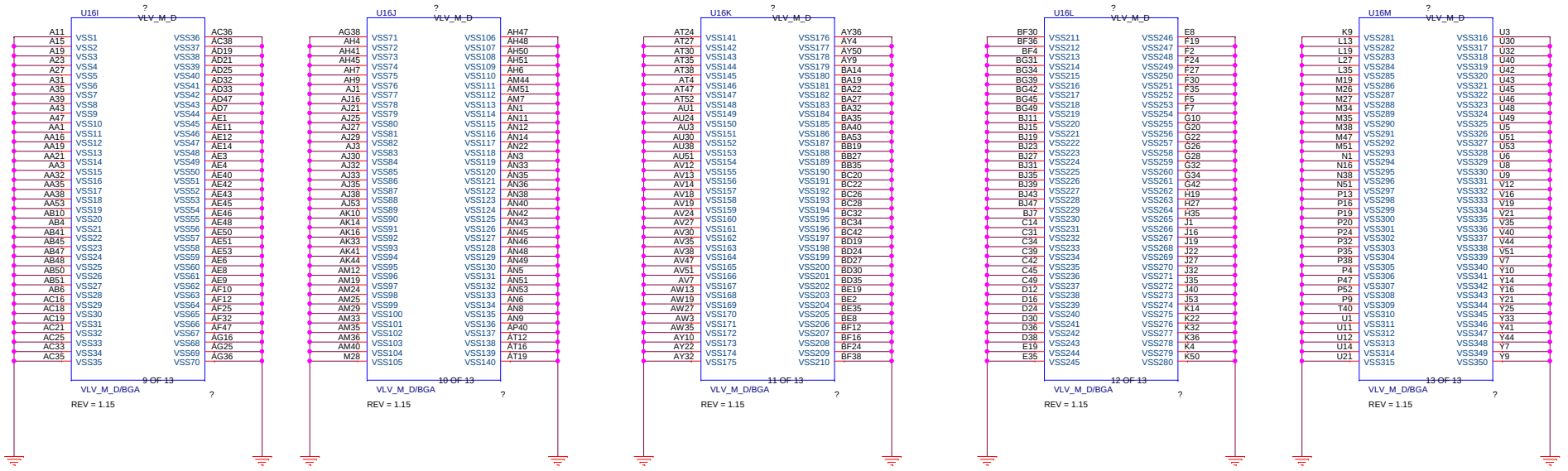


Quanta Computer Inc.		
PROJECT : ZM8		
Size	Document Number: Valley 7/9 (Power 1)	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 8 of 39	

SoC (CPU)



Quanta Computer Inc.	
PROJECT : ZM8	
Size	Document Number: Valley 8/9 (Power 2) — Rev: 1A
Date: Thursday, September 25, 2014	Sheet 9 of 39



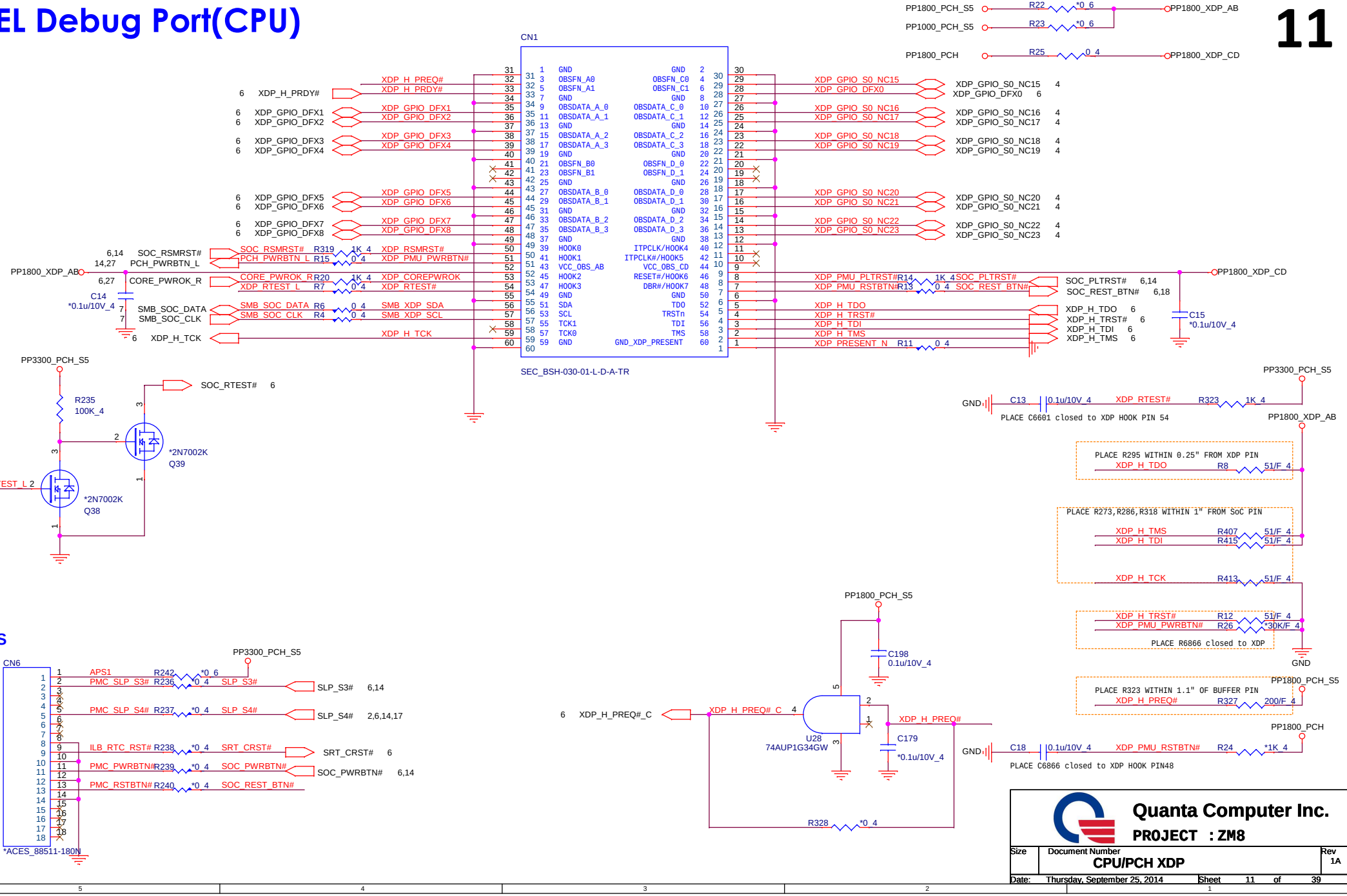
Quanta Computer Inc.

PROJECT : ZM8

Size	Document Number	Rev
	Valley 9/9 (GND)	1A

Date: Thursday, September 25, 2014 Sheet 10 of 39

INTEL Debug Port(CPU)



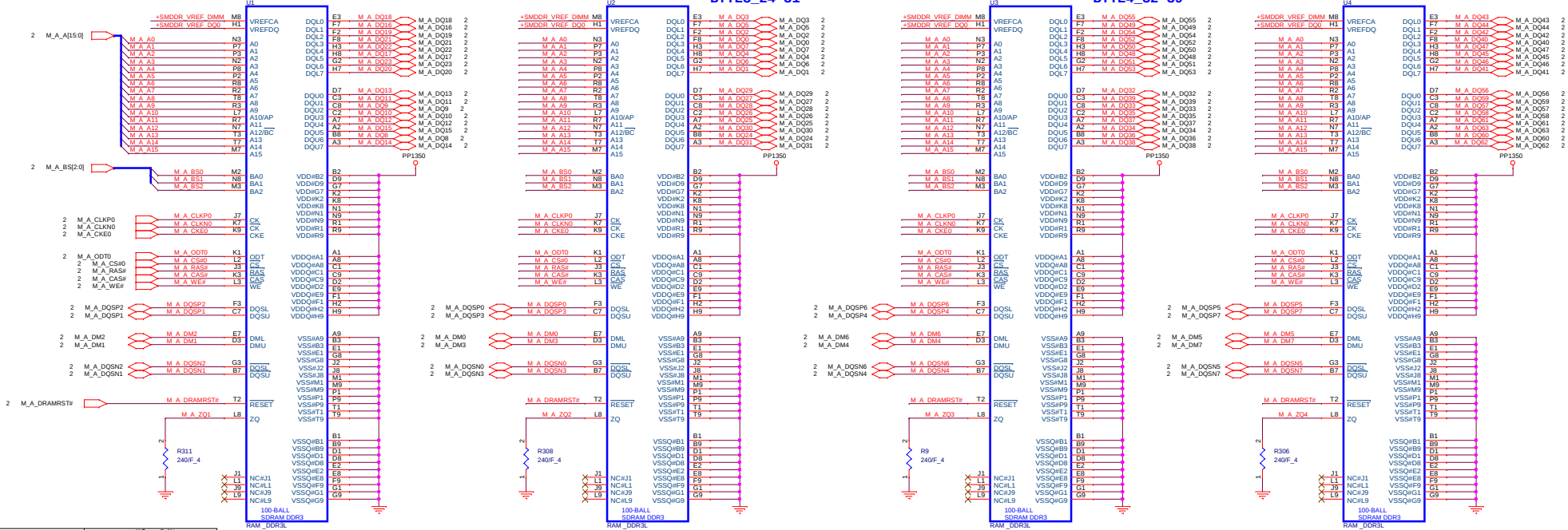
APS

Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	CPU/PCH XDP	1A
Date: Thursday, September 25, 2014	Sheet 11 of 39	

On board memory (OBM)

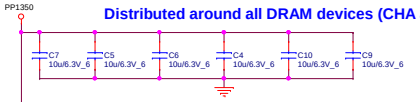
BYTE2_16-23
BYTE1_8-15
BYTE0_0-7
BYTE3_24-31
BYTE6_48-55
BYTE4_32-39
BYTE5_40-47
BYTE7_56-63



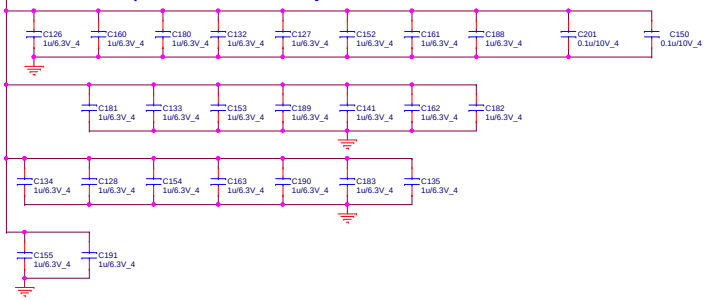
Hynix AKD5JGETW00--H5TC4G63AFR-PBA

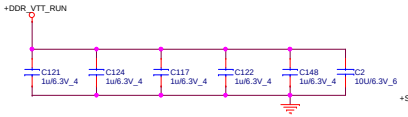
Vendor	P/N	Mfr. P/N
Hynix	AKD5JGETW15 (WIN BSQ)	H5TC4G63AFR-PBA
Micron	AKD5JGSTL15 (WIN BSQ)	MT41K256M16HA-125:E
Samsung	AKD5PGST516 (WIN BSQ)	K4B4G1646Q-HYK0

Distributed around all DRAM devices (CHA and CHB)

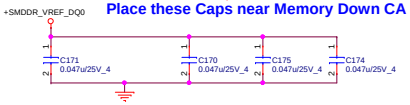


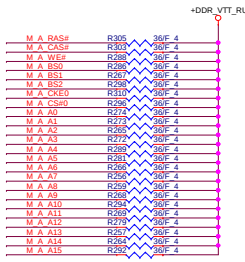
Place these Caps near each X16 Memory Down

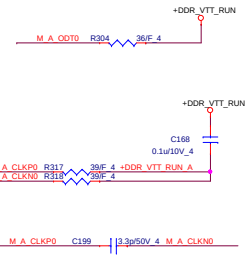




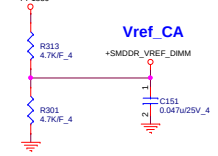
Place these Caps near Memory Down CA & DQ pin



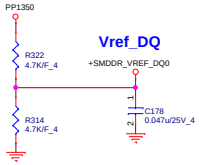




M1 solution



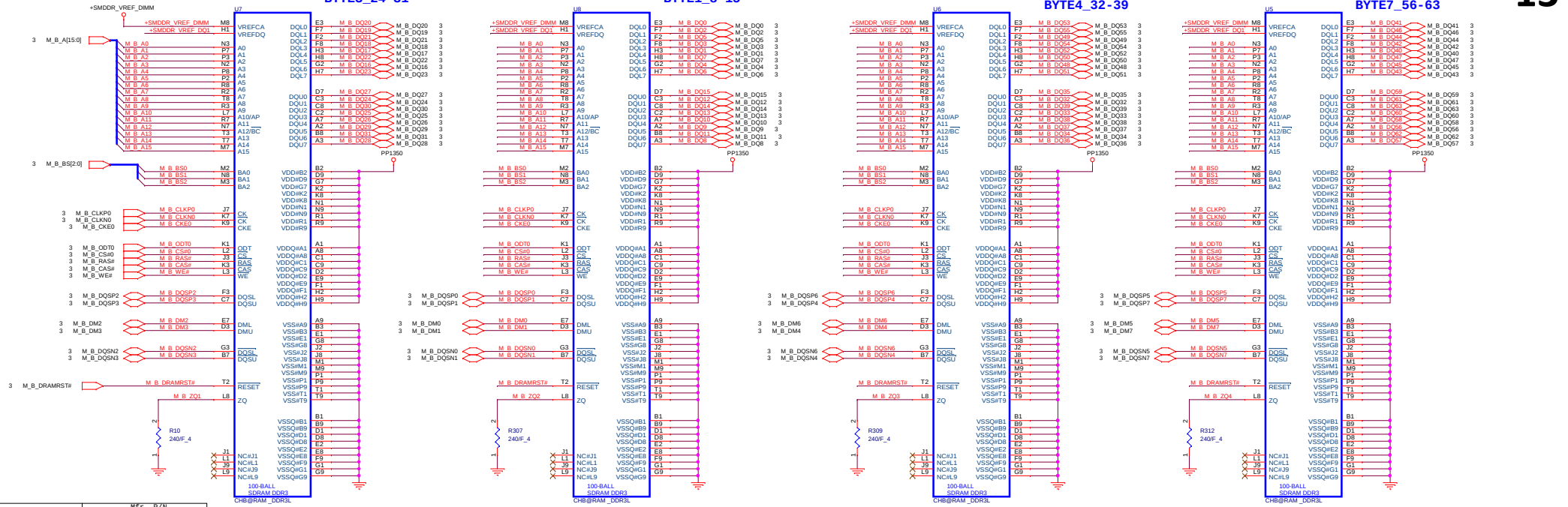
M1 solution



Quanta Computer Inc. PROJECT : ZM8			
Size	Document Number	DDR3L MEMORY DOWNx16 A	Rev 1A
Date: Thursday, September 25, 2014	Sheet 12 of 39		

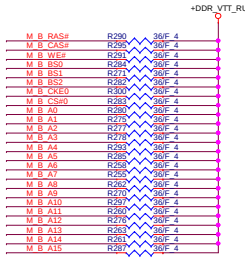
On board memory (OBM)

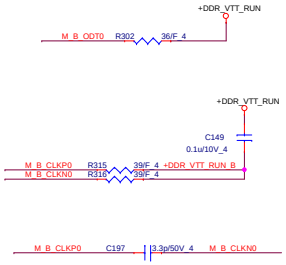
BYTE2_16-23
BYTE3_24-31
BYTE0_0-7
BYTE1_8-15
BYTE6_48-55
BYTE4_32-39
BYTE5_40-47
BYTE7_56-63

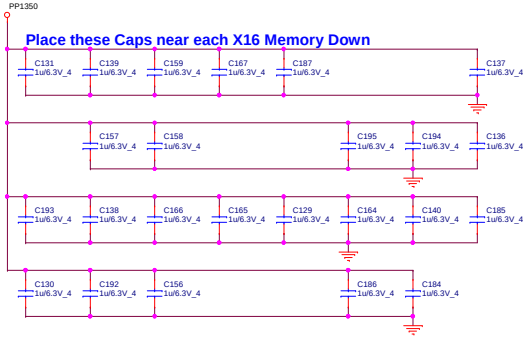


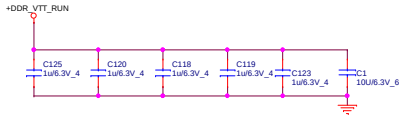
Hynix AKD5JGETW00--H5TC4G63AFR-PBA

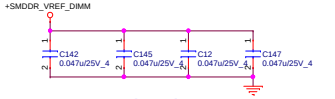
Vendor	P/N	Mfr. P/N
Hynix	AKD5JGETW15 (WIN BSQ)	H5TC4G63AFR-PBA
Micron	AKD5JGSTL15 (WIN BSQ)	MT41K256M16HA-125:E
Samsung	AKD5PGST516 (WIN BSQ)	K4B4G1646Q-HYK0

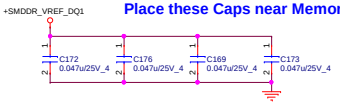






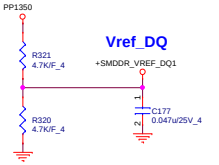






Place these Caps near Memory Down CA & DQ pin

M1 solution

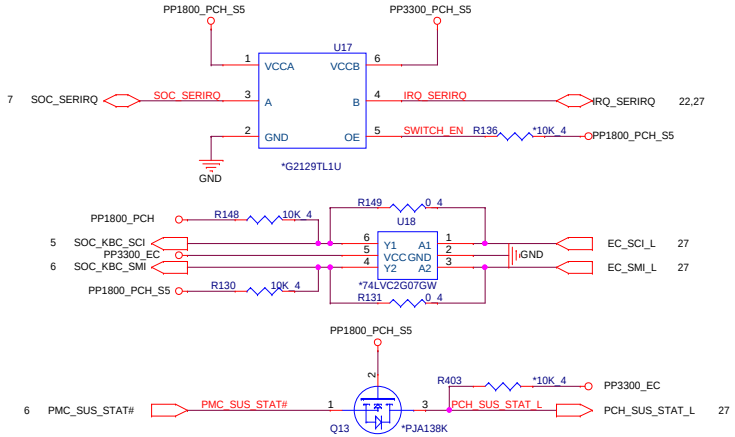


Quanta Computer Inc.
PROJECT : ZM8

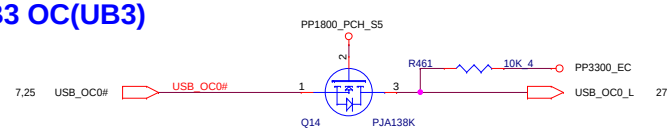
Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 B	1A

Date: Thursday, September 25, 2014 Sheet 13 of 39

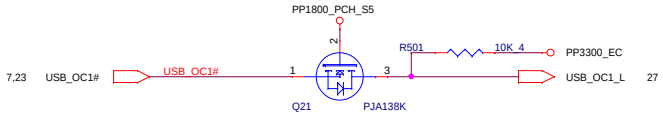
PWRON SEQUENCE(CPU)



USB3 OC(UB3)

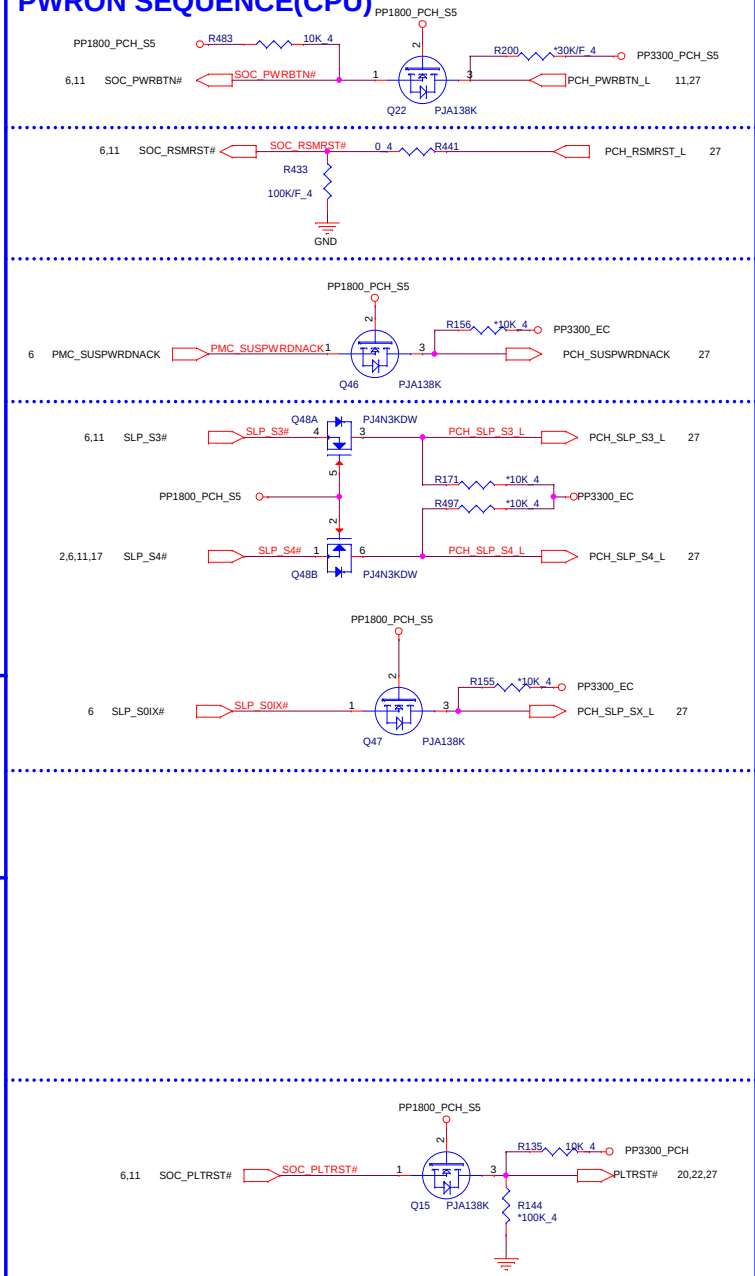


USB2 OC(UB2)



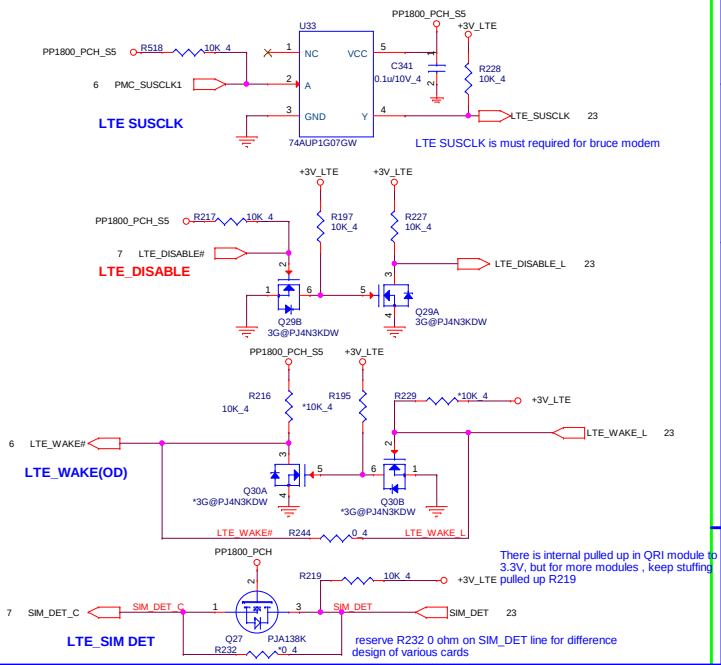
Stuffing for notifying EC

PWRON SEQUENCE(CPU)

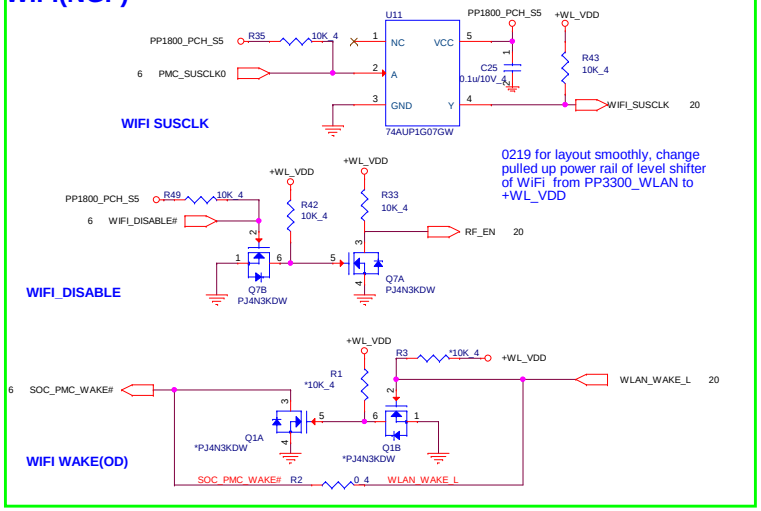


Quanta Computer Inc.		
PROJECT : ZM8		
Size	Document Number: Level Shfiter (SOC_EC)	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 14 of 39	

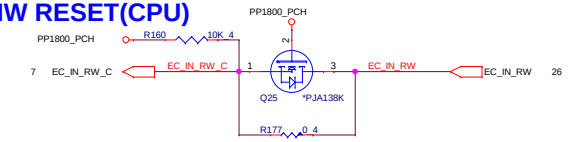
LTE(MNC)



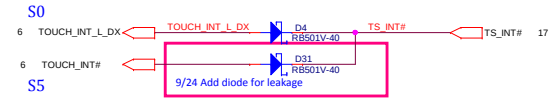
WIFI(NGF)



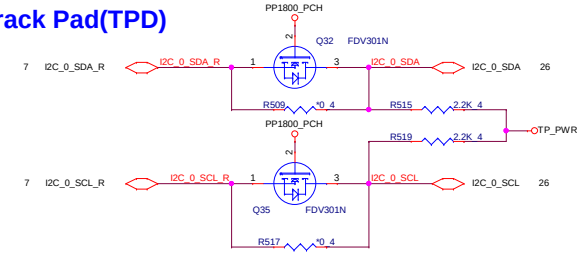
HW RESET(CPU)



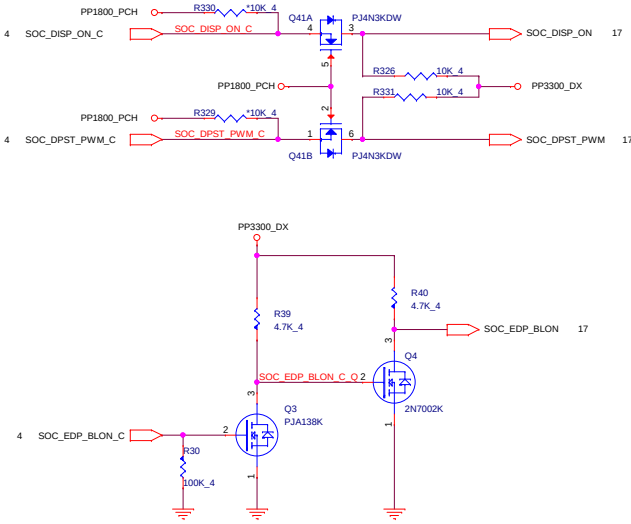
Touch Screen(TSN)



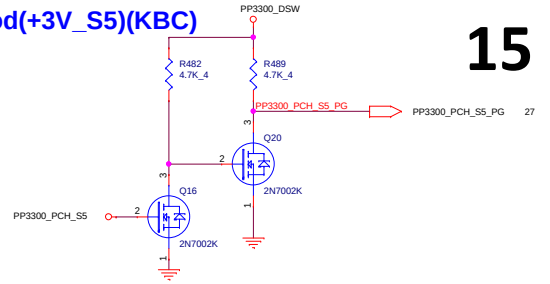
Track Pad(TPD)



eDP control pin(LDS)

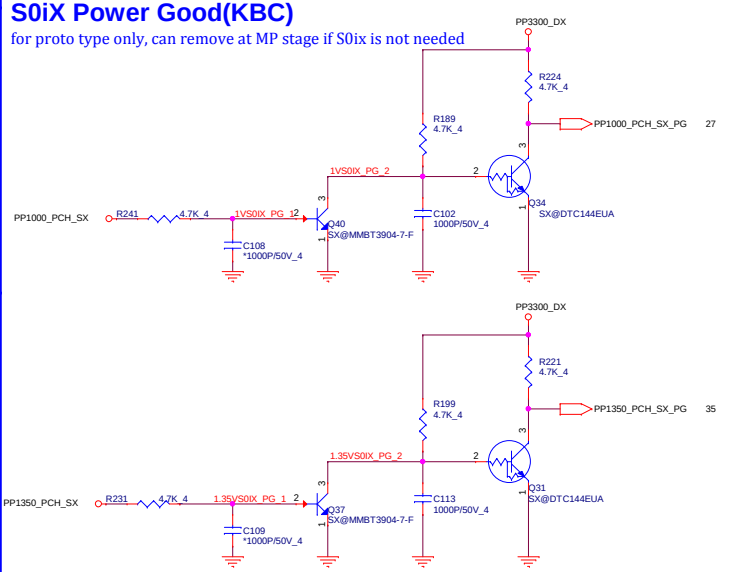


S5 Power Good(+3V_S5)(KBC)

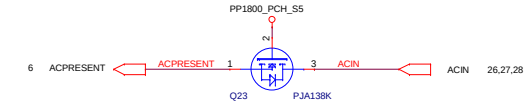


S0iX Power Good(KBC)

for proto type only, can remove at MP stage if S0ix is not needed



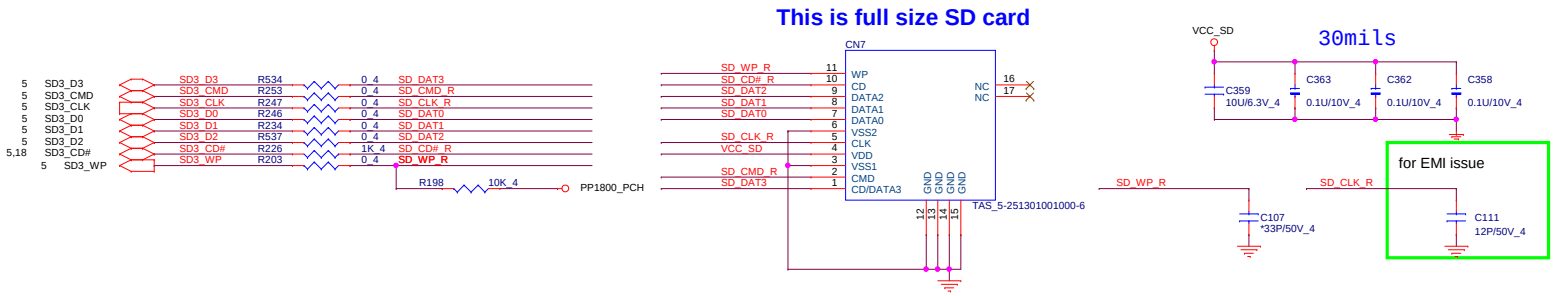
AC Detect(CPU)

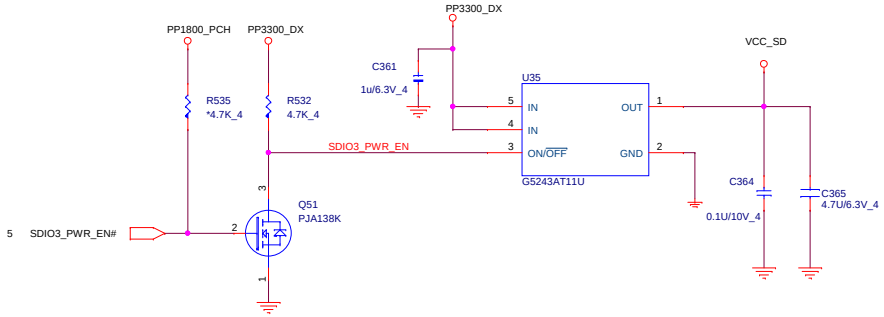


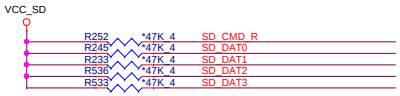
Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	Level Shfiter (SOC_DEV)	1A
Date: Thursday, September 25, 2014	Sheet 15 of 39	

SD/MMC CARD READER CONNECTOR (CRD)

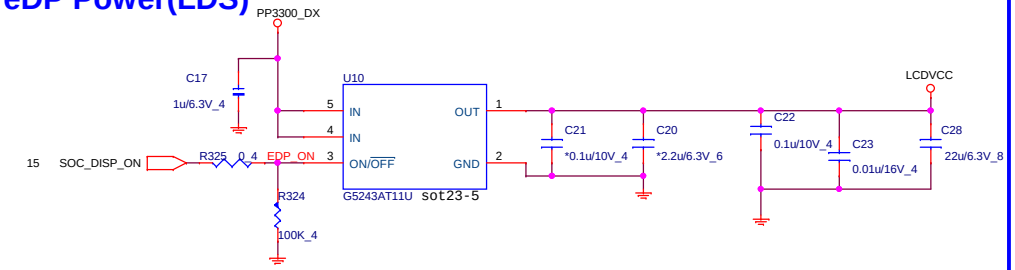




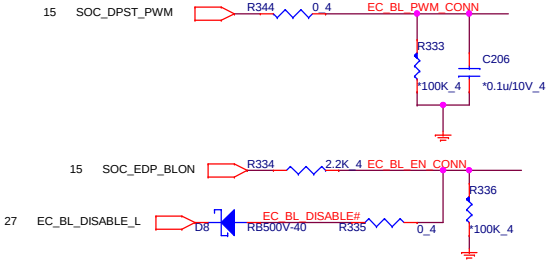


Quanta Computer Inc.			
PROJECT : ZM8			
Size	Document Number		Rev
	SDIO CardReader		1A
Date: Thursday, September 25, 2014		Sheet 16 of 39	

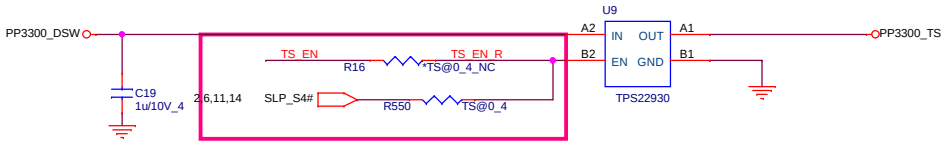
eDP Power(LDS)



eDP panel control(LDS)

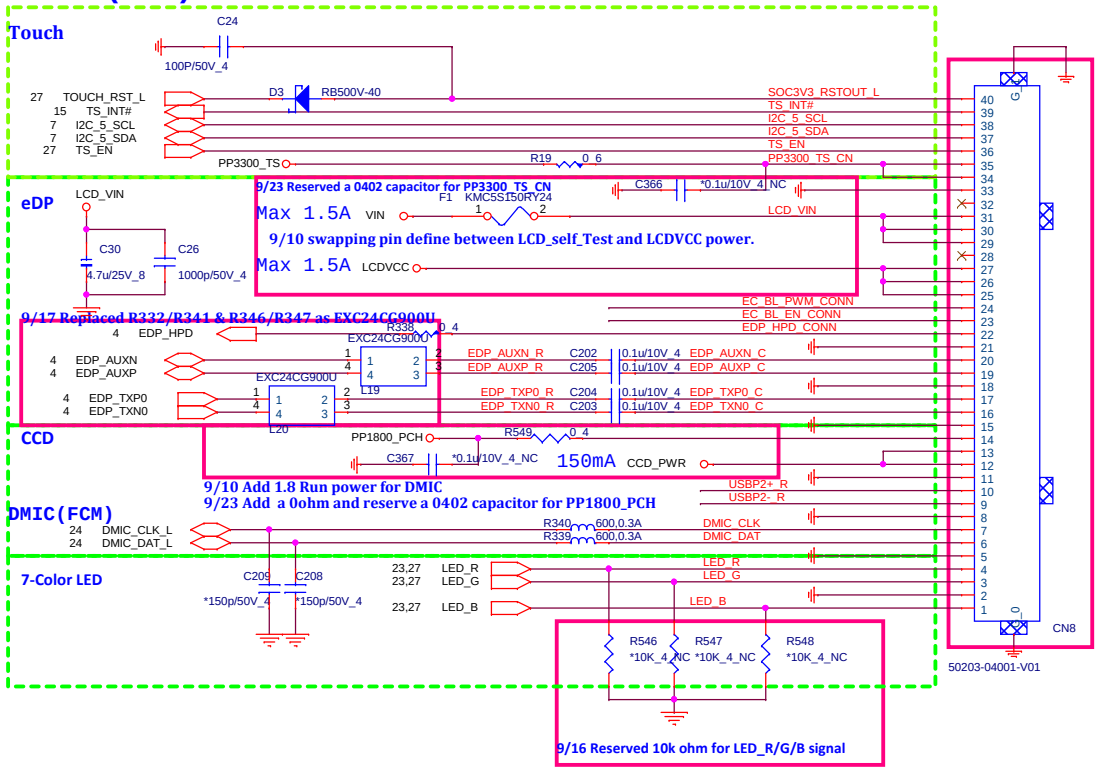


Touch Screen(TSN)

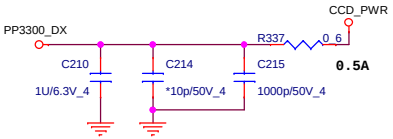


9/23 For touch screen sequence request, used S4# to enable PP3300_TS

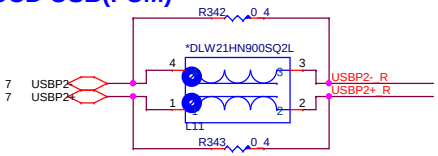
eDP(LDS)



CCD power(FCM)



CCD USB(FCM)



Quanta Computer Inc.		
PROJECT : ZM8		
Size	Document Number	Rev
	LVDS/CCD/DMIC/TS	1A
Date: Thursday, September 25, 2014	Sheet 17 of 39	

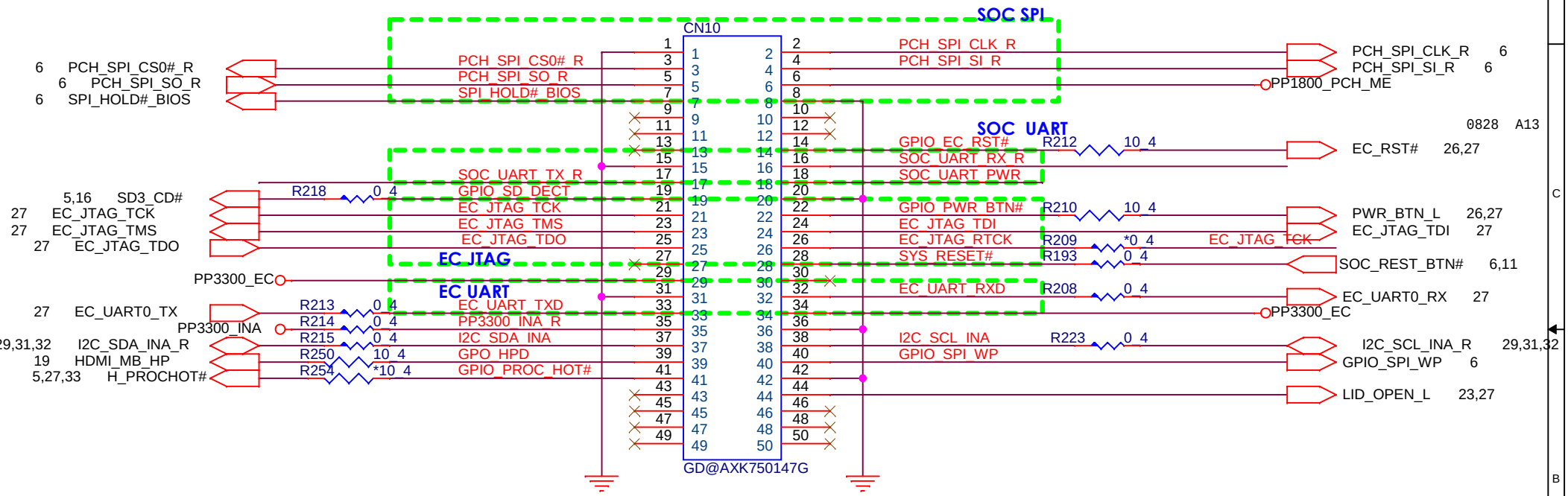
GOOGLE Debug Port(OTH)

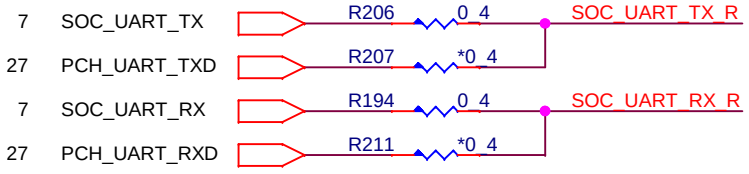
50 pin BTB is MUST, don't use 42 pin

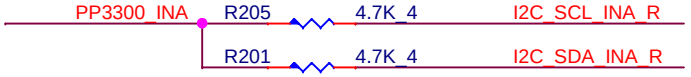
Socket part number AXK750147G

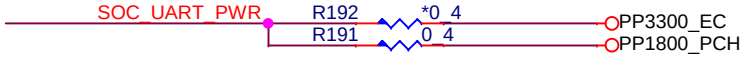
PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD

18







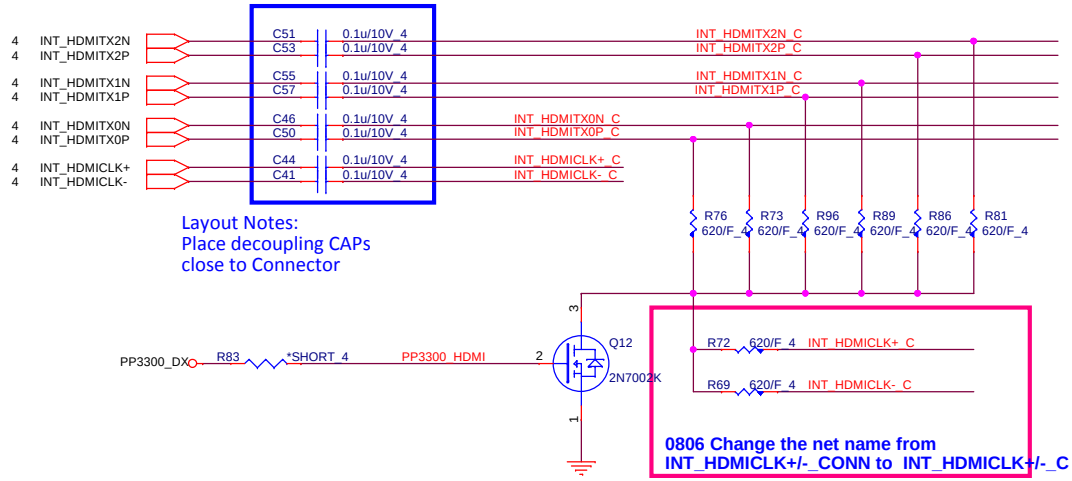


Quanta Computer Inc.

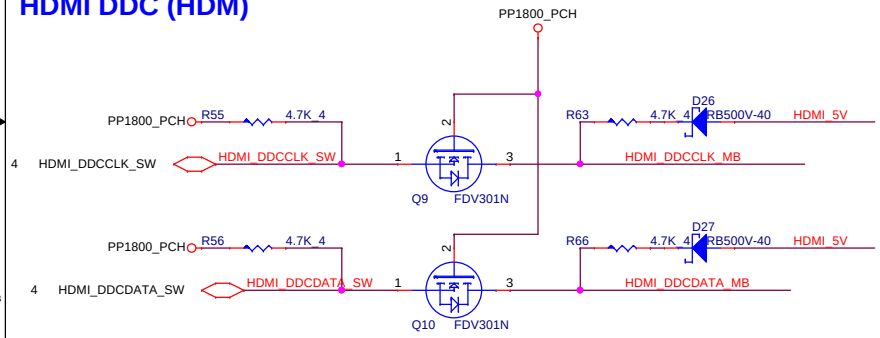
PROJECT : ZM8

Size	Document Number	Rev
	Google Debug	1A
Date: Thursday, September 25, 2014	Sheet 18 of 39	

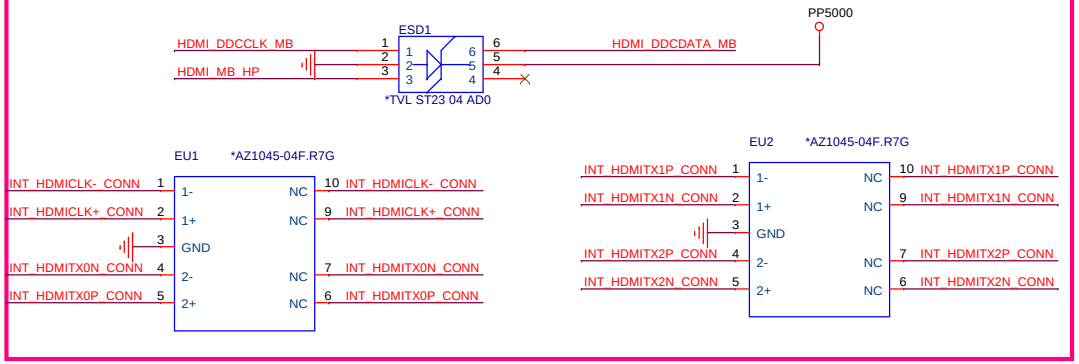
HDMI Cost Reduced level shift (HDM)



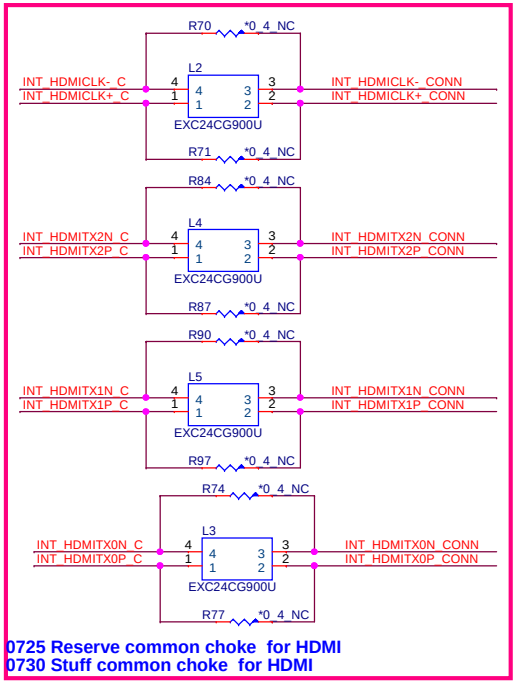
HDMI DDC (HDM)

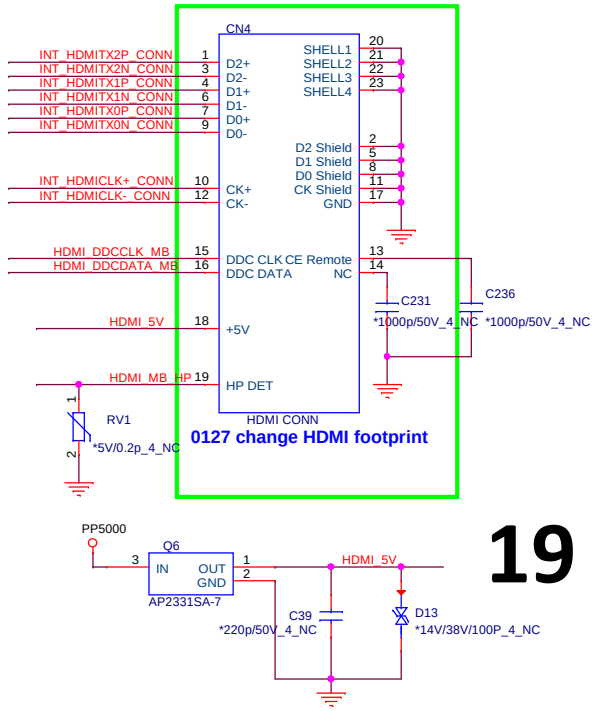


For ESD

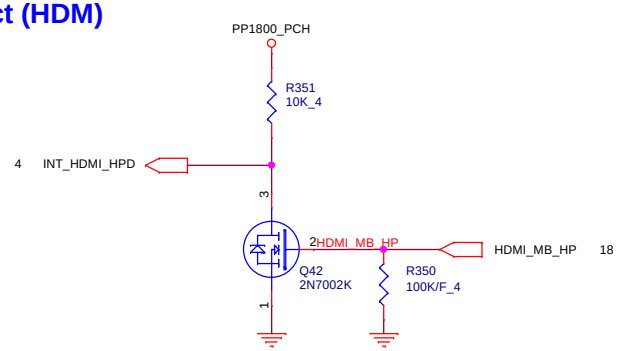


HDMI connector (HDM)





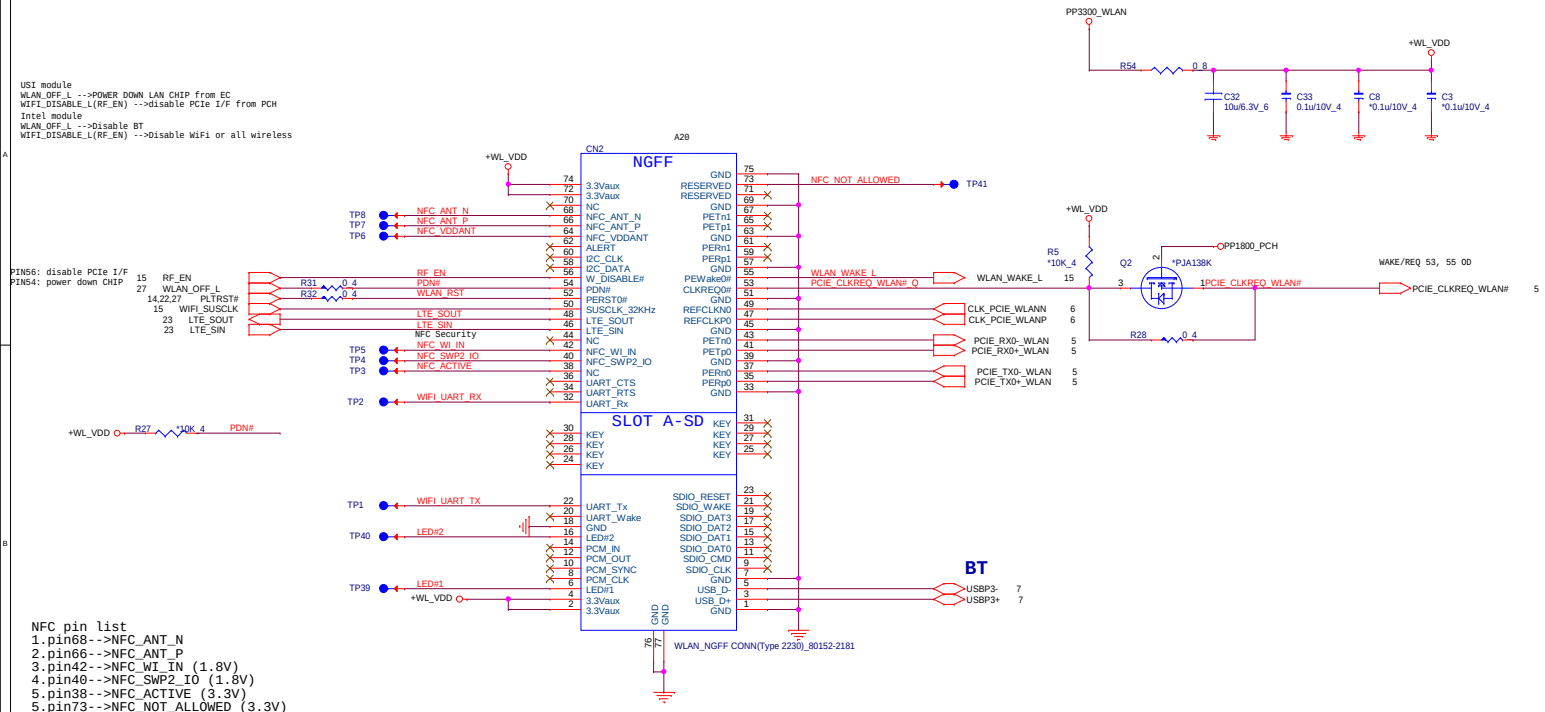
HDMI-detect (HDM)



19

Quanta Computer Inc.		
PROJECT : ZM8		
Size	Document Number: HDMI	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 19 of 39	

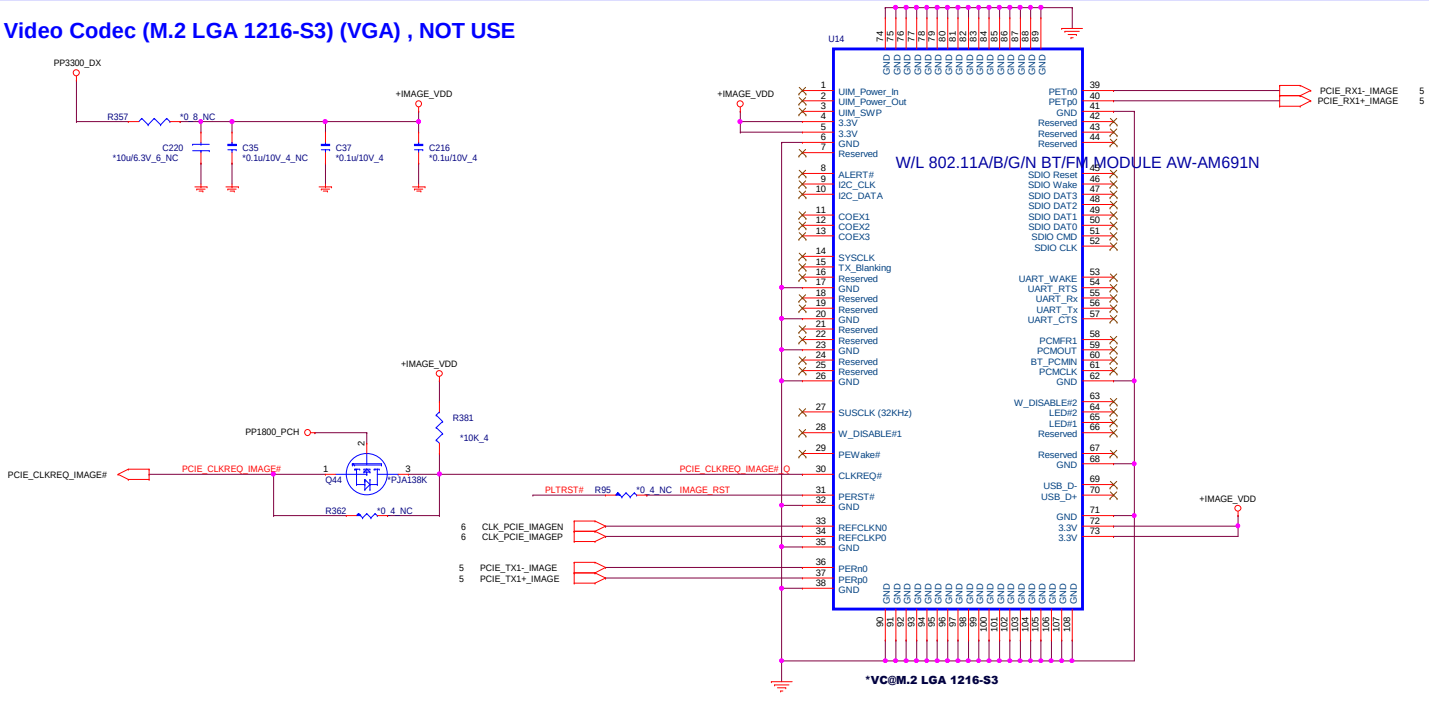
WIFI/BT COMBO (NGFF E KEY)(NGF)



NFC pin list
1.pin68-->NFC_ANT_N
2.pin66-->NFC_ANT_P
3.pin42-->NFC_WI_IN (1.8V)
4.pin40-->NFC_SWP2_IO (1.8V)
5.pin38-->NFC_ACTIVE (3.3V)
5.pin73-->NFC_NOT_ALLOWED (3.3V)
LTE Coexistence pin list (based on V0.2 spec
1.pin48-->LTE_SOUT (3.3V)
2.pin46-->LTE_SIN (3.3V)

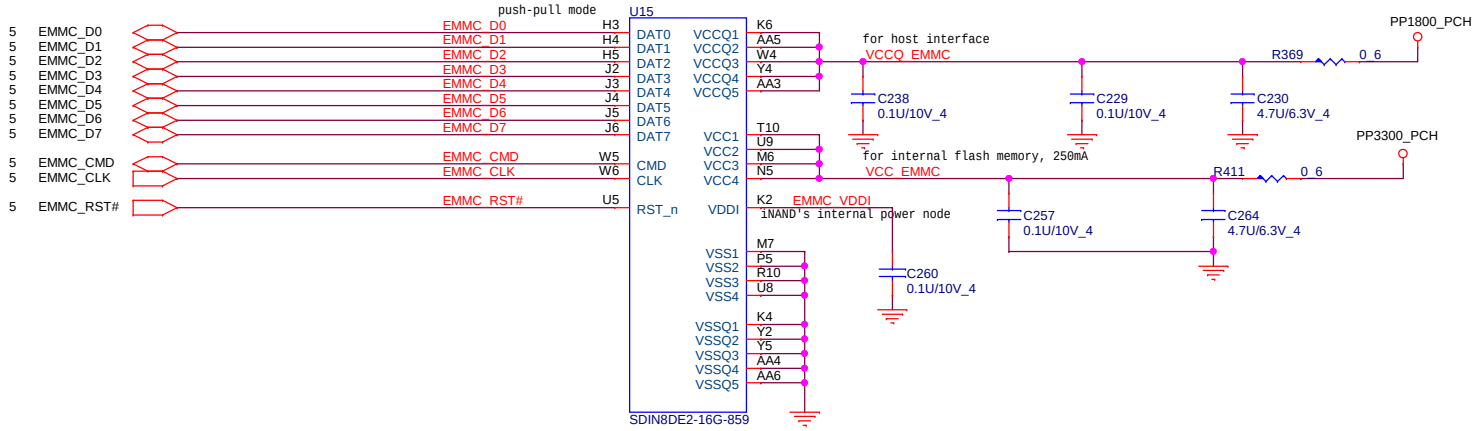
0811 CN2 DFHS75FR108 was EOD so use DFHS75FR105 for substitute.

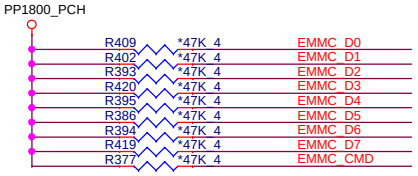
Video Codec (M.2 LGA 1216-S3) (VGA) , NOT USE



Quanta Computer Inc.			
PROJECT : ZM8			
Size	Document Number		Rev 1A
	WIFI / BT / Image Codec		
Date: Thursday, September 25, 2014	Sheet 20 of 39		

EMMC (MMC)





1st source	Hynix: AKE3FG-TW03 (Quanta buy)	H26M52103FMR
2nd source	Samsung: AKE2RF-T502 (Quanta buy)	KLMAG2GEAC-B031
3rd source	Sandisk: AKE3RZ-T115	SDIN8DE2-16G-859

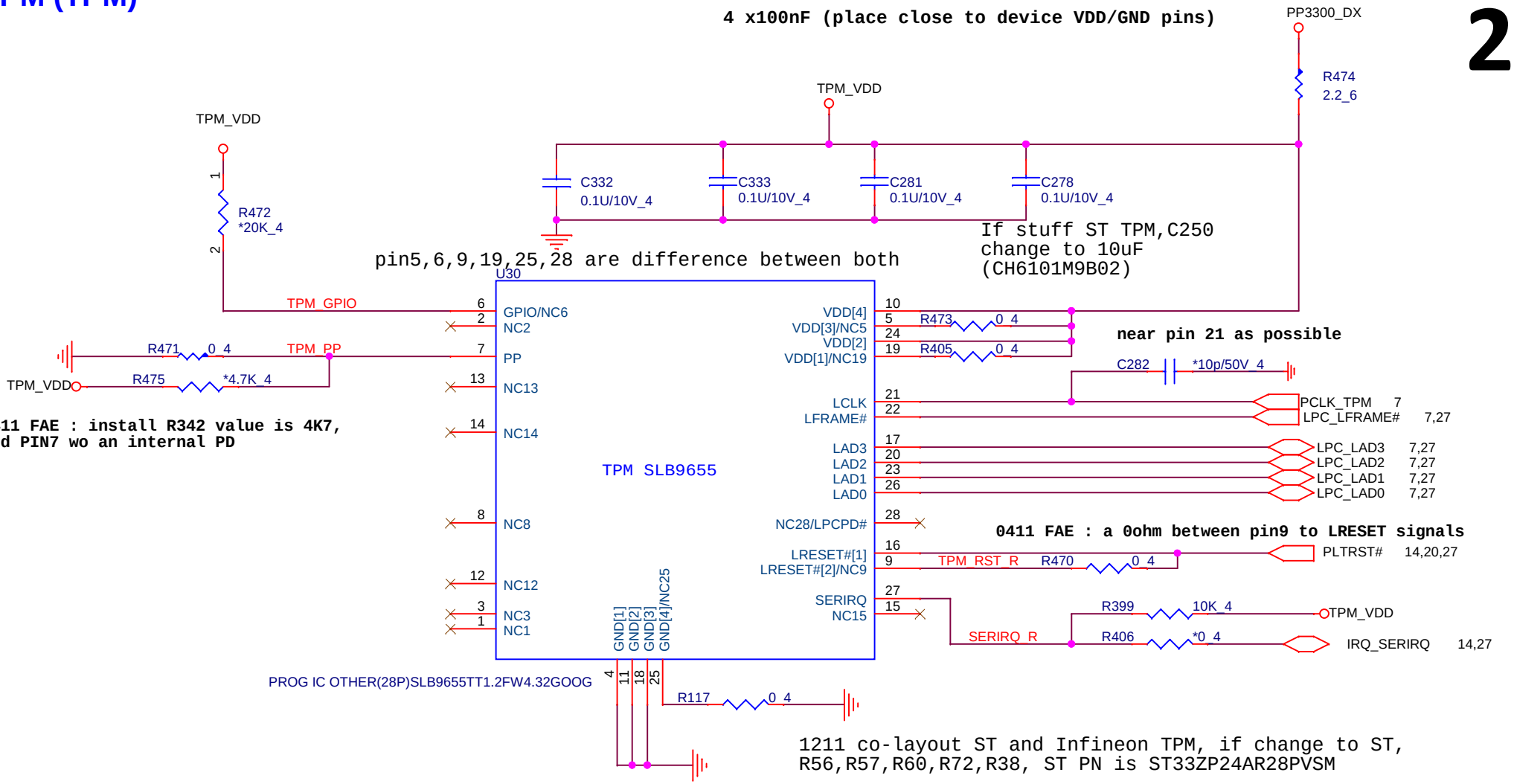
9/25 Update new Sandisk EMMC QP/N: AKE3RZ-T115

Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	EMMC	1A

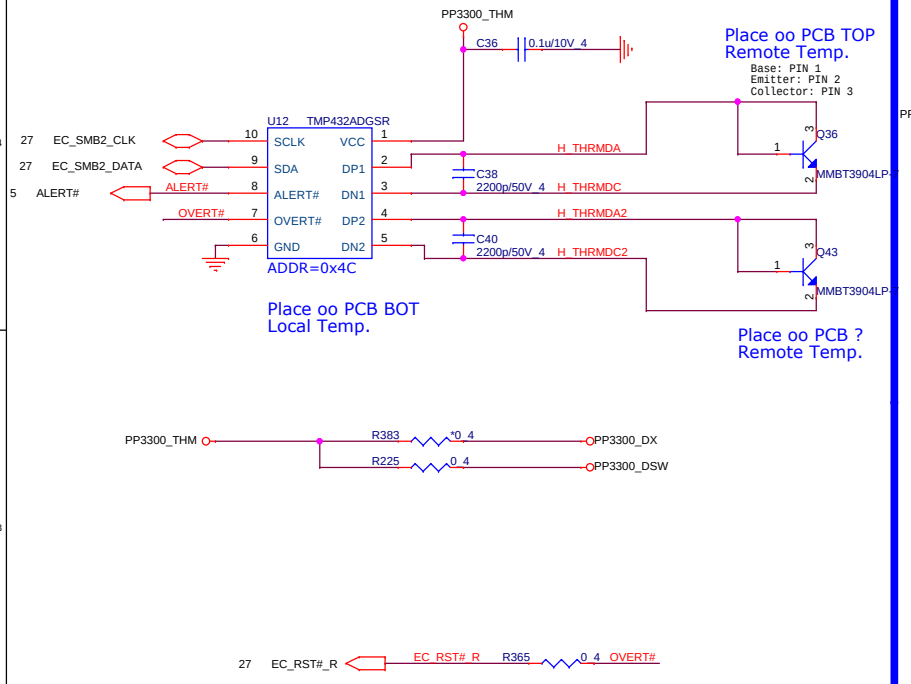
Date: Thursday, September 25, 2014 Sheet 21 of 39

TPM (TPM)

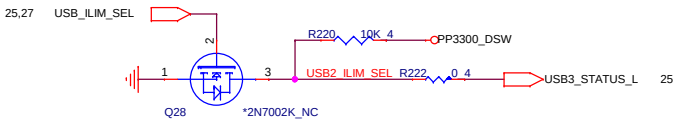


Quanta Computer Inc.		
PROJECT : ZM8		
Size	Document Number: TPM SLB9655	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 22 of 39	

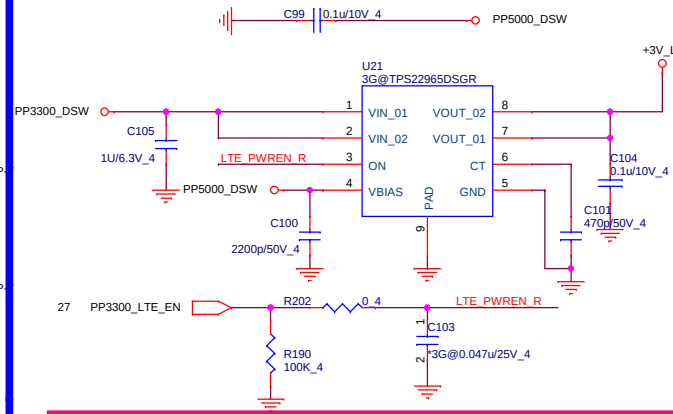
Thermal Sensor(THM)



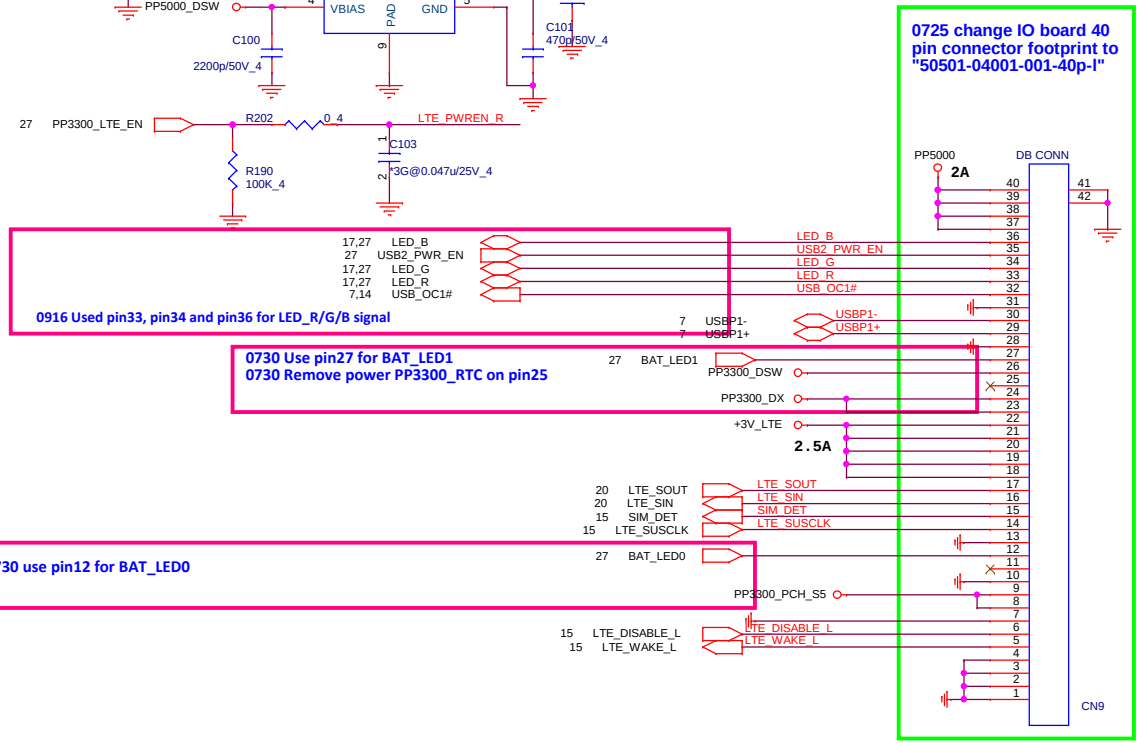
USB Switch Current Control(UBC)



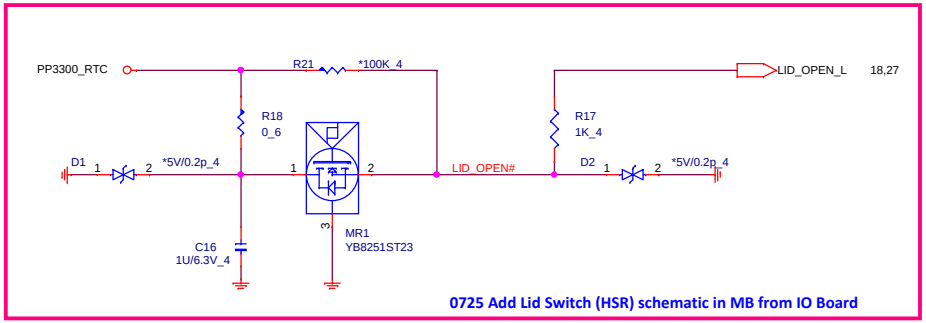
LTE power switch(MNC)



USB/B connector(UB2)



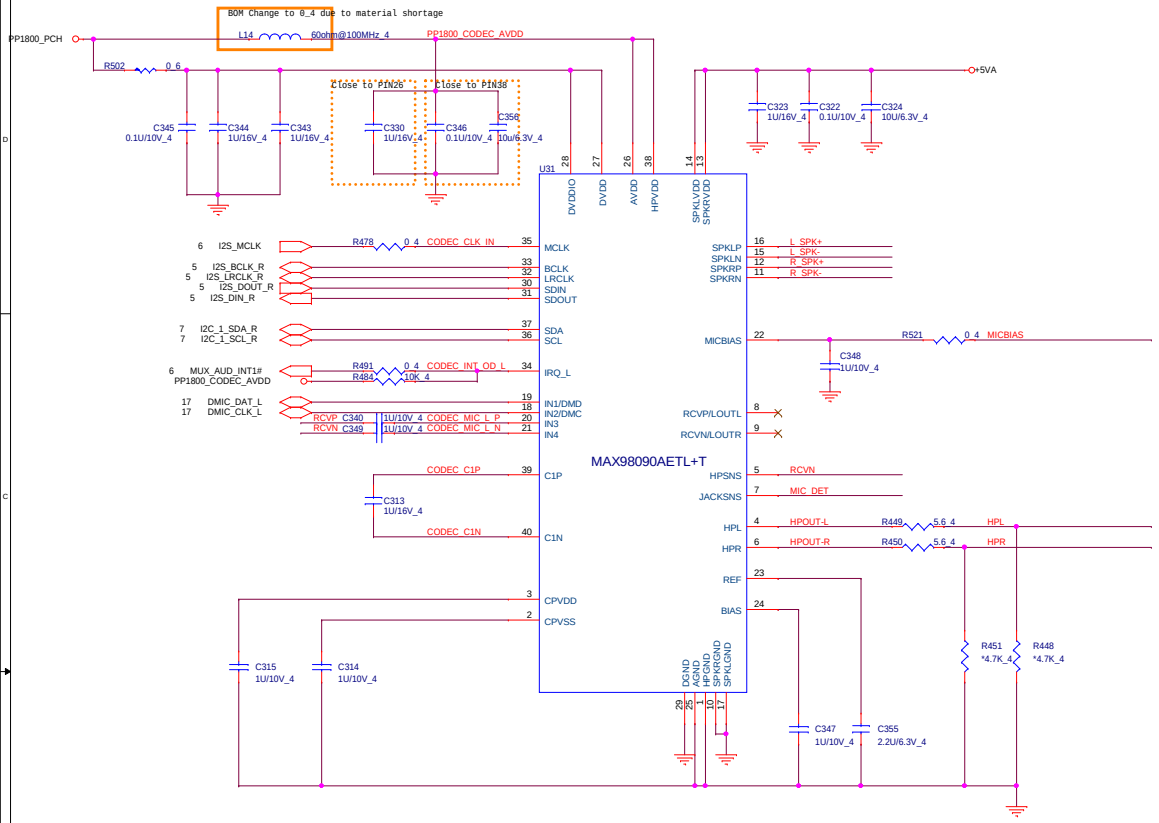
Lid Switch (HSR)



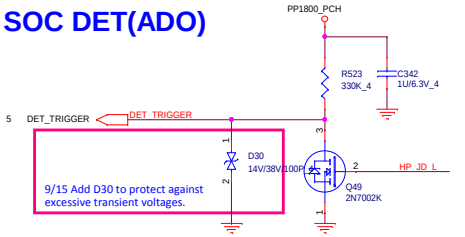
Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	DB/ALS/Thermal sensor/LID	1A
Date: Thursday, September 25, 2014	Sheet 23 of 39	

AUDIO CODEC (ADO)



SOC DET(ADO)



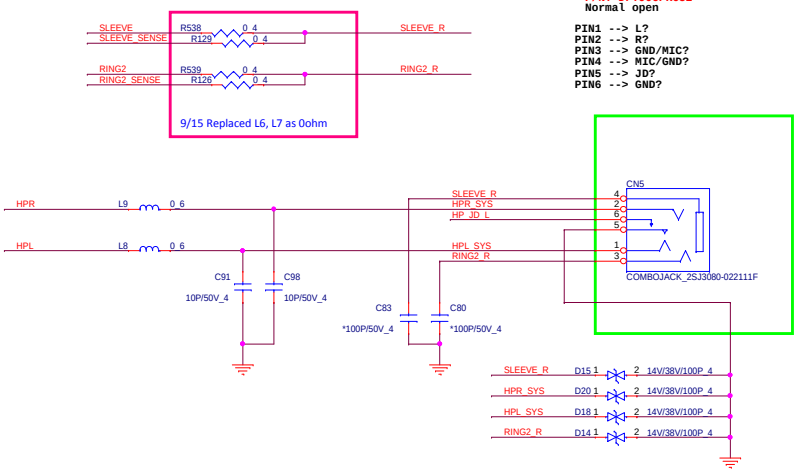
24

HEADPHONE/Mic combo(ADO)

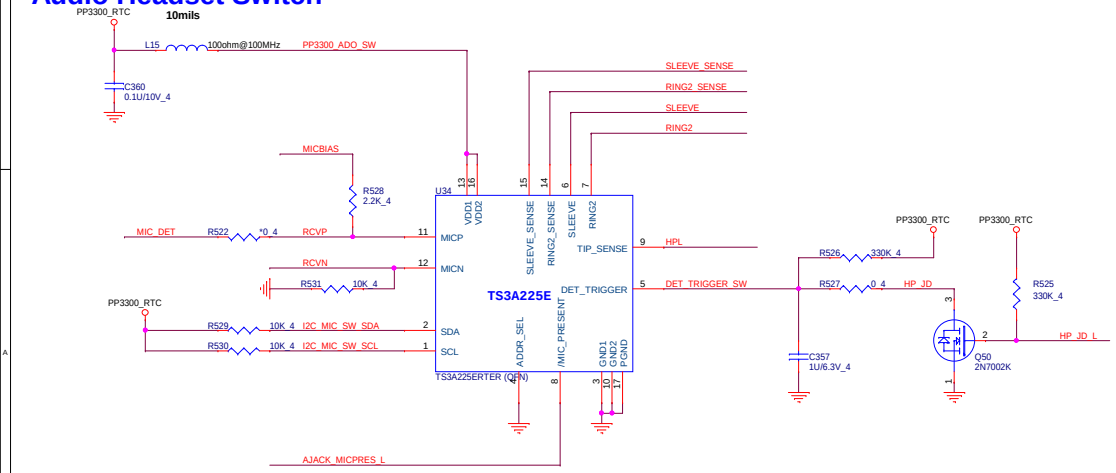
combo jack
Normal Open

P/N: DFTJ06FR652
Normal open

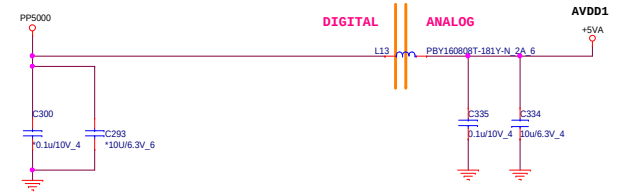
PIN1 --> L?
PIN2 --> R?
PIN3 --> GND/MIC?
PIN4 --> MIC/GND?
PIN5 --> JD?
PIN6 --> GND?



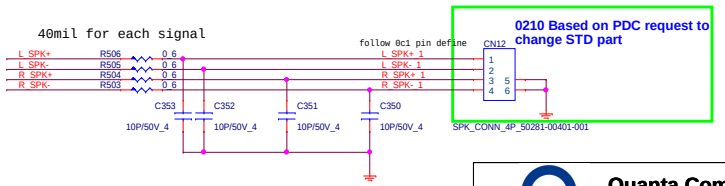
Audio Headset Switch



Codec PWR 5V(ADO)



Internal Speaker(ADO)

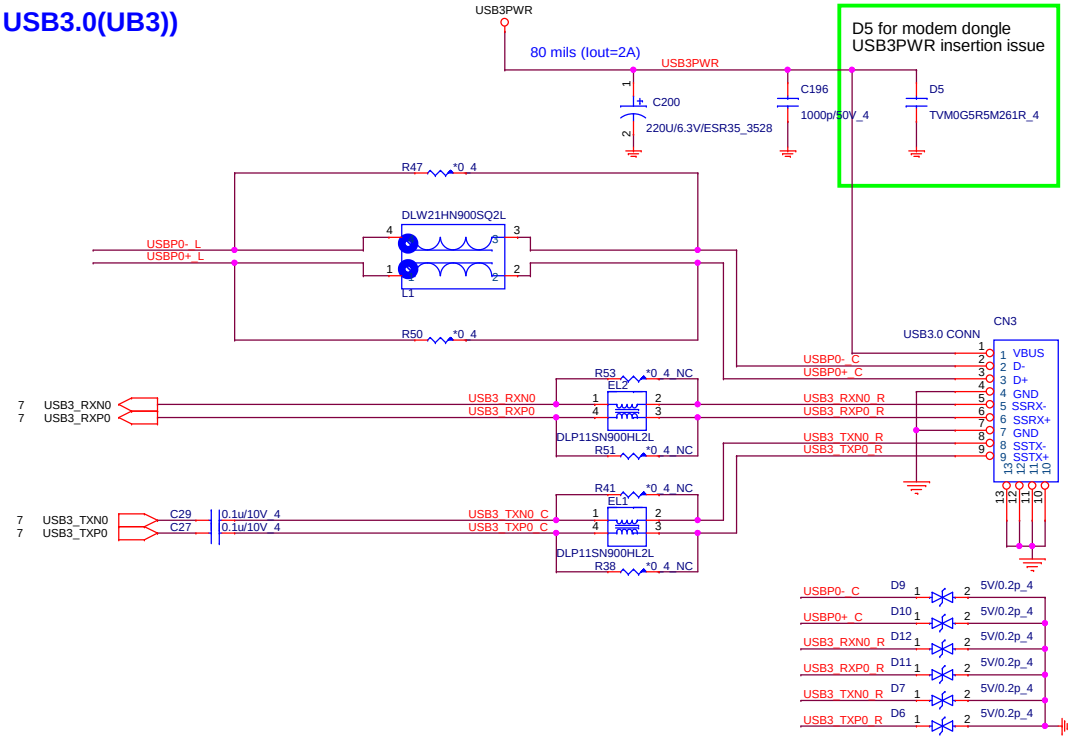


Quanta Computer Inc.
PROJECT : ZM8

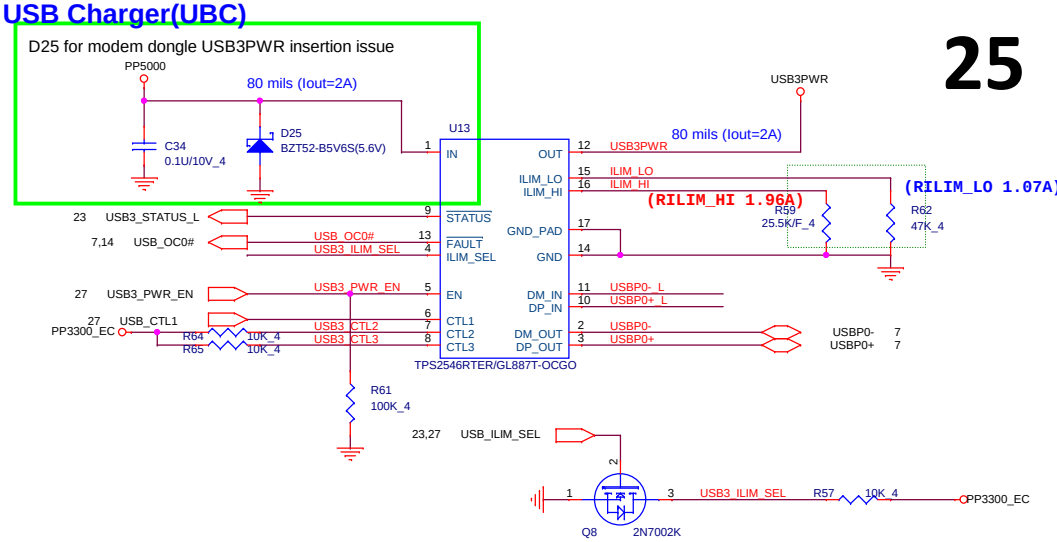
Size	Document Number	Rev
	MAX98090/HP/SPK	1A

Date: Thursday, September 25, 2014 Sheet 24 of 39

USB3.0(UB3))



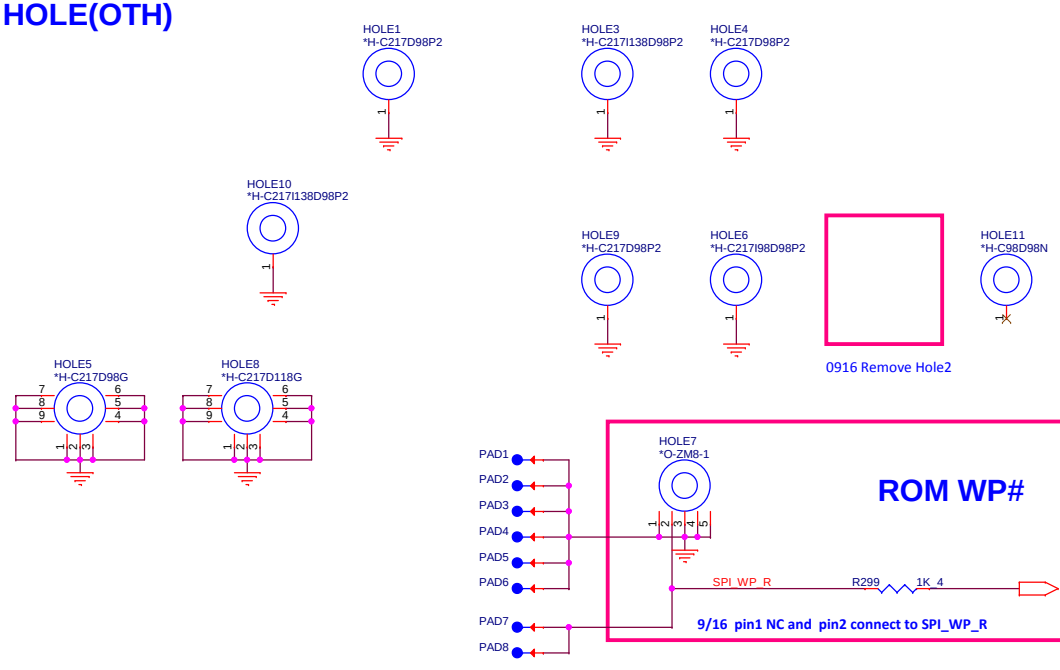
USB Charger(UBC)



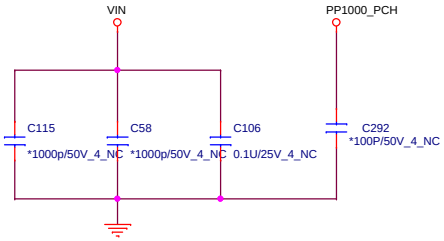
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

HOLE(OTH)



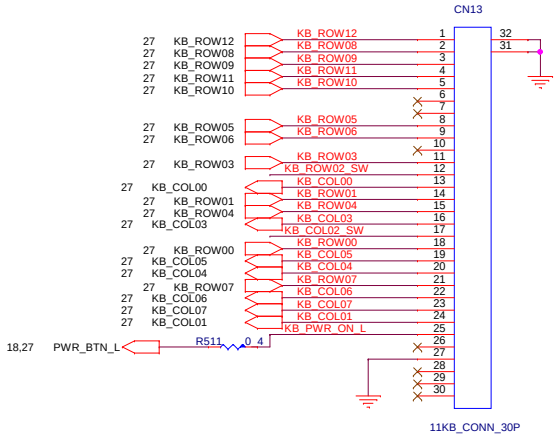
EMI(EMC)



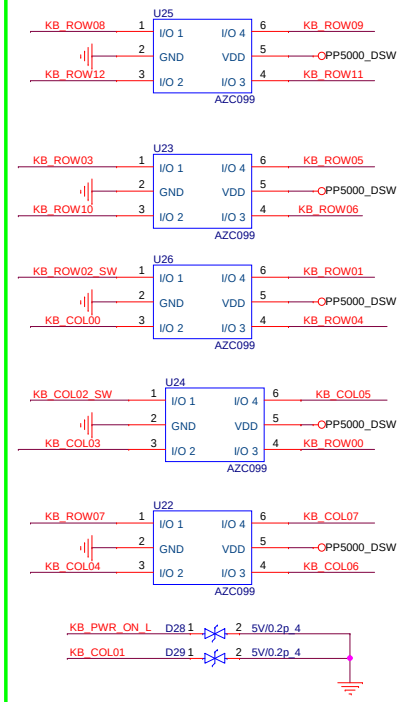
Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	USB3/Charger/Hole	1A
Date: Thursday, September 25, 2014	Sheet 25 of 39	

K/B (KBC)



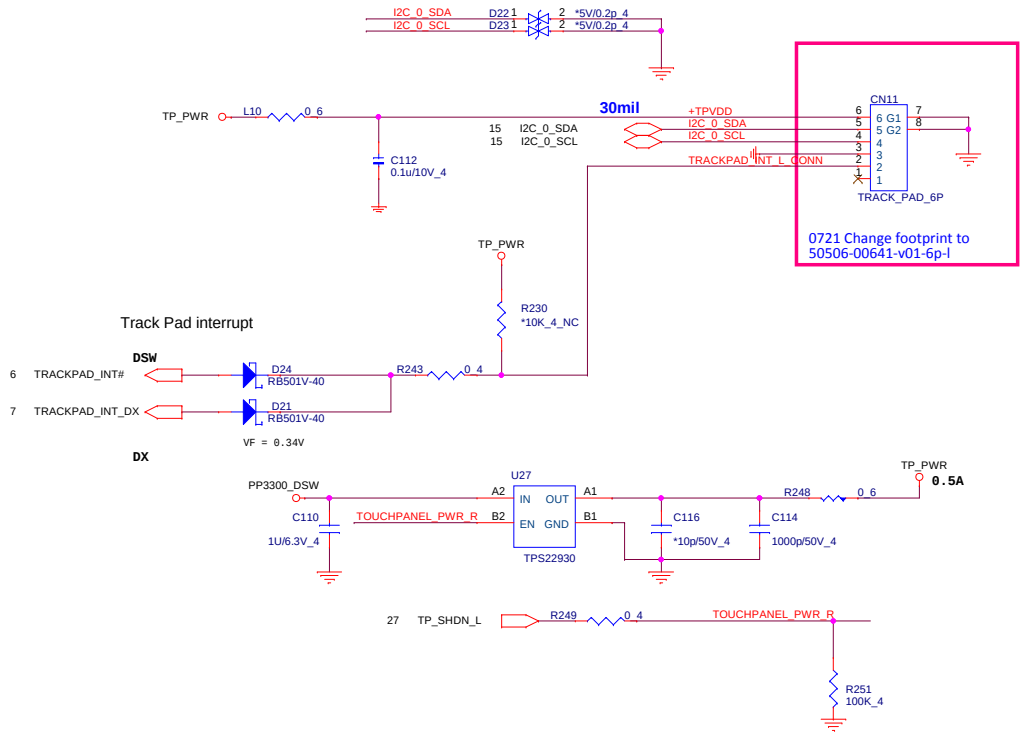
K/B ESD (EMC)



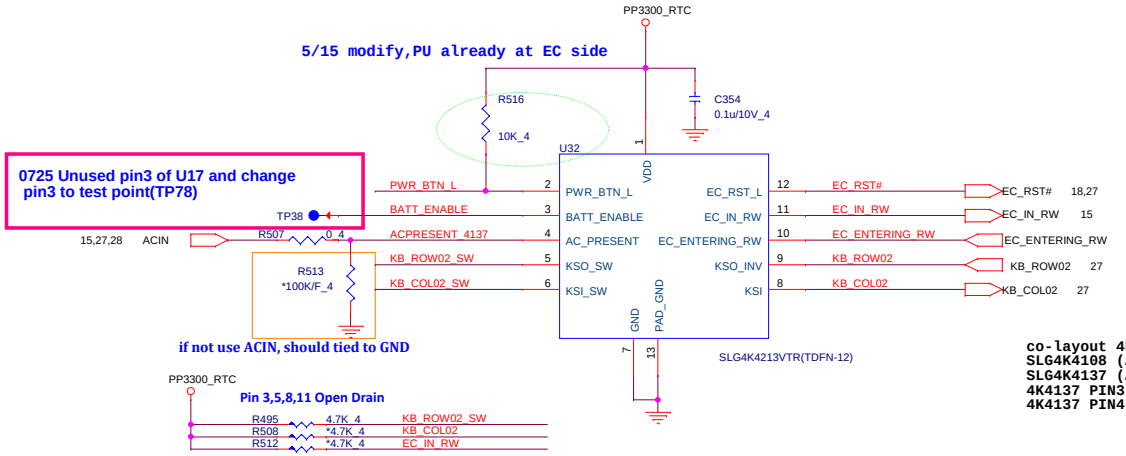
0220 Add and stuff ESD components on KB nets

0221 swap pin of U1002~U1006 for layout

Track PAD BOARD CONN (TPD)



HOLELESS RESET 2-CHIP(KBC)



co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	KB/TP/FAN/HW Reset	1A
Date: Thursday, September 25, 2014	Sheet 26 of 39	

EC(KBC)

9/9 CX18AG12019 EOD, change to CX5AG121002 and F/P change to rc0402

0725 Use pinB6 for PBAT_TEMP signal

0721 USB2_PWR_EN active high, check with EC

0915 Reserved 0ohm at LED_R/G/B for LED function selection

0806 use 000 for Board ID of EVT

SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

SM BUS/I2C PU(KBC)

BATT and CHARGER / LCD BL

THERMAL SENSOR

EC HIB WAKE SOURCES

Add diode for leakage issue

HWPG(KBC)

OD pin list

- EC_REST_L
- BAT_LED0
- BAT_LED1
- PCH_RSMRST_L
- SMBUS
- IRQ_SERIRQ
- EC_BL_DISABLE_L

Stage	EC_ID3	EC_ID2	EC_ID1	
EVT	0	0	0	
DVT1	0	0	1	
DVT2	0	1	0	

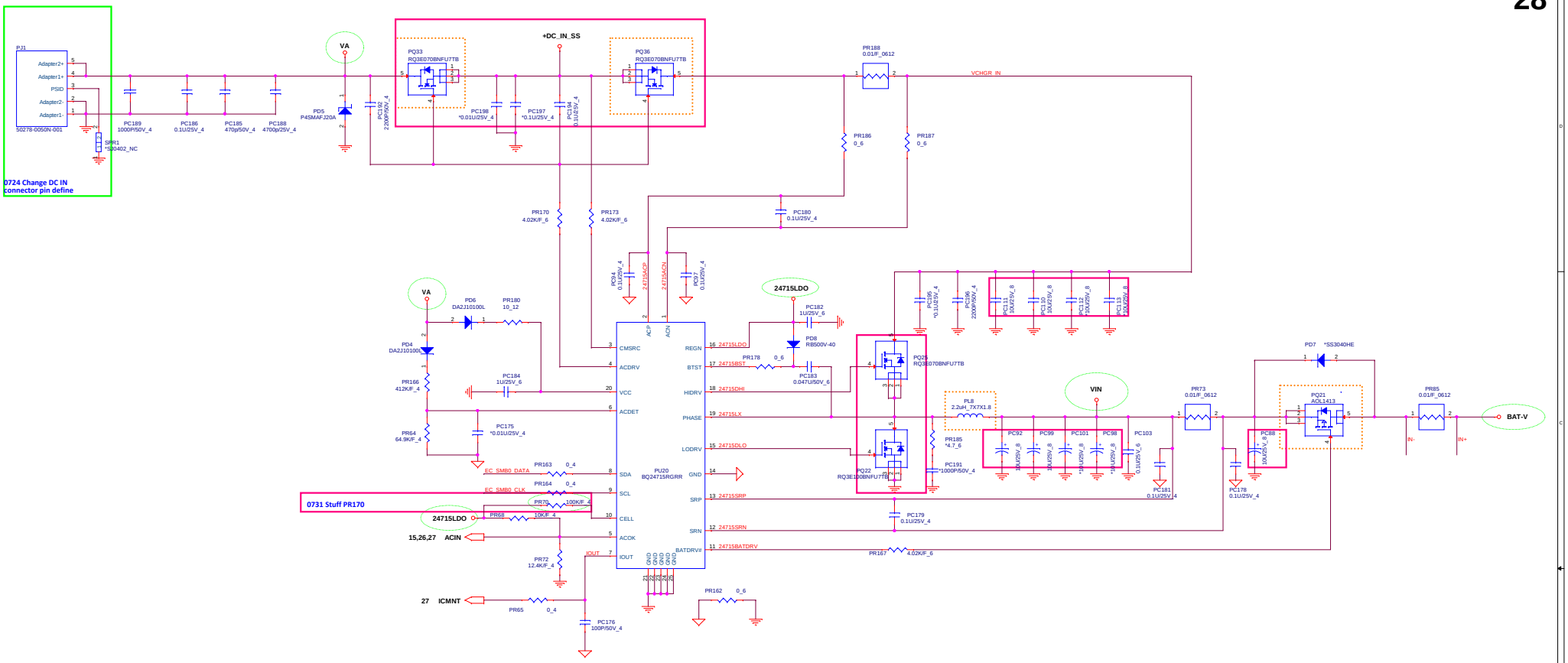
Quanta Computer Inc.

PROJECT : ZM8

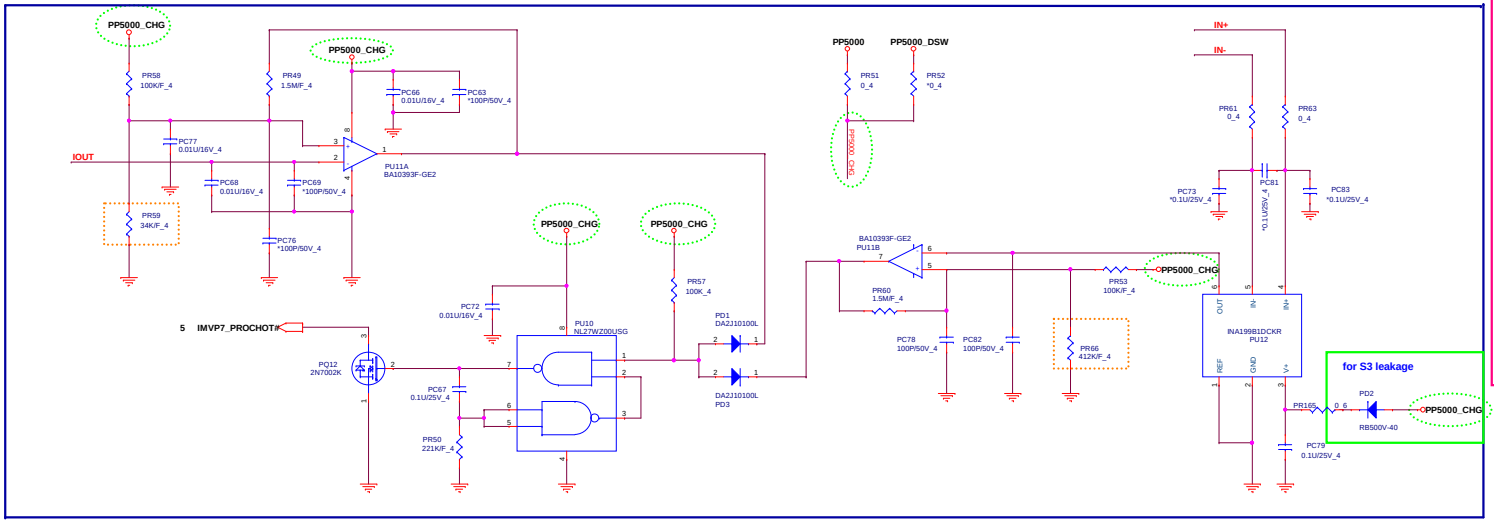
Size	Document Number	Rev
	KBC TI TM4E1G31H6ZRBI	1A

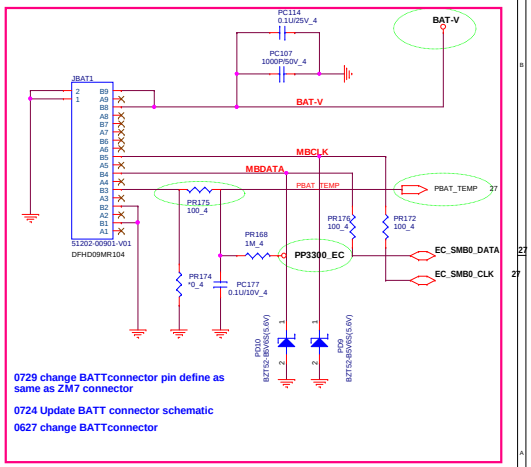
Date: Thursday, September 25, 2014 Sheet 27 of 39

Battery Charger (CRG)



10ms one-shot circuit





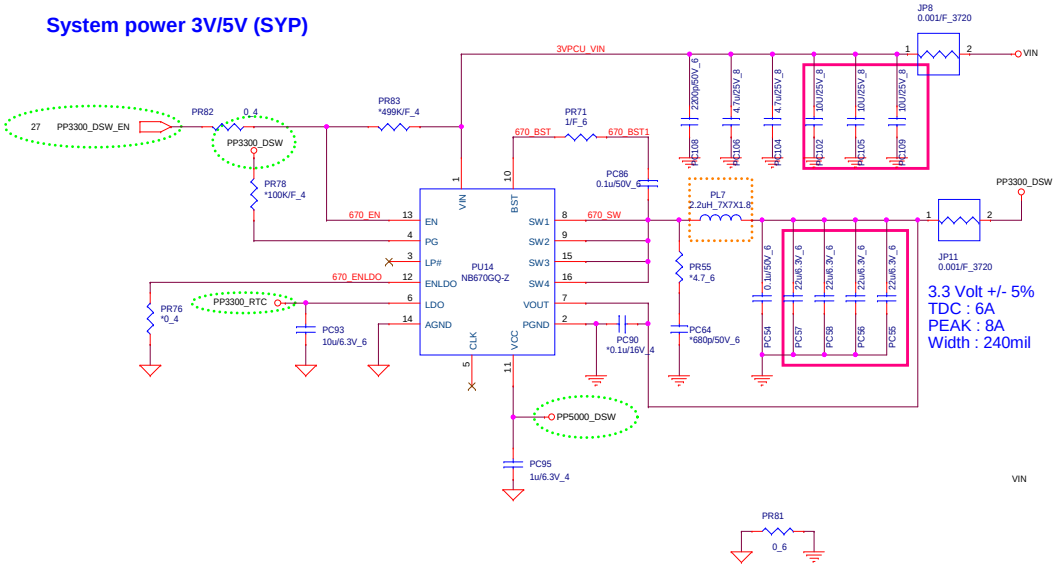
Quanta Computer Inc.

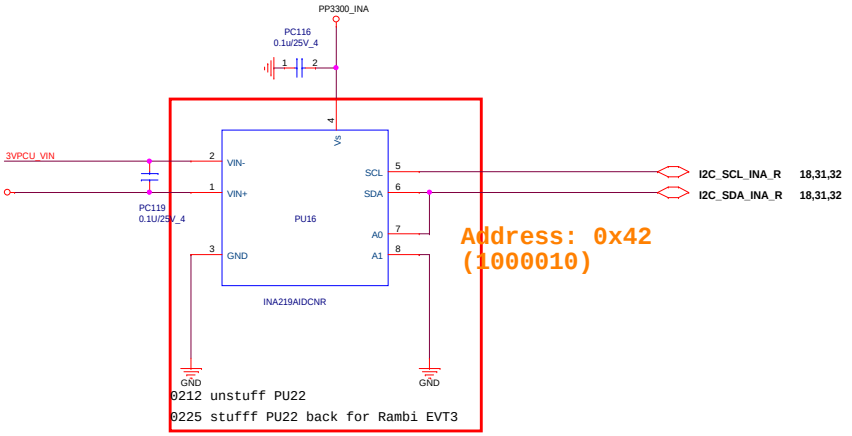
PROJECT :

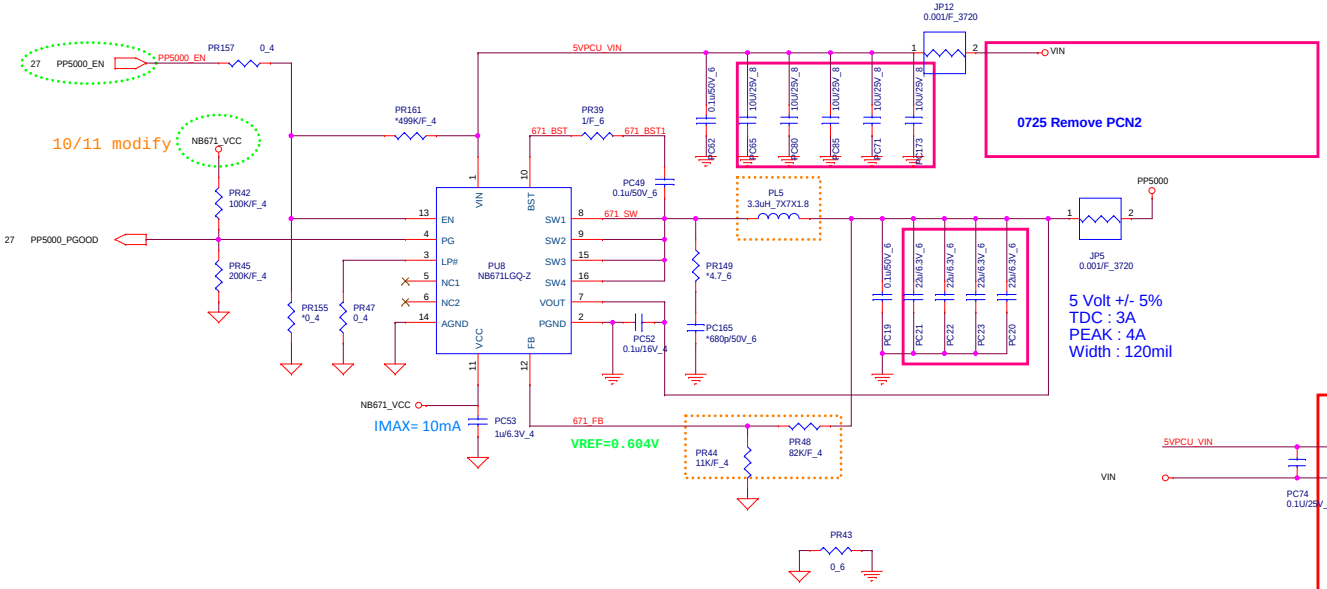
Size	Document Number	Rev
	Charger(BQ24715)	1A

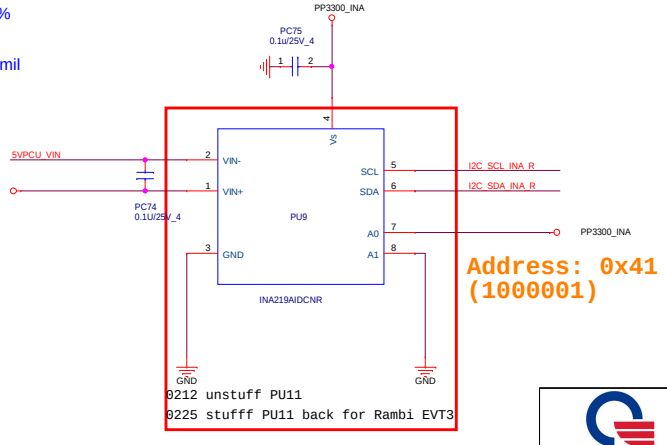
Date: Thursday, September 25, 2014 Sheet 28 of 39

System power 3V/5V (SYP)









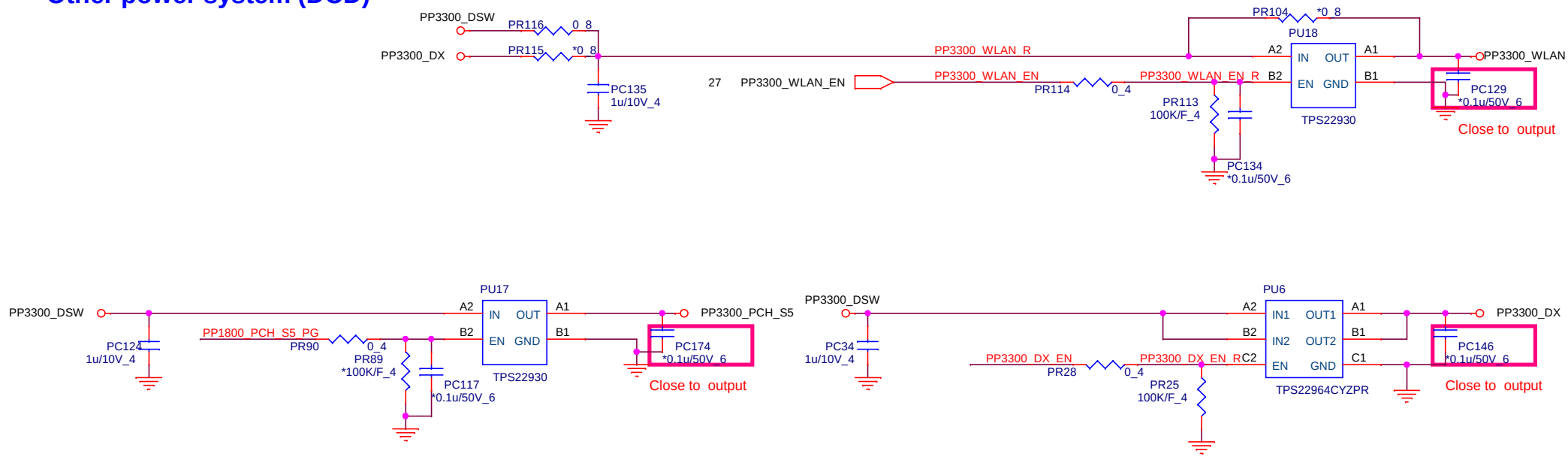
Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	SYSTEM 5V/3V (MPS670/671)	1A
Date: Thursday, September 25, 2014	Sheet 29 of 39	

35 PP1800_PCH_S5_PG
27 PP3300_DX_EN

PP1800_PCH_S5_PG
PP3300_DX_EN

Other power system (DCD)

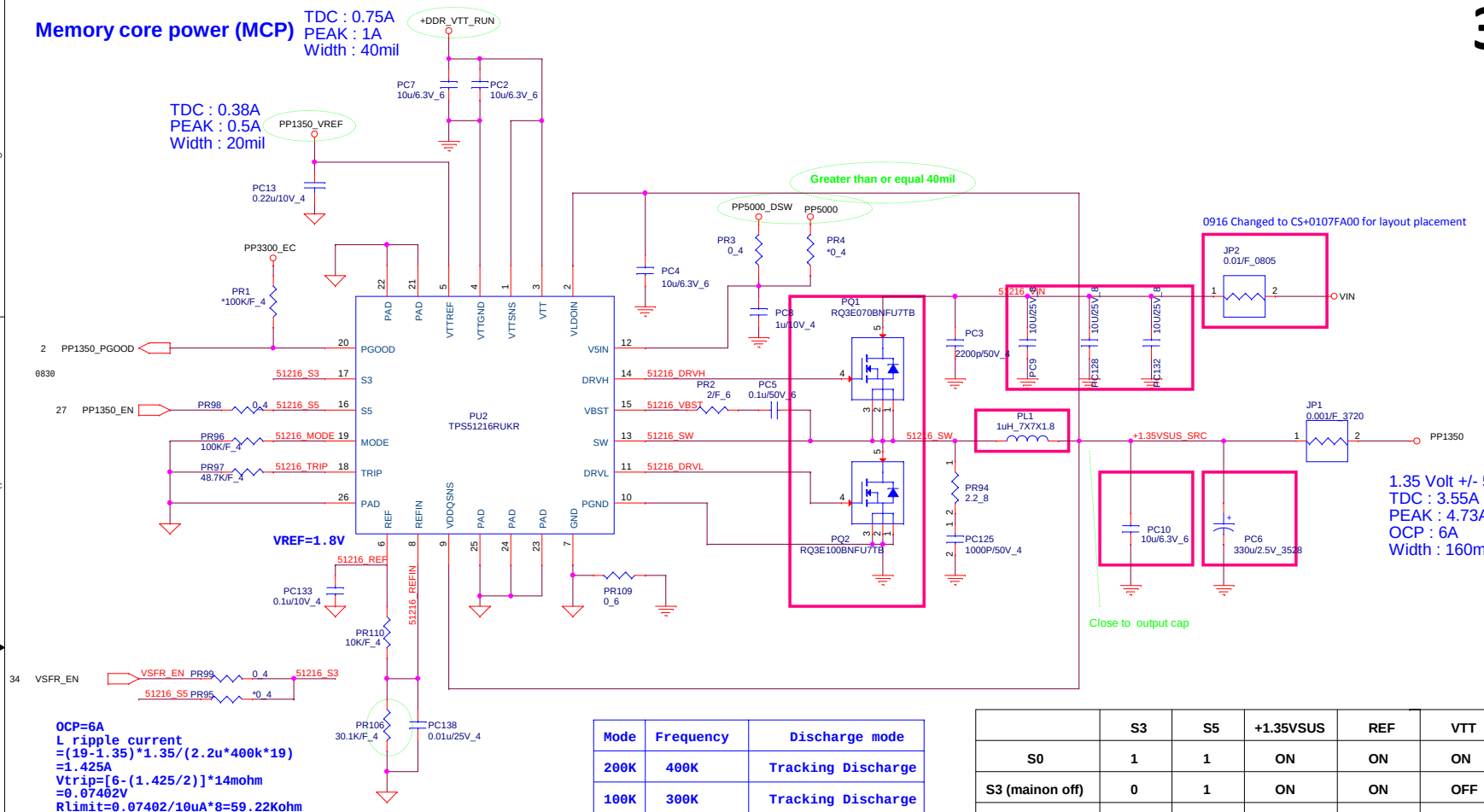


Quanta Computer Inc.		
PROJECT :		
Size	Document Number: Load Switch	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 30 of 39	

Memory core power (MCP)

TDC : 0.75A
PEAK : 1A
Width : 40mil

TDC : 0.38A
PEAK : 0.5A
Width : 20mil

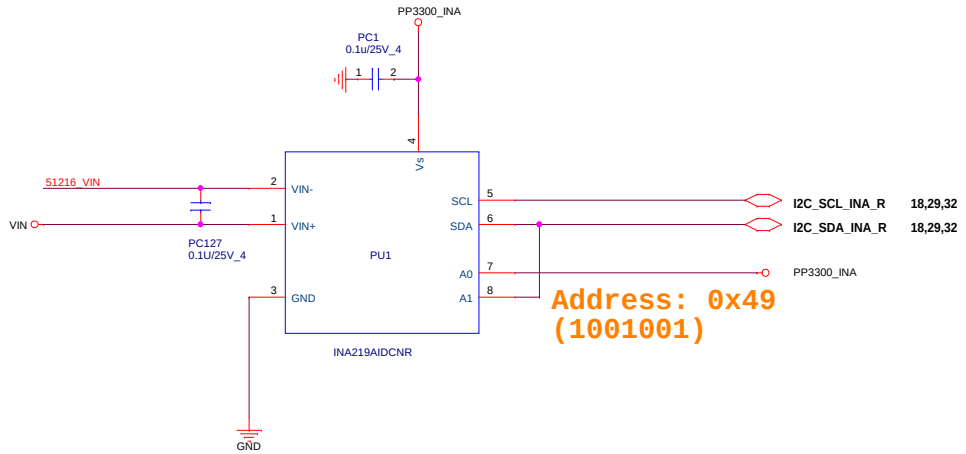


1.35 Volt +/- 5%
TDC : 3.55A
PEAK : 4.73A
OCP : 6A
Width : 160mil

OCP=6A
L ripple current
=(19-1.35)*1.35/(2.2u*400k*19)
=1.425A
Vtrip=[6-(1.425/2)]*14mohm
=0.07402V
Rlimit=0.07402/10uA*8=59.22Kohm

Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



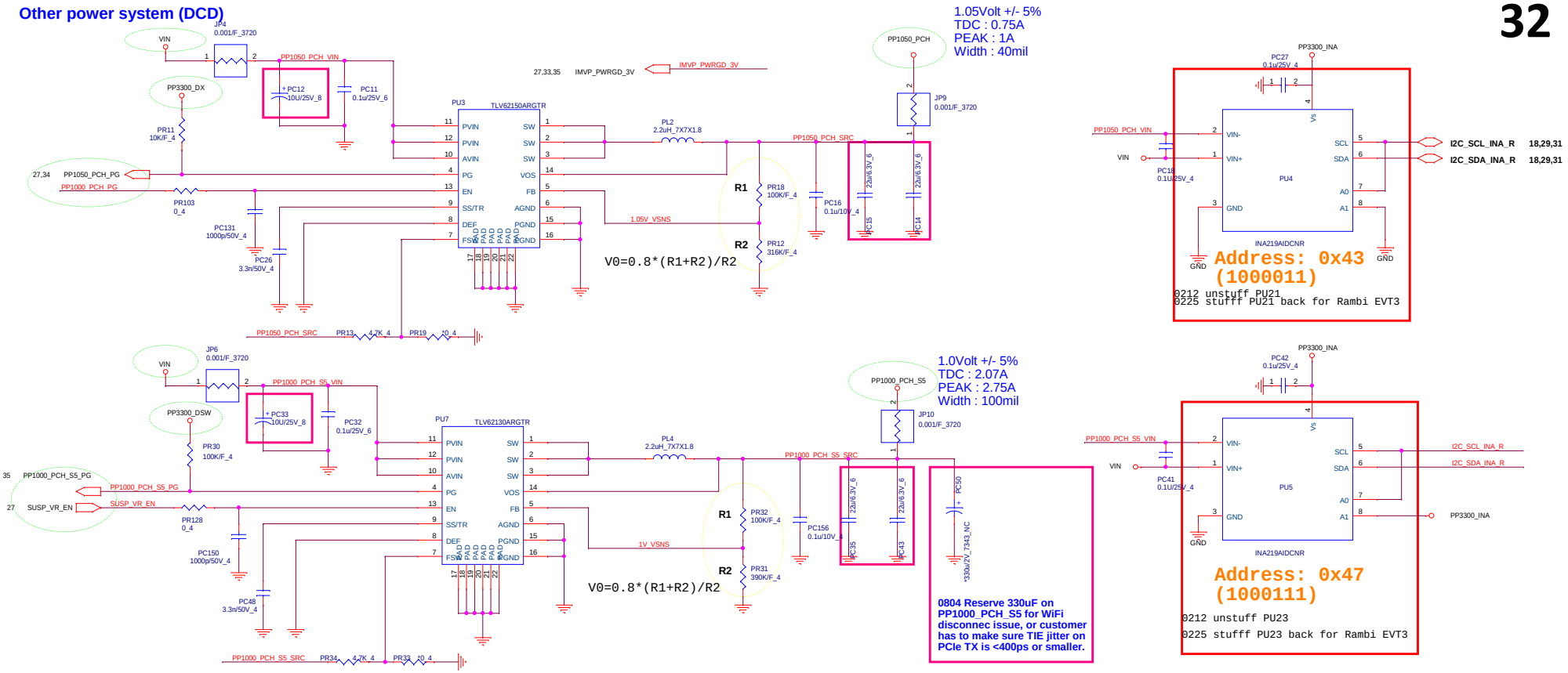
Address: 0x49 (1001001)

Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	DDR 1.35V(TPS51216)	1A

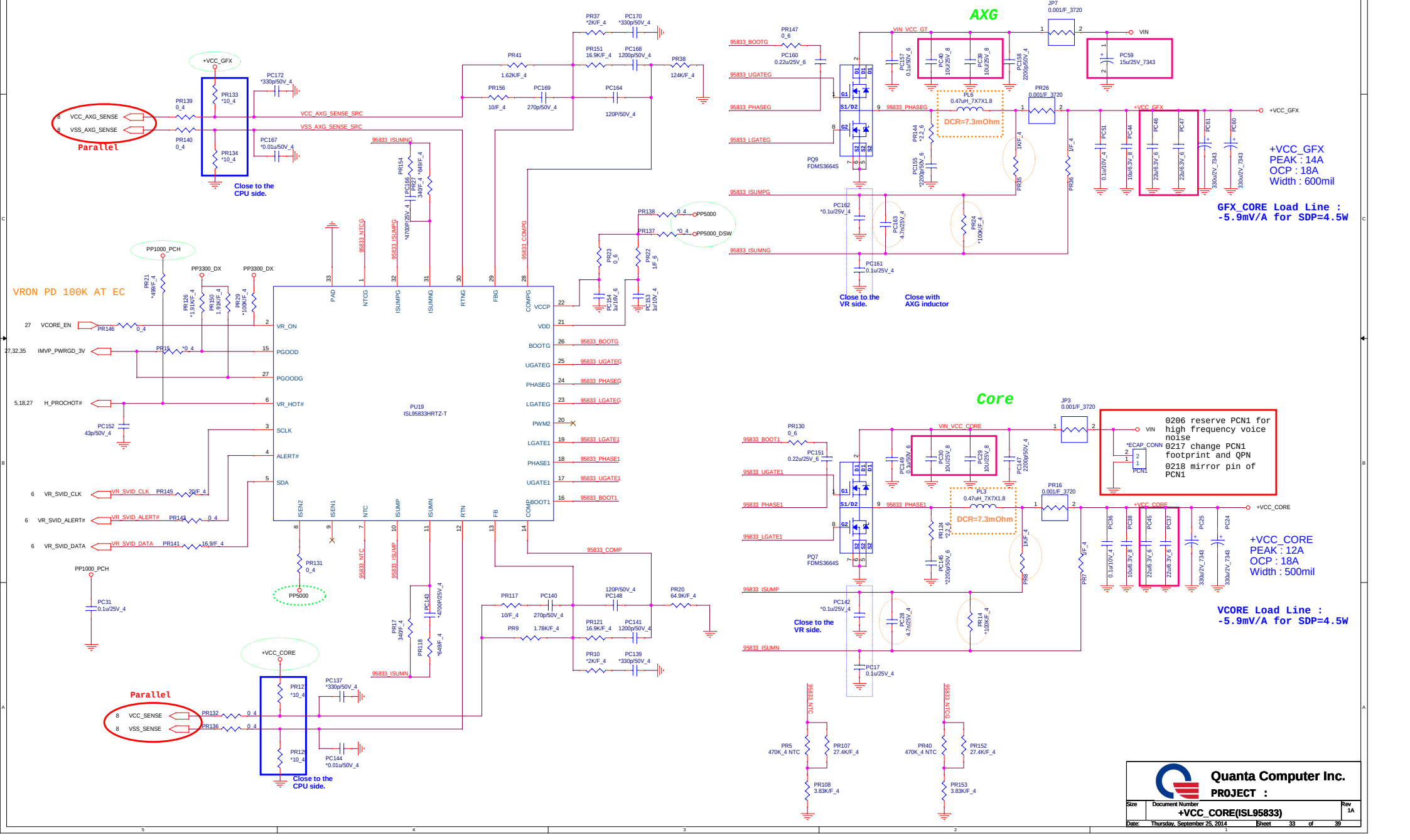
Date: Thursday, September 25, 2014 Sheet 31 of 39

Other power system (DCD)



Quanta Computer Inc.		
PROJECT :		
Size	Document Number: +1.05V/+1V(TPS54318)	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 32 of 39	

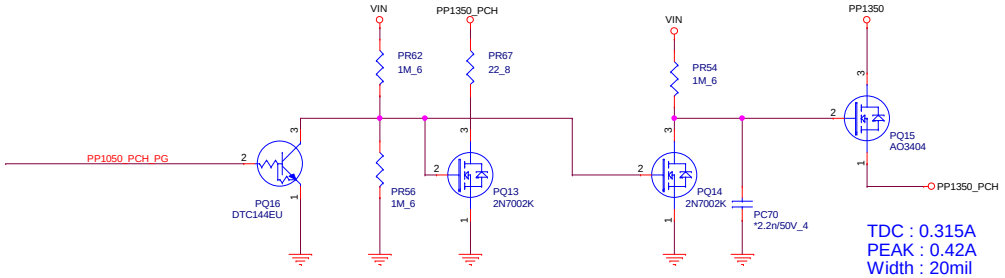
CPU core power(VCP)



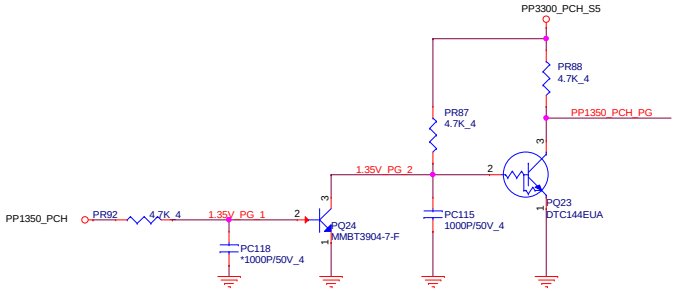
Quanta Computer Inc.			
PROJECT :			
Size	Document Number		Rev
	+VCC_CORE(ISL95833)		1A
Date: Thursday, September 25, 2014	Sheet 33 of 39		

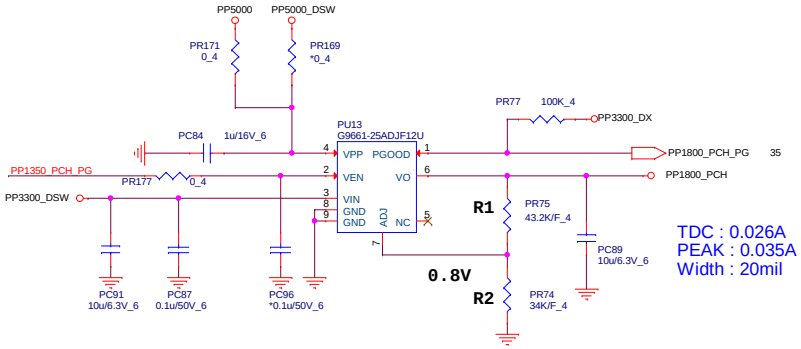
Other power system (DCD)

31 VSFR_EN → VSFR_EN
27,32 SUSP_VR_EN
27,32 PP1050_PCH_PG



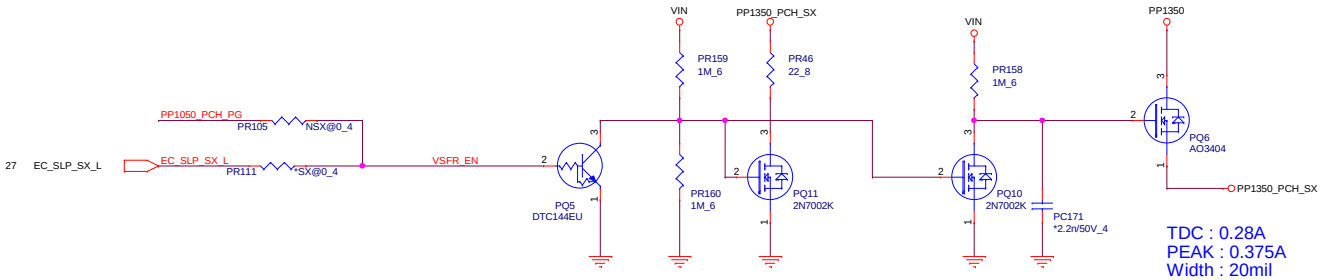
TDC : 0.315A
PEAK : 0.42A
Width : 20mil





TDC : 0.026A
PEAK : 0.035A
Width : 20mil

Vout =0.8(1+R1/R2)
=1.8V

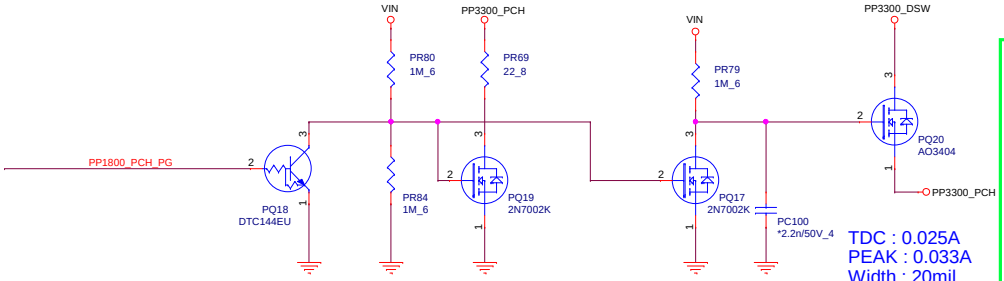


TDC : 0.28A
PEAK : 0.375A
Width : 20mil

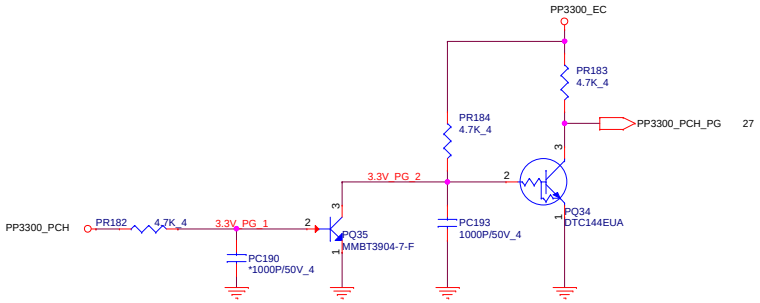
Quanta Computer Inc.		
PROJECT :		
Size	Document Number: LDO (1V/1.35V/1.5V/1.8V)	Rev: 1A
Date: Thursday, September 25, 2014	Sheet 34 of 39	

Other power system (DCD)

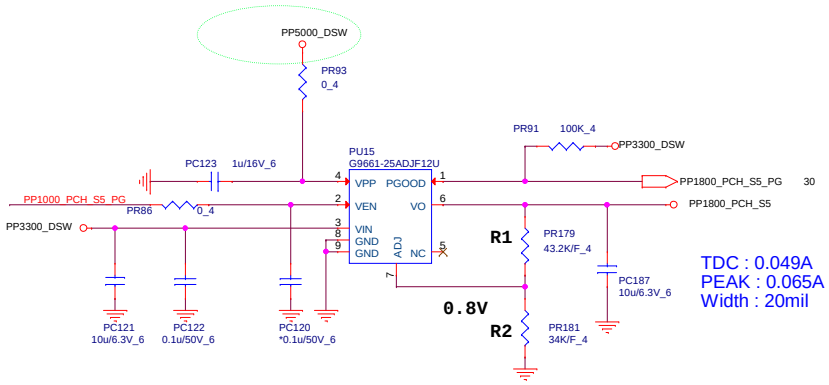
34 PP1800_PCH_PG
32 PP1000_PCH_S5_PG



TDC : 0.025A
PEAK : 0.033A
Width : 20mil

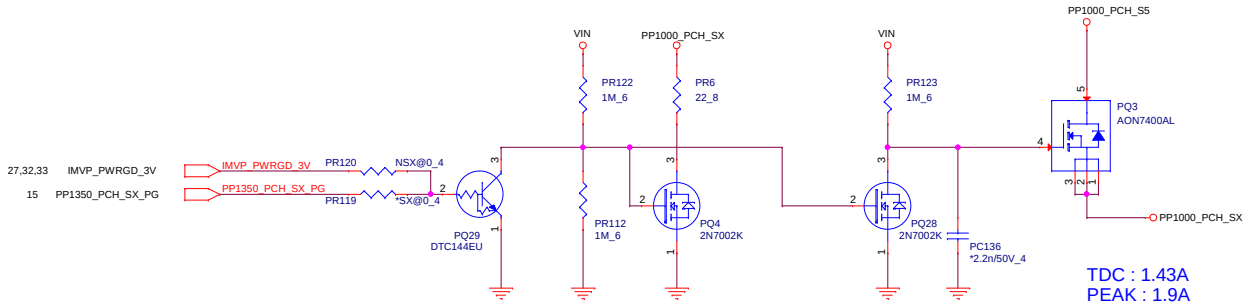


0219 Change G9661 to TPS62243 for PP1800_PCH_S5
0220 change back to LDO for PP1800_PCH_S5



TDC : 0.049A
PEAK : 0.065A
Width : 20mil

Vout =0.8(1+R1/R2)
=1.8V

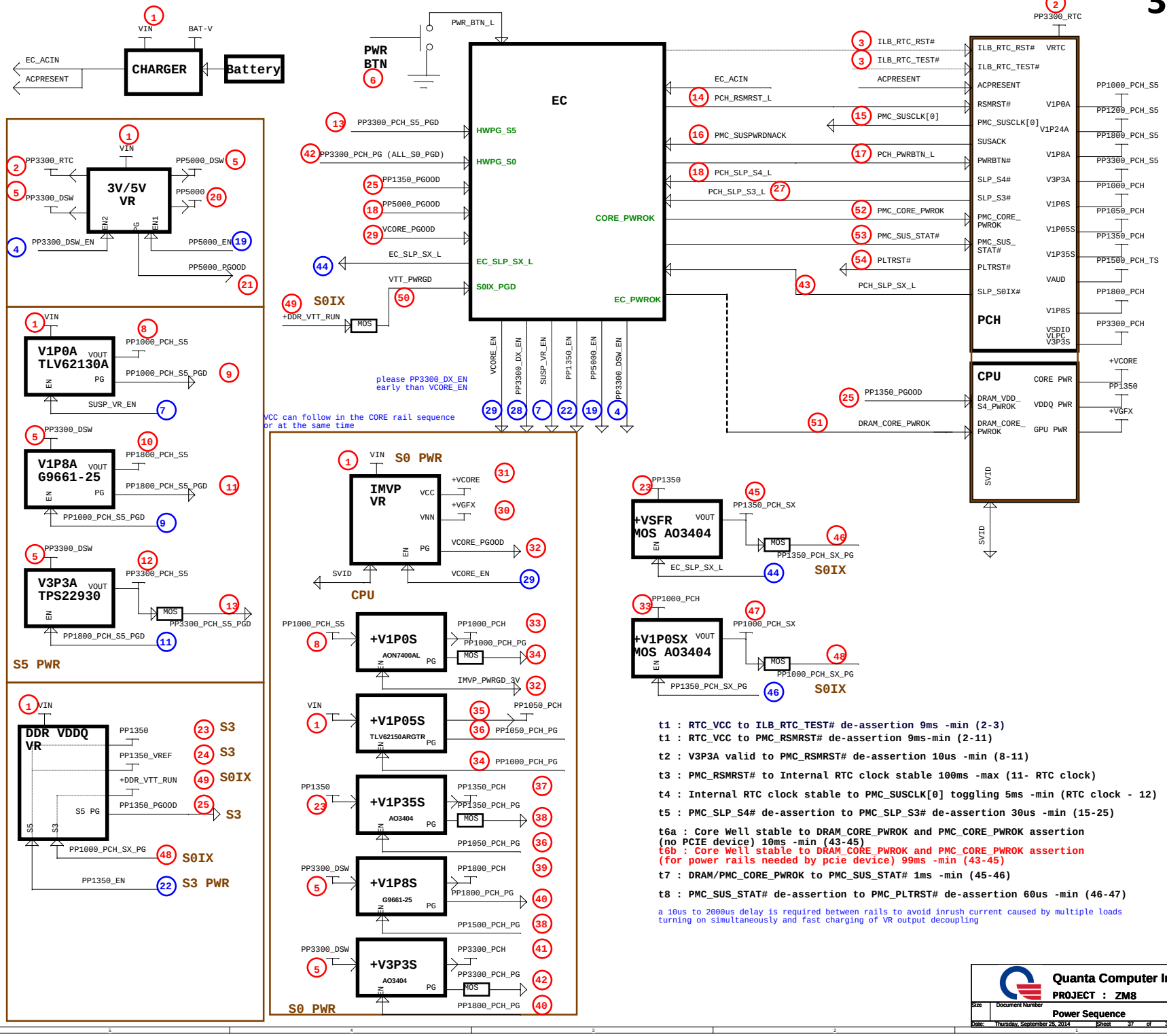


TDC : 1.43A
PEAK : 1.9A
Width : 80mil

Quanta Computer Inc.		
PROJECT :		
Size	Document Number	Rev
	LDO(1.2V/3.3V/1.8V)	1A
Date: Thursday, September 25, 2014	Sheet 35 of 39	

Quanta Computer Inc.			
PROJECT :			
Size	Document Number: Thermal protect		Rev: 1A
Date: Thursday, September 25, 2014		Sheet 36 of 39	

Support S0iX



t1 : RTC_VCC to ILB_RTC_TEST# de-assertion 9ms -min (2-3)
t1 : RTC_VCC to PMC_RSMRST# de-assertion 9ms-min (2-11)

t2 : V3P3A valid to PMC_RSMRST# de-assertion 10us -min (8-11)

t3 : PMC_RSMRST# to Internal RTC clock stable 100ms -max (11- RTC clock)

t4 : Internal RTC clock stable to PMC_SUSCLK[0] toggling 5ms -min (RTC clock - 12)

t5 : PMC_SLP_S4# de-assertion to PMC_SLP_S3# de-assertion 30us -min (15-25)

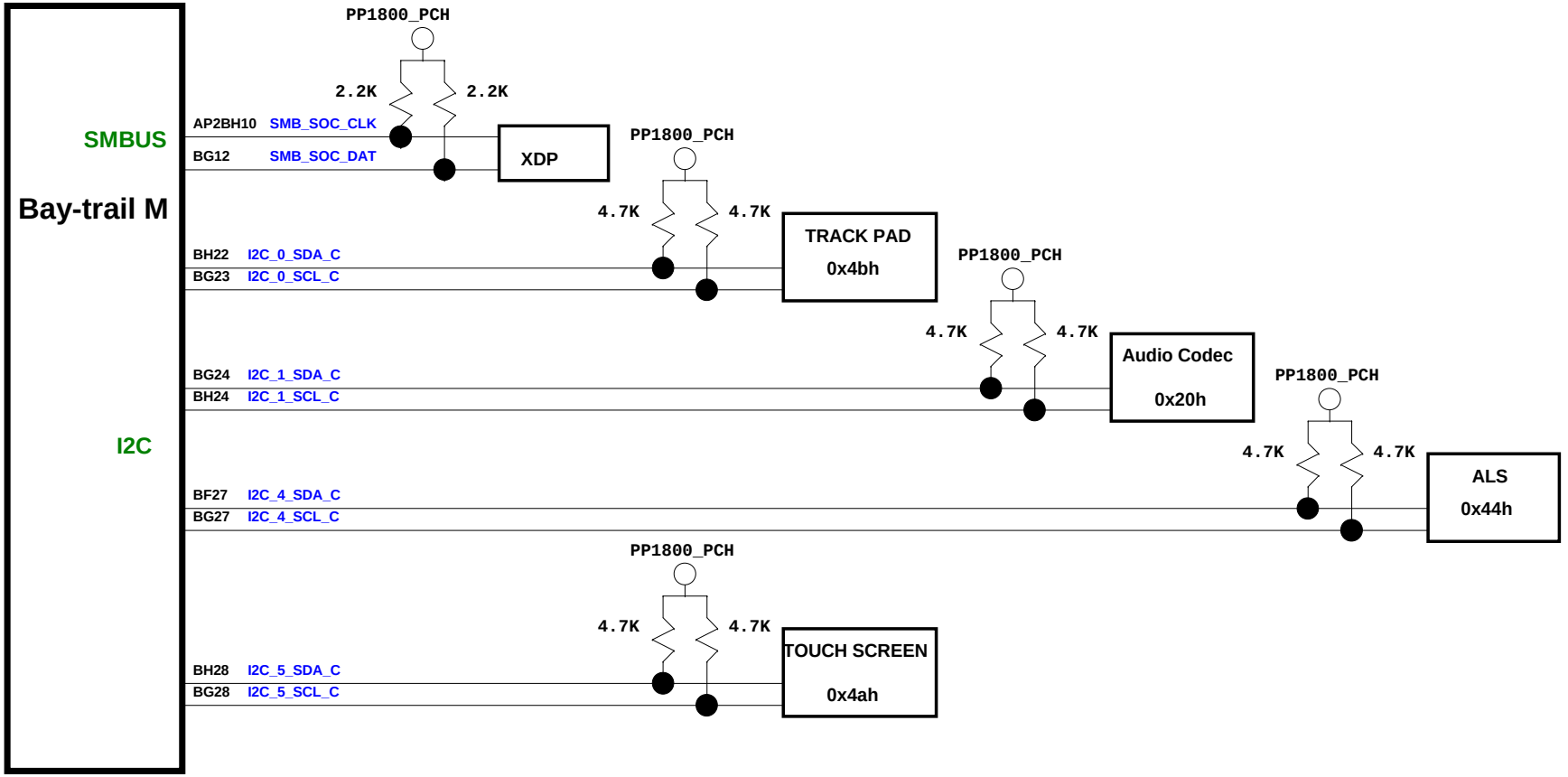
t6a : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (no PCIE device) 10ms -min (43-45)
t6b : Core Well stable to DRAM_CORE_PWROK and PMC_CORE_PWROK assertion (for power rails needed by pcie device) 99ms -min (43-45)

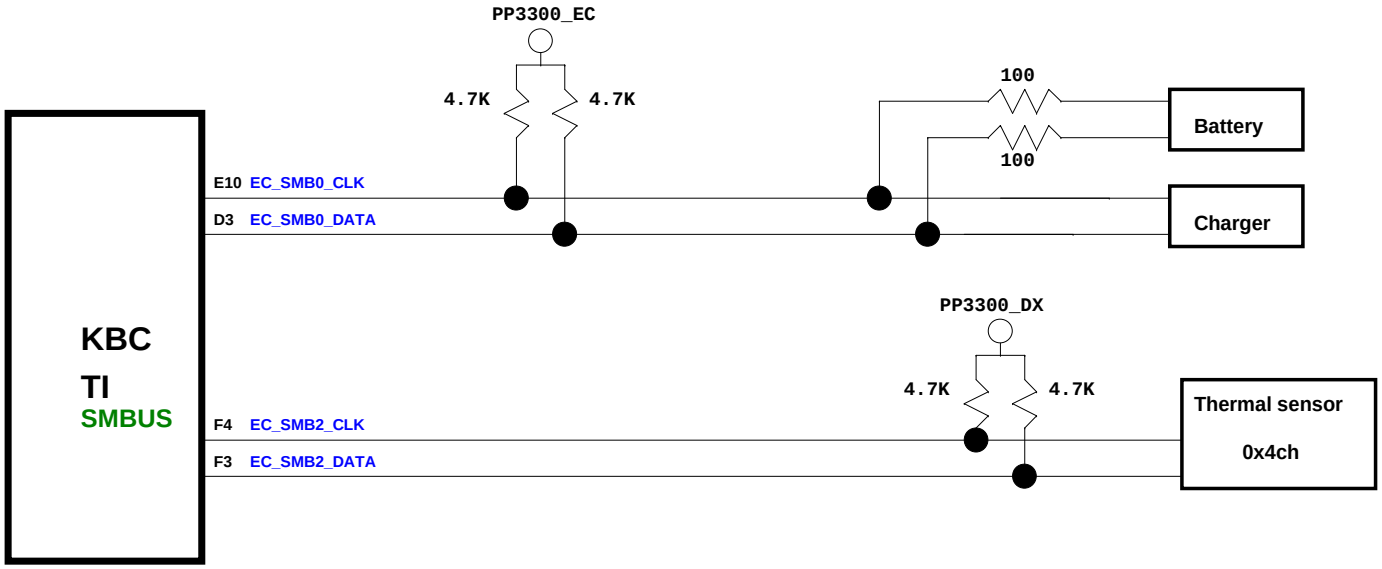
t7 : DRAM/PMC_CORE_PWROK to PMC_SUS_STAT# 1ms -min (45-46)

t8 : PMC_SUS_STAT# de-assertion to PMC_PLTRST# de-assertion 60us -min (46-47)

a 10us to 2000us delay is required between rails to avoid inrush current caused by multiple loads turning on simultaneously and fast charging of VR output decoupling

Quanta Computer Inc.
PROJECT : ZM8
Power Sequence
Rev 1A
Date: Thursday, September 25, 2014 Sheet 37 of 39

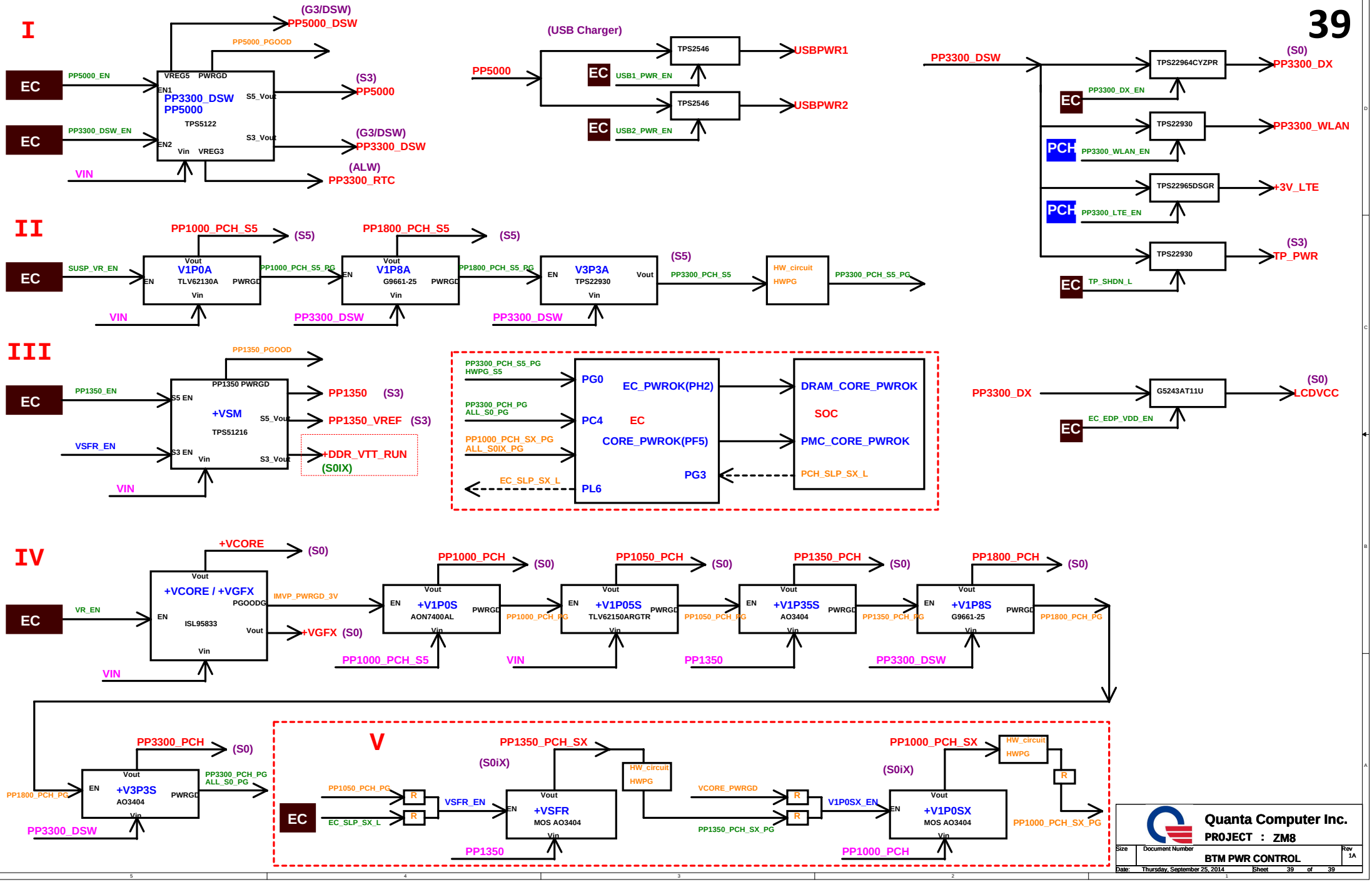




Quanta Computer Inc.
PROJECT : ZM8

Size	Document Number	Rev
	SMBUS_I2C	1A

Date: Thursday, September 25, 2014 Sheet 38 of 39


I
EC
PP5000_EN
VREG5 PWRGD
EN1
PP3300_DSW
PP5000
S5_Vout
TPS5122
S3_Vout
EN2
Vin VREG3
PP3300_DSW_EN
VIN
(G3/DSW)
PP5000_DSW
PP5000_PGOOD
(S3)
PP5000
(G3/DSW)
PP3300_DSW
(ALW)
PP3300_RTC
(USB Charger)
PP5000
TPS2546
USB1_PWR_EN
USBPWR1
TPS2546
USB2_PWR_EN
USBPWR2
PP3300_DSW
TPS22964CYZPR
(S0)
PP3300_DX
PP3300_DX_EN
PCH
PP3300_WLAN_EN
TPS22930
PP3300_WLAN
TPS22965DSGR
+3V_LTE
PP3300_LTE_EN
TPS22930
(S3)
TP_PWR
TP_SHDN_L
II
SUSP_VR_EN
Vout
V1P0A
EN
TLV62130A
PWRGD
Vin
PP1000_PCH_S5_PG
V1P8A
G9661-25
PP1800_PCH_S5_PG
V3P3A
TPS22930
PP3300_PCH_S5
HW_circuit
HWPG
PP3300_PCH_S5_PG
PP1000_PCH_S5
(S5)
PP1800_PCH_S5
(S5)
(S5)
VIN
PP3300_DSW
PP3300_DSW
III
PP1350_EN
PP1350_PGOOD
PP1350 PWRGD
S5 EN
+VSM
TPS51216
S5_Vout
S3 EN
Vin
S3_Vout
VSFR_EN
VIN
PP1350
(S3)
PP1350_VREF
(S3)
+DDR_VTT_RUN
(S0iX)
PP3300_PCH_S5_PG
HWPG_S5
PG0
EC_PWROK(PH2)
DRAM_CORE_PWROK
PP3300_PCH_PG
ALL_S0_PG
PC4
EC
SOC
PP1000_PCH_SX_PG
ALL_S0iX_PG
CORE_PWROK(PF5)
PMC_CORE_PWROK
PG3
PCH_SLP_SX_L
EC_SLP_SX_L
PL6
PP3300_DX
G5243AT11U
(S0)
LCDVCC
EC_EDP_VDD_EN
IV
+VCORE
(S0)
Vout
+VCORE / +VGFX
PGOODG
EN
ISL95833
Vout
Vin
VR_EN
VIN
IMVP_PWRGD_3V
+VGFX (S0)
PP1000_PCH
(S0)
Vout
EN
+V1P0S
AON7400AL
PWRGD
Vin
PP1000_PCH_PG
PP1000_PCH_S5
PP1050_PCH
(S0)
+V1P05S
TLV62150ARGTR
PP1050_PCH_PG
VIN
PP1350_PCH
(S0)
+V1P35S
AO3404
PP1350_PCH_PG
PP1350
PP1800_PCH
(S0)
+V1P8S
G9661-25
PP1800_PCH_PG
PP3300_DSW
PP3300_PCH
(S0)
+V3P3S
AO3404
PP3300_PCH_PG
ALL_S0_PG
PP1800_PCH_PG
PP3300_DSW
V
PP1350_PCH_SX
(S0iX)
HW_circuit
HWPG
PP1050_PCH_PG
R
R
EC_SLP_SX_L
VSFR_EN
+VSFR
MOS AO3404
PP1350
VCORE_PWRGD
R
R
PP1350_PCH_SX_PG
V1P0SX_EN
+V1P0SX
MOS AO3404
PP1000_PCH
PP1000_PCH_SX
(S0iX)
HW_circuit
HWPG
R
PP1000_PCH_SX_PG
Quanta Computer Inc.
PROJECT : ZM8
Size
Document Number
BTM PWR CONTROL
Rev
1A
Date: Thursday, September 25, 2014
Sheet 39 of 39