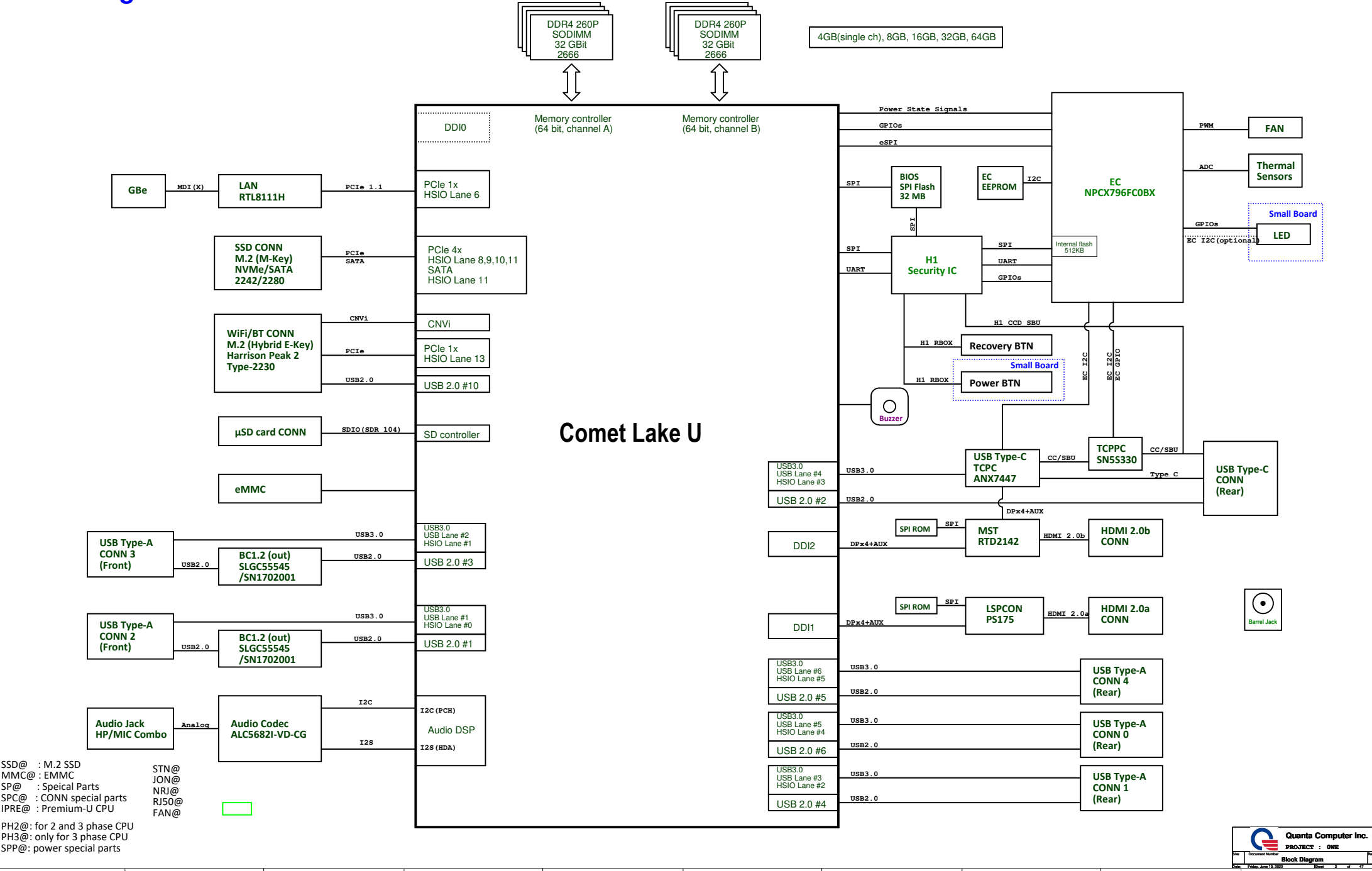


SHEET NO.	SHEET NAME
1	TABLE OF CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	USB BLOCK DIAGRAM
4	POWER TREE
5	POWER SEQUENCING
6	I2C MAP
7	CML: MEMORY
8	CML: DISPLAY
9	CML: USB/PCIE
10	CML: EMMC/HP/SD/CNVI/STRAPS
11	CML: ESPI/SPI/UART/I2C
12	CML: POWER SEQ
13	CML: CORE POWER
14	CML: PCH POWER
15	CML: GND
16	CML: DEBUG/RSVD
17	CML: POWER RAIL DECOUPLING
18	MEMORY CH A DDR4 SODIMM
19	MEMORY CH B DDR4 SODIMM
20	MEMORY DECOUPLING/TERM
21	LAN, SD CARD
22	SSD: NVME/SATA/EMMC
23	WIFI
24	AUDIO: HEADPHONE AMP
25	SPI ROM, EEPROM
26	H1
27	SERVO DEBUG
28	EC
29	POWER: 5V, 3.3V, 1.8V
30	POWER: VCCPRIM CORE, 1.05, VCCIO

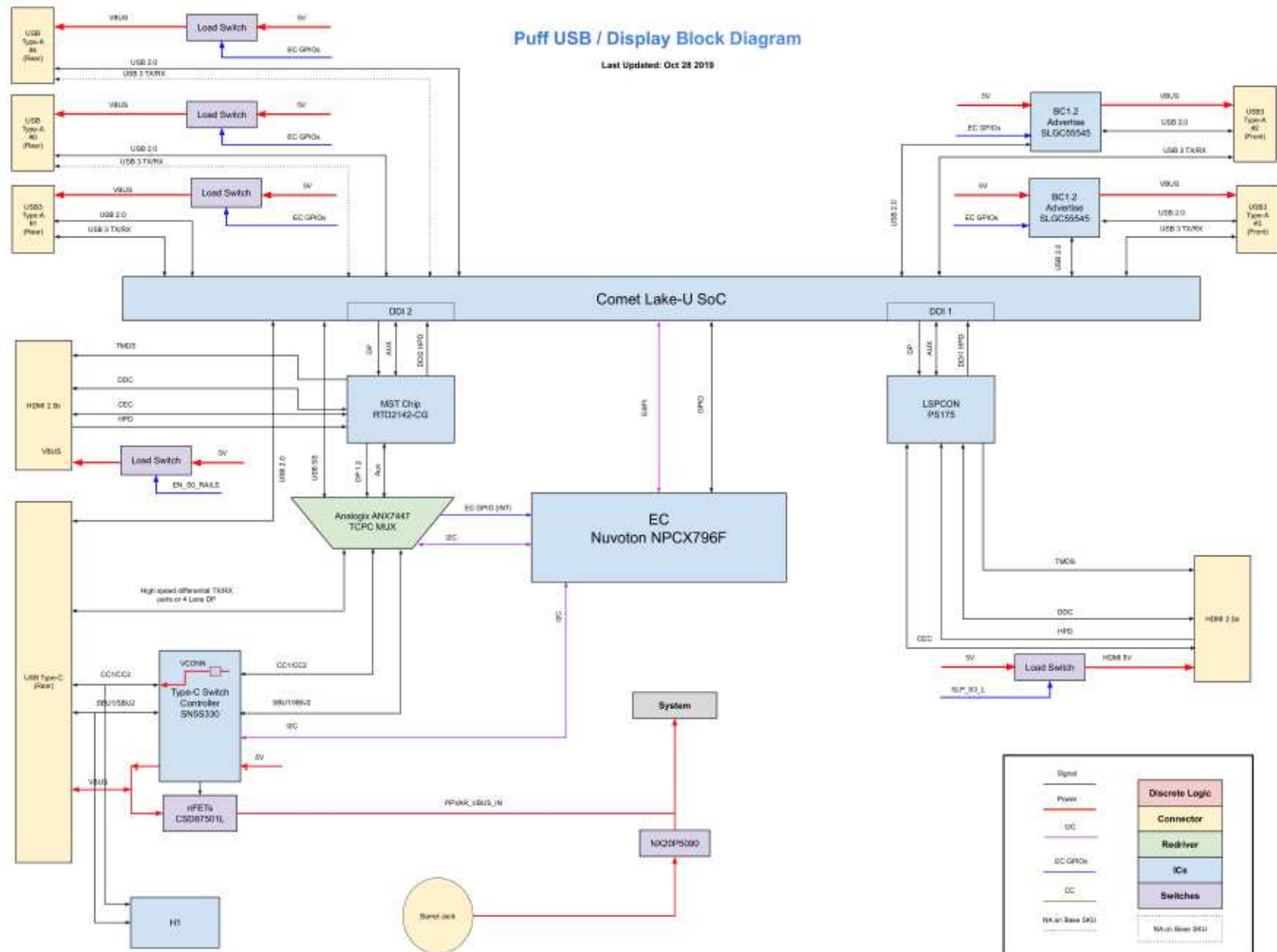
[illegible]

Block Diagram



Puff USB / Display Block Diagram

Last Updated: Oct 28 2019



Quanta Computer Inc.
PROJECT : 0WE

	Parent Rail	Separation	Rail	G3	S5	S3	S6ix	Peak Current	Devices	Enable	Enable From	Regulators	Comments
PPVAR_VBUS_IN	PPVAR_C0_VBUS or PPVAR_S3_AD0P	Load Switch											17.21V
VR	PP3300_G			ON	ON	ON	ON	7.620		ACOK		SYV236BRHC 4V-24V, 8A	
	PP3300_G	Direct	PP3300_G	ON	ON	ON	ON	0.052 PCH		ACOK			
	PP3300_G	Direct	PP3300_G	ON	ON	ON	ON	0.028 H1		ACOK			
	PP3300_G	Direct	PP3300_G	ON	ON	ON	ON	0.090 EC + 1TCPPG + 1TCPC		ACOK			
	PP3300_G	VR	PP2500_DRAM_U	OFF	OFF	ON	ON	1.136 DDR4, 16GB		SLP_S4_L	AP	TLV02565 5V, 2A	
	PP3300_G	VR	PP1800_A	OFF	ON	ON	ON	0.275		PQ_PP3300_A	EC	TLV02565 5V, 2A	
	PP3300_G	LDO	PP1800_EC	ON	ON	ON	ON	EC 1.8 Rail 3		ACOK			
	PP3300_G	Resistor	PP3300_SSD_A	OFF	ON	ON	ON	2.500 M.2 2280 SATA: 2.15A (17B) eMMC 250mA nvMe 2280: 1.7A (512 GB) nvMe 2280 2.5A (max)					OLD: Need active discharge OLD: Need reset to come from AP NEW: Don't Power Cycle SSD NEW: To support S3 as fallback enable from SLP_S3_L
	PP3300_G	Load Switch	PP3300_SD_0X	OFF	OFF	OFF	ON	0.400 SD Card		EN_PP3300_SD_0X	EC		Make sure to route FAULT
	PP3300_G	Load Switch	PP3300_MST	OFF	OFF	OFF	OFF	0.105 MST Hub		EN_PP_MST	AP		Use LS for proto and evaluate power Also only way to reset is POR
Load Switch	PP3300_G	Load Switch	PP3300_PCON_U	OFF	OFF	ON	ON	0.038 PCON		EN_A_RAILS	AP		PDB pin should take care of power RESET_H should take care of reset
	PP3300_G	Load Switch	PP3300_A	OFF	ON	ON	ON	3.116 PP3300_A Rail		EN_A_RAILS	EC		
	PP3300_A			OFF	ON	ON	ON	3.116		EN_A_RAILS	EC		
	PP3300_A	Resistor	PP3300_SOC_A	OFF	ON	ON	ON	0.211 Merged 3.3AOSW VCCPRM_3P3: 0.207A VCCDSW_3P3: 0.094A		EN_A_RAILS	EC		
	PP3300_A	Resistor	PP3300_WLAN_A	OFF	ON	ON	ON	2.000 Jefferson Peak (1.3A) Thunder Peak (1.5A) Hambrook Peak (2.0A)		EN_A_RAILS	EC		
	PP3300_A	Resistor	PP3300_DRAM_SPO_A	OFF	OFF	ON	ON	0.105 VDDSPD for DRAM		EN_A_RAILS	AP		
	PP3300_A	Resistor	PP3300_LAN_A	OFF	OFF	ON	ON	0.800 MAX RTL8111H-CG		EN_A_RAILS	AP		
	PP5000_A			OFF	ON	ON	ON	9.580		EN_PP5000_A	EC	SY8270CTMC, 5.5-23V, 16A max	iCie Reset pin. Grun's note
	PP5000_A	Load Switch	PPVAR_USB_C0_VBUS	OFF	OFF	ON	ON	3.740 Type-C Port 0 (PPC max at 3.3A)		EN_USB_C0_SV_OUT	EC		
	PP5000_A	Load Switch	PP0000_USB_A0_VBUS	OFF	OFF	ON	ON	1.800 Type-A Port 0 ((@ 0.9A or 1.7A max) Front		EN_USB_A_SV	EC		Make it individual
VR	PP5000_A	Load Switch	PPVAR_USB_A1_VBUS	OFF	OFF	ON	ON	1.800 Type-A Port 1 ((@ 0.9A or 1.7A max) Front		EN_USB_A_SV	EC		Make it individual
	PP5000_A	Load Switch	PP0000_USB_A2_VBUS	OFF	OFF	ON	ON	1.075 Type-A Port 2 ((@ 0.9A) Rear		EN_USB_A_SV	EC		Make it individual
	PP5000_A	Load Switch	PP0000_USB_A3_VBUS	OFF	OFF	ON	ON	1.075 Type-A Port 3 ((@ 0.9A) Rear		EN_USB_A_SV	EC		Make it individual
	PP5000_A	Load Switch	PP0000_USB_A4_VBUS	OFF	OFF	ON	ON	1.075 Type-A Port 3 ((@ 0.9A) Rear		EN_USB_A_SV	EC		Make it individual
	PP5000_A	Load Switch	VCONN_C0	OFF	OFF	ON	ON	0.550 VCONN C0 ((@0.3 or .55A max each)		EC_DC_USB_C0_PD_***	EC		
	VR	PP1100_MST	PP1100_MST	OFF	OFF	OFF	OFF	0.285 MST Hub					Use LS for proto and evaluate power Use PWM to turn off FAN
	PP5000_A	Resistor	PP0000_FAN	OFF	OFF	OFF	OFF	0.500 Fan		EC_FAN_PWM	EC		LS required because of OCP
	PP5000_A	Load Switch	PP0000_HDMI	OFF	OFF	OFF	OFF	1.100 HDMI (500mA per port)		EN_S0_RAILS	EC		
	PP1800_A			OFF	ON	ON	ON	0.454		SLP_SUS_L	AP	TLV02565 5V, 2A	
	PP1800_A	Resistor	PP1800_HP_A	OFF	ON	ON	ON	0.050 Headphone Jack (0.05A)		SLP_SUS_L	AP		
VR	PP1800_A	Resistor	PP1800_SOC_A	OFF	ON	ON	ON	0.134 PCH Rail (0.7A for WHL)		SLP_SUS_L	AP		
	PP1800_A	Resistor	PP1800_EMMC_A	OFF	ON	ON	ON	0.270 eMMC I/O rail		SLP_SUS_L	AP		
	PPVAR_VPRIM_CORE_A	Direct	PPVAR_PRIM_CORE_A	OFF	ON	ON	ON	4.240 PCH Core (0.73 - 1.05A)		PQ_PP1800_A	REQ	NB69200, 28V, 6.5A	
	PP1050_A			OFF	ON	ON	ON	5.057		PQ_PPVAR_VPRIM_CORE_A	AP	NB69200, 28V, 6.5A	
	PP1050_A	Direct	PP1050_A	OFF	ON	ON	ON	4.887 PCH		PQ_PPVAR_VPRIM_CORE_A	AP		
	PP1050_A	Load Switch	PP1050_ST_S	OFF	OFF	OFF	ON	0.340 CPU: Sustain voltage + PLL		SLP_S3_L	AP		
	PP1050_A	Load Switch	PP1050_STG_S0	OFF	OFF	OFF	OFF	0.050 CPU: Sustain voltage for standby		VCCSTG_EN (EN_S0_RAILS)	SLG		
	PP1200_U			OFF	ON	ON	ON	11.673		SLP_S4_L	AP	SYV010, 4-26V 12A pk 15A cont.	
	PP1200_U	Direct	PP1200_DRAM_U	OFF	OFF	ON	ON	10.500 DDR4 (64GB) (~7.3A) CPU (3.2A)		SLP_S4_L	AP		
	PP1200_U	Load Switch	PP1200_PLLOC_S0	OFF	OFF	OFF	OFF	0.170 CPU: Processor PLLs (0.12 for WHL)		SLP_S3_L && CPU_C10_GATE_L	AP		
VR	PP1200_U	LDO	PP0000_DRAM_U	OFF	OFF	ON	ON	0.500		TBD	AP		PDB pin should take care of power
	PP1200_U	Resistor	PP1200_PCON_U	OFF	OFF	OFF	OFF	0.502 PCON 5.94Gbps HDMI output		PDB pin not name here			
	PP2500_DRAM_U			OFF	OFF	ON	ON	1.260		SLP_S4_L	AP	TLV02565 5V, 2A	
	PP2500_DRAM_U	Direct	PP2500_DRAM_U	OFF	OFF	ON	ON	1.200 DDR4 (64GB) (~1.2A)		SLP_S4_L	AP		
	PP0000_DRAM_U			OFF	OFF	ON	ON	0.500		SLP_S4_L		SYV010	
	PP0000_DRAM_U	Direct	PP0000_DRAM_U	OFF	OFF	ON	ON	0.500 DDR4 termination		SLP_S4_L			
	PP0000_VCCIO			OFF	OFF	OFF	ON	3.300 CPU		SLP_S3_L && VDDQ_PG			
	PP0000_VCCIO	Direct	PP0000_VCCIO	OFF	OFF	OFF	ON	3.300 CPU					
	PPVAR_VCC			OFF	OFF	OFF	OFF	65.000				MP06041GQVT-Z, 3 phase	
	PPVAR_VCC	Direct	PPVAR_VCC	OFF	OFF	OFF	OFF	65.000 CPU: Core 75A for 2+2 70A for Baseline 4+2, 6+2 85A for Performance 4+2, 6+2		SVID			
PMIC IMVP8	PPVAR_GT			OFF	OFF	OFF	OFF	31.000				MP06041GQVT-Z	
	PPVAR_GT	Direct	PPVAR_GT	OFF	OFF	OFF	OFF	31.000 CPU: Graphics		SVID			
	PPVAR_SA			OFF	OFF	OFF	OFF	6.000				MP06041GQVT-Z	
	PPVAR_SA	Direct	PPVAR_SA	OFF	OFF	OFF	OFF	6.000 CPU: SA		SVID			

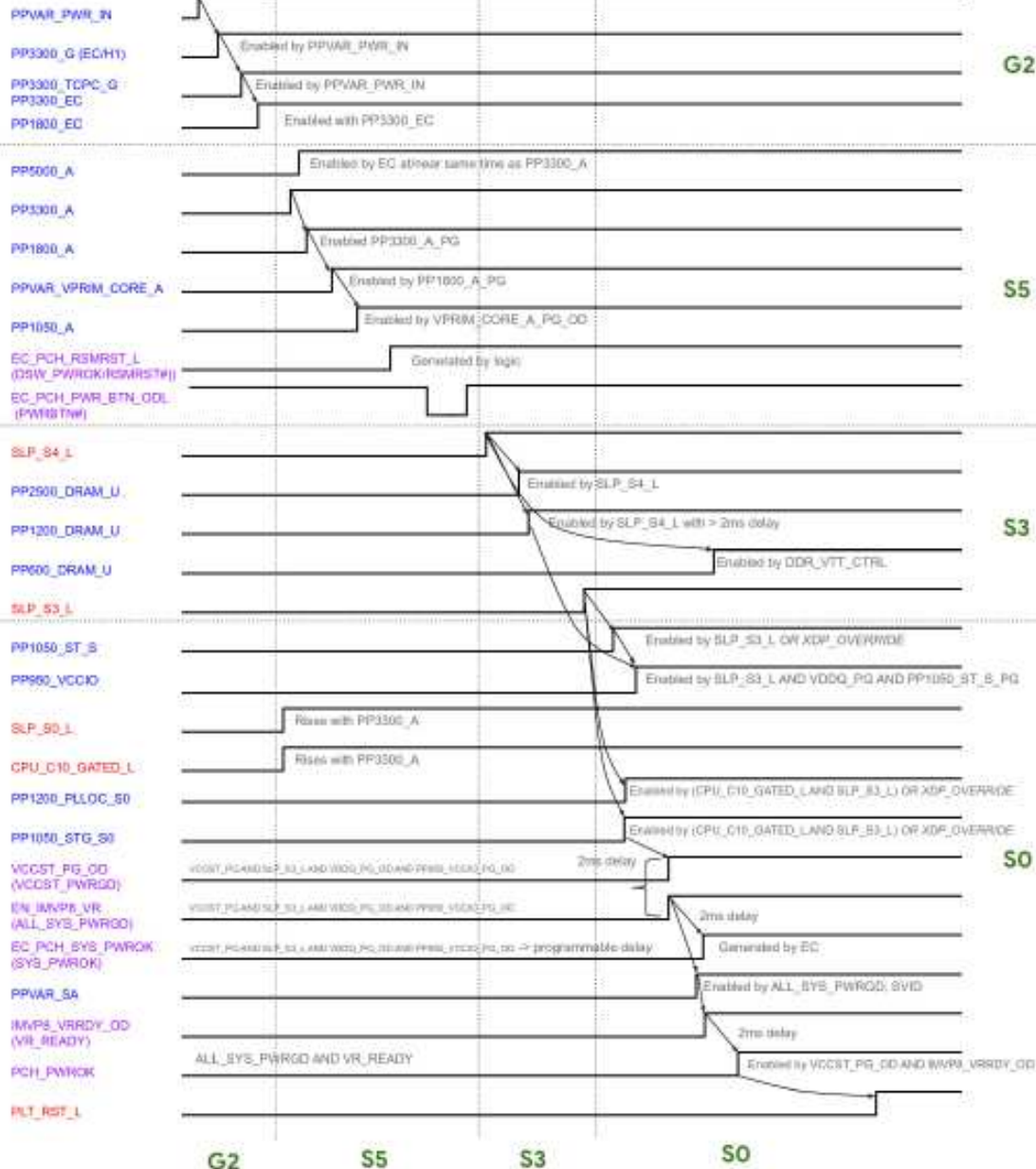


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PROJECT : OWE

POWER TREE

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Date:	Thursday, June 11, 2020	Sheet 4 of 47



Power Rail
 Signal from PCH
 Signal from Platform (EC)

Puff Power Sequencing

Updated: Sept 11 2019



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PROJECT : OWE

Size	Document Number	Rev 1A
Date: Thursday, June 11, 2020	Sheet 5 of 47	

POWER SEQUENCING

Puff I2C Map

Updated: Sept 11 2019

LEGEND

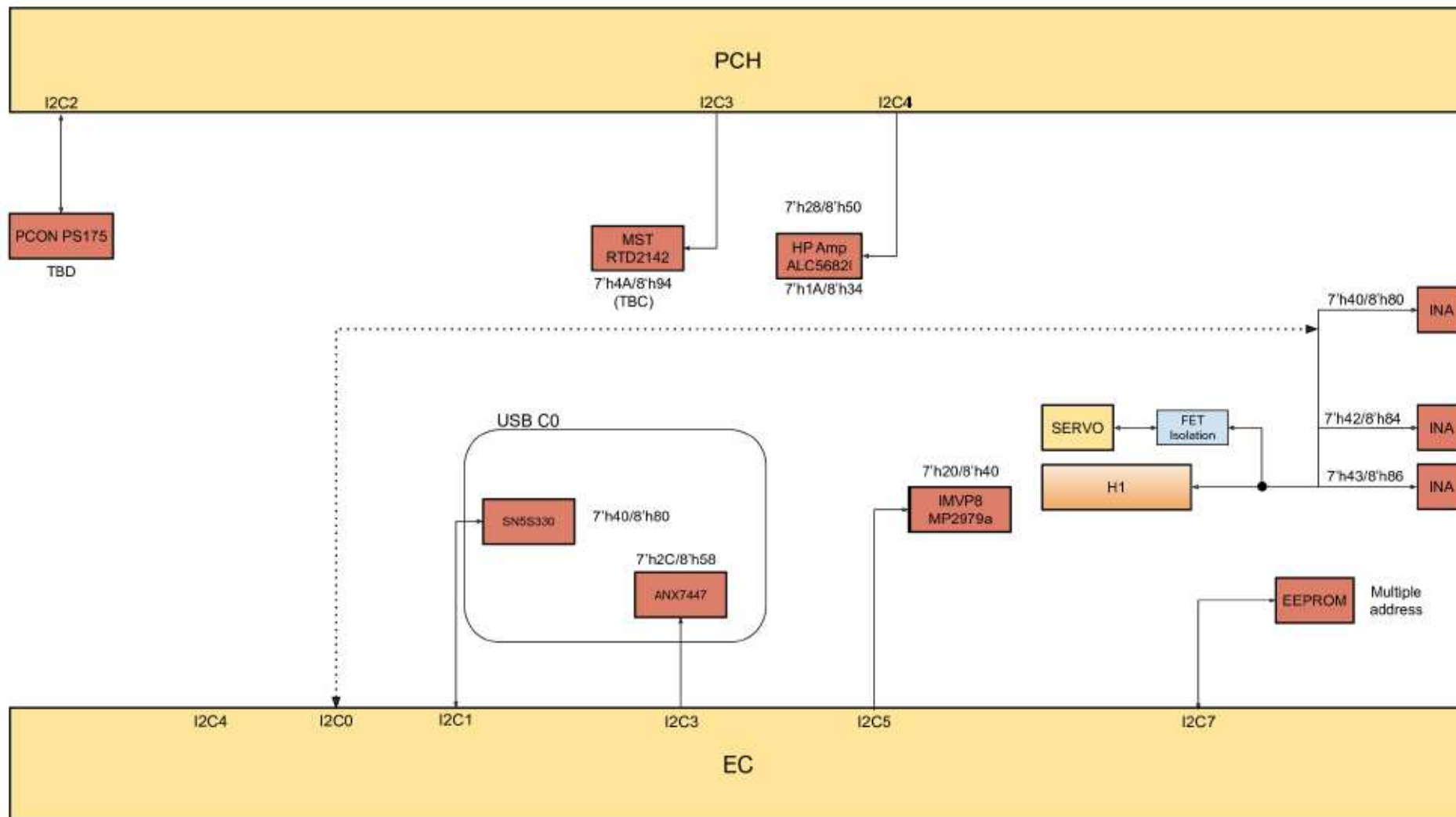
I2C Master
& Slave

I2C Master

I2C Slaves

Unstuffed in
P0

I2C addresses given in both 7 and 8 bit forms



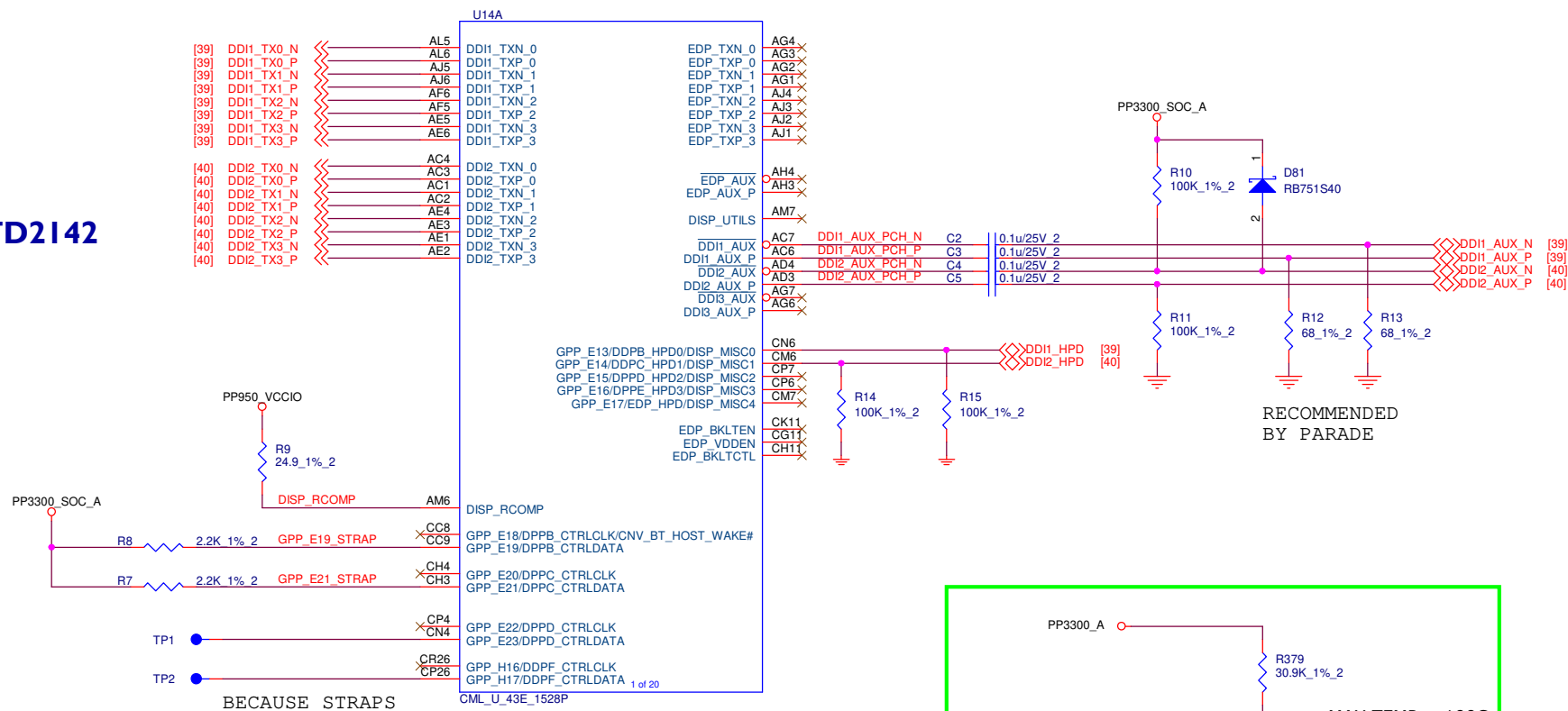
Quanta Computer Inc.

PROJECT : OWE

Size	Document Number	Rev 1A
Date: Thursday, June 11, 2020	I2C MAP	Sheet 6 of 47

**PORT B
to PSI175**

**PORT C
to MST RTD2142**



PP950_VCCIO [8,13,17,30]
PP3300_SOC_A [8,9,10,11,12,14,22,26,35]



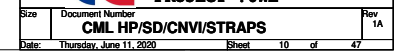
Quanta Computer Inc.

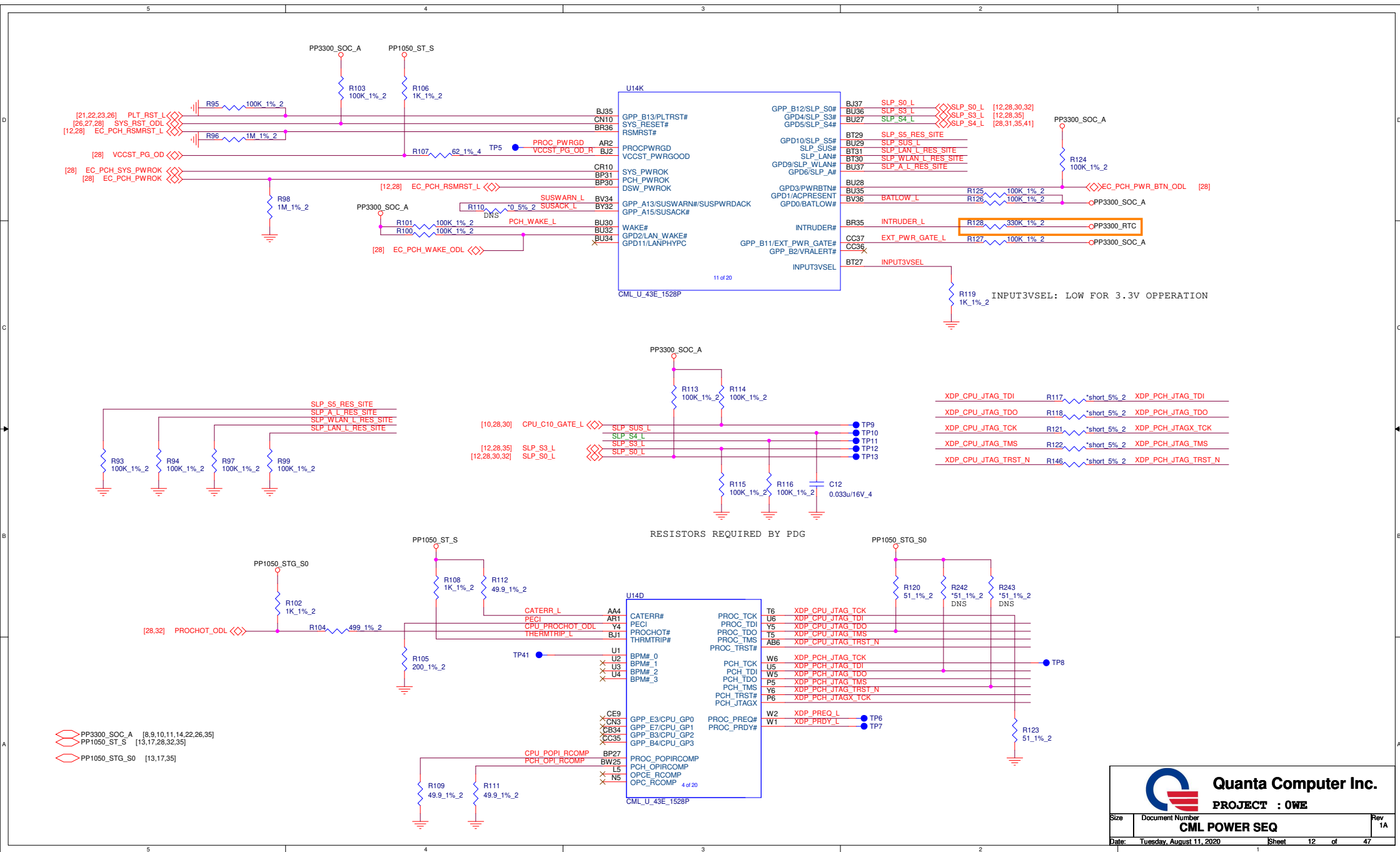
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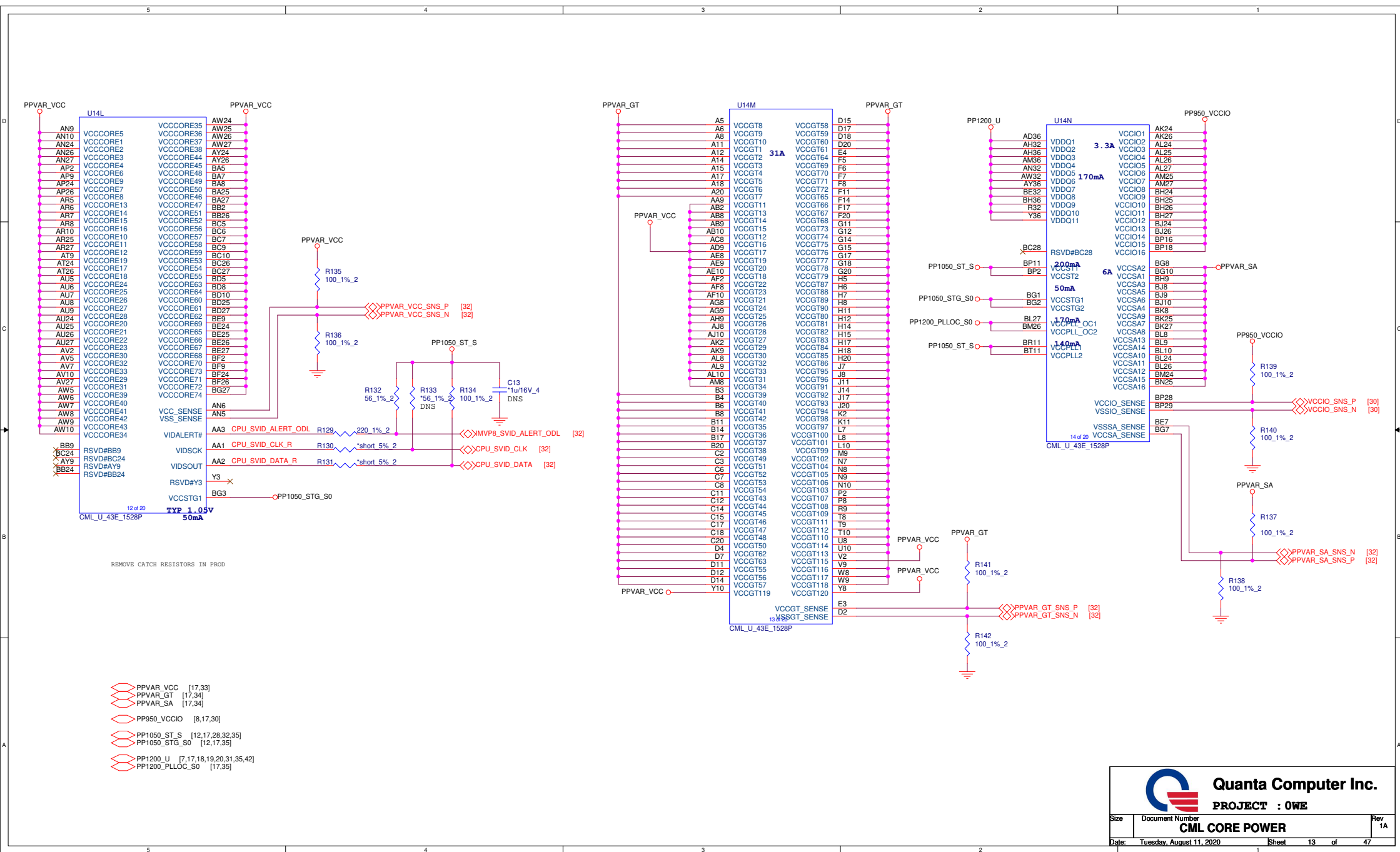
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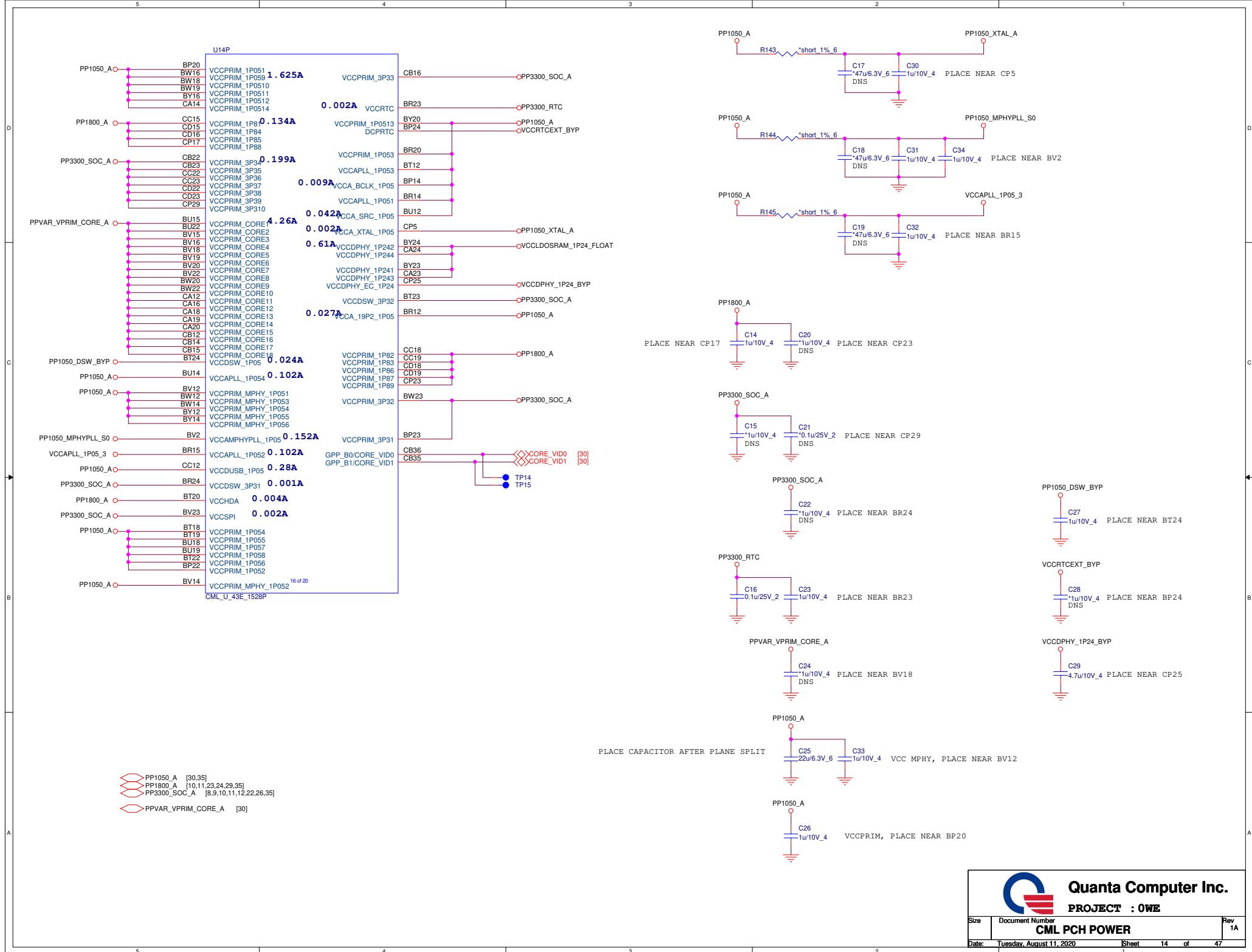
Rev
1A

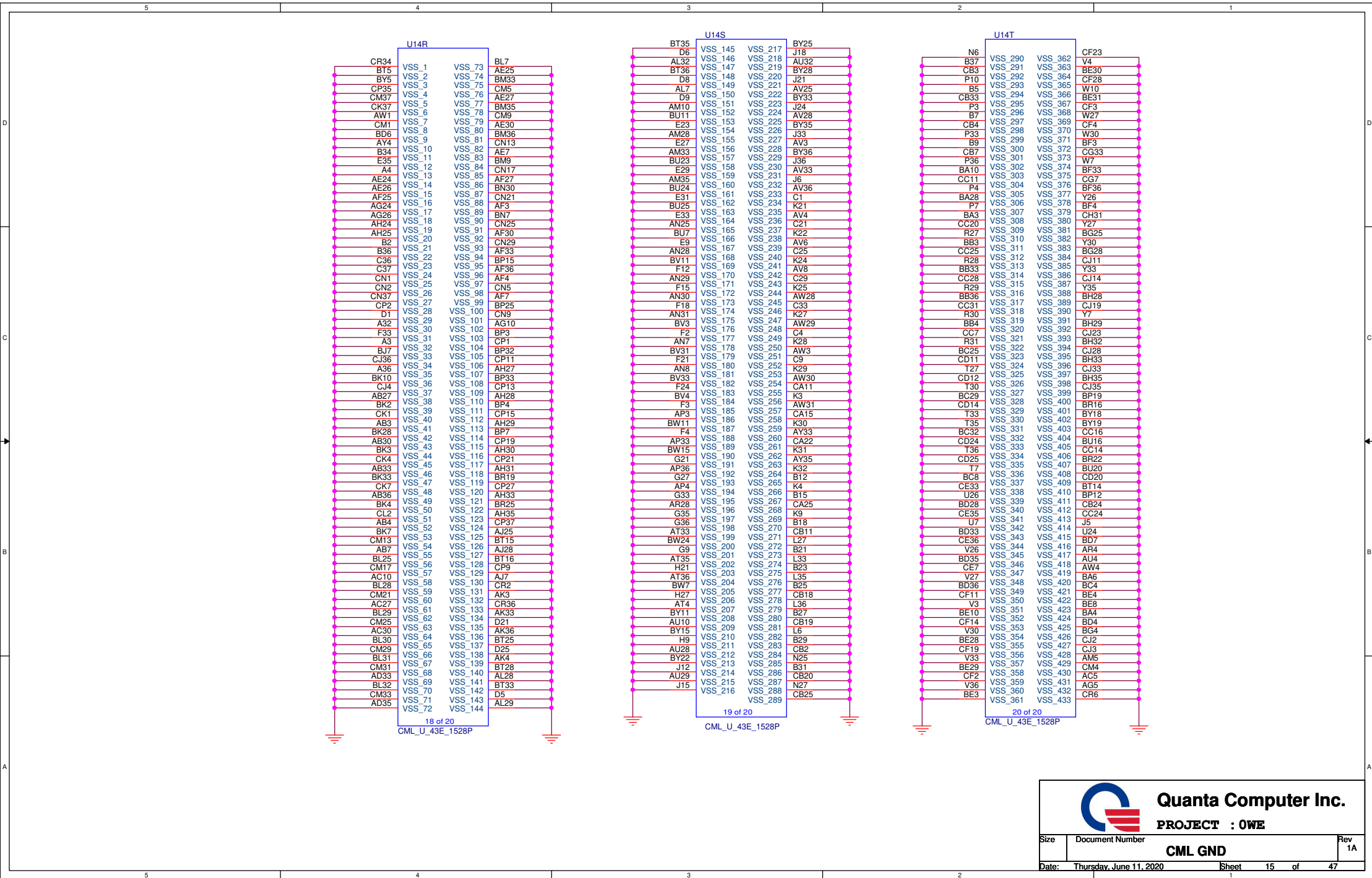
Date: Thursday, June 11, 2020 Sheet 8 of 47



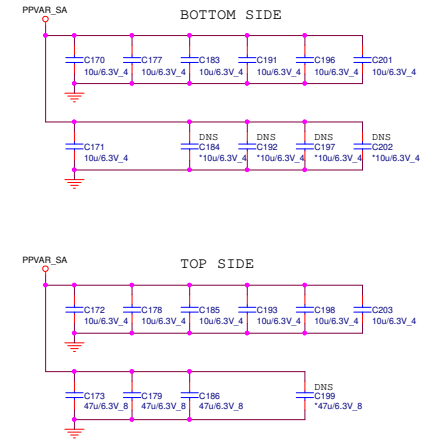
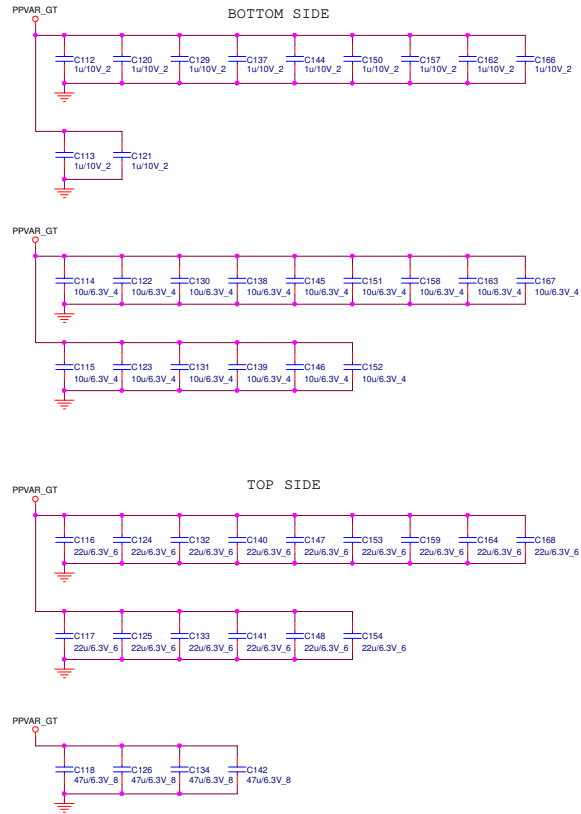








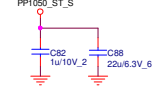
CPU DECOUPLING



BOTTOM SIDE VCCPLL

EITHER SIDE VCCPLL

TOP SIDE



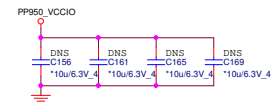
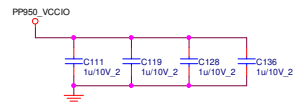
TOP SIDE VCCPLL

TOP SIDE



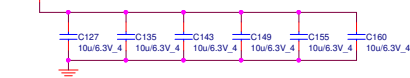
TOP SIDE

PP950_VCCIO

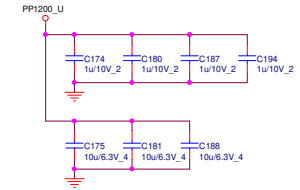


PP950_VCCIO

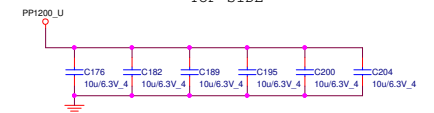
EITHER SIDE



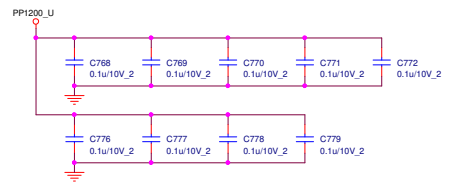
BOTTOM SIDE



TOP SIDE



For SI

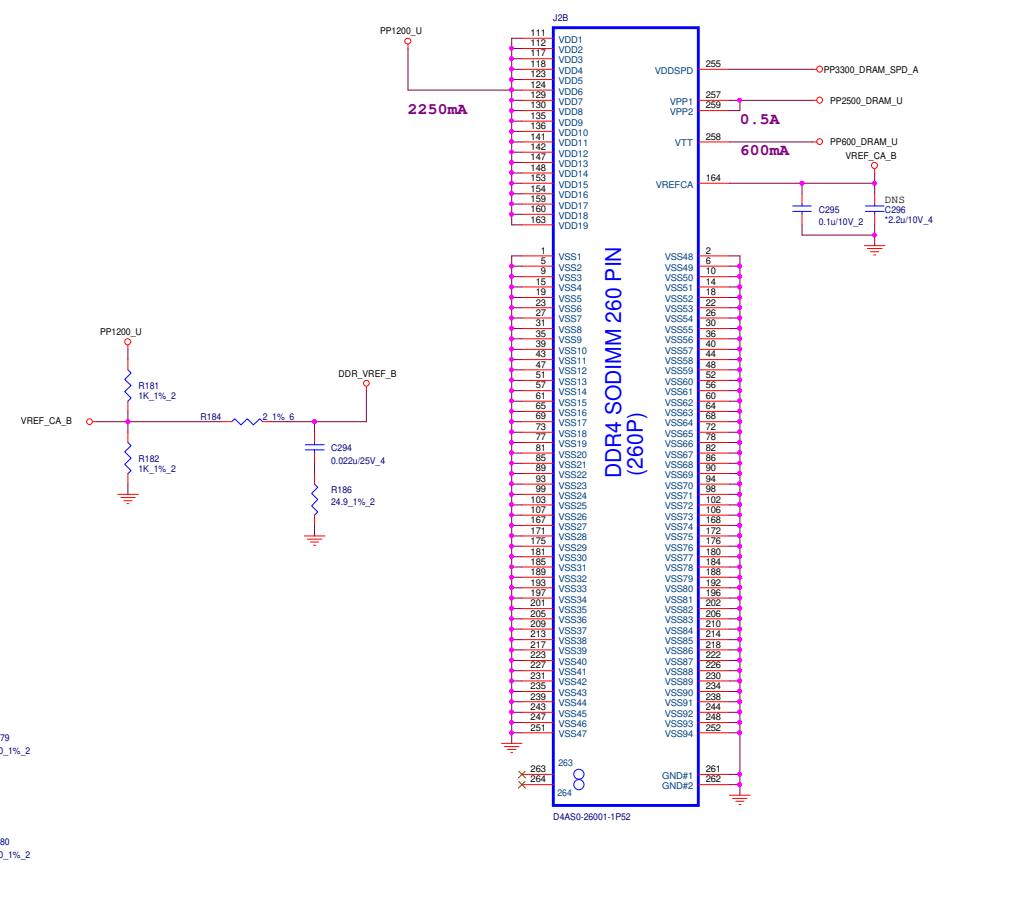
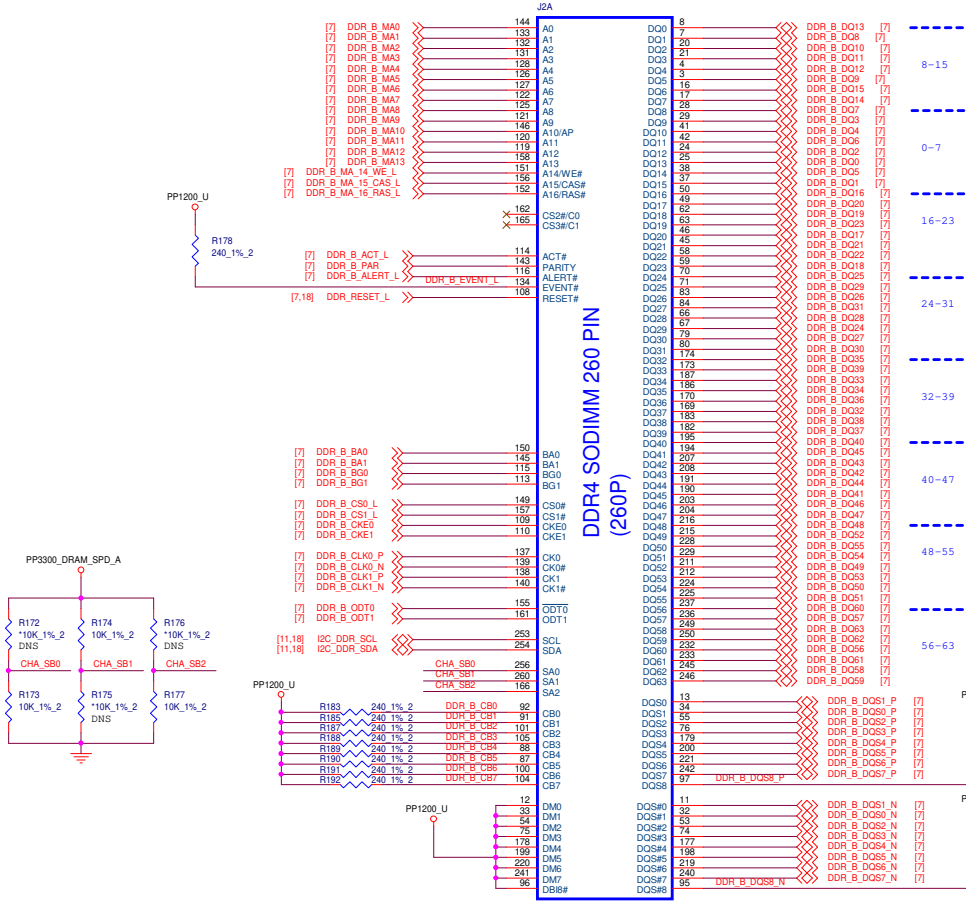


- PPVAR_VCC [13,33]
- PPVAR_GT [13,34]
- PPVAR_SA [13,34]
- PP1200_PLLC_S0 [13,35]
- PP1200_U [7,13,18,19,20,31,35,42]
- PP1050_ST_S [12,13,26,32,35]
- PP1050_STG_S0 [12,13,35]
- PP950_VCCIO [8,13,35]

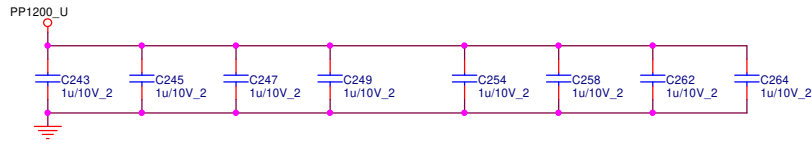
PP3300_DRAM_SPD_A [11,19,20,35]
 PP2500_DRAM_U [19,20,31,42]
 PP1200_U [7,13,17,19,20,31,35,42]
 PP600_DRAM_U [19,20,31]
 DDR_VREF_A [7]

D4AS0-26001-1P92

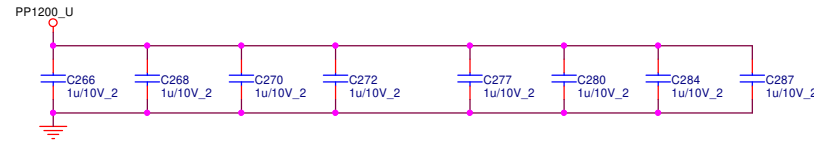
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VDDQ DECOUPLING

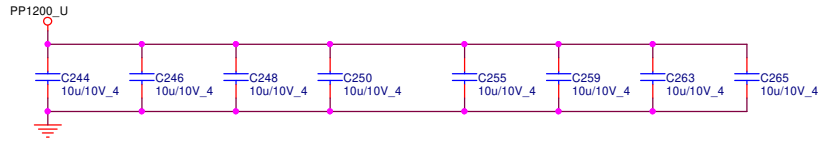
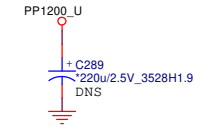


CHANNEL A

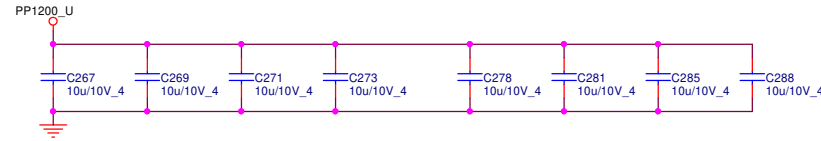


CHANNEL B

4 pcs PER EACH SIDE OF DIMM, CLOSE TO VDD PINS

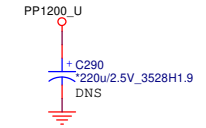


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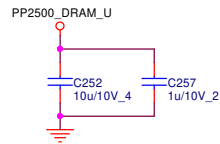


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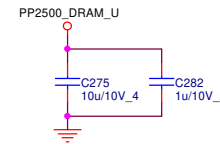
4 pcs PER EACH SIDE OF DIMM, CLOSE TO VDD PINS



VPP DECOUPLING



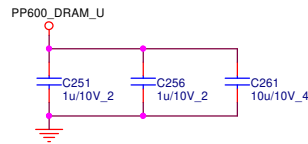
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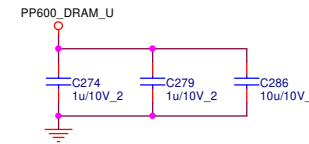
CHANNEL B

DIMM PIN SIDE, ONE CAP PER DIMM

VTT DECOUPLING



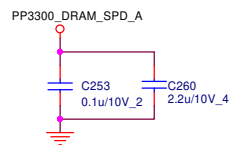
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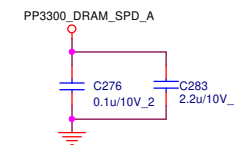
CHANNEL B

PLACE ON VTT PLANE CLOSE TO DIMM

VDDSPD DECOUPLING



CHANNEL A

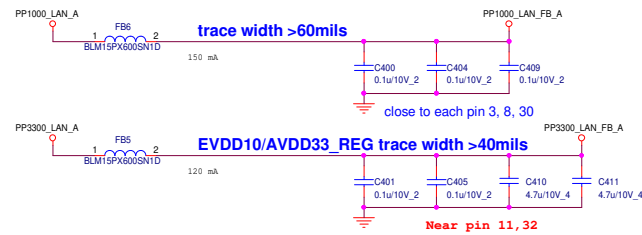
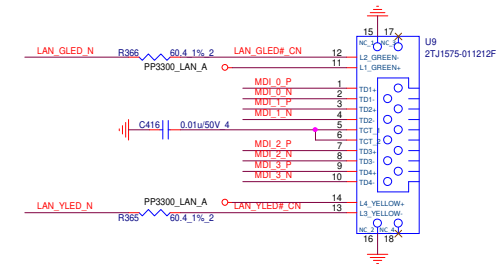
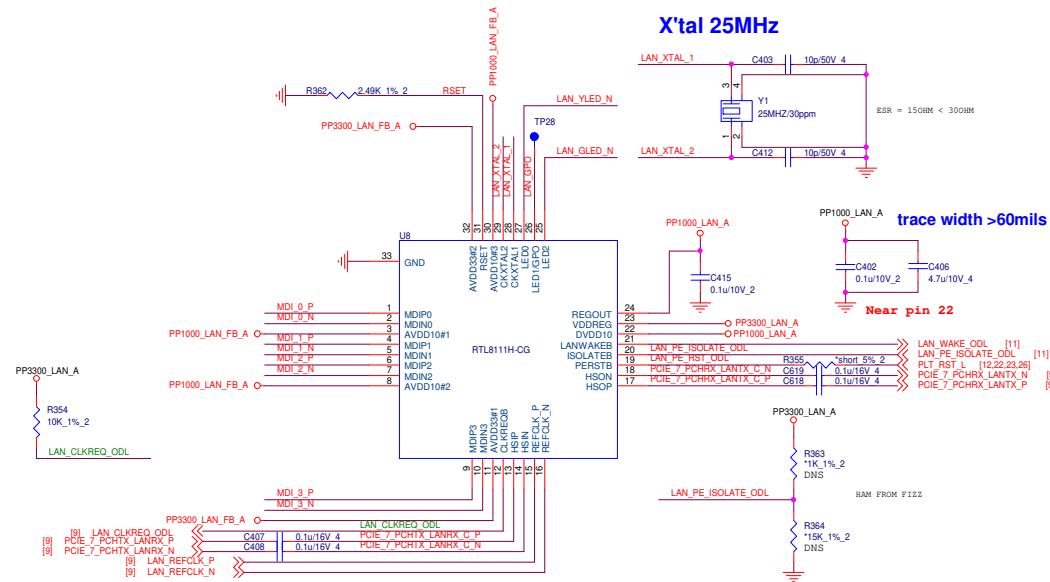
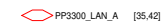


CHANNEL B

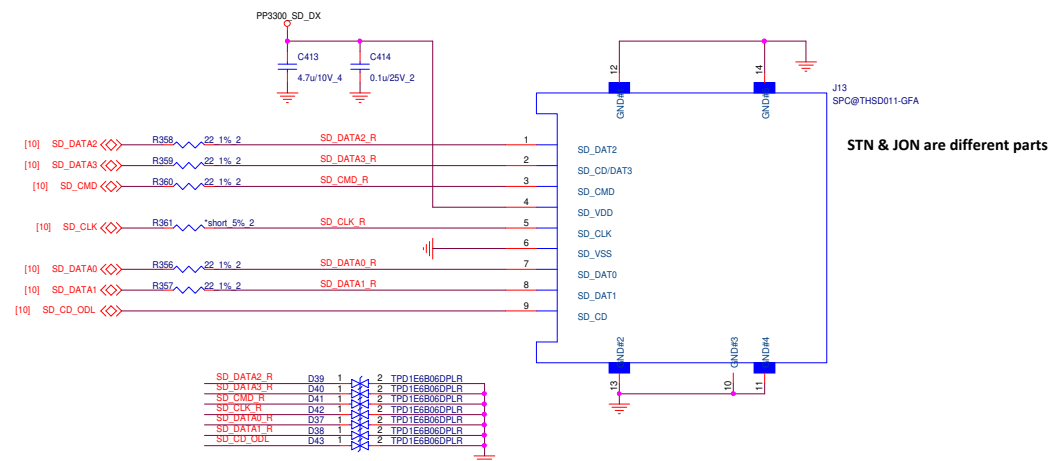
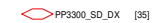
PLACE ON VTT PLANE CLOSE TO DIMM

PP1200_U [7,13,17,18,19,31,35,42]
PP2500_DRAM_U [18,19,31,42]
PP600_DRAM_U [18,19,31]
PP3300_DRAM_SPD_A [11,18,19,35]

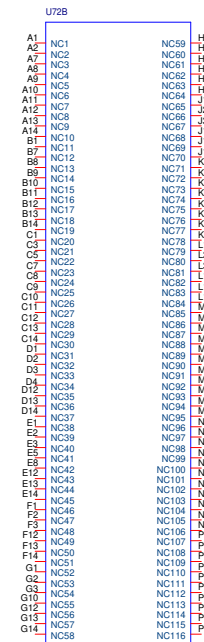
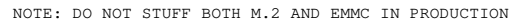
LAN



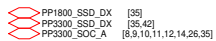
3 MICRO SD CARD (CRD)



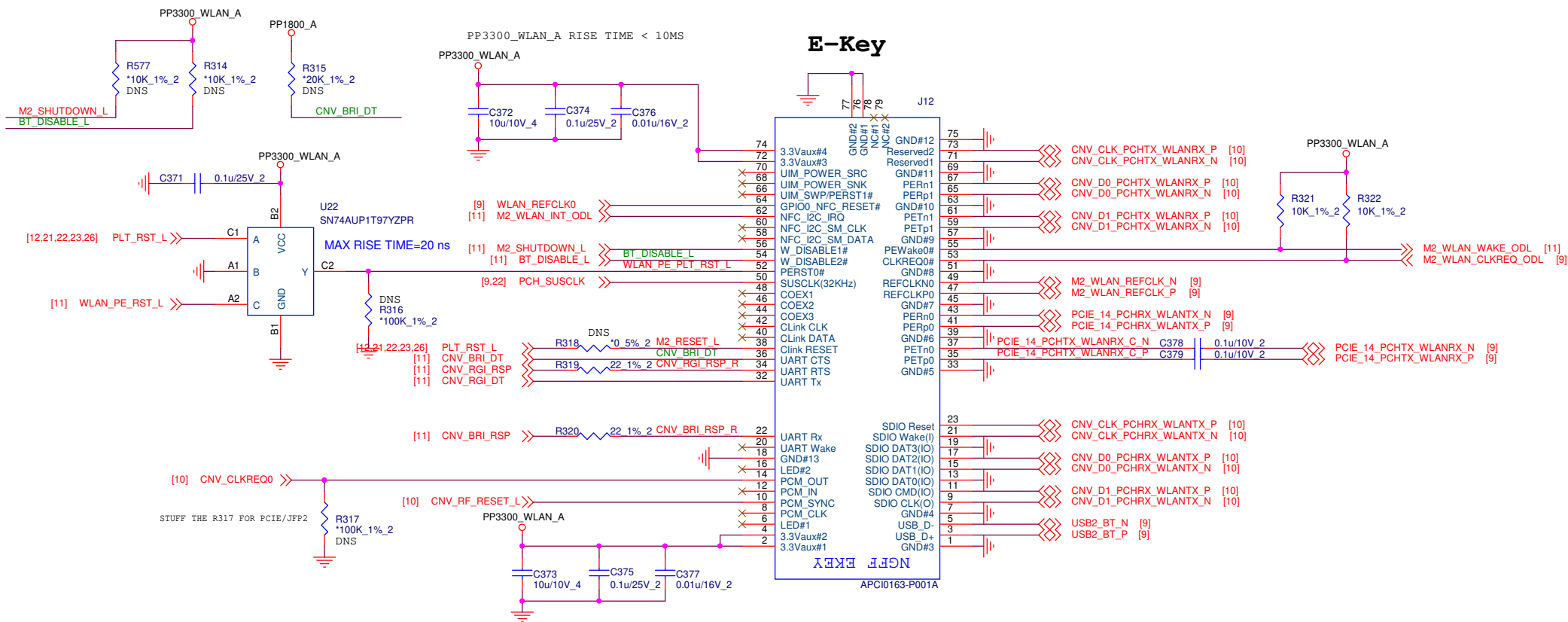
eMMC



MMC@H26M62002JPR



NGFF_M.2 WiFi & BT (NGF)

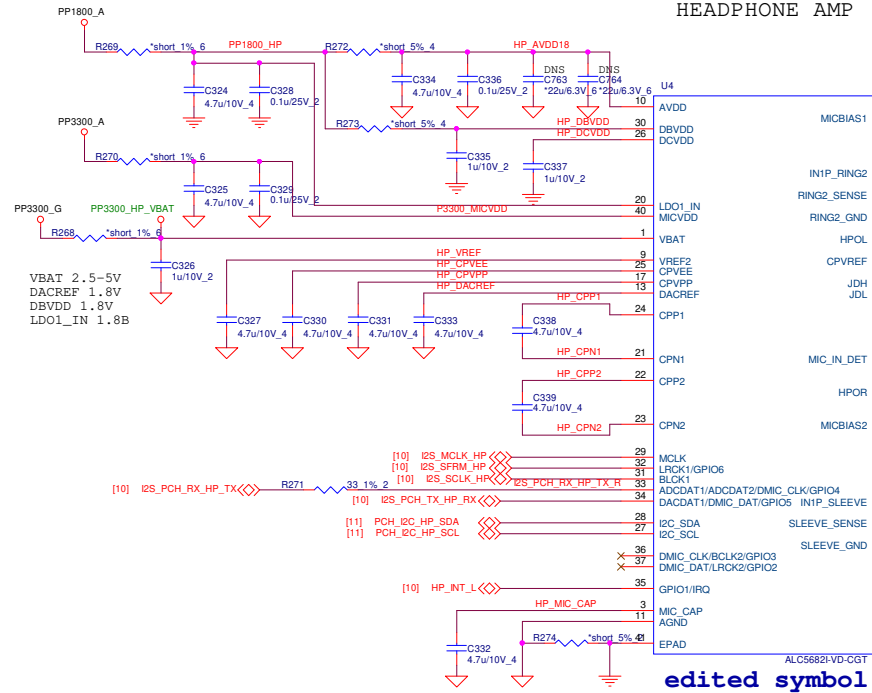


PP3300_WLAN_A [35,42]
PP1800_A [10,11,14,24,29,35]

ADO

VBAT ON EC RAIL TO REDUCE 60HZ
POWERED SPEAKER NOISE
OTHER POWER ON SOC RAILS TO PREVENT LEAKEGE

HEADPHONE AMP



LAYOUT NOTES

ROUTE HP_RING2 AND HP_RING2_SENSE DIFFERENTIALLY
ROUTE HP_SLEEVE AND HP_SLEEVE_SENSE DIFFERENTIALLY

combo jack
Normal open

edited symbol

FINE TUNE RESISTOR STUFFING FOR EMI

PP1800_A [10,11,14,23,29,35]
PP3300_A [7,8,11,25,26,27,28,30,31,32,33,34,35,41,42]
PP3300_G [9,22,25,26,27,28,29,35,36,41,42]

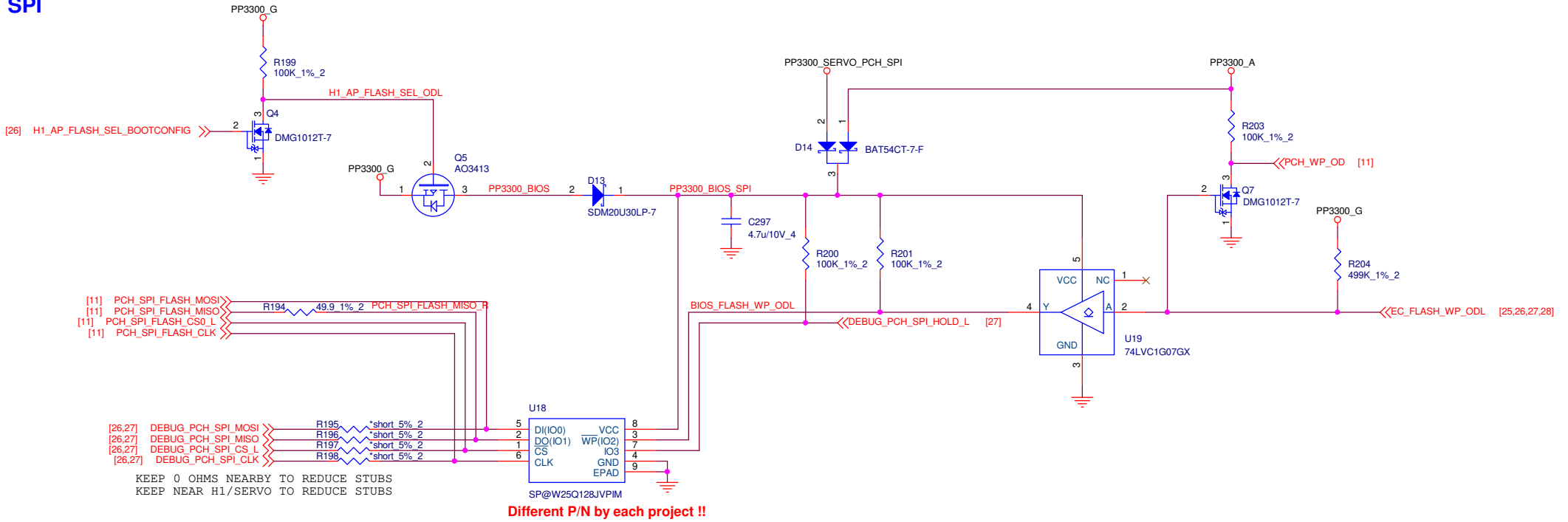


Quanta Computer Inc.

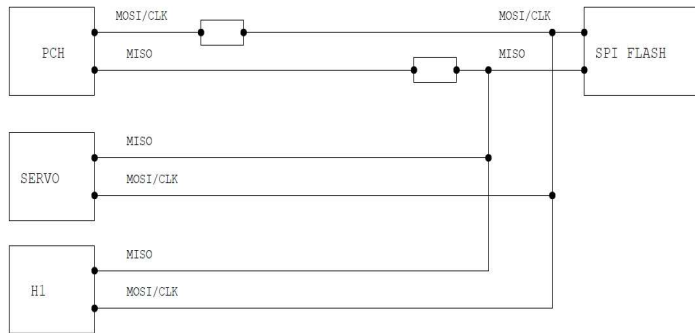
PROJECT : OWE

Size	Document Number	Rev
	AUDIO HEADPHONE AMP	1A
Date	Tuesday, August 11, 2020	Sheet 24 of 47

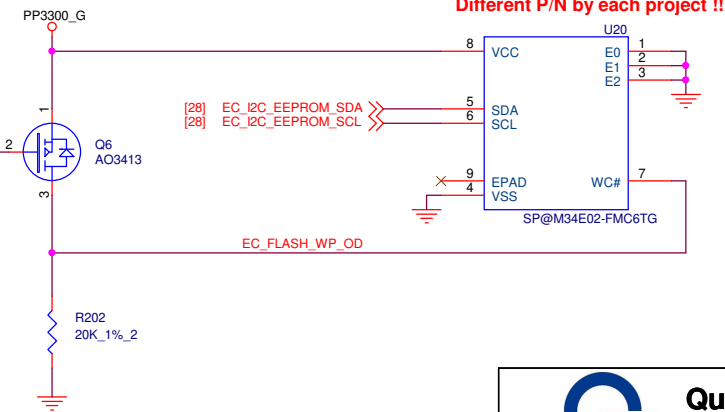
SPI



Different P/N by each project !!



[25,26,27,28] EC_FLASH_WP_ODL >>

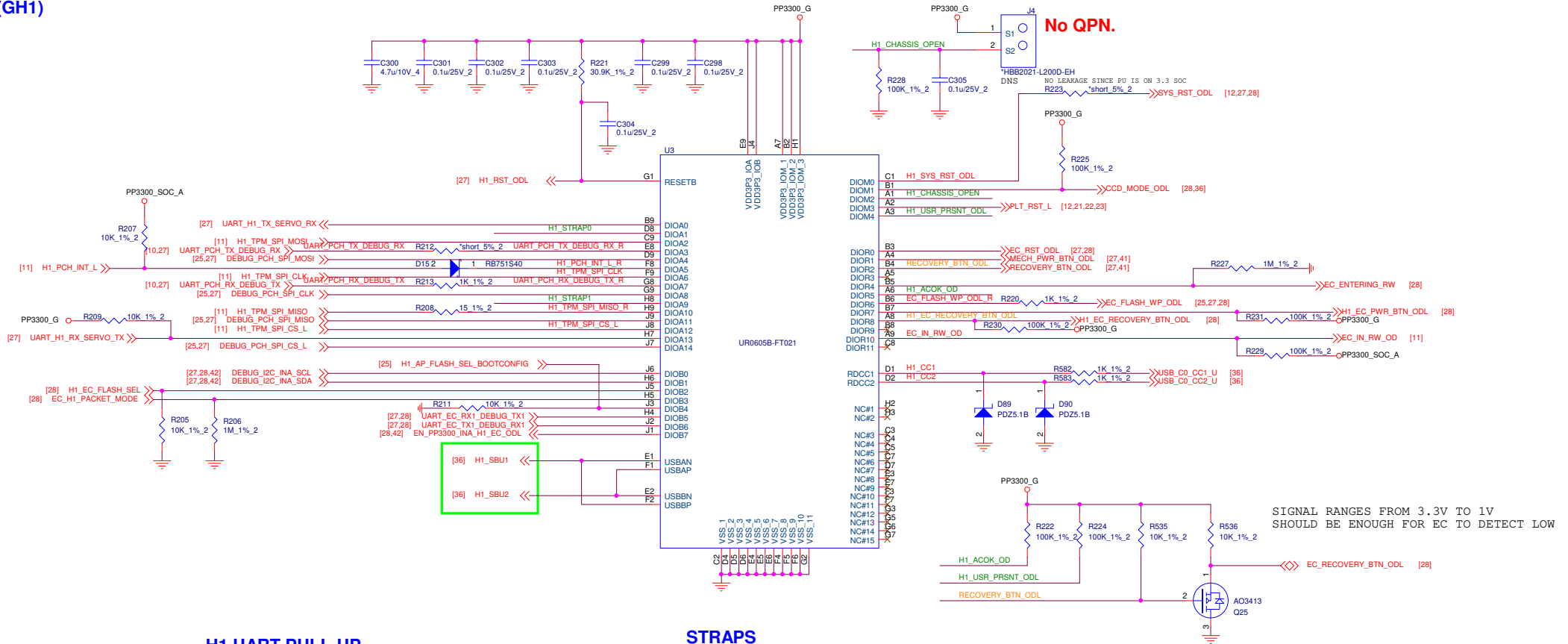


PP3300_G [9,22,24,26,27,28,29,35,36,41,42]

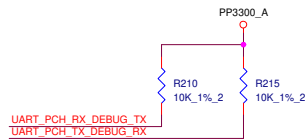
PP3300_SERVO_PCH_SPI [27]

PP3300_A [7,8,11,24,26,27,28,30,31,32,33,34,35,41,42]

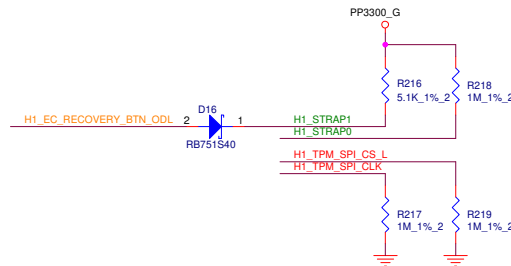
(GH1)



H1 UART PULL-UP



STRAPS



STRAP SIGNAL	SPI TPM
H1_TPM_SPI_CLK	PD
H1_TPM_SPI_CS_L	PD
H1_STRAP1	1M PU
H1_STRAP0	1M PU

PP3300_SOC_A [8,9,10,11,12,14,22,35]
PP3300_A [7,8,11,24,25,27,28,30,31,32,33,34,35,41,42]
PP3300_G [9,22,24,25,27,28,29,35,36,41,42]
PP5000_A [9,29,35,36,37,38,41,42]

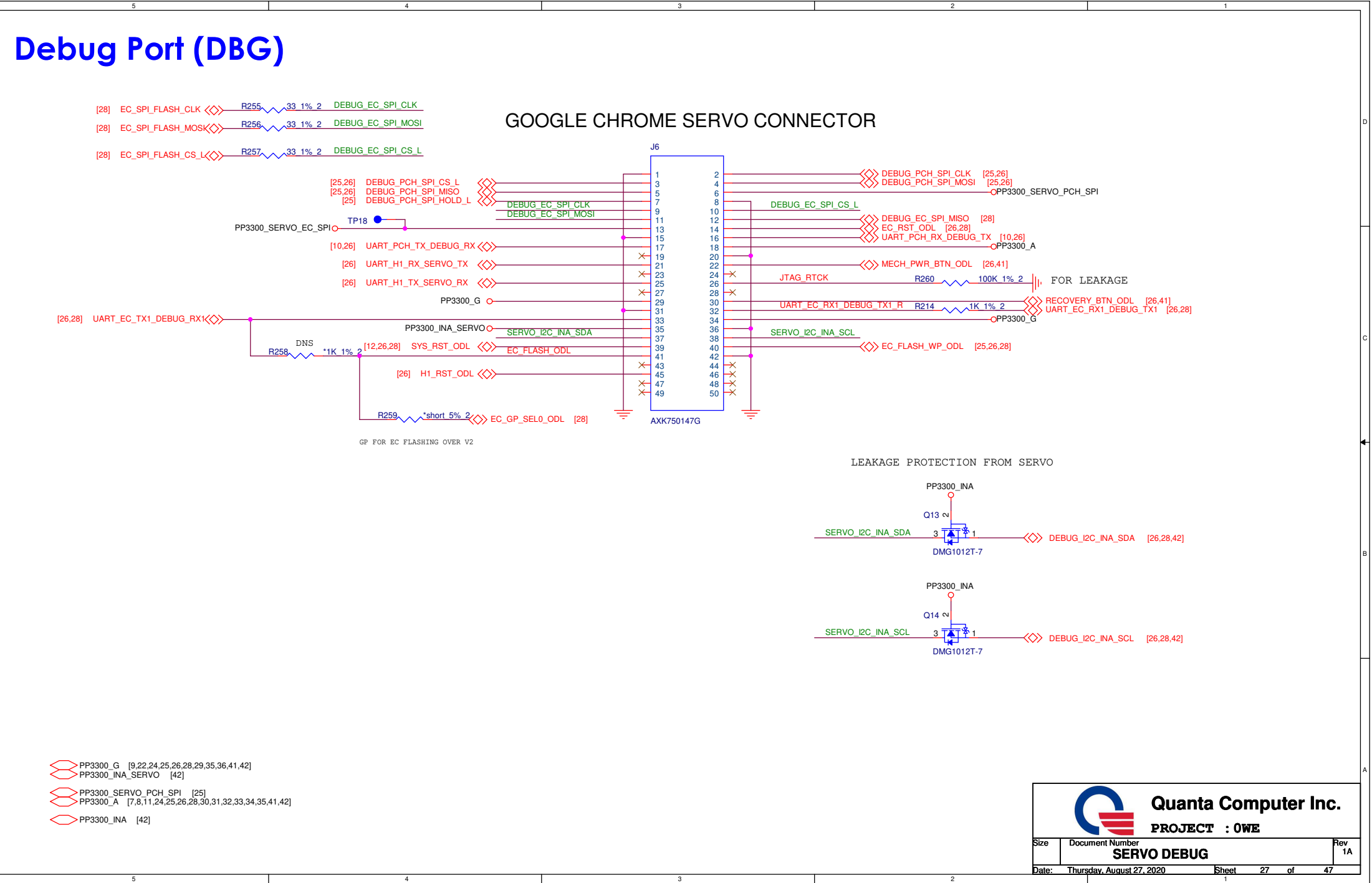
Debug Port (DBG)

GP FOR EC FLASHING OVER V2

LEAKAGE PROTECTION FROM SERVO

- PP3300_G [9,22,24,25,26,28,29,35,36,41,42]
- PP3300_INA_SERVO [42]
- PP3300_SERVO_PCH_SPI [25]
- PP3300_A [7,8,11,24,25,26,28,30,31,32,33,34,35,41,42]
- PP3300_INA [42]


Quanta Computer Inc.
PROJECT : 0WE
SERVO DEBUG
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Debug Port (DBG)

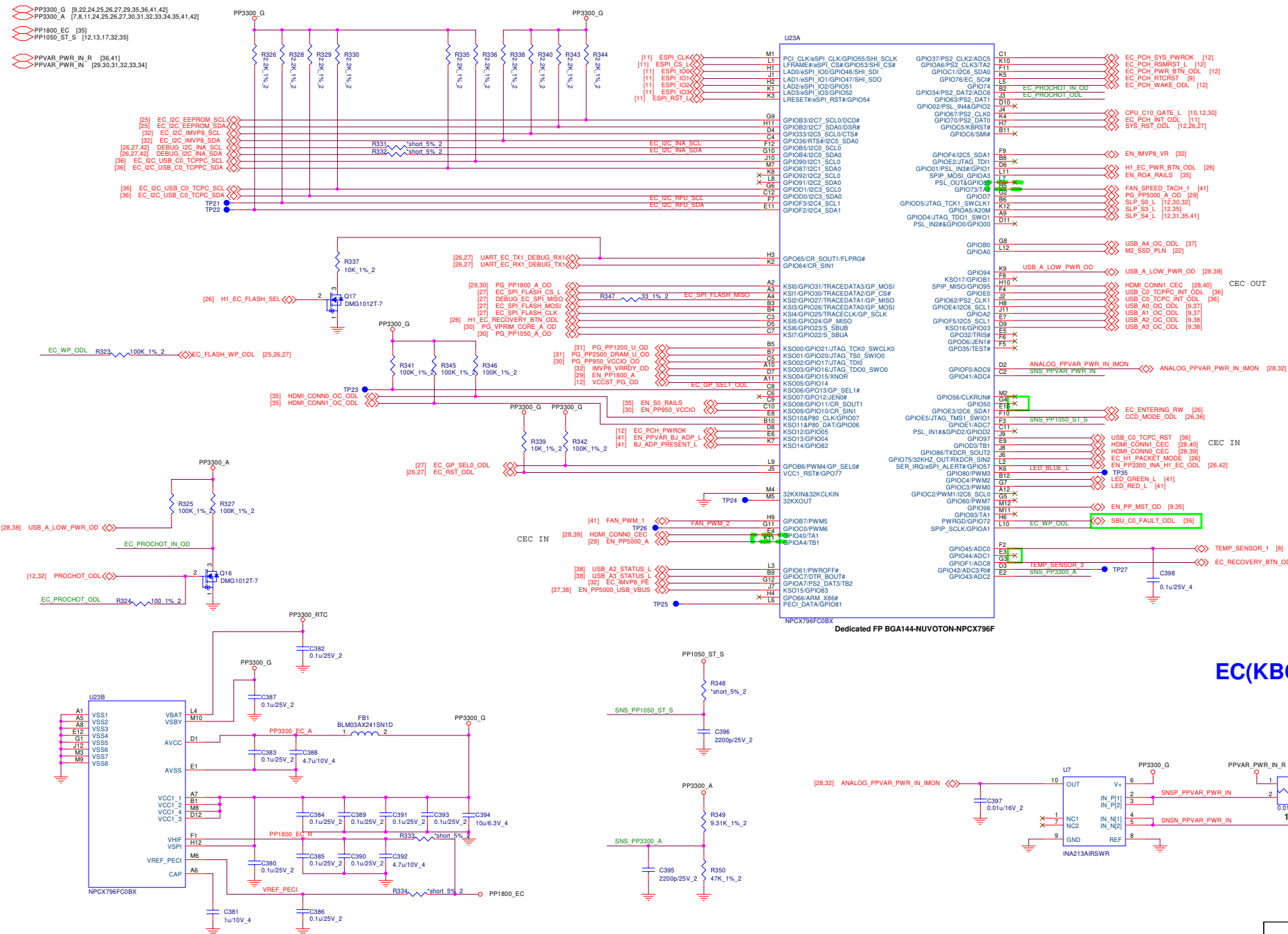
GP FOR EC FLASHING OVER V2

LEAKAGE PROTECTION FROM SERVO

- PP3300_G [9,22,24,25,26,28,29,35,36,41,42]
- PP3300_INA_SERVO [42]
- PP3300_SERVO_PCH_SPI [25]
- PP3300_A [7,8,11,24,25,26,28,30,31,32,33,34,35,41,42]
- PP3300_INA [42]


Quanta Computer Inc.
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EC(KBC)



EC(KBCPWR)

IMAX = 0.5A
ISAT = 0.6A
FSW = 1500KHZ



IMAX=9.6A
ISAT=12A
FSW=600KHZ

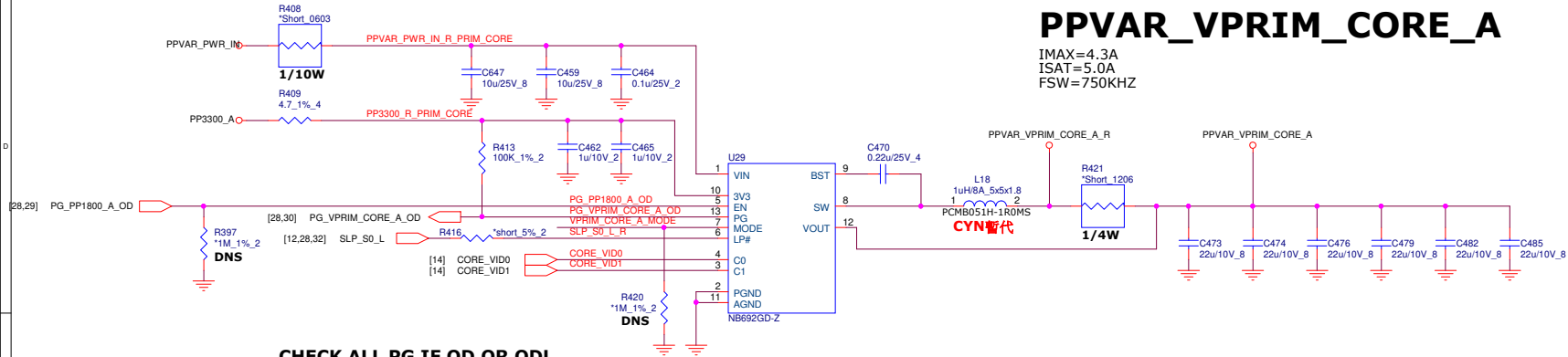


IMAX=7.5A
ISAT=9.3A
FSW=600KHZ



PPVAR_VPRIM_CORE_A

IMAX=4.3A
ISAT=5.0A
FSW=750KHZ



SETTINGS

	VOUT	LP_L	C0	C1
PPVAR_VPRIM_CORE_A	0.75	0	x	x
	0.90	1	0	0
	0.95	1	0	1
	1.00	1	1	0
	1.05	1	1	1
PP1050_A	1.05	1	1	1
PP950_VCCIO	0.95	1	0	1

*LP_L, C0, C1 PULLED HIGH INTERNALLY

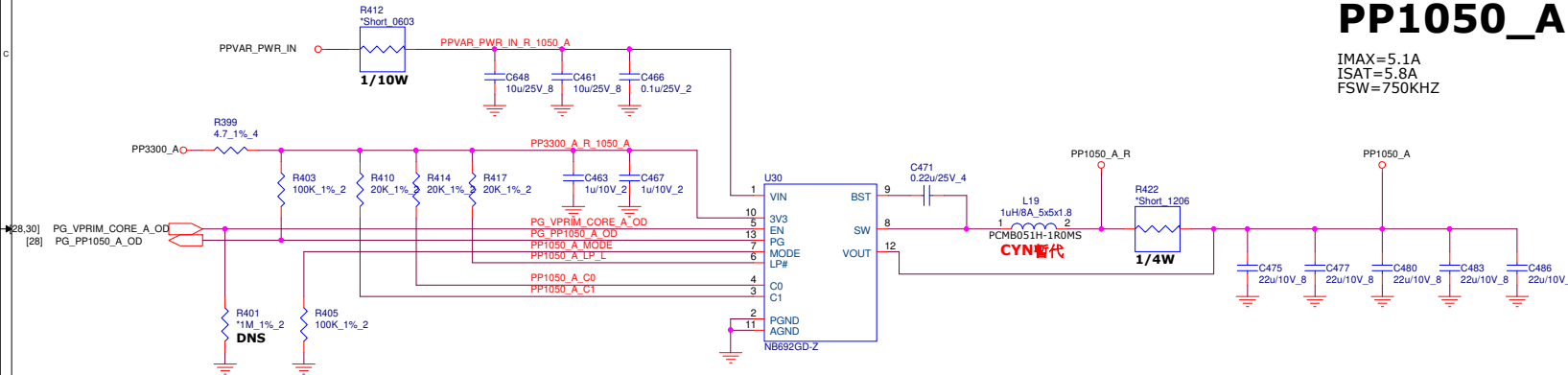
RAIL	MODE PIN PD RES
PPVAR_VPRIM_CORE_A	FLOAT OR >230K
VCCOPC/V1.0A/EOP10	100K
VCCIO	0

OPERATING MODE	EN PIN VOLTAGE [V]
ULTRASONIC (USM)	1.3 - 1.7
NORMAL	> 2.3

*EN PIN HAS 800K INTERNAL PU

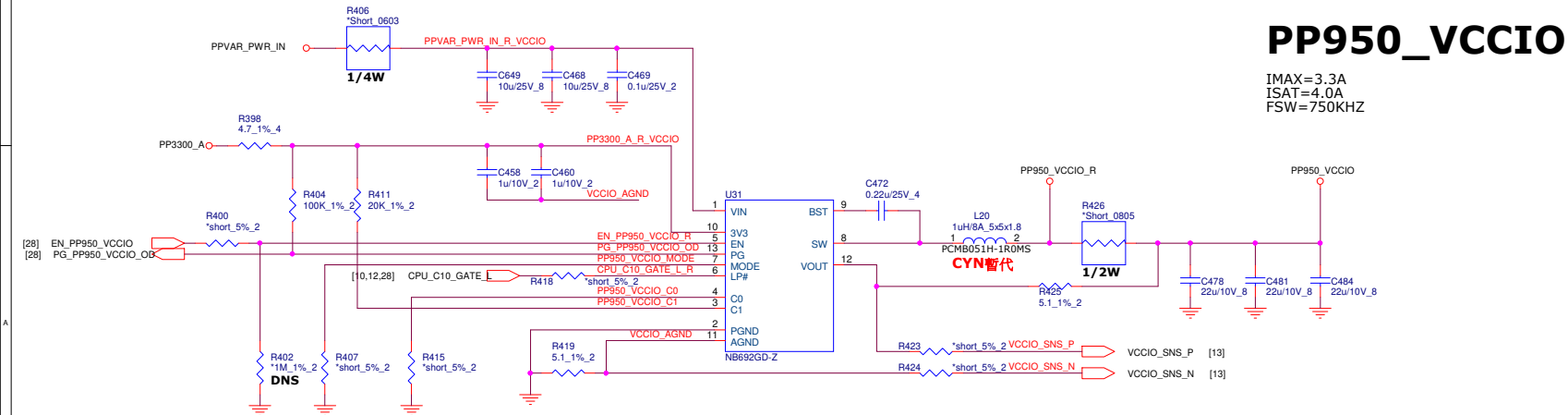
PP1050_A

IMAX=5.1A
ISAT=5.8A
FSW=750KHZ



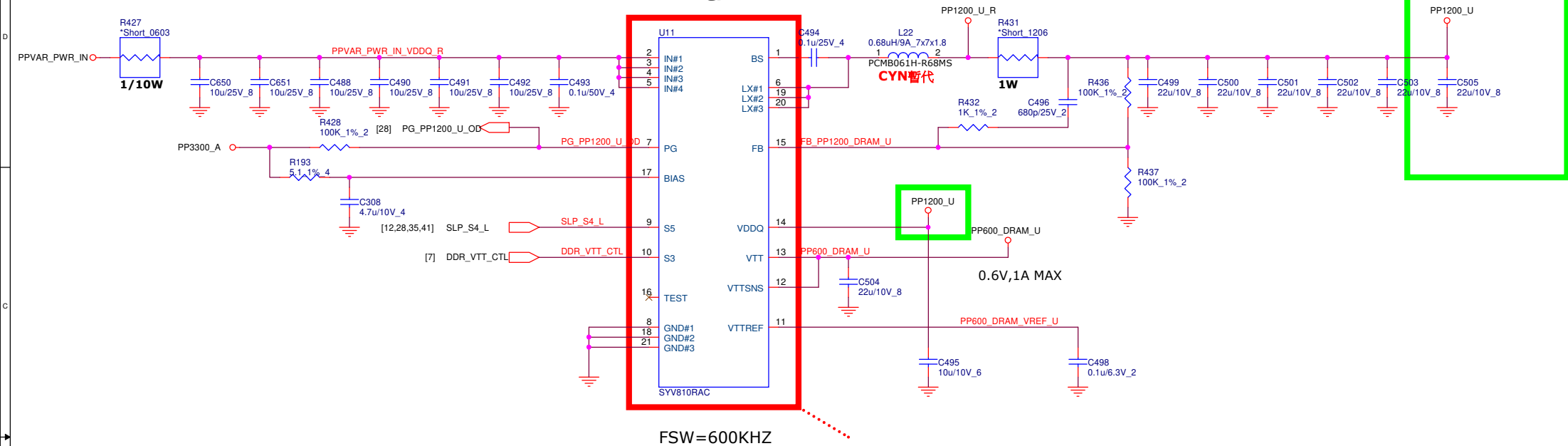
PP950_VCCIO

IMAX=3.3A
ISAT=4.0A
FSW=750KHZ



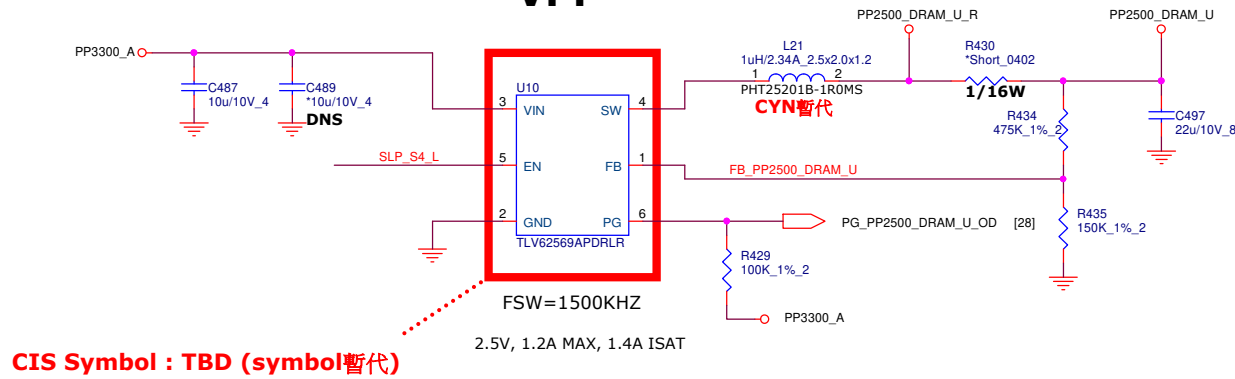
VDDQ, VTT

1.2V, 12A MAX, 13.4A ISAT
NEED INDUCTOR WITH HIGHER IDC



CAN USE TPS51486 IF ONLY SUPPORTING 16GB MEMORY

VPP



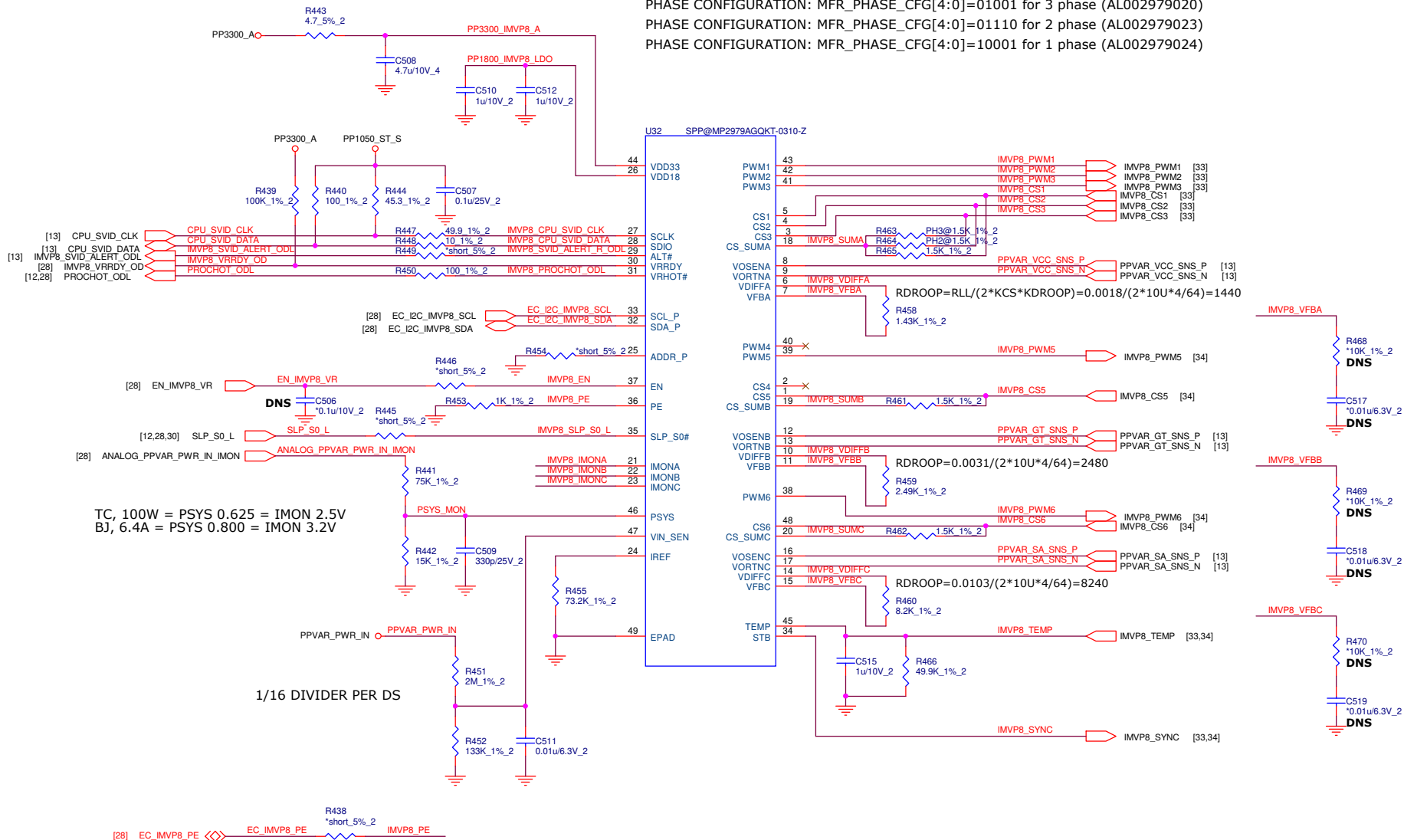
Quanta Computer Inc.

PROJECT :

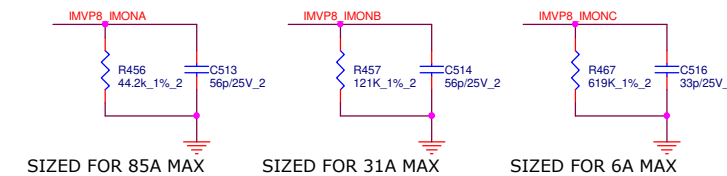
Size	Document Number	Rev
		1A
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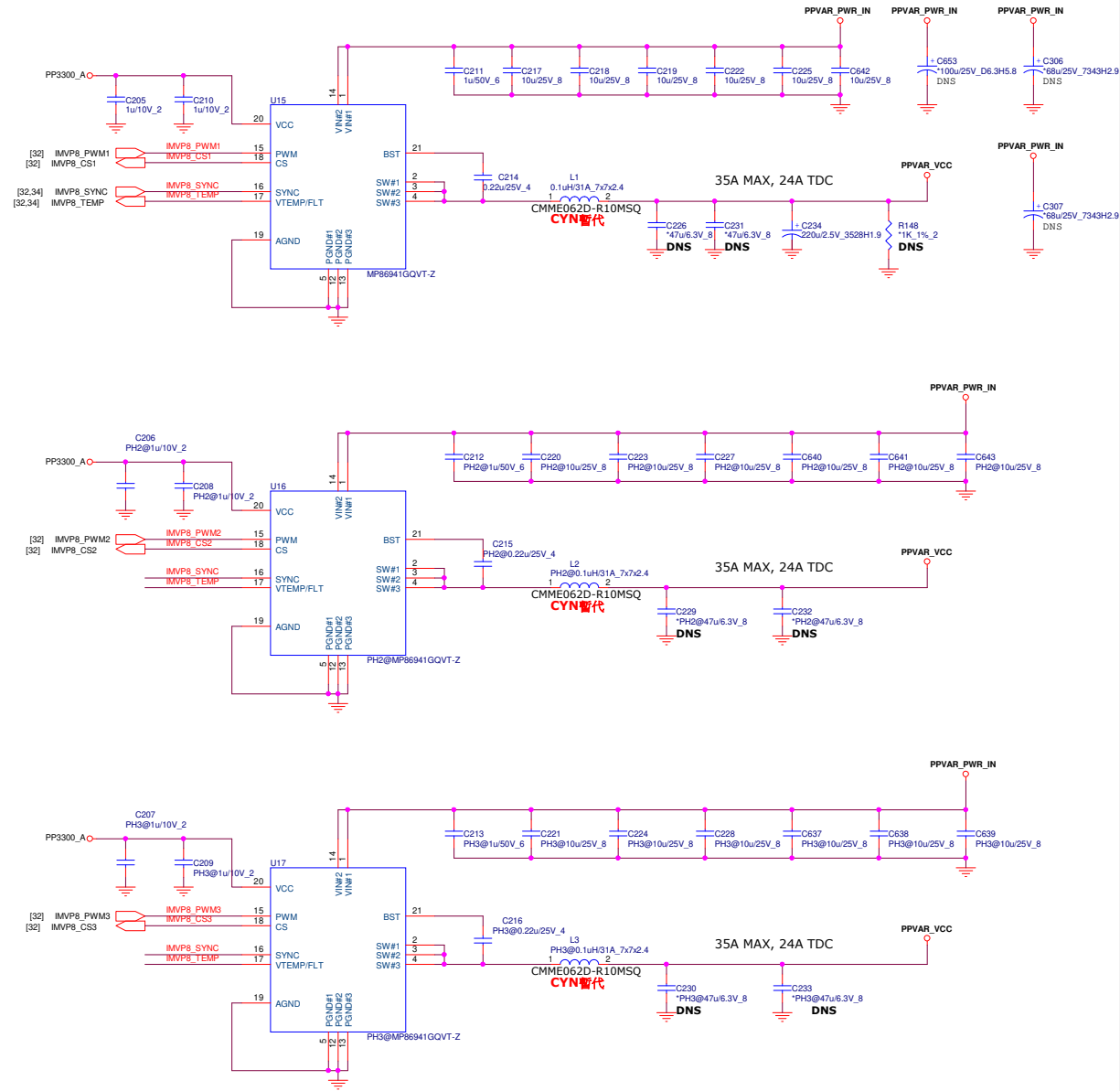
POWER: DDR4 RAILS

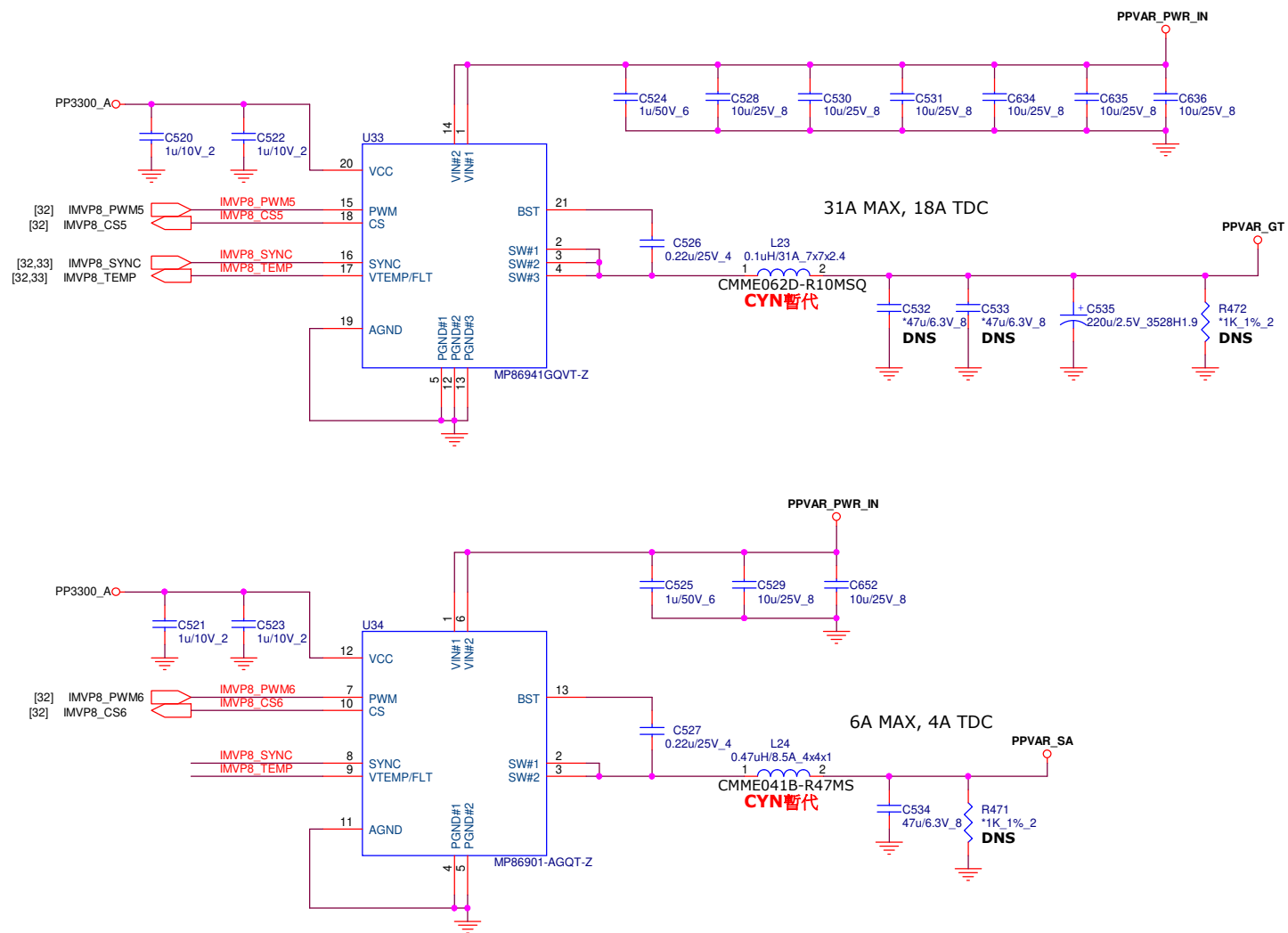
PHASE CONFIGURATION: MFR_PHASE_CFG[4:0]=01001 for 3 phase (AL002979020)
 PHASE CONFIGURATION: MFR_PHASE_CFG[4:0]=01110 for 2 phase (AL002979023)
 PHASE CONFIGURATION: MFR_PHASE_CFG[4:0]=10001 for 1 phase (AL002979024)



IMON=32*VIMON_MAX/(ICCMAX*KCS), WHERE VIMON_MAX=1.1636, KCS=10U



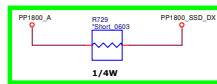




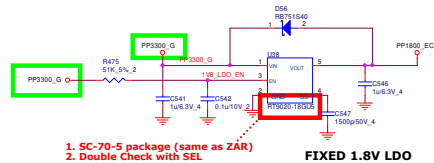
Quanta Computer Inc.

PROJECT :

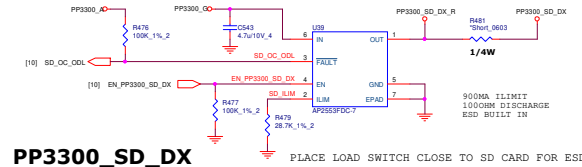
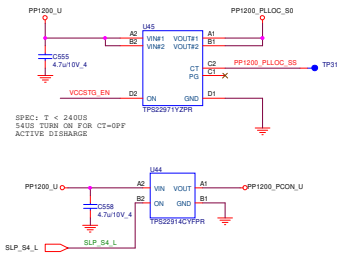
Size	Document Number	Rev
	POWER: IMVP8 DRMos GT, SA	1A
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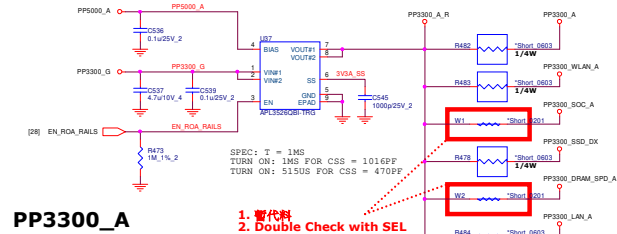
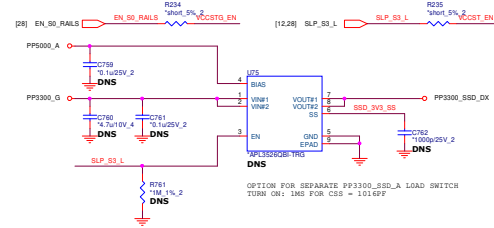
PP1800_*



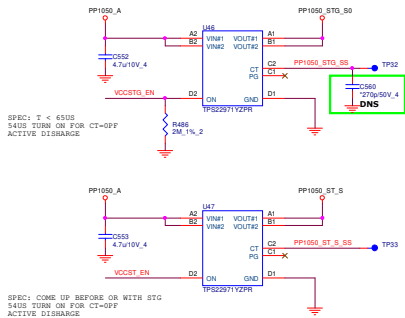
PP1200



PP3300_SD_DX

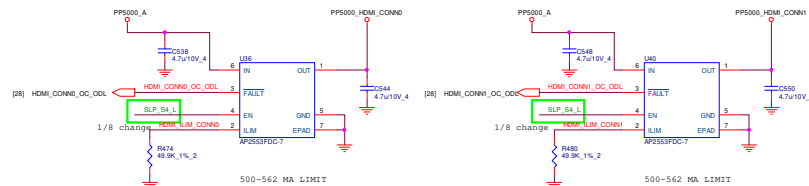


PP3300_A

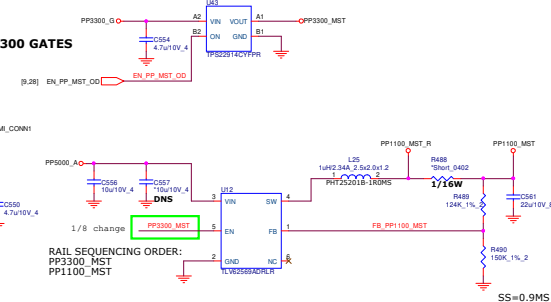


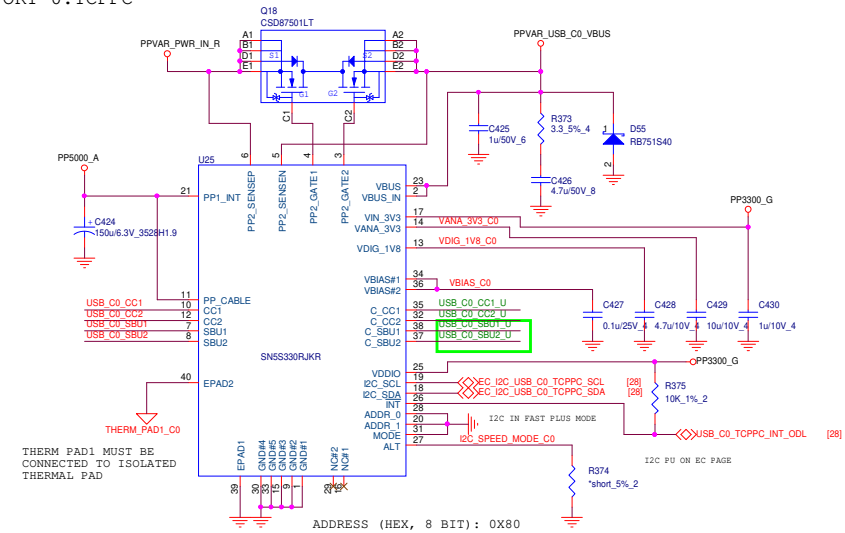
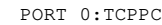
PP1050

HDMI RELATED

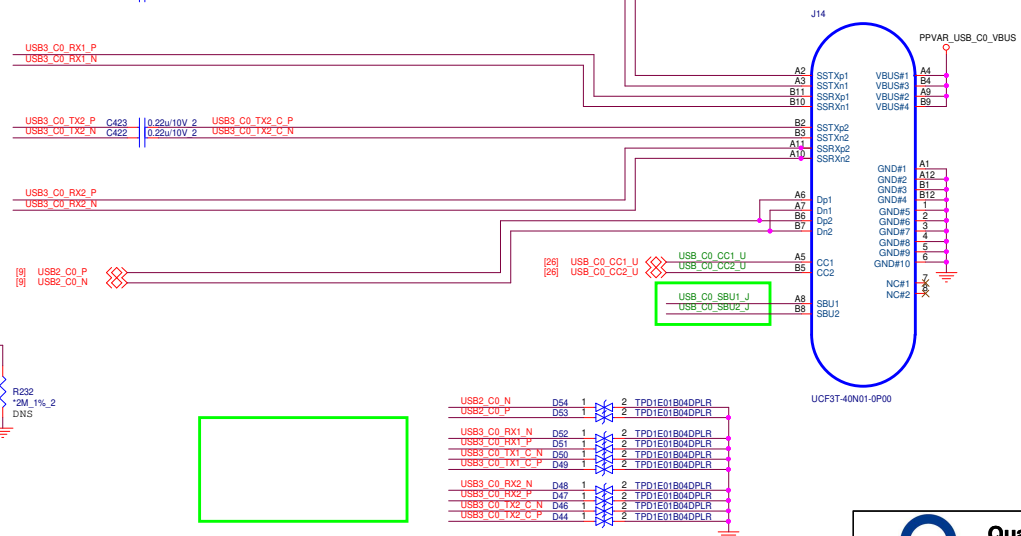


PP3300 GATES





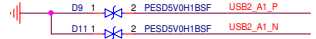
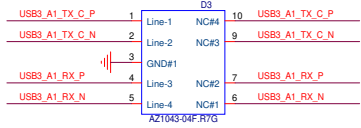
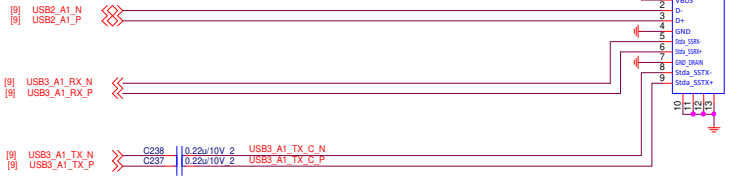
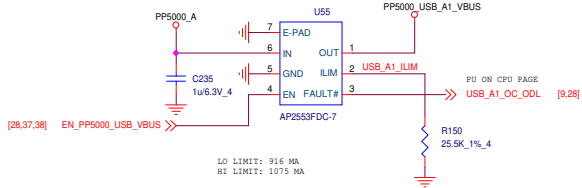
USB3_C0_TX1_P	C421	0.22u/10V 2	USB3_C0_TX1_C_P
USB3_C0_TX1_N	C420	0.22u/10V 2	USB3_C0_TX1_C_N



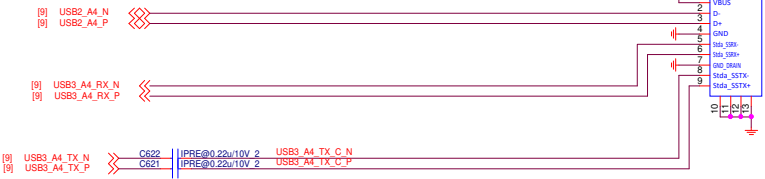
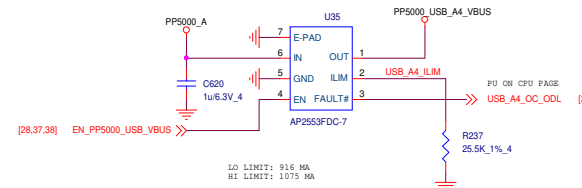
 Quanta Computer Inc. PROJECT : 0WE			
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	USB C0	1A	
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USB3.0 Rear Single Port (UB3)

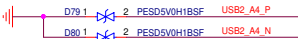
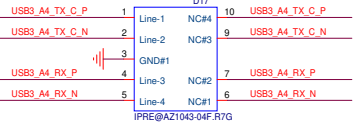
TYPE-A: PORT 1



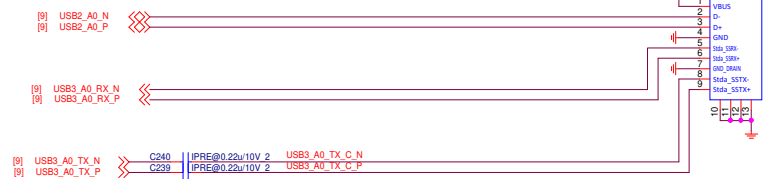
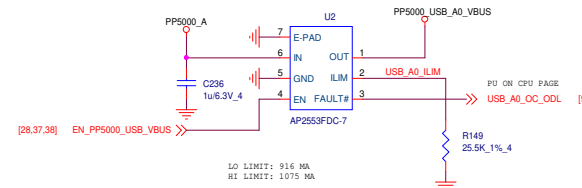
TYPE-A: PORT 4



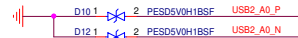
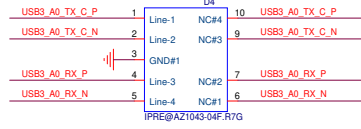
after OEM EVT build
USB2: straight /black DFHS04FRA50 (4P) for Base-U.



TYPE-A: PORT 0



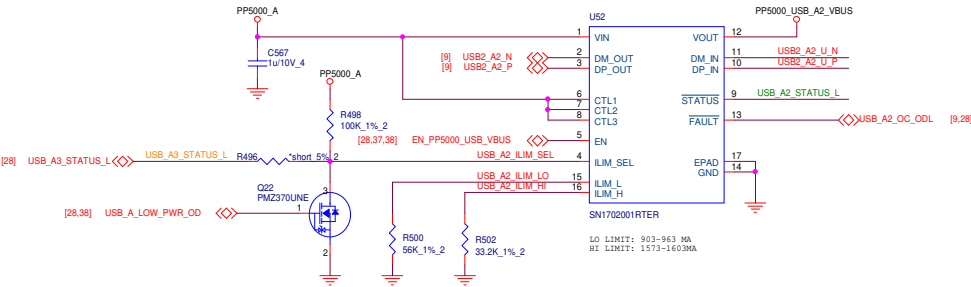
after OEM EVT build
USB2 /straight /black DFHS04FRA50 (4P) for Base-U.



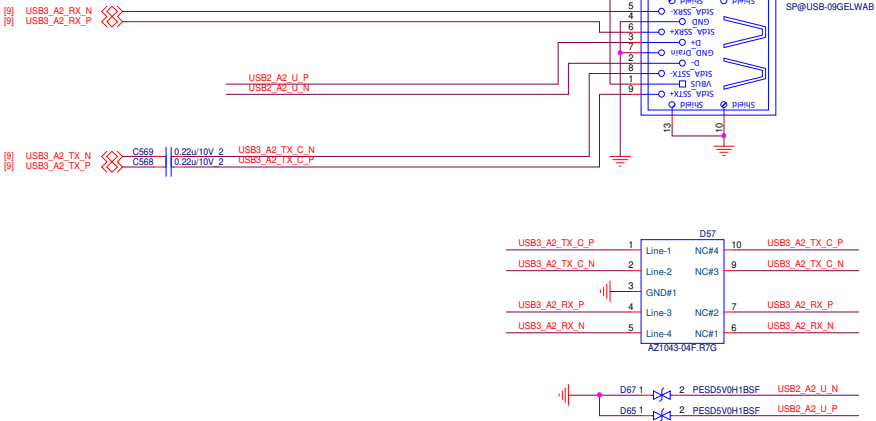
PP5000_A [9,29,35,36,38,41,42]

USB3.0 with Charger /Front (UB3)

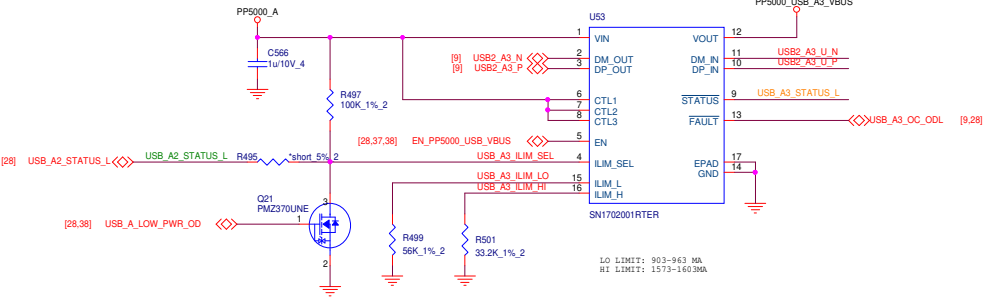
BC1.2 FOR TYPE-A: PORT A2



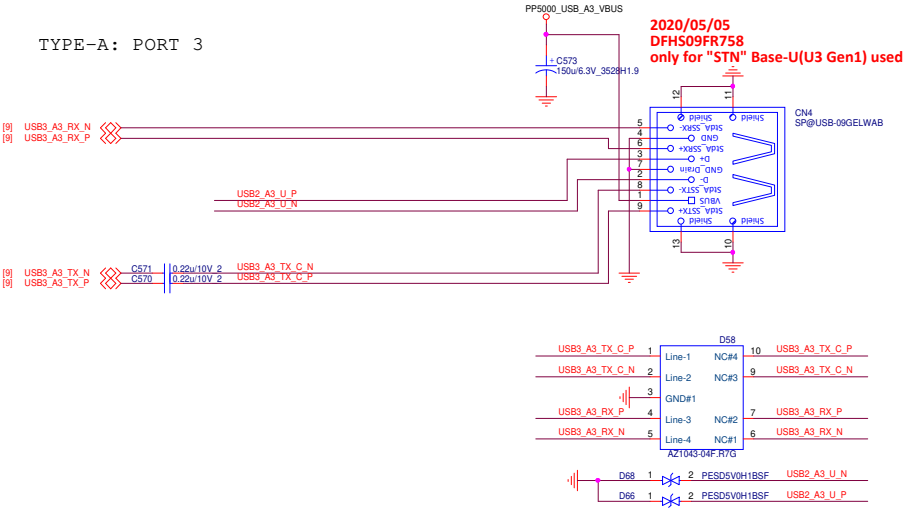
TYPE-A: PORT 2



BC1.2 FOR TYPE-A: PORT A3

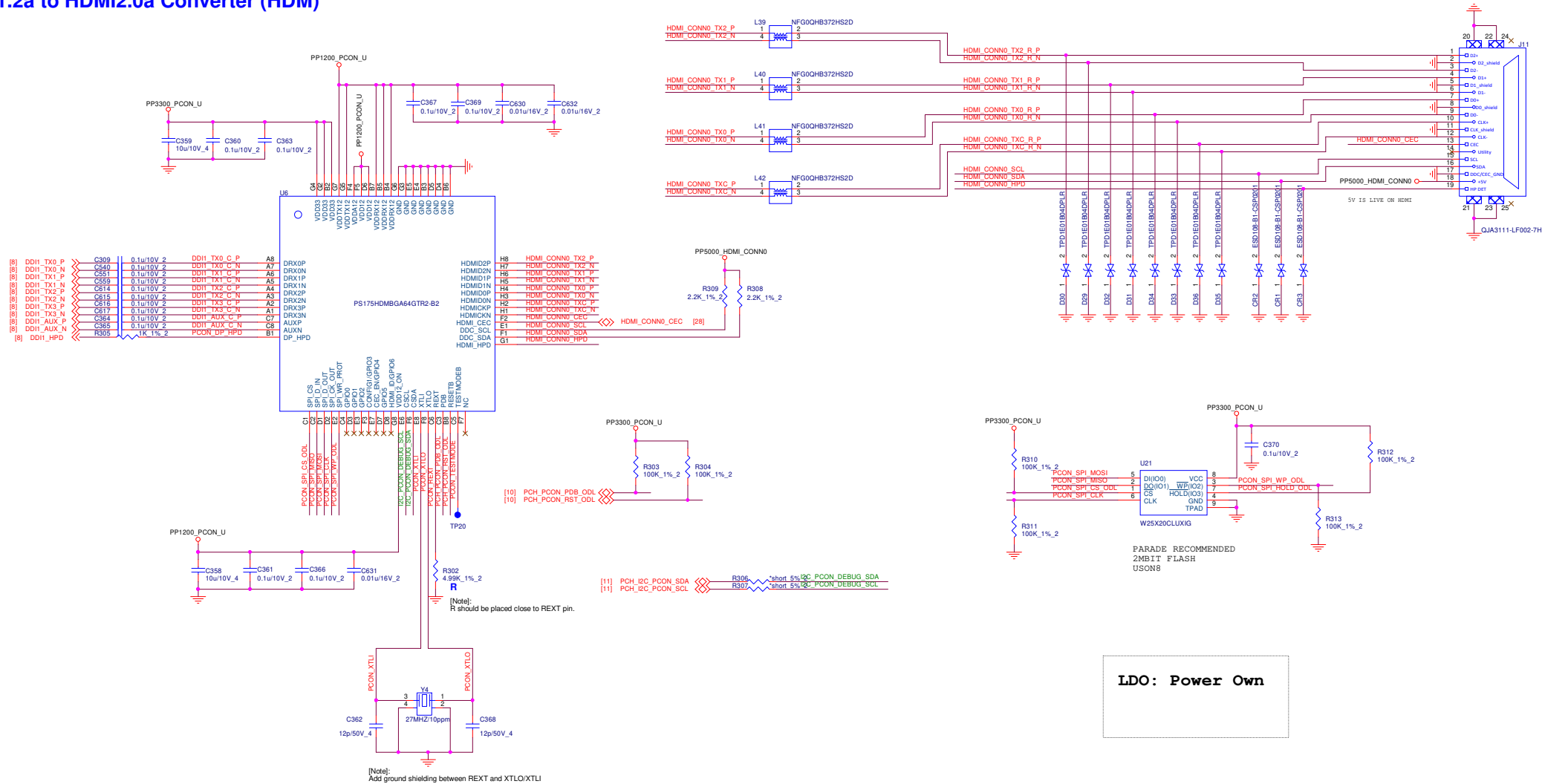


TYPE-A: PORT 3



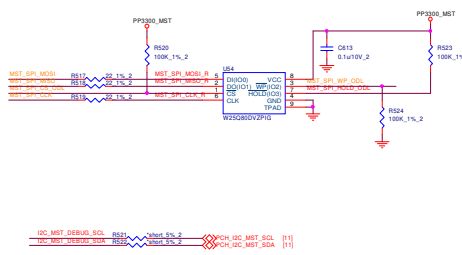
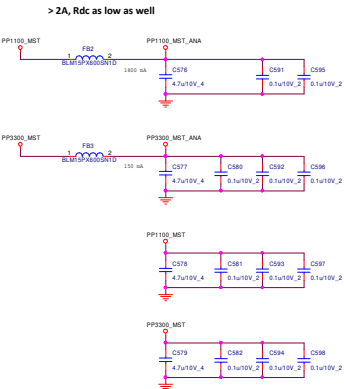
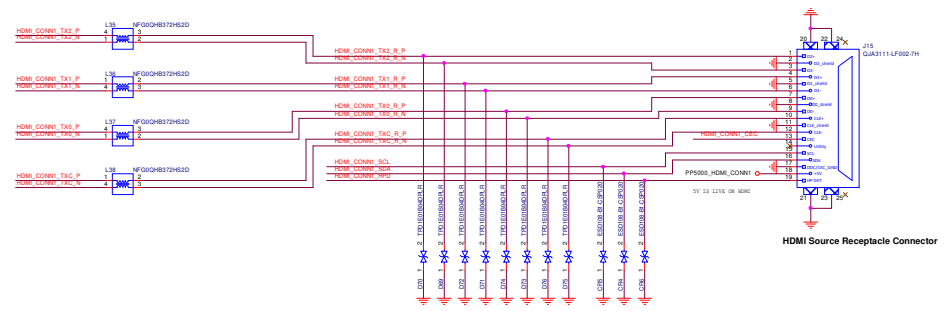
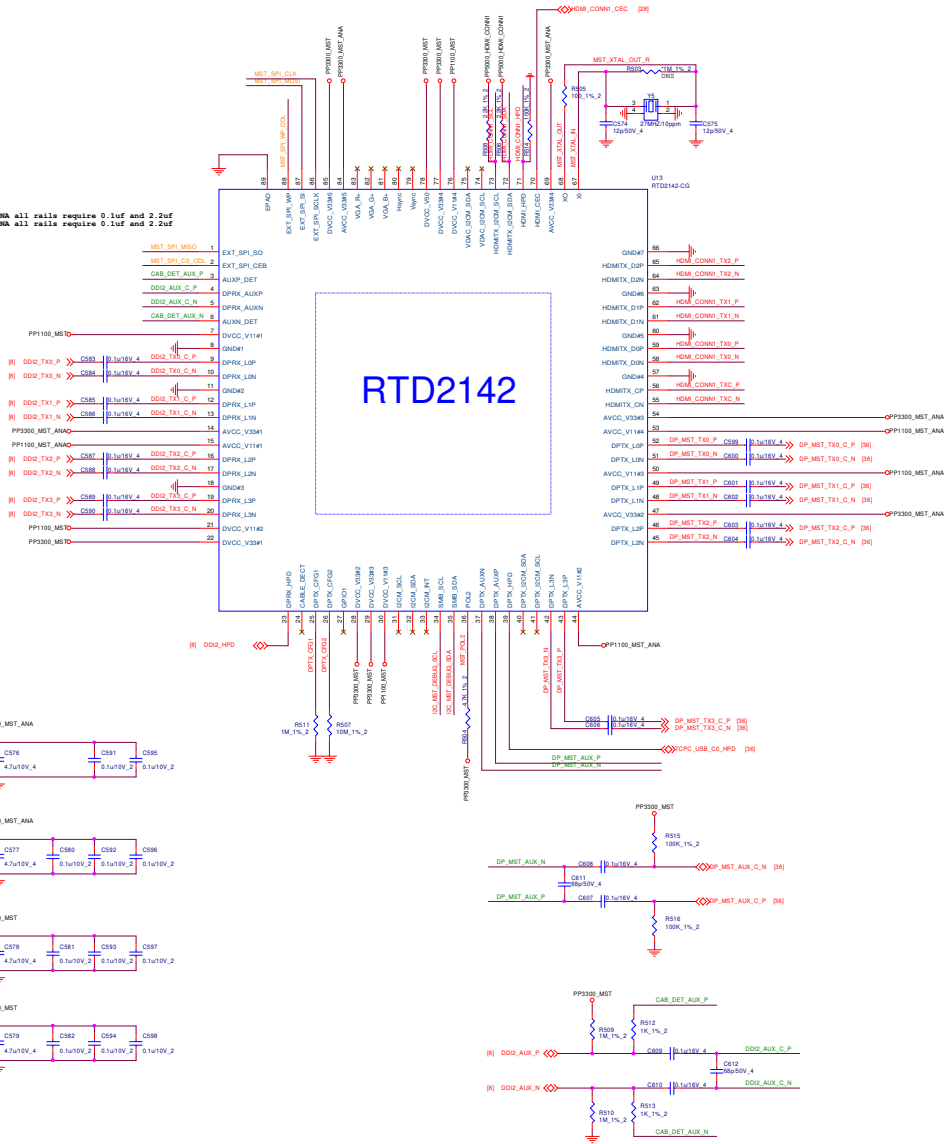
PP5000_A [9,29,35,36,37,41,42]

DP1.2a to HDMI2.0a Converter (HDM)



PP3300_PCON_U [35]
PP1200_PCON_U [35]
PP5000_HDMI_CONNO [35]

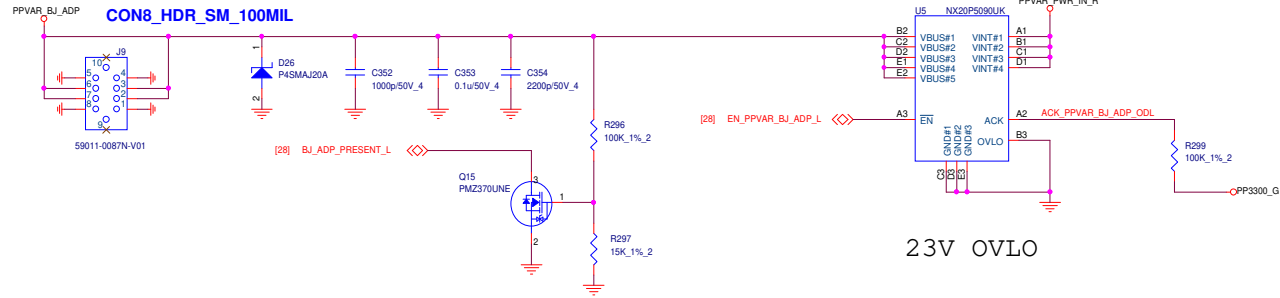
0128
PP1100_MST / PP1100_MST_ANA all rails require 0.1uf and 2.2uf
PP3300_MST / PP3300_MST_ANA all rails require 0.1uf and 2.2uf



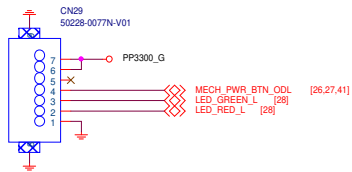
PP1100_MST [D5]
PP3300_MST [D5]
PP5000_MST [D5]

(PDI)

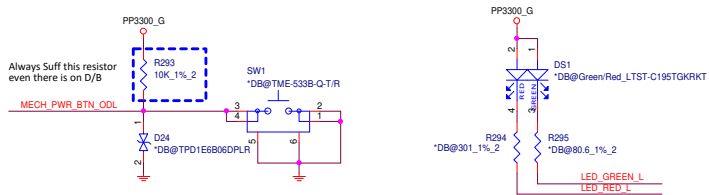
DC JACK



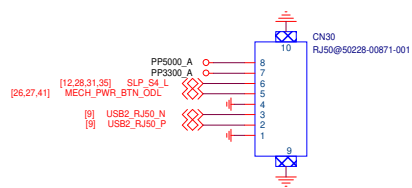
To PWR BTN DB#1



DB#1's Components

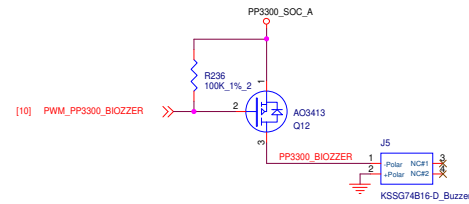


To RJ50 DB

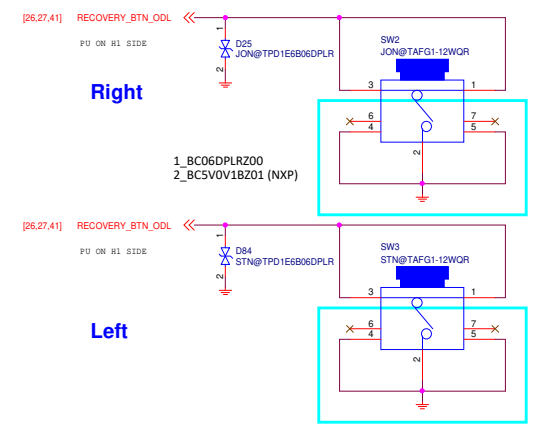


- PPVAR_PWR_IN_R [28,36]
- PP3300_G [9,22,24,25,26,27,28,29,35,36,42]
- PP3300_A [7,8,11,24,25,26,27,28,30,31,32,33,34,35,42]
- PP5000_A [9,29,35,36,37,38,42]

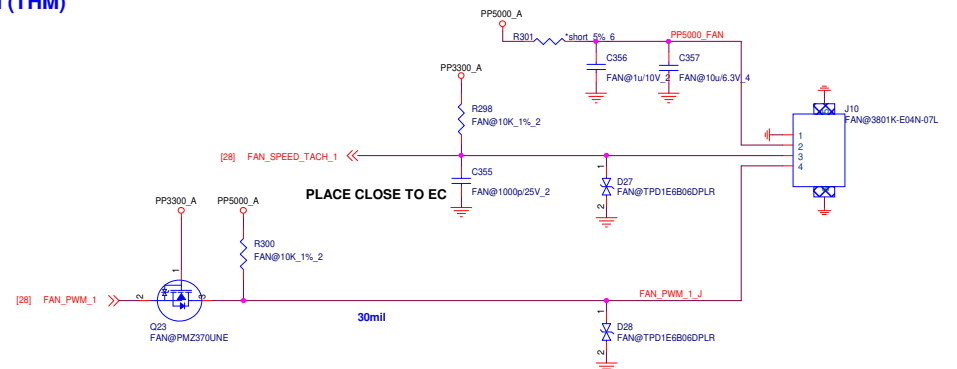
Buzzer (BUZ)

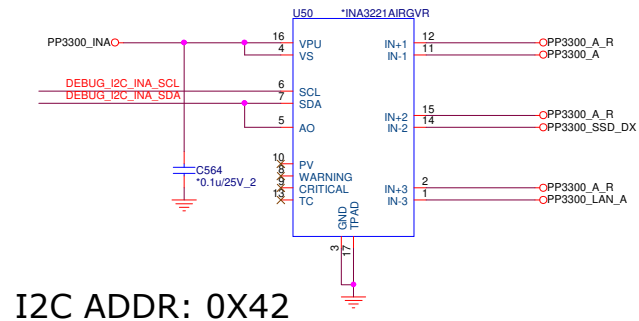
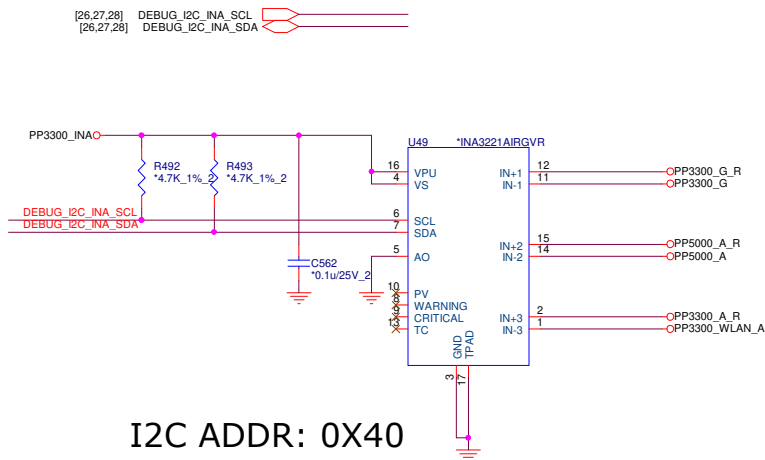


Recovery switch (FSW)

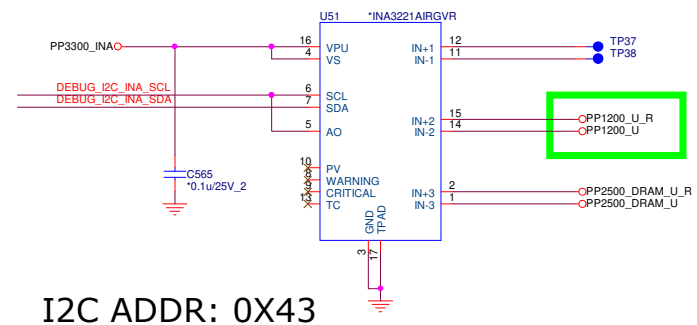
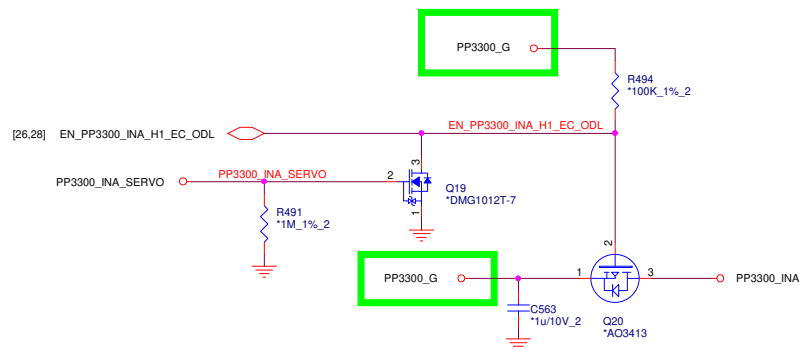


CPU FAN (THM)

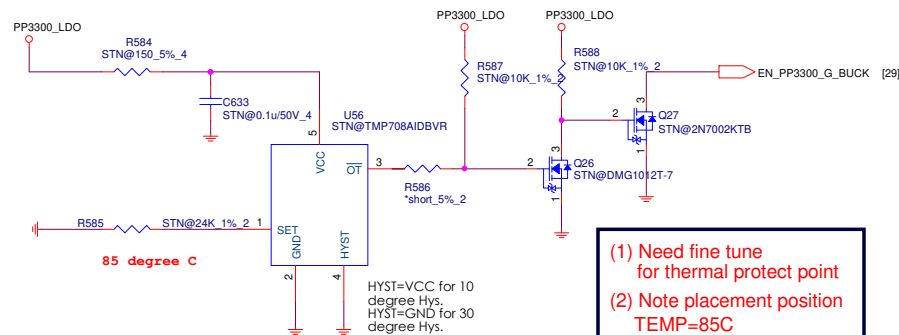




INA POWER



Thermal protection



CML U			2020 Chromebox - [Puff]	2020 Chromebox - [Puff]
Premium	Base		Premium	Base
DDI0	DDI0		--	--
DDI1	DDI1		HDMI 2.0a [LSPCON]	HDMI 2.0a [LSPCON]
DDI2	DDI2		TypeC Rear (DP) + HDMI 2.0b [MST]	TypeC Rear (DP) + HDMI 2.0b [MST]
USB3 Port1	USB3 Port1	PCIe Port1	USB 3 Type-A Front (Port 2)	USB 3 Type-A Front (Port 2)
USB3 Port2	USB3 Port2	PCIe Port2	USB 3 Type-A Front (Port 3)	USB 3 Type-A Front (Port 3)
USB3 Port3	USB3 Port3	PCIe Port3	USB 3 Type-A Rear (Port 1)	USB 3 Type-A Rear (Port 1)
USB3 Port4	USB3 Port4	PCIe Port4	USB Type-C Rear	USB Type-C Rear
USB3 Port5	PCIe	PCIe Port5	USB 3 Type-A Rear (Port 0)	USB 2 Type-A Rear
USB3 Port6	PCIe	PCIe Port6	USB 3 Type-A Rear (Port 4)	USB 2 Type-A Rear
GbE	GbE	PCIe Port7	LAN	LAN
GbE	GbE	PCIe Port8	M-key M.2 SSD (PCIe x4/SATA) MB 2242/2280	M-key M.2 SSD (PCIe x4/SATA) MB 2242/2280
GbE	GbE	PCIe Port9		
PCIe	PCIe	PCIe Port10		
SATA0	SATA0	PCIe Port11		
SATA1a	SATA1a	PCIe Port12	M.2 SSD (SATA) MB 2242	M.2 SSD (SATA) MB 2242
GbE	GbE	PCIe Port13	M.2 E-key WiFi 2230	M.2 E-key WiFi 2230
GbE	GbE	PCIe Port14		
SATA1b	PCIe	PCIe Port15		
SATA2	PCIe	PCIe Port16		
USB2 Port1	USB2 Port1		USB 3 Type-A Front (Port 2)	USB 3 Type-A Front (Port 2)
USB2 Port2	USB2 Port2		USB 3 Type-C Rear	USB 3 Type-C Rear
USB2 Port3	USB2 Port3		USB 3 Type-A Front (Port 3)	USB 3 Type-A Front (Port 3)
USB2 Port4	USB2 Port4		USB 3 Type-A Rear (Port 1)	USB 3 Type-A Rear (Port 1)
USB2 Port5	USB2 Port5		USB 3 Type-A Rear (Port 4)	USB 3 Type-A Rear (Port 4)
USB2 Port6	USB2 Port6		USB 3 Type-A Rear (Port 0)	USB 3 Type-A Rear (Port 0)
USB2 Port7	USB2 Port7			
USB2 Port8				
USB2 Port9				
USB2 Port10	USB2 Port10		Bluetooth	Bluetooth



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Change List

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Change List

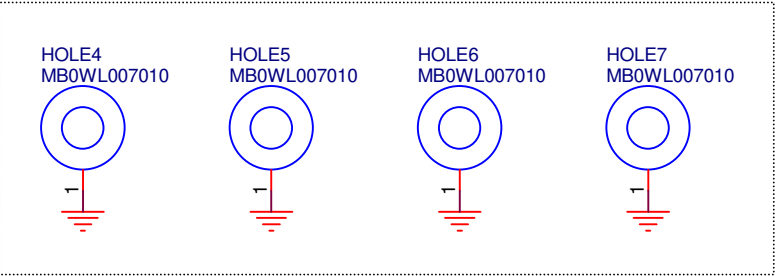
Rev
1A

Date: Thursday, June 11, 2020

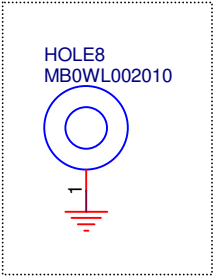
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Screw Hole (OTH)

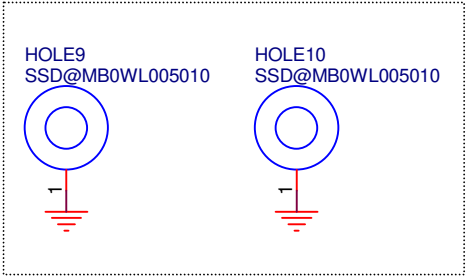
CPU/TOP side



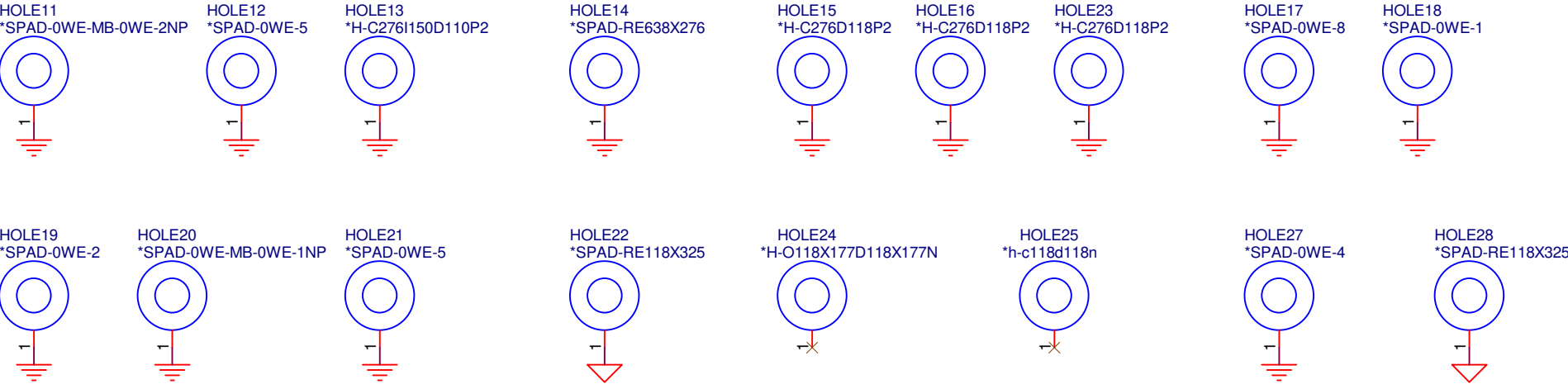
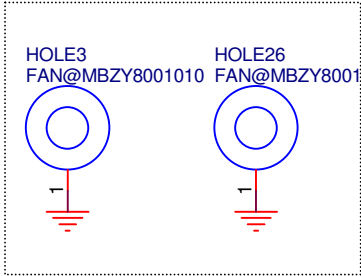
Wifi/BOT side



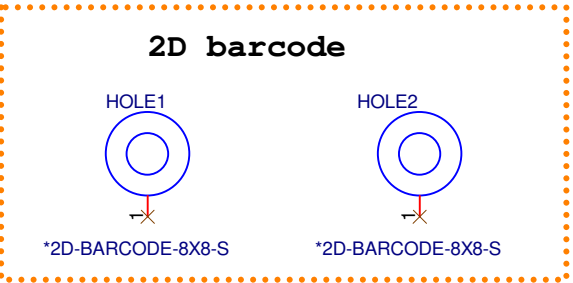
SSD/TOP side



FAN/TOP side



2D barcode



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Shielding Clip x8

