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PROJECT : ZAR

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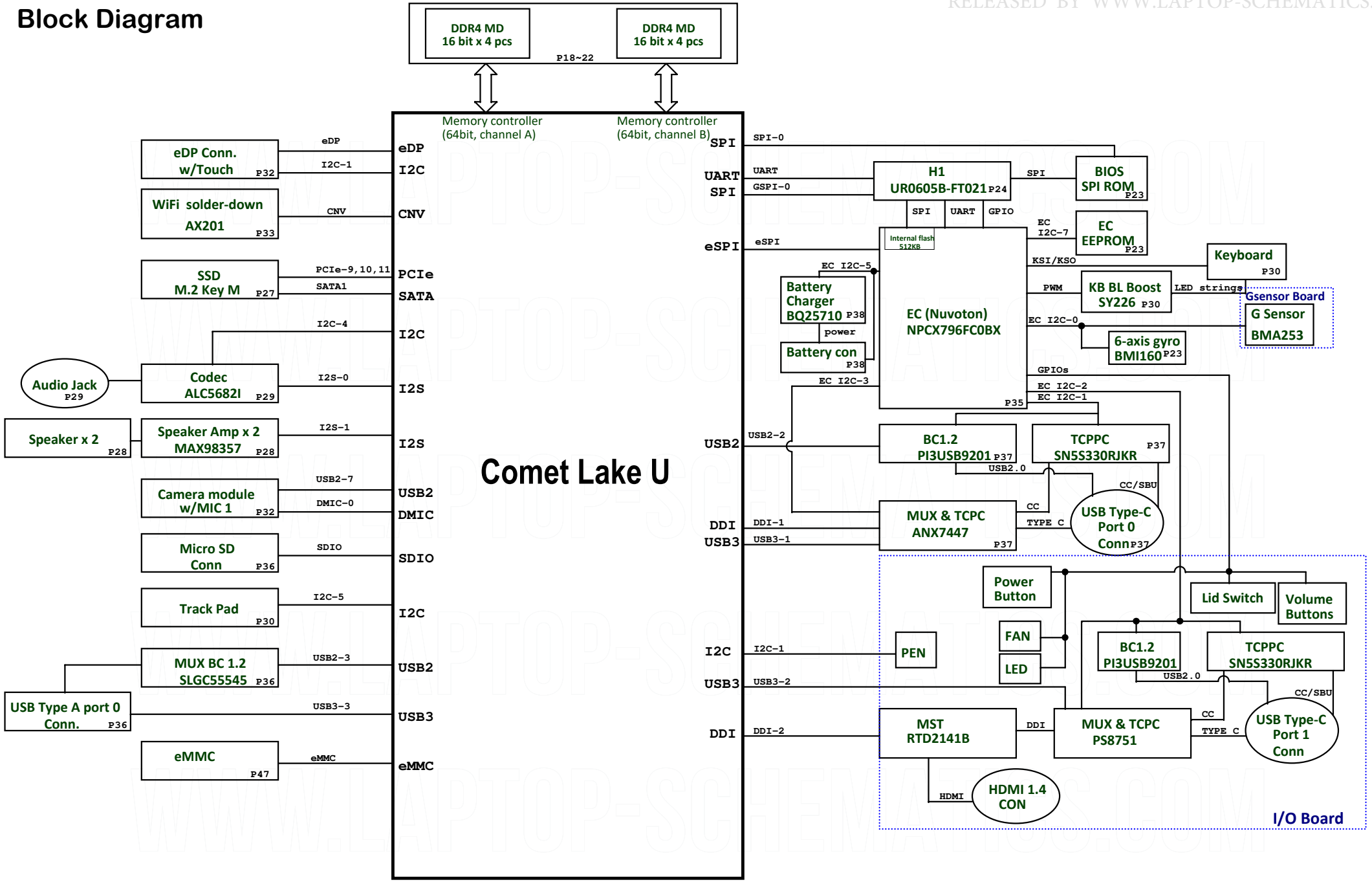
Block Diagram



Quanta Computer Inc.
PROJECT : ZAR
SYSTEM BLOCK DIAGRAM
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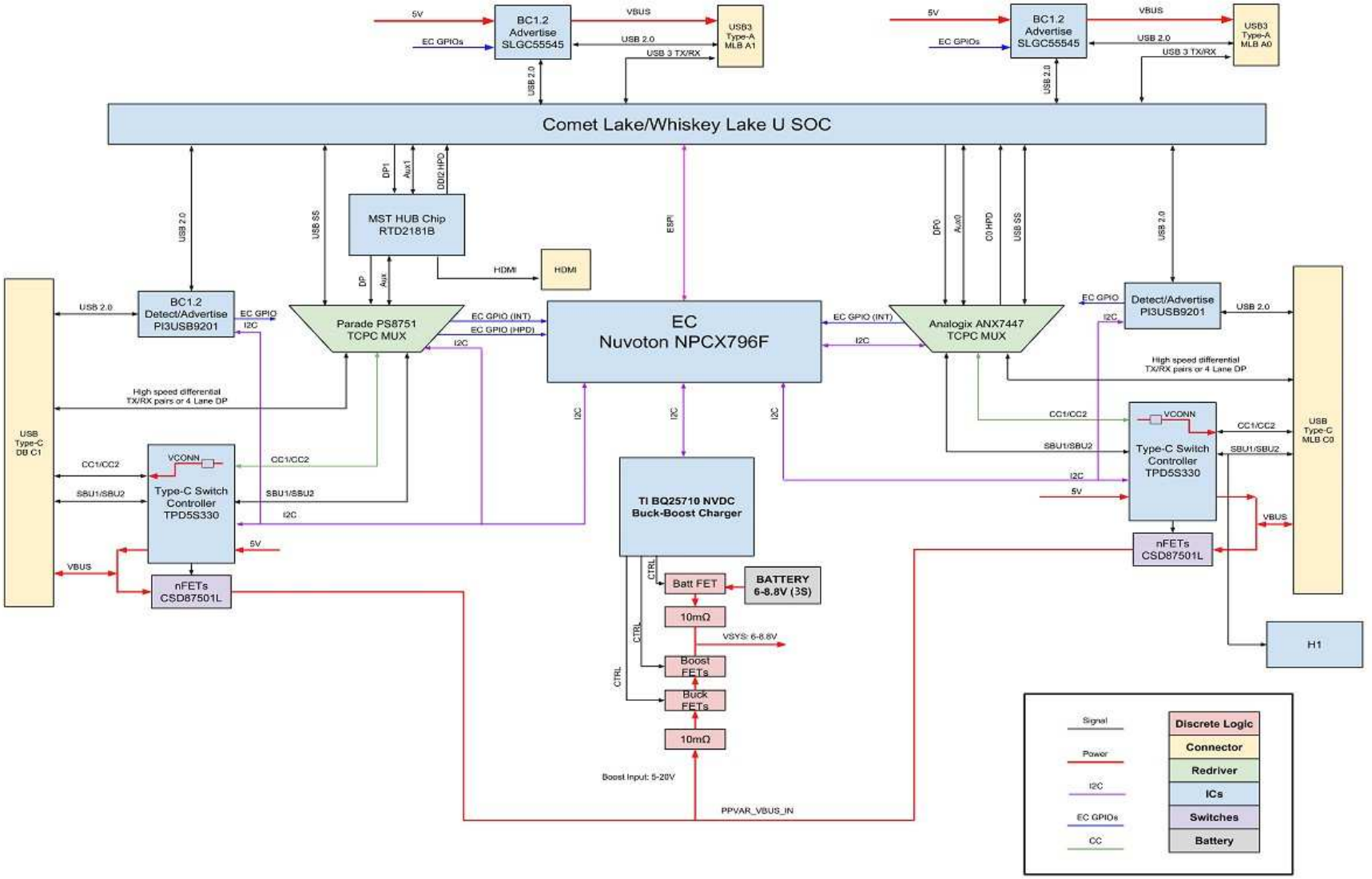
Hatch USB Block Diagram

Updated: 11/19/2018



Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: TYPE-C BLOCK DIAGRAM	Rev 1C
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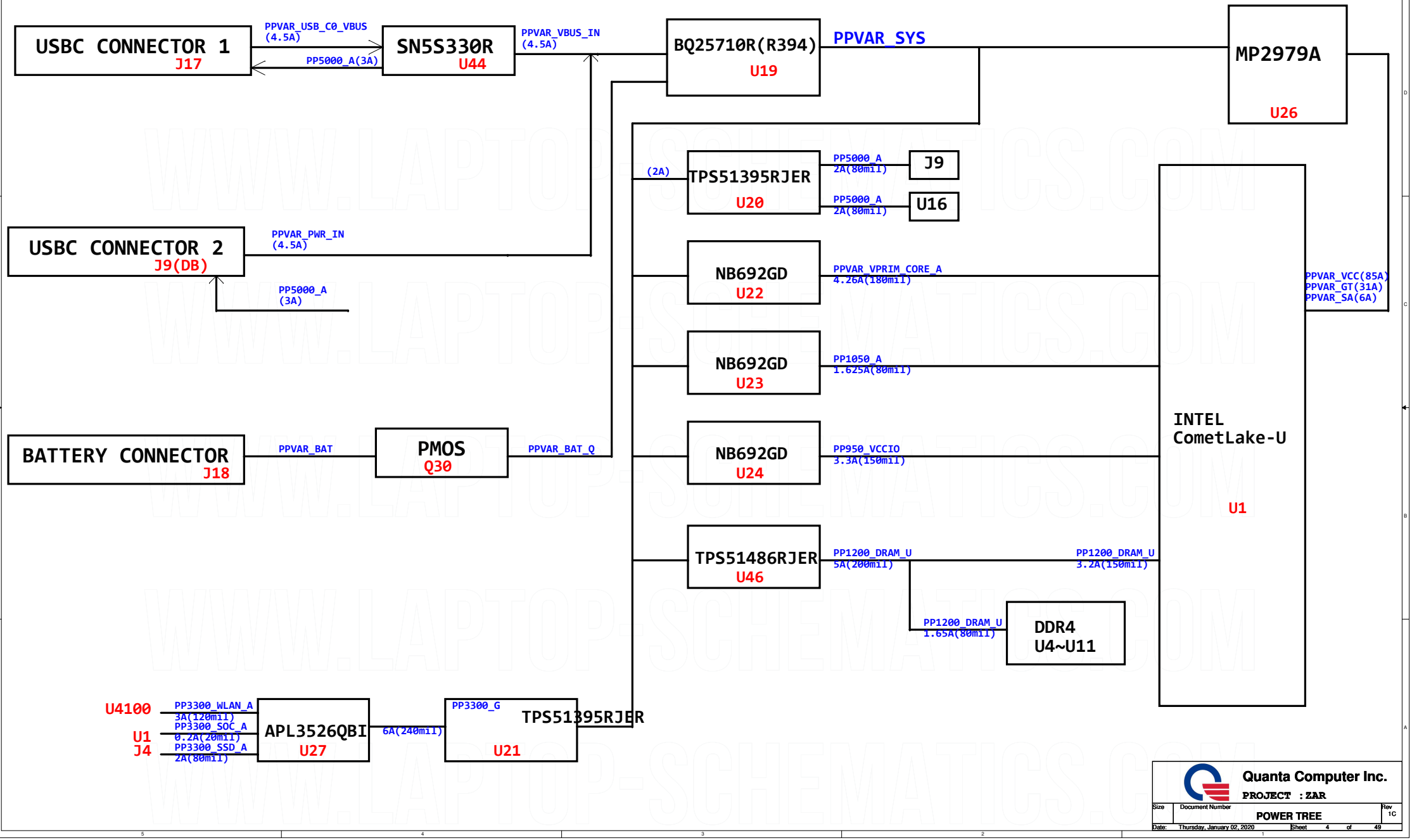

Quanta Computer Inc.

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Size	Document Number	Rev
	POWER TREE	1C

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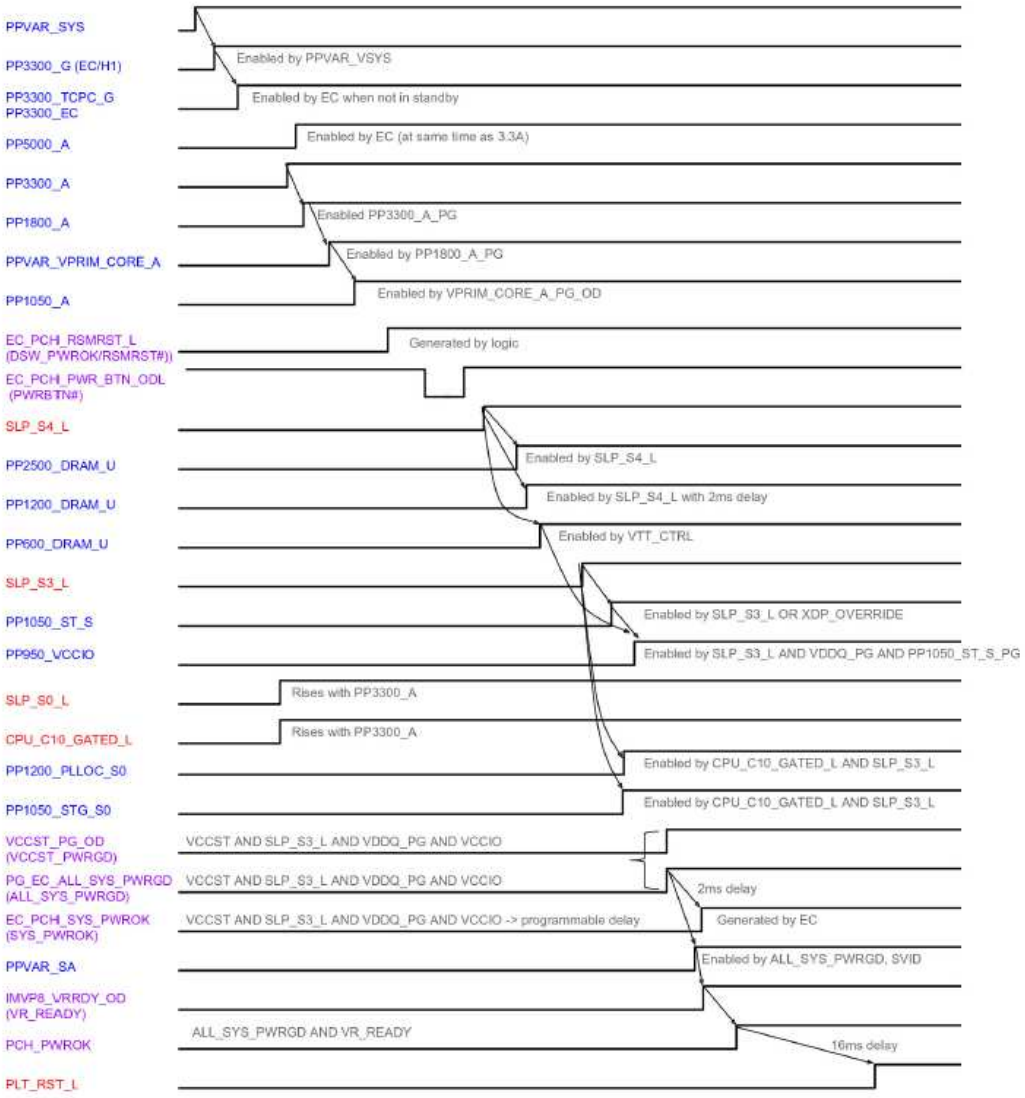

Power Rail
Signal from PCH
Signal from Platform

Hatch Power Sequencing

Updated: 11/29/2018

Quanta Computer Inc.

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Size	Document Number	Rev
	POWER SEQUENCING	1C
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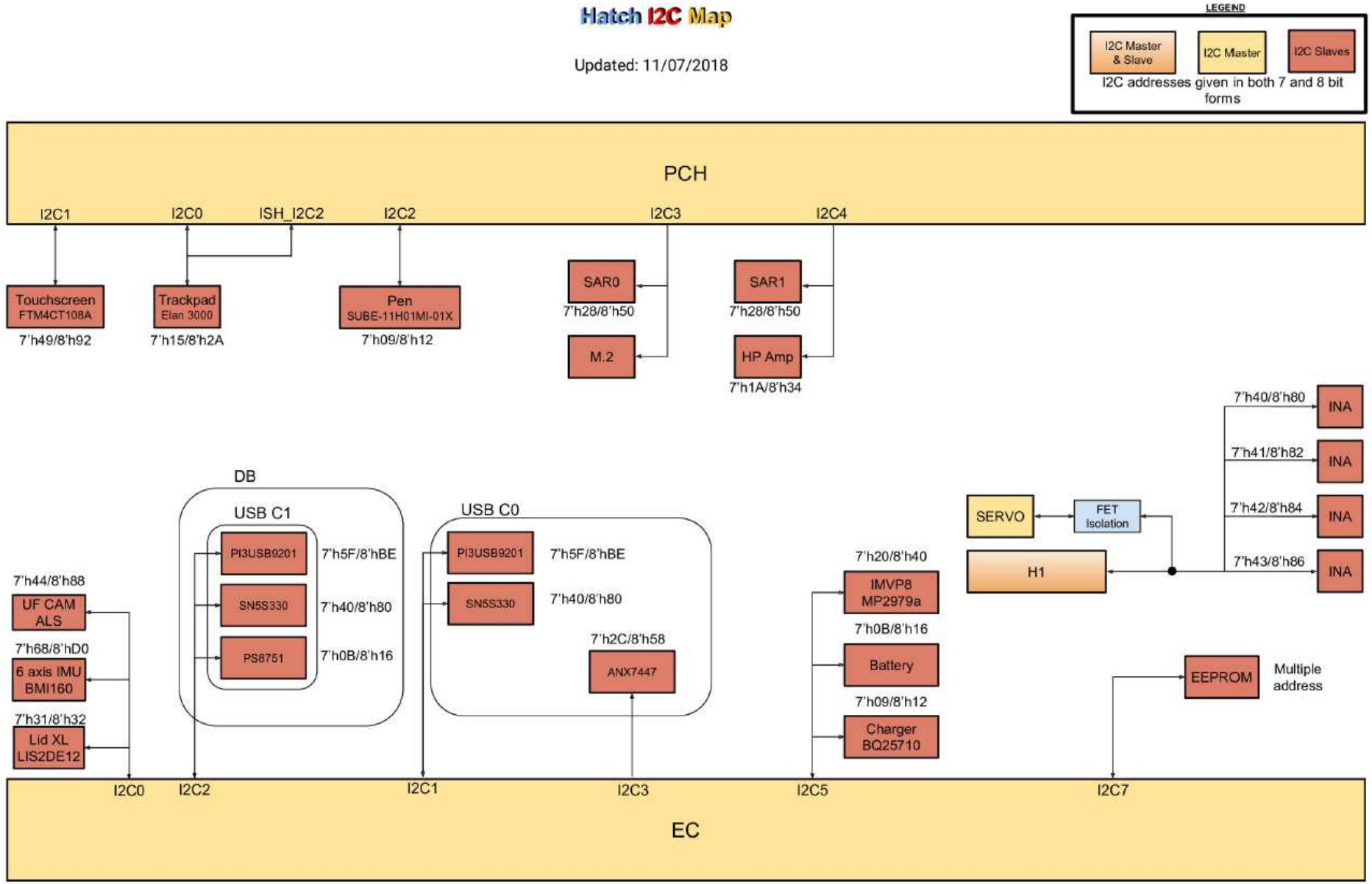
Hatch I2C Map

Updated: 11/07/2018



Quanta Computer Inc.		
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Size	Document Number: I2C MAP	Rev: 1C
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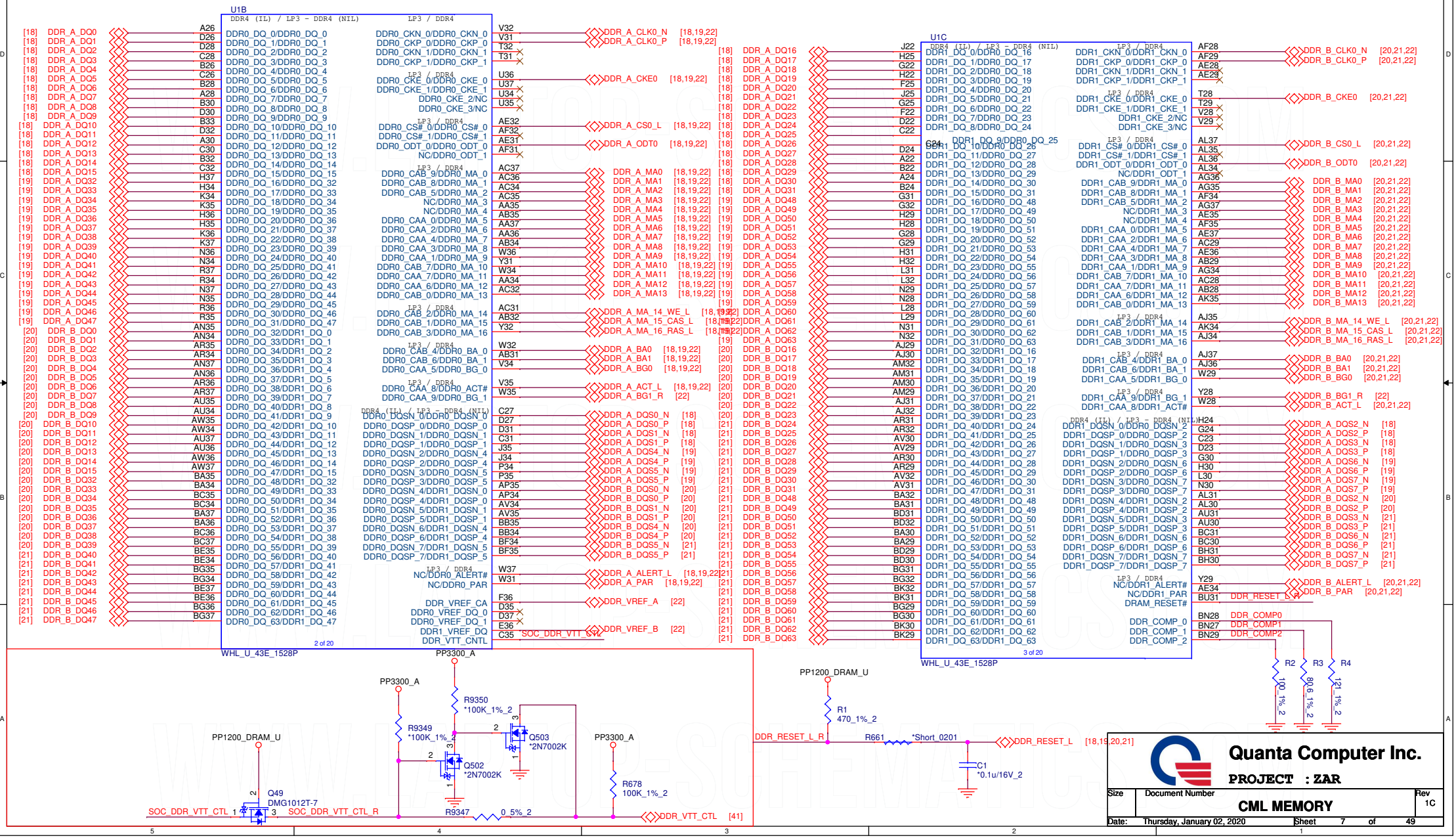

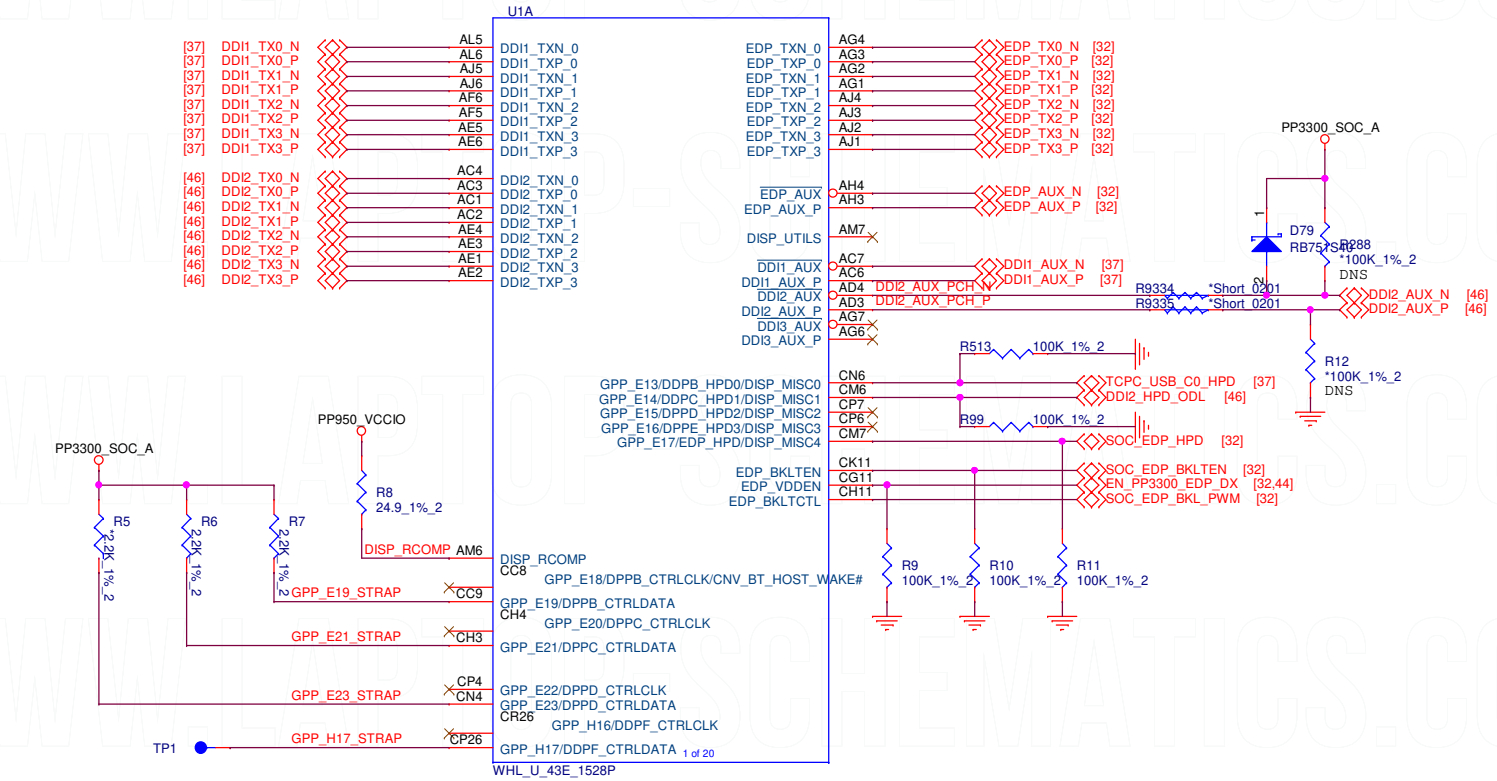

[9,10,11,12,14,25,44,45] PP3300_SOC_A
[13,17,40,45] PP950_VCCIO

Quanta Computer Inc.

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Size	Document Number	Rev
	CML DISPLAY	1C
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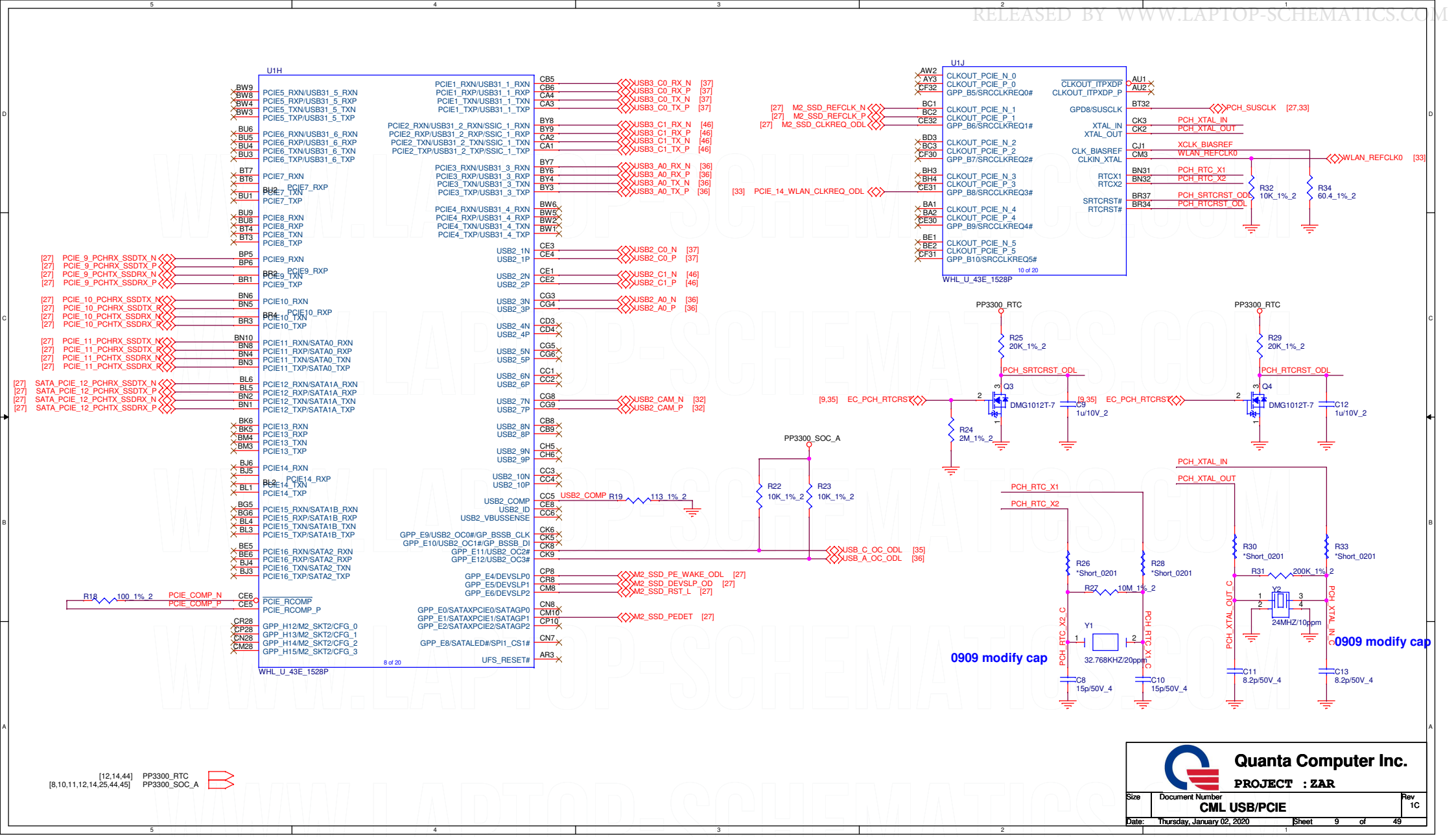

Quanta Computer Inc.

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Size	Document Number	Rev
	CML USB/PCIE	1C
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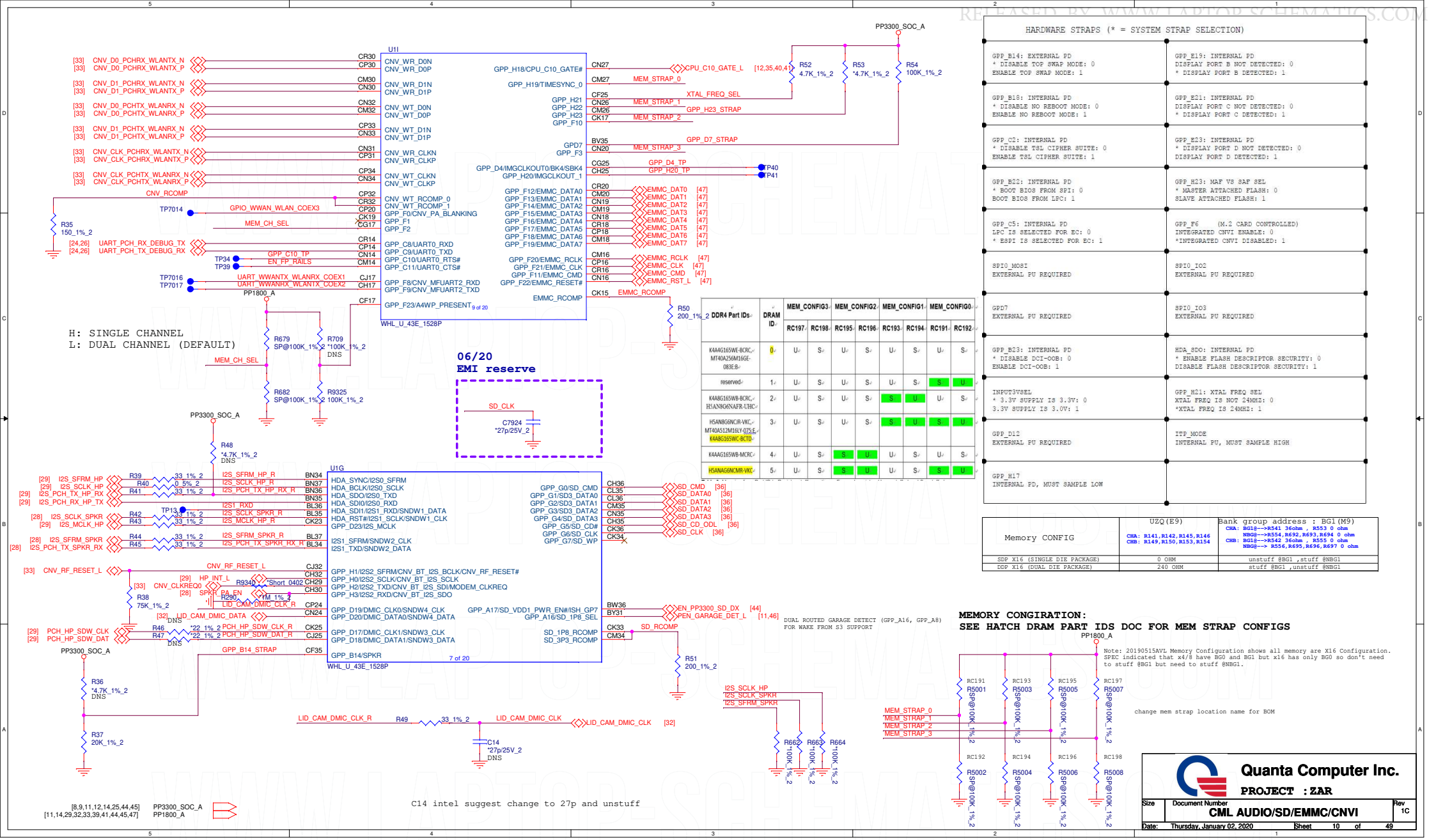
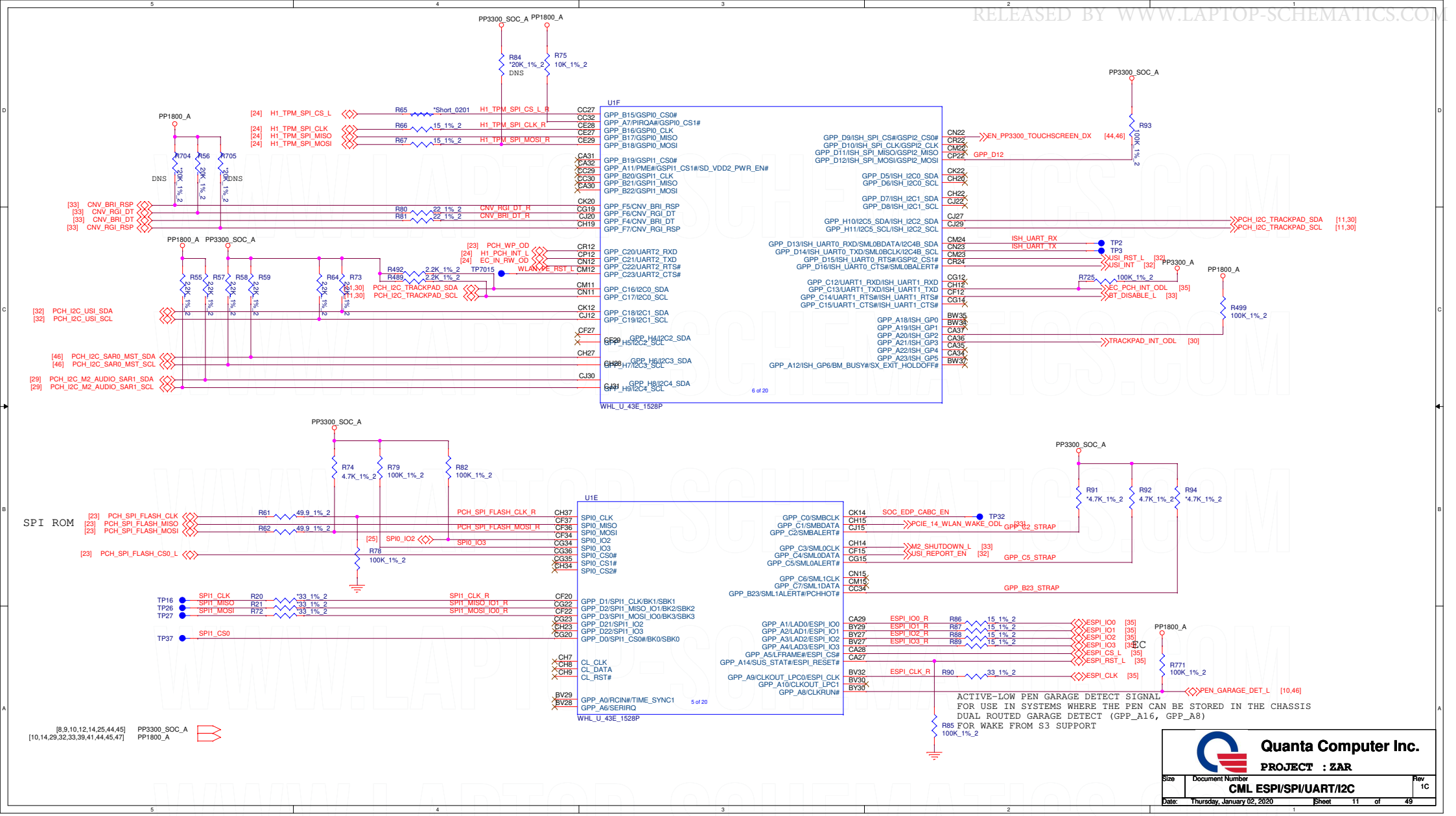


DDR4 Part IDs	DRAM ID	MEM_CONFIG3 RC197	MEM_CONFIG3 RC198	MEM_CONFIG2 RC195	MEM_CONFIG2 RC196	MEM_CONFIG1 RC193	MEM_CONFIG1 RC194	MEM_CONFIG0 RC191	MEM_CONFIG0 RC192
K4A4G165WE-BCRC, MT40A256M16GE-083E:B	0	U	S	U	S	U	S	U	S
reserved	1	U	S	U	S	U	S	S	U
K4A8G165WB-BCRC, H5AN8G6NAFR-UHC	2	U	S	U	S	S	U	U	S
H5AN8G6NCJR-VKC, MT40A512M16LY-075:E, K4A8G165WC-BCTD	3	U	S	U	S	S	U	S	U
K4AAG165WB-MCRC	4	U	S	S	U	U	S	U	S
H5ANAG6NCMR-VKC	5	U	S	S	U	U	S	S	U

Memory CONFIG	UZQ(E9)	Bank group address : BG1(M9)
	CHA: R141,R142,R145,R146 CHB: R149,R150,R153,R154	CHA: BG1@-->R541 36ohm , R553 0 ohm NBG@-->R554,R692,R693,R694 0 ohm CHB: BG1@-->R542 36ohm , R555 0 ohm NBG@--> R556,R695,R696,R697 0 ohm
SDP X16 (SINGLE DIE PACKAGE)	0 OHM	unstuff @BG1 ,stuff @NBG1
DDP X16 (DUAL DIE PACKAGE)	240 OHM	stuff @BG1 ,unstuff @NBG1



Quanta Computer Inc.

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Size	Document Number	Rev
	CML ESPI/SPI/UART/I2C	1C
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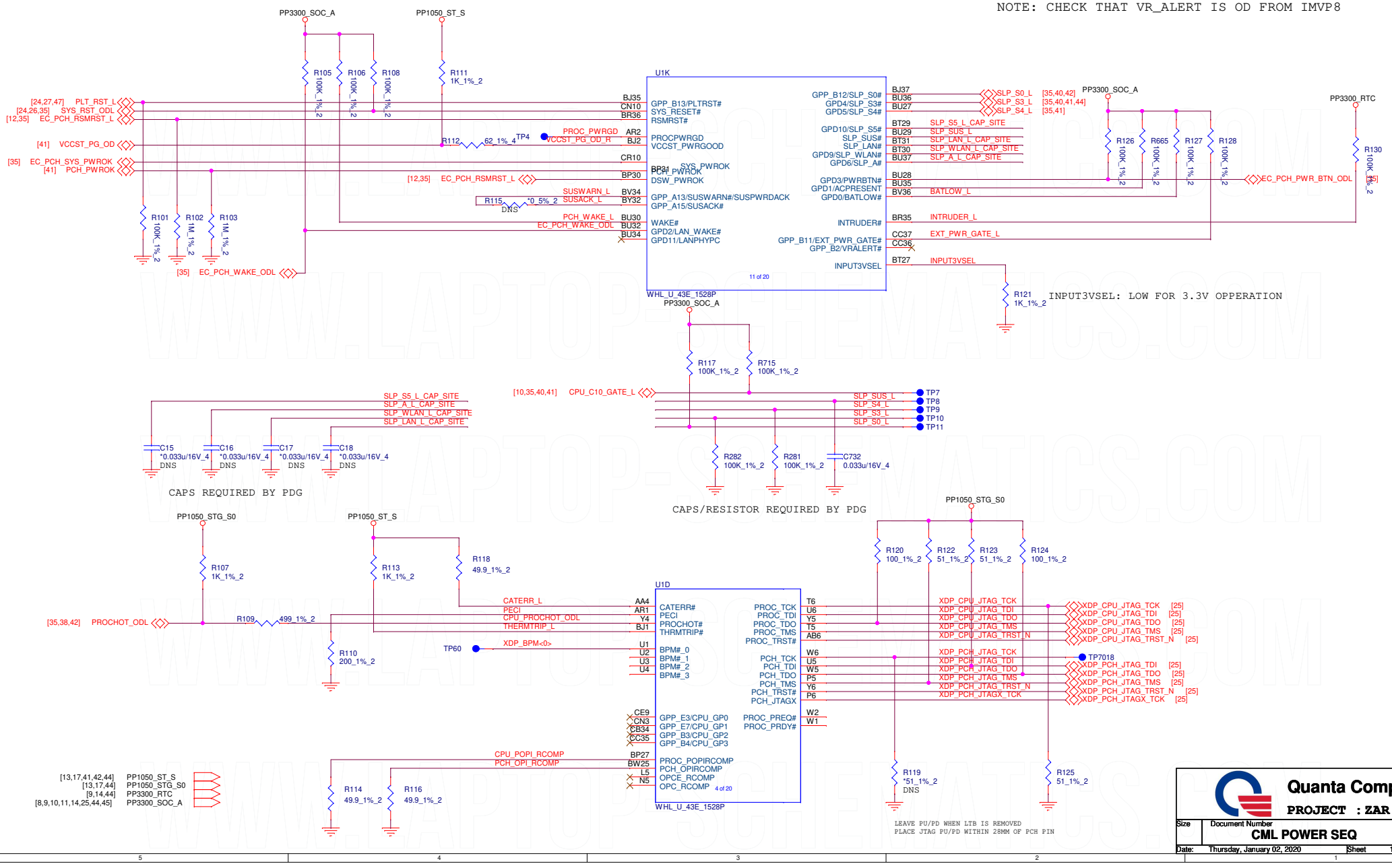
NOTE: CHECK THAT VR_ALERT IS OD FROM IMVP8



Quanta Computer Inc.

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Size	Document Number	Rev
	CML POWER SEQ	1C
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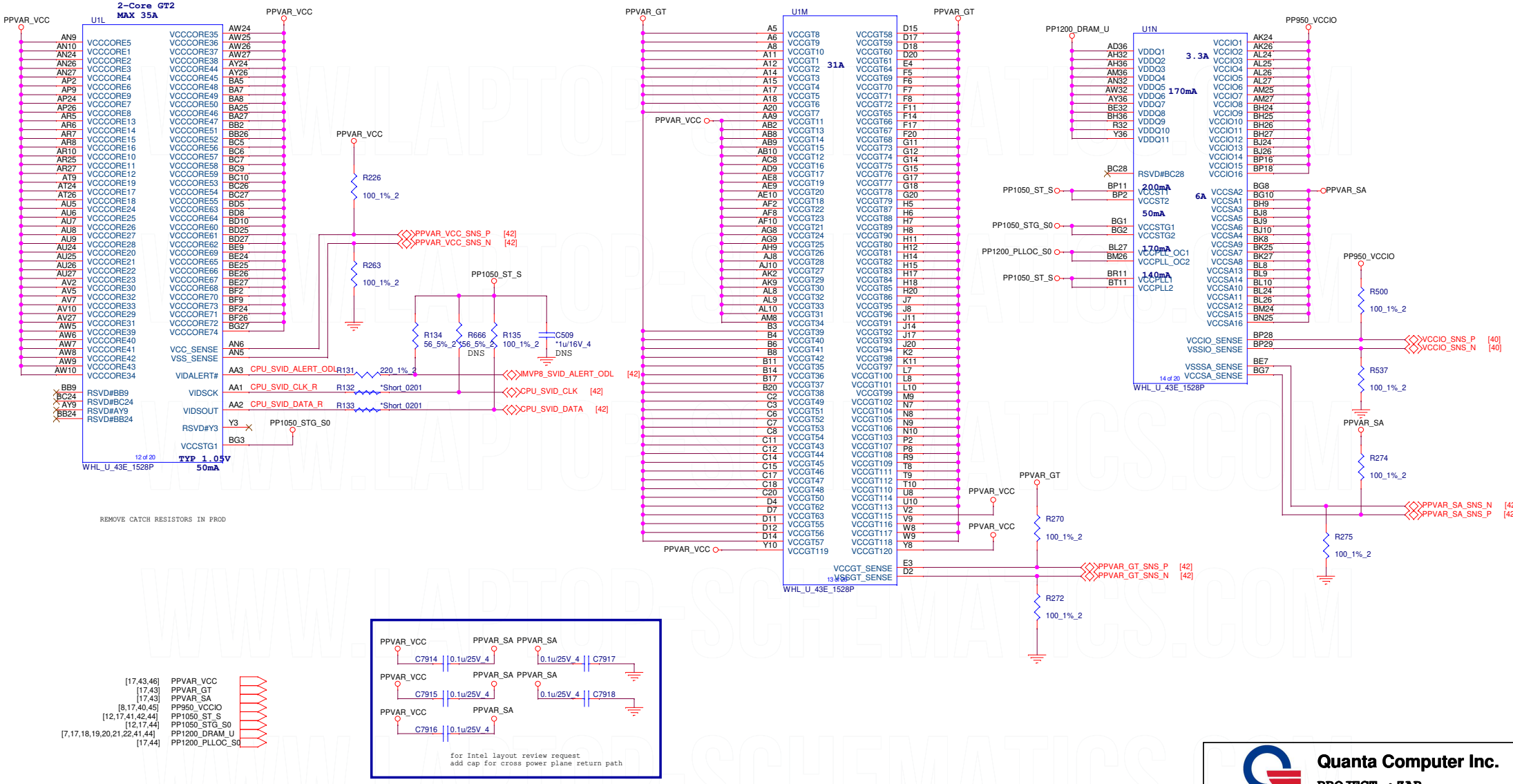
4/6 -Core GT2
MAX 70A(2 phase)

2-Core GT2
MAX 35A



[17,43,46] PPVAR_VCC
[17,43] PPVAR_GT
[17,43] PPVAR_SA
[8,17,40,45] PP950_VCCIO
[12,17,41,42,44] PP1050_ST_S
[12,17,44] PP1050_STG_S0
[7,17,18,19,20,21,22,41,44] PP1200_DRAM_U
[17,44] PP1200_PLLOC_S0

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Size	Document Number		Rev
	CML CORE POWER		1C
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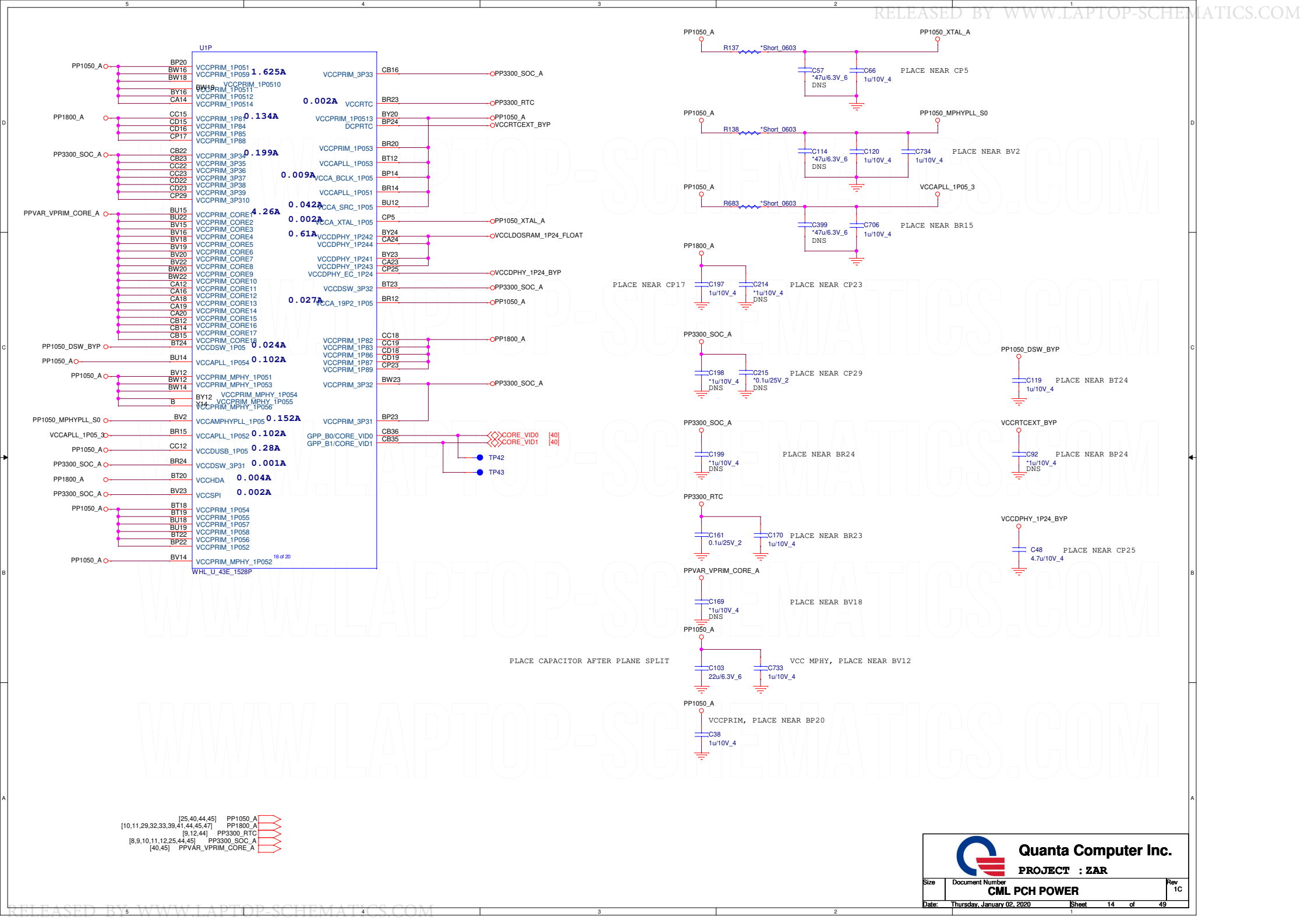

Quanta Computer Inc.		
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Size	Document Number: CML PCH POWER	Rev: 1C
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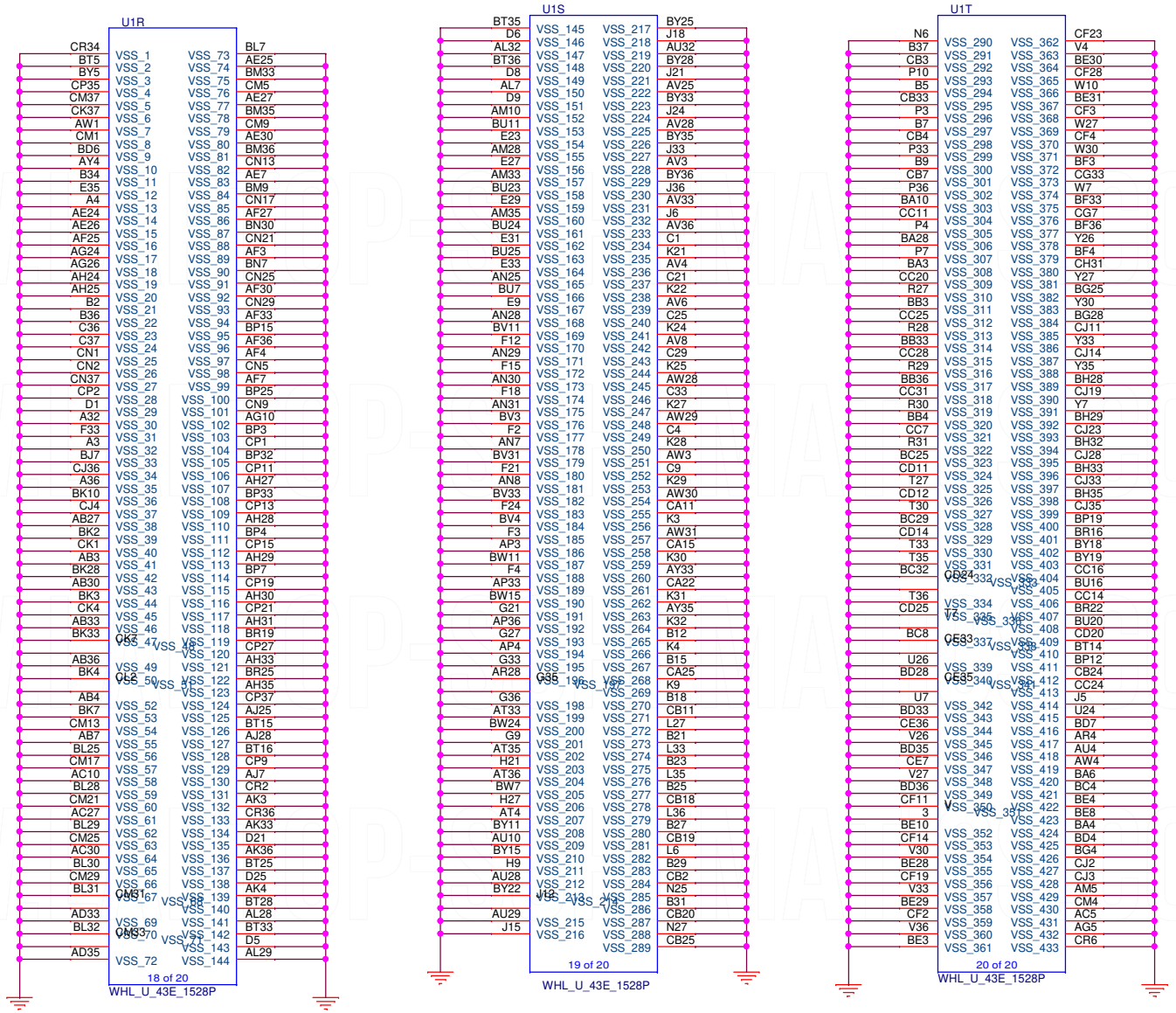

Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	CML GND	1C

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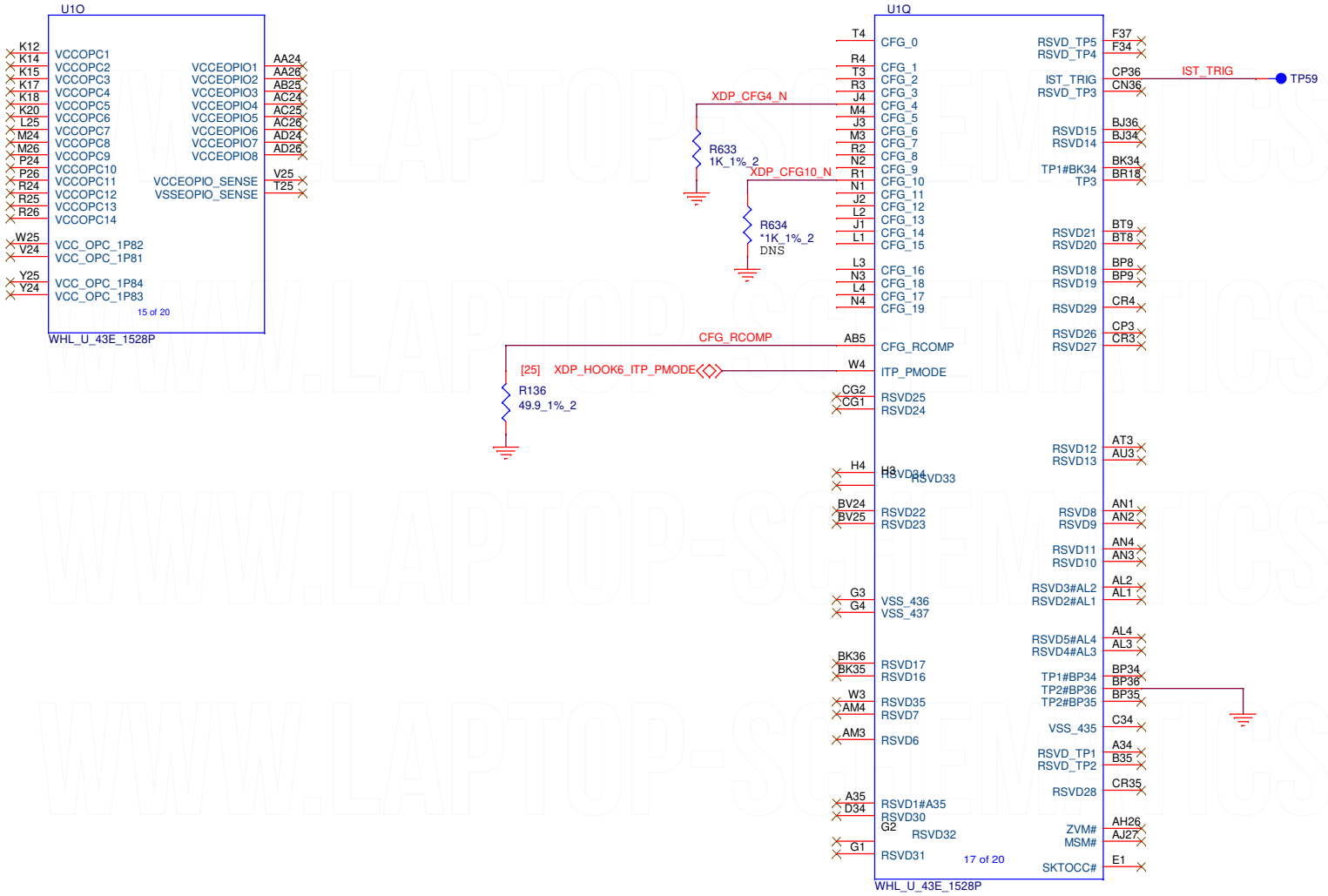

Quanta Computer Inc.

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Size	Document Number	Rev
	CML DEBUG/RSVD	1C

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CPU DECOUPLING

BOTTOM SIDE

PPVAR_VCC

C22 2.2u/10V_4, C30 2.2u/10V_4, C40 2.2u/10V_4, C49 2.2u/10V_4, C58 2.2u/10V_4, C67 2.2u/10V_4, C75 2.2u/10V_4, C82 2.2u/10V_4, C88 2.2u/10V_4, C95 2.2u/10V_4, C99 2.2u/10V_4, C104 2.2u/10V_4, C108 2.2u/10V_4, C115 2.2u/10V_4

C23 2.2u/10V_4, C31 2.2u/10V_4, C41 2.2u/10V_4, C50 2.2u/10V_4, C59 2.2u/10V_4, C68 2.2u/10V_4, C76 2.2u/10V_4

PPVAR_VCC

C24 10u/6.3V_4, C32 10u/6.3V_4, C42 10u/6.3V_4, C51 10u/6.3V_4, C60 10u/6.3V_4, C69 10u/6.3V_4, C77 10u/6.3V_4, C83 10u/6.3V_4, C89 10u/6.3V_4, C96 10u/6.3V_4, C100 10u/6.3V_4, C105 10u/6.3V_4, C109 10u/6.3V_4, C116 10u/6.3V_4

C26 22u/6.3V_6, C34 22u/6.3V_6, C44 22u/6.3V_6, C53 22u/6.3V_6, C62 22u/6.3V_6, C71 22u/6.3V_6, C79 22u/6.3V_6, C84 22u/6.3V_6, C90 22u/6.3V_6

TOP SIDE

PPVAR_VCC

C27 10u/6.3V_4, C35 10u/6.3V_4, C45 10u/6.3V_4, C54 10u/6.3V_4, C63 10u/6.3V_4, C72 10u/6.3V_4, C80 10u/6.3V_4, C85 10u/6.3V_4

CH5223MEB00
CAP CHIP 2.2U 16V(+-20%,X6S,0402)

CH6101MEB01
CAP CHIP 10UF 6.3V(+-20%,X6S,0402)

CH6221ME900
CAP CHIP 22U 6.3V(+-20%,X6S,0603)

PPVAR_VCC

C28 47u/6.3V_8, C36 47u/6.3V_8, C46 47u/6.3V_8, C55 47u/6.3V_8 high, C64 47u/6.3V_8, C73 47u/6.3V_8 high, C81 47u/6.3V_8, C86 47u/6.3V_8 high, C91 47u/6.3V_8 high, C98 47u/6.3V_8 high, C102 47u/6.3V_8, C107 47u/6.3V_8, C111 47u/6.3V_8, C118 47u/6.3V_8 high

C29 47u/6.3V_8 high, C37 47u/6.3V_8 high, C47 47u/6.3V_8, C56 47u/6.3V_8

BOTTOM SIDE VCCPLLOC

PP1200_PLLOC_S0

C39 1u/10V_4

EITHER SIDE VCCPLL

PP1050_ST_S

C87 1u/10V_4, C94 22u/6.3V_6

TOP SIDE

PP1050_STG_S0

C113 1u/10V_4

TOP SIDE VCCPLL

PP1050_ST_S

C93 1u/10V_4

TOP SIDE

PP1050_ST_S

C112 1u/10V_4

[12,13,41,42,44] PP1050_ST_S
[12,13,44] PP1050_STG_S0
[7,13,18,19,20,21,22,41,44] PP1200_DRAM_U
[13,44] PP1200_PLLOC_S0
[8,13,40,45] PP950_VCCIO
[13,43,46] PPVAR_VCC
[13,43] PPVAR_GT
[13,43] PPVAR_SA

BOTTOM SIDE

PPVAR_GT

C121 1u/10V_2, C130 1u/10V_2, C139 1u/10V_2, C147 1u/10V_2, C155 1u/10V_2, C162 1u/10V_2, C171 1u/10V_2, C175 1u/10V_2, C179 1u/10V_2

C122 1u/10V_2, C131 1u/10V_2

PPVAR_GT

C123 10u/6.3V_4, C132 10u/6.3V_4, C140 10u/6.3V_4, C148 10u/6.3V_4, C156 10u/6.3V_4, C163 10u/6.3V_4, C172 10u/6.3V_4, C176 10u/6.3V_4, C180 10u/6.3V_4

C124 10u/6.3V_4, C133 10u/6.3V_4, C141 10u/6.3V_4, C149 10u/6.3V_4, C157 10u/6.3V_4, C164 10u/6.3V_4

TOP SIDE

PPVAR_GT

C125 22u/6.3V_6, C134 22u/6.3V_6, C142 22u/6.3V_6, C150 22u/6.3V_6, C158 22u/6.3V_6, C165 22u/6.3V_6, C173 22u/6.3V_6, C177 22u/6.3V_6, C181 22u/6.3V_6

C126 22u/6.3V_6, C135 22u/6.3V_6, C143 22u/6.3V_6, C151 22u/6.3V_6, C159 22u/6.3V_6, C166 22u/6.3V_6

PPVAR_GT

C127 47u/6.3V_8, C136 47u/6.3V_8, C144 47u/6.3V_8 high, C152 47u/6.3V_8 high

TOP SIDE

PP950_VCCIO

C128 1u/10V_2, C137 1u/10V_2, C145 1u/10V_2, C153 1u/10V_2

PP950_VCCIO

C167 *10u/6.3V_4, C174 *10u/6.3V_4, C178 *10u/6.3V_4, C182 *10u/6.3V_4

EITHER SIDE

PP950_VCCIO

C129 10u/6.3V_4, C138 10u/6.3V_4, C146 10u/6.3V_4, C154 10u/6.3V_4, C160 10u/6.3V_4, C168 10u/6.3V_4

BOTTOM SIDE

PPVAR_SA

C183 10u/6.3V_4, C190 10u/6.3V_4, C200 10u/6.3V_4, C208 10u/6.3V_4, C216 10u/6.3V_4, C220 10u/6.3V_4

C184 *10u/6.3V_4, C191 *10u/6.3V_4, C201 *10u/6.3V_4, C209 *10u/6.3V_4, C217 10u/6.3V_4

TOP SIDE

PPVAR_SA

C185 10u/6.3V_4, C192 10u/6.3V_4, C202 10u/6.3V_4, C210 10u/6.3V_4, C218 10u/6.3V_4, C221 10u/6.3V_4

C186 47u/6.3V_8 high, C193 47u/6.3V_8 high, C203 *47u/6.3V_8 high, C211 47u/6.3V_8 high

BOTTOM SIDE

PP1200_DRAM_U

C187 1u/10V_2, C194 1u/10V_2, C204 1u/10V_2, C212 1u/10V_2

C188 10u/6.3V_4, C195 10u/6.3V_4, C205 10u/6.3V_4

TOP SIDE

PP1200_DRAM_U

C189 10u/6.3V_4, C196 10u/6.3V_4, C206 10u/6.3V_4, C213 10u/6.3V_4, C219 10u/6.3V_4, C222 10u/6.3V_4

PP1200_DRAM_U

C207 22u/6.3V_6

Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	CML POWER RAIL DECOUPLING	1C
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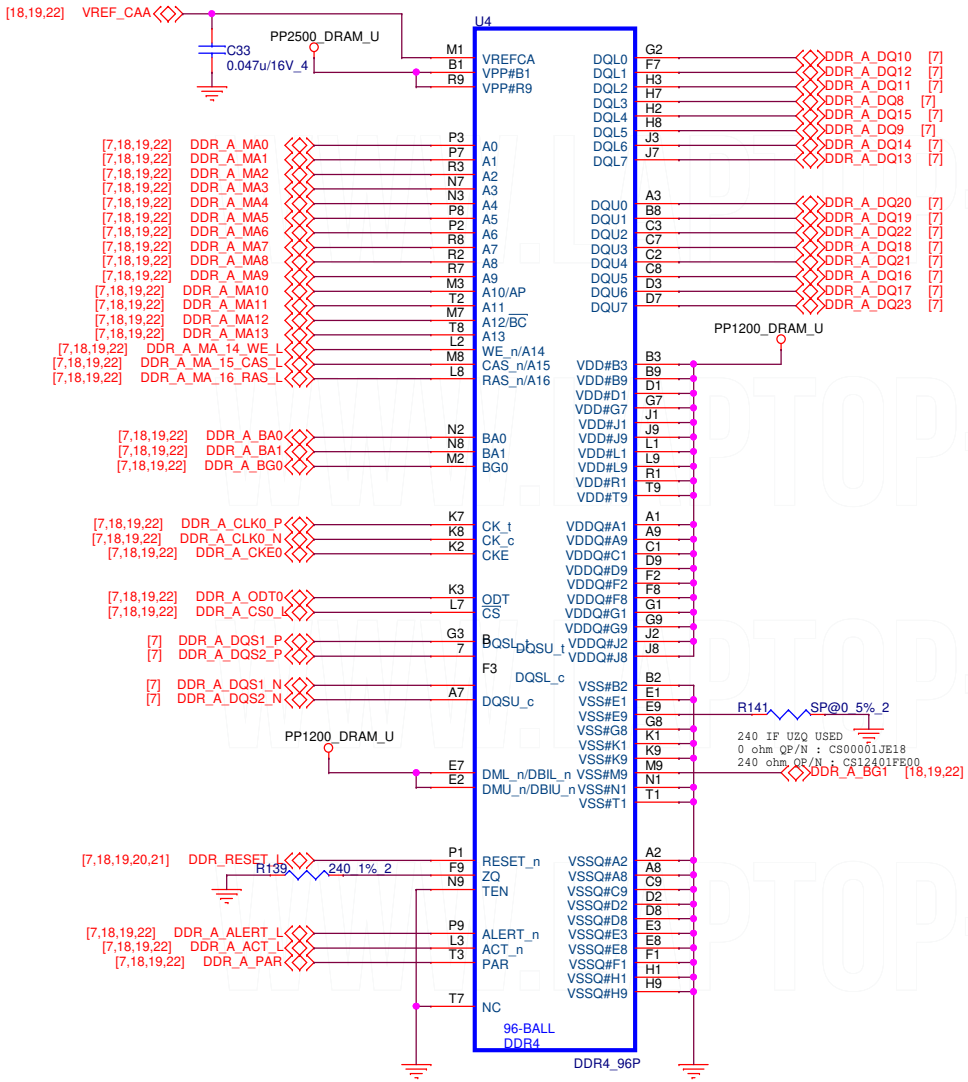

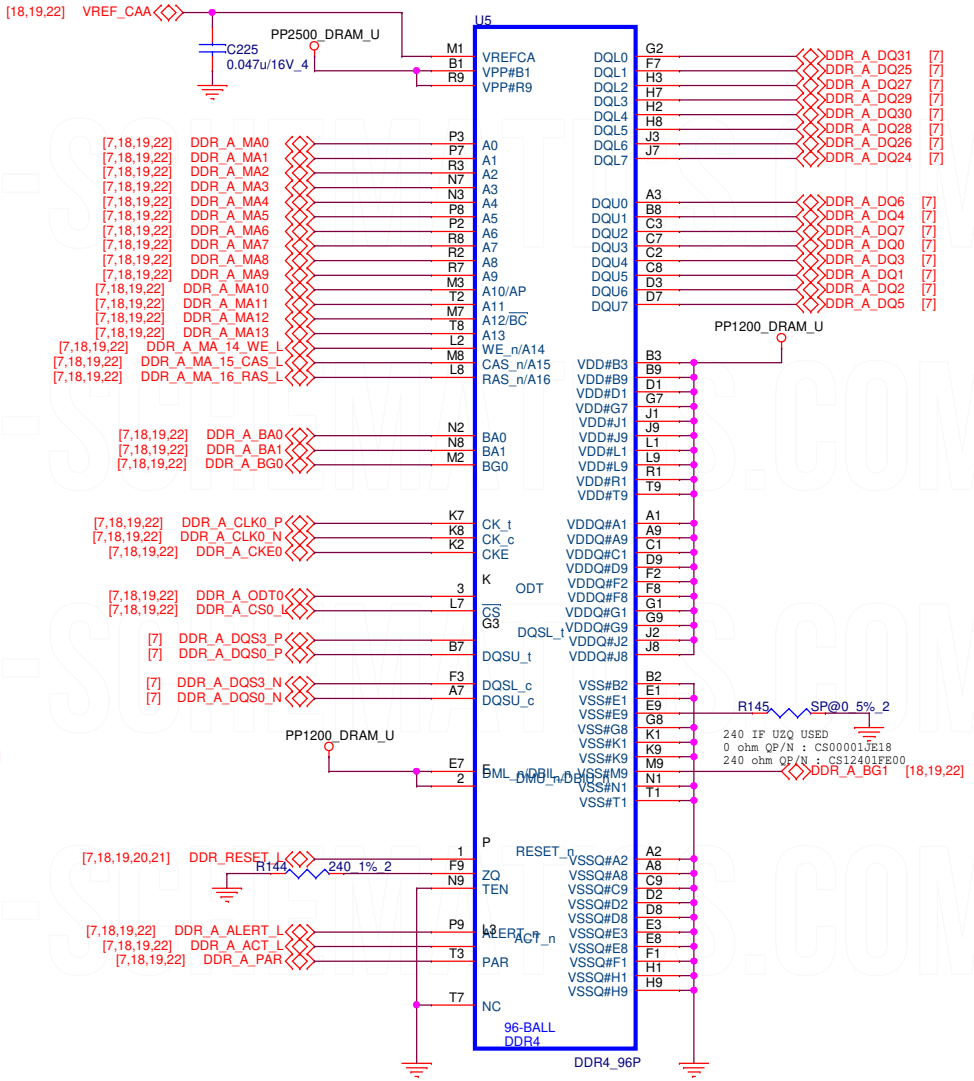

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Size	Document Number: MEMORY CH A-1 DDR4	Rev: 1C
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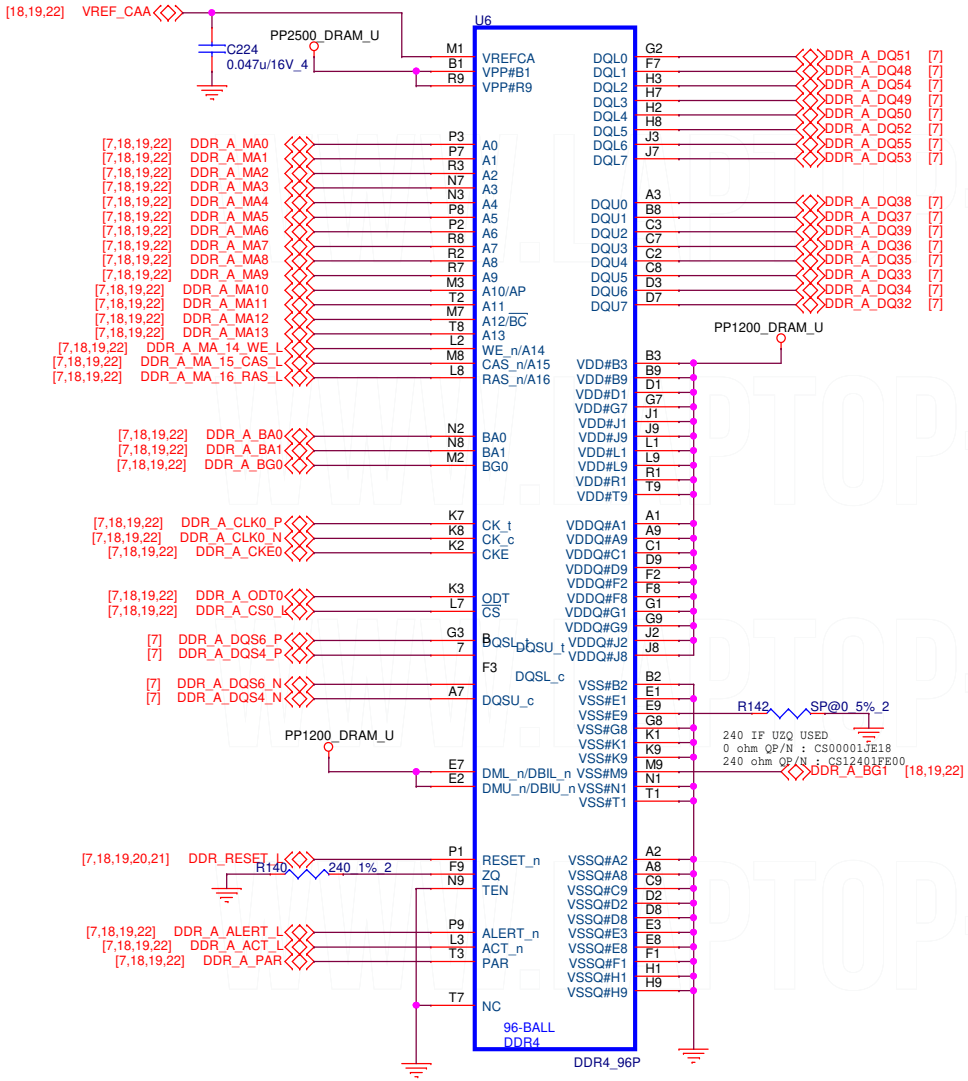

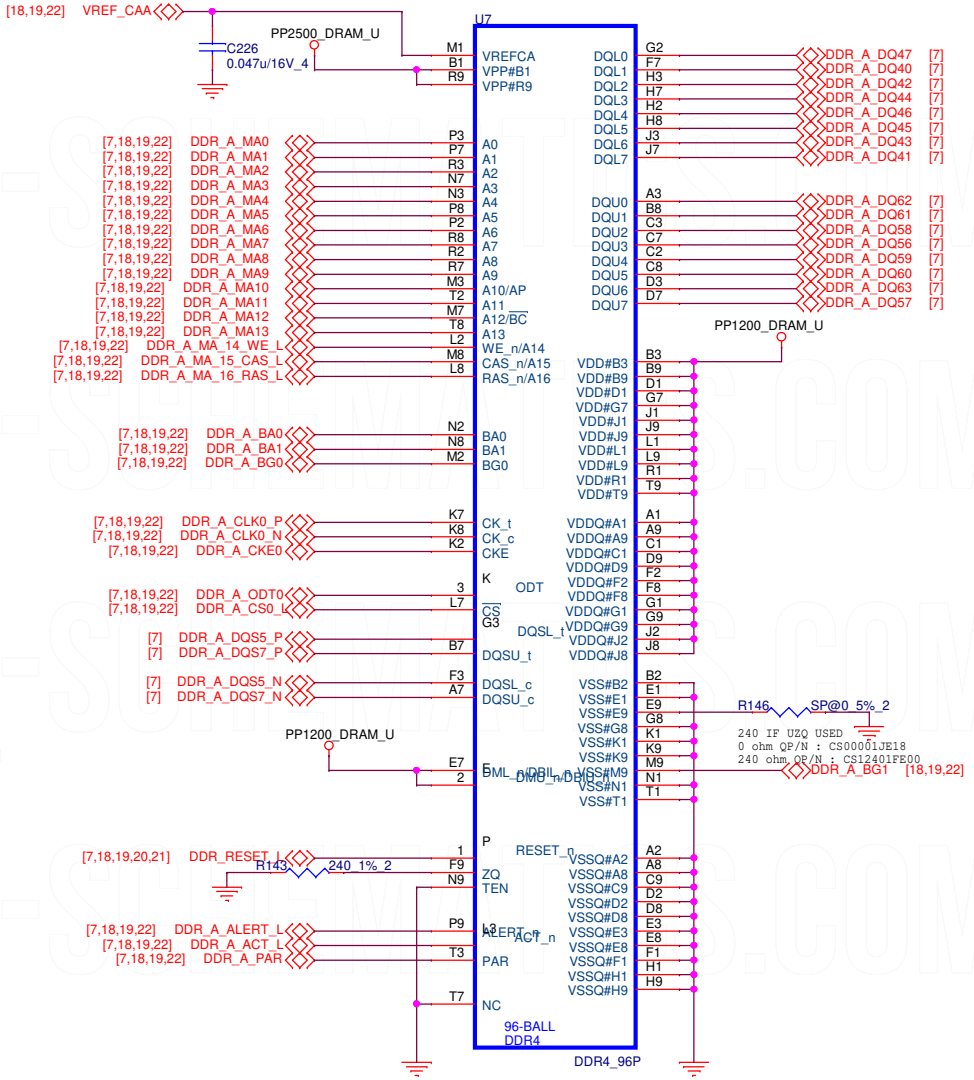

[7,13,17,18,20,21,22,41,44] PP1200_DRAM_U
[18,20,21,22,41,45] PP2500_DRAM_U

Quanta Computer Inc.

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Size	Document Number	Rev
	MEMORY CH A-2 DDR4	1C
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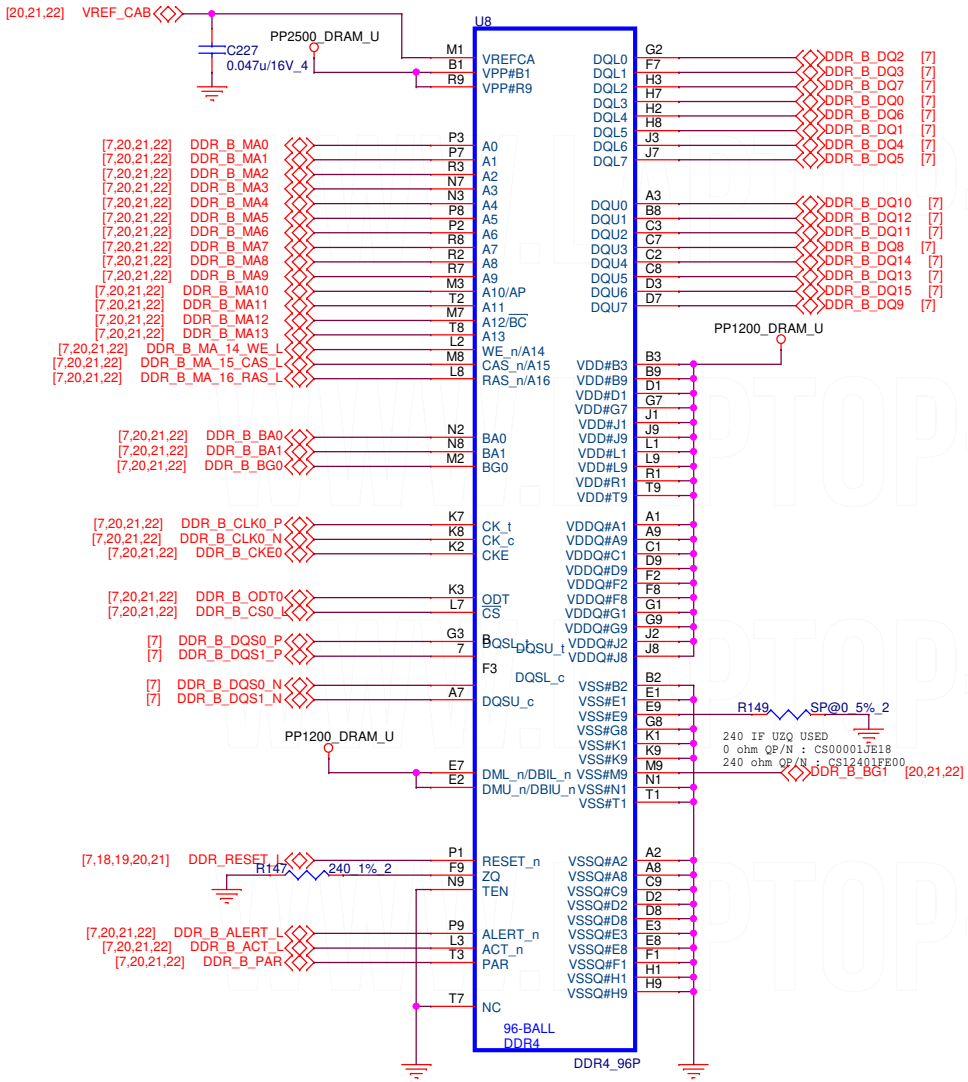

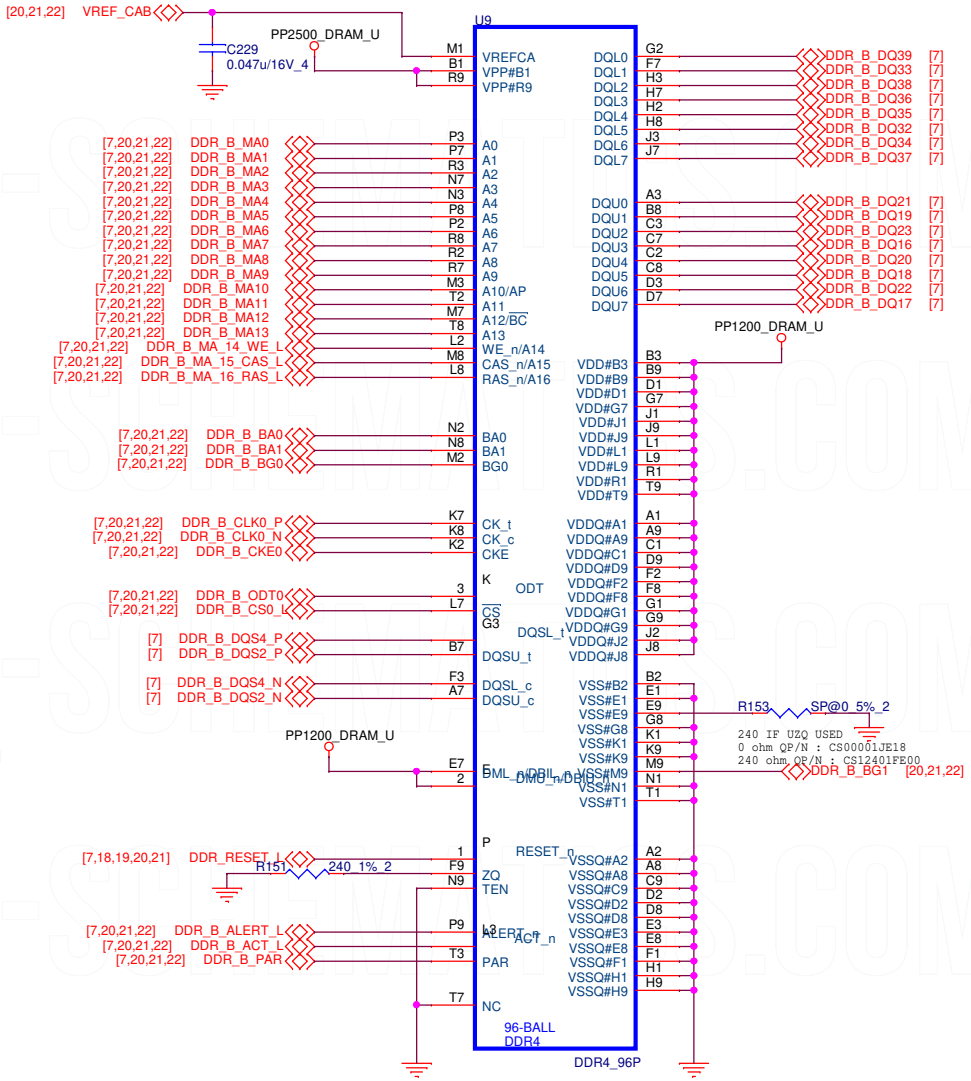

[7,13,17,18,19,21,22,41,44] PP1200_DRAM_U
[18,19,21,22,41,45] PP2500_DRAM_U

Quanta Computer Inc.

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Size	Document Number	Rev
	MEMORY CH B-1 DDR4	1C
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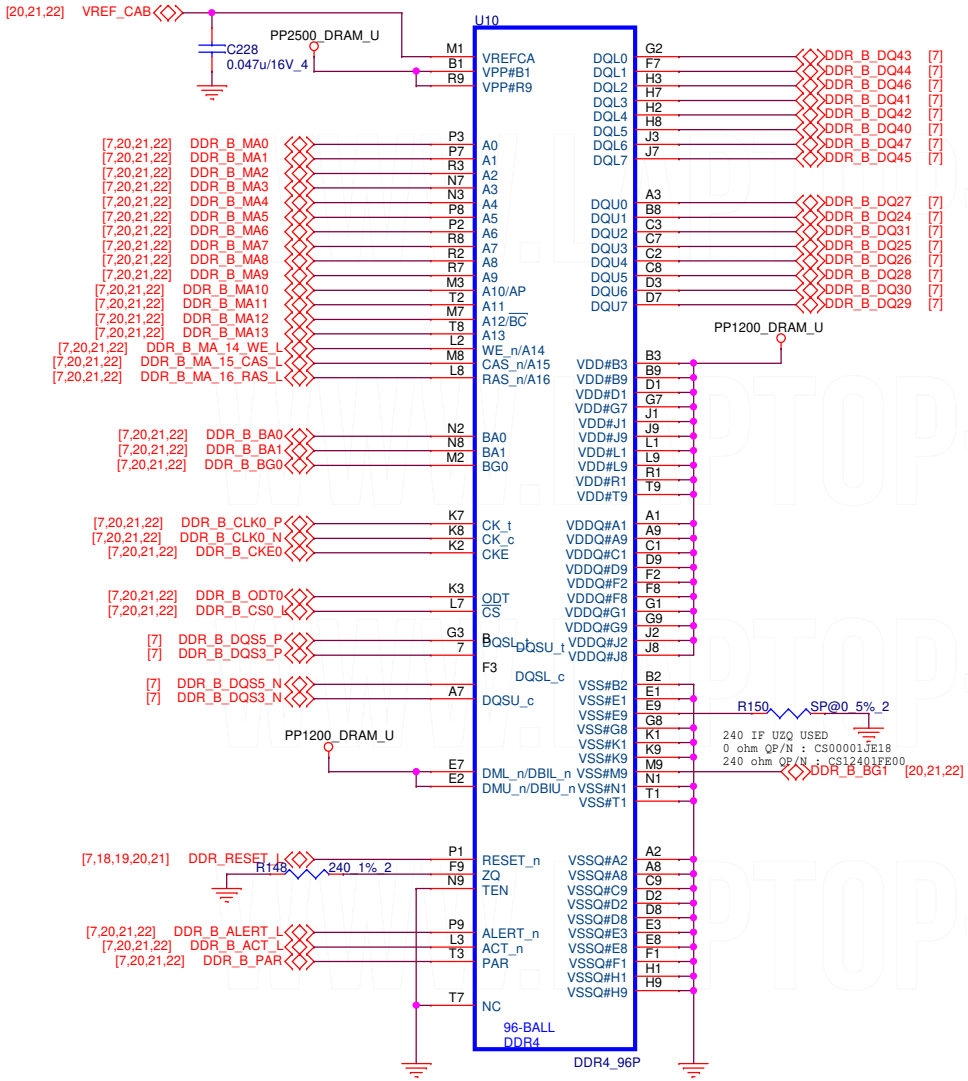

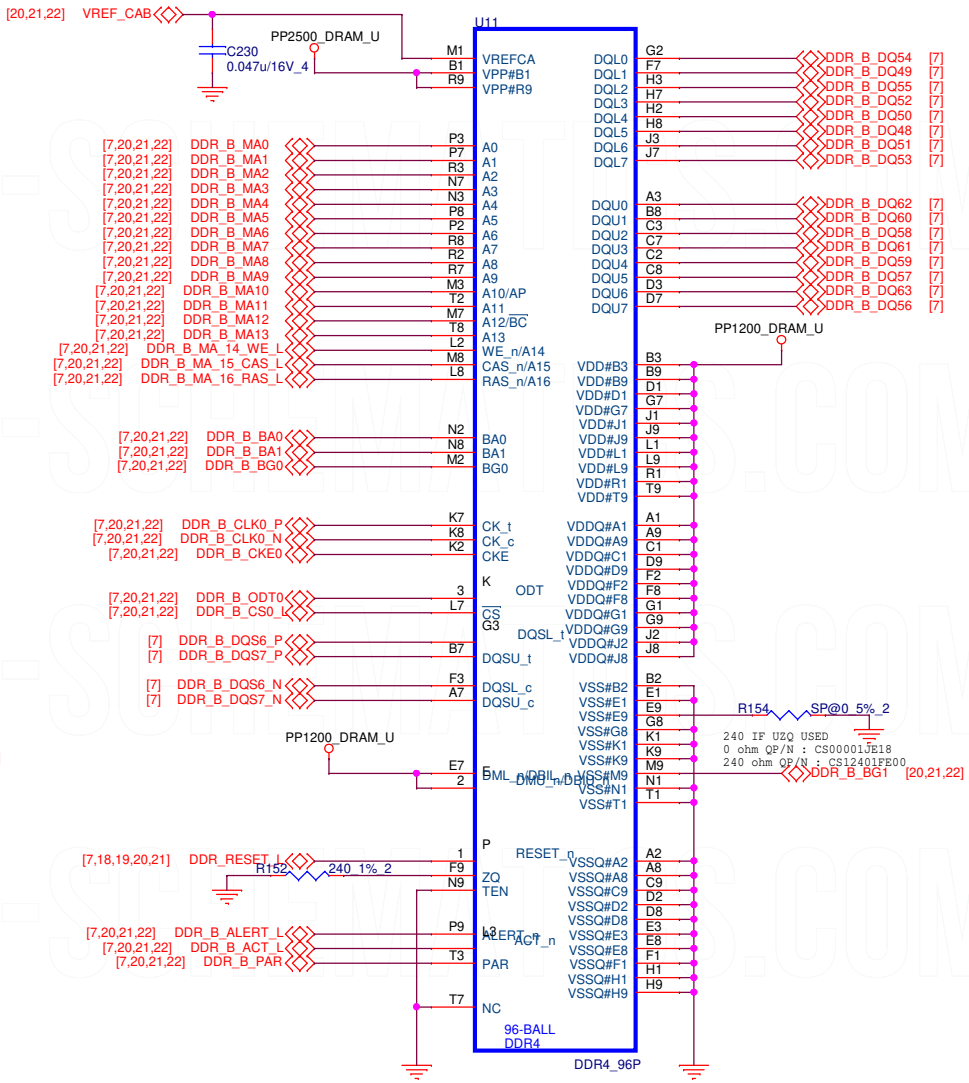

[7,13,17,18,19,20,22,41,44] PP1200_DRAM_U
[18,19,20,22,41,45] PP2500_DRAM_U

Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: MEMORY CH B-2 DDR4	Rev: 1C
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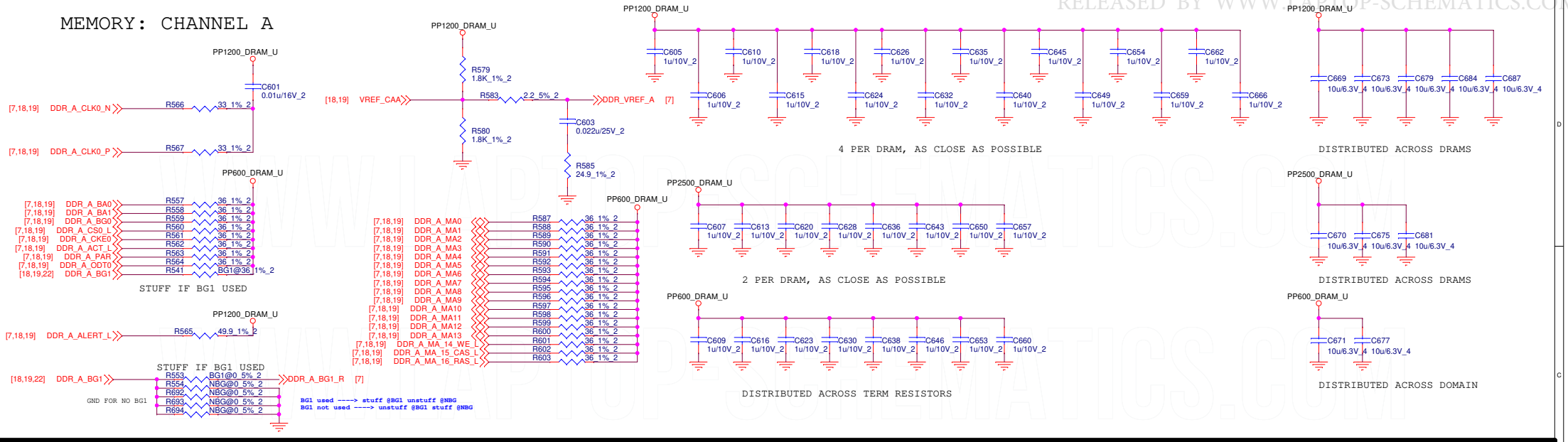
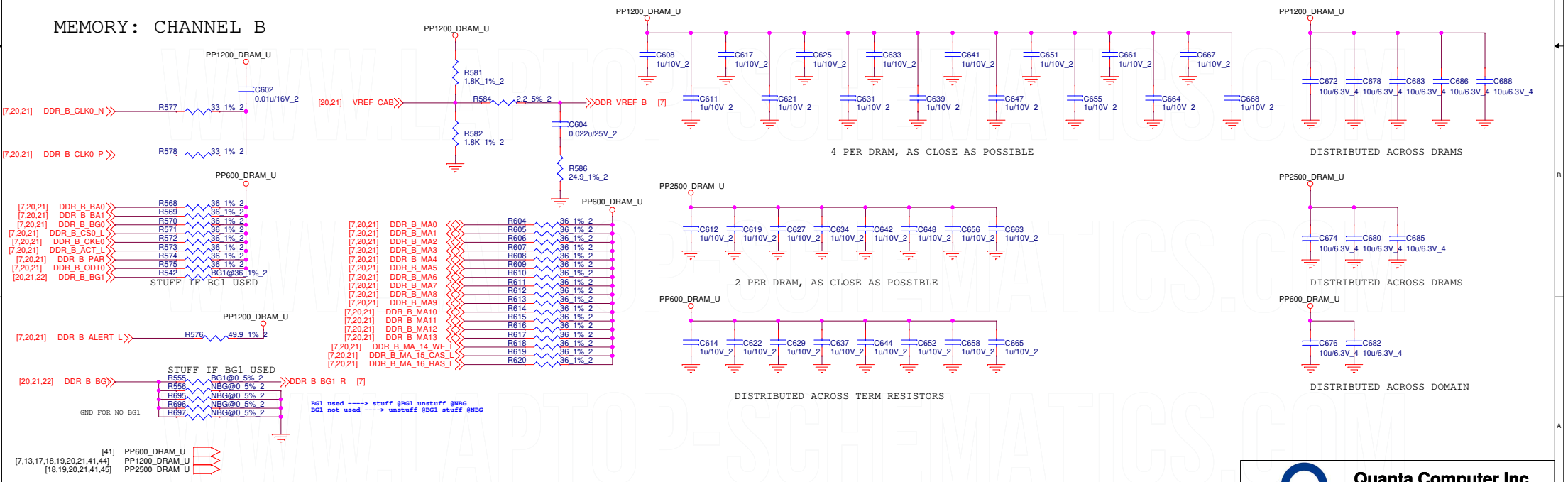
MEMORY: CHANNEL A



MEMORY: CHANNEL B



Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	MEMORY DECOUPLING/TERM	1C
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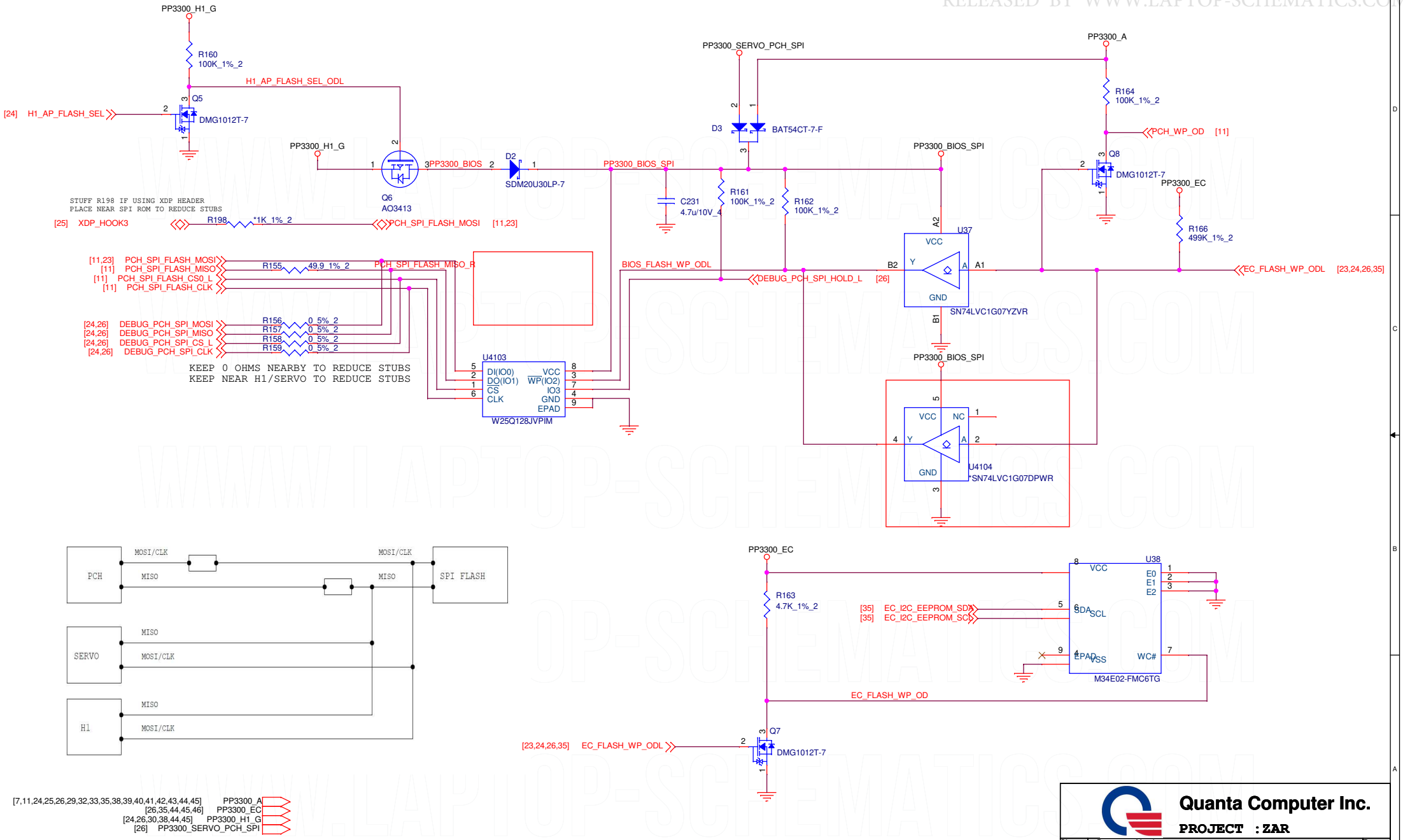

Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	SPI ROM	1C
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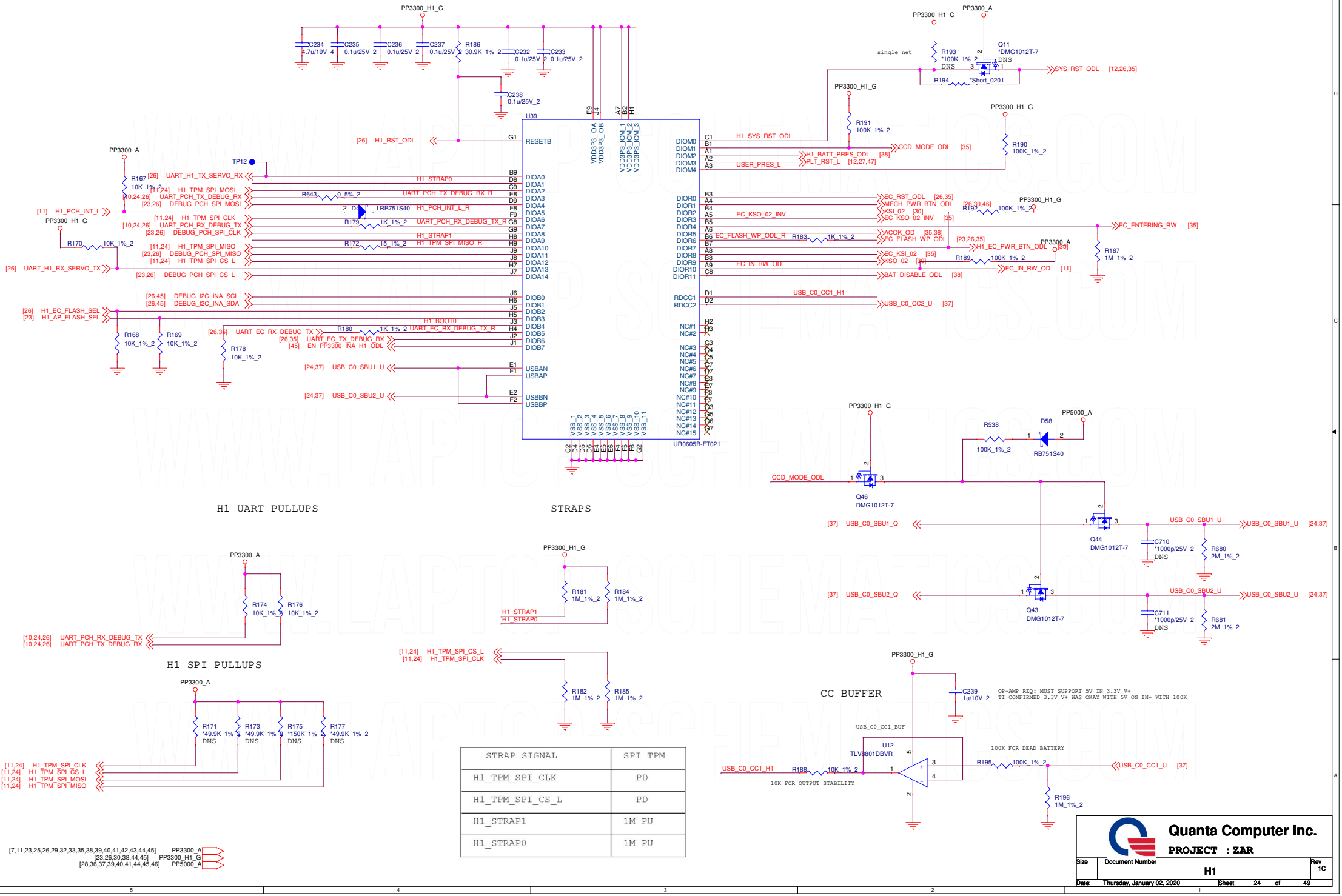

STRAP SIGNAL	SPI TPM
H1_TPM_SPI_CLK	PD
H1_TPM_SPI_CS_L	PD
H1_STRAP1	1M PU
H1_STRAP0	1M PU

Quanta Computer Inc.		
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	H1	1C
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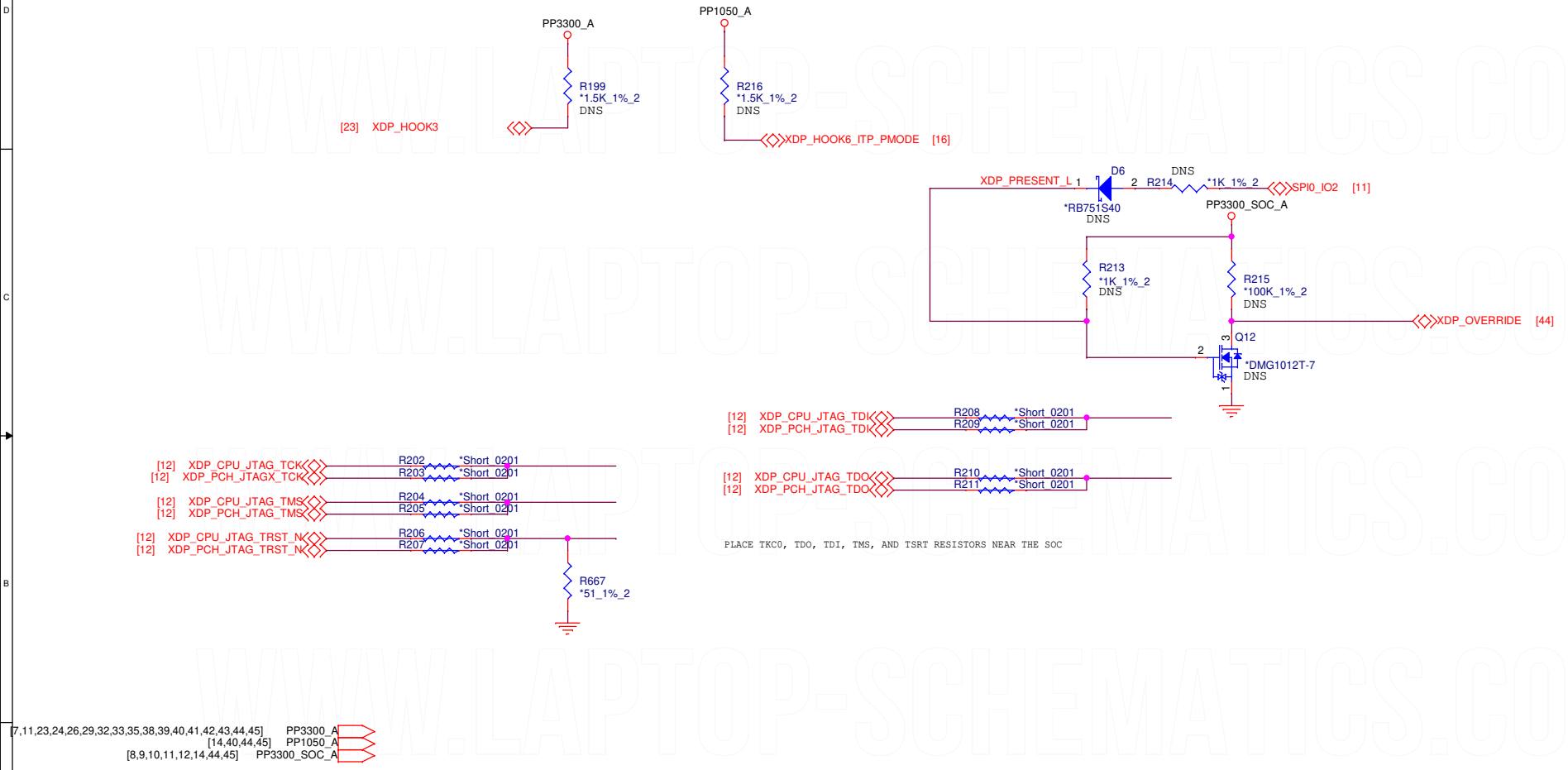

Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	XDP DEBUG HEADER	1C
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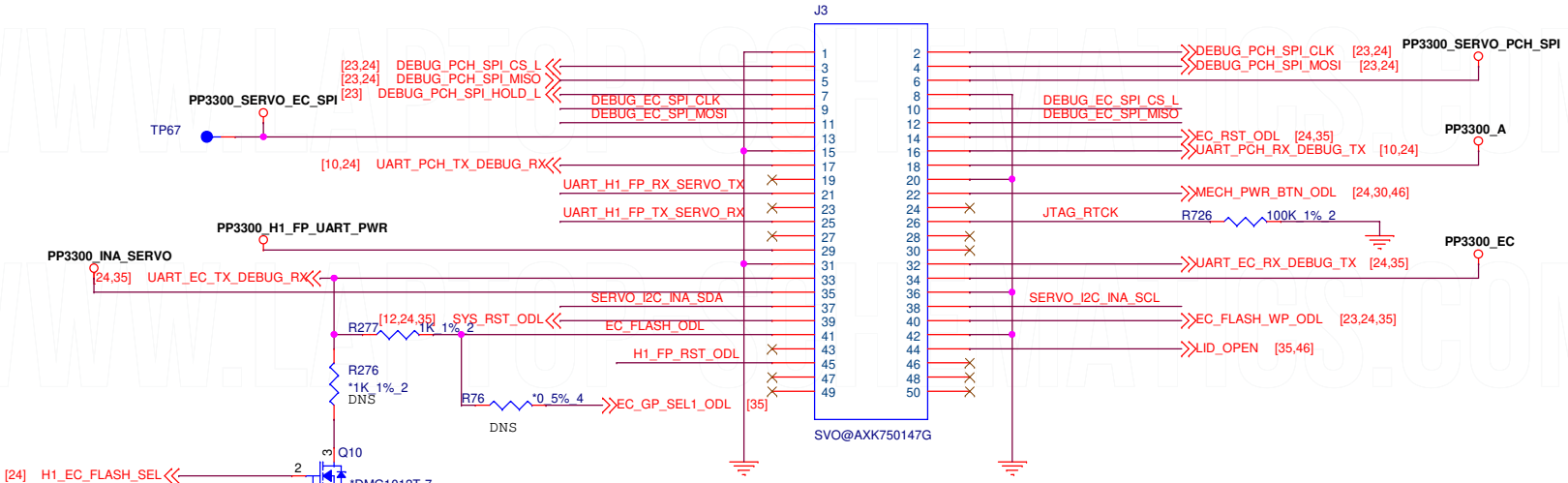
[35] KSI_04_EC_SPI_FLASH_CLK — R221 33_1%_2 — DEBUG_EC_SPI_CLK
[35] KSI_00_EC_SPI_FLASH_MOSI — R222 33_1%_2 — DEBUG_EC_SPI_MOSI
[35] KSI_05_EC_SPI_FLASH_MISO — R223 *Short_0201 — DEBUG_EC_SPI_MISO
[35] KSI_01_EC_SPI_FLASH_CS_L — R224 33_1%_2 — DEBUG_EC_SPI_CS_L

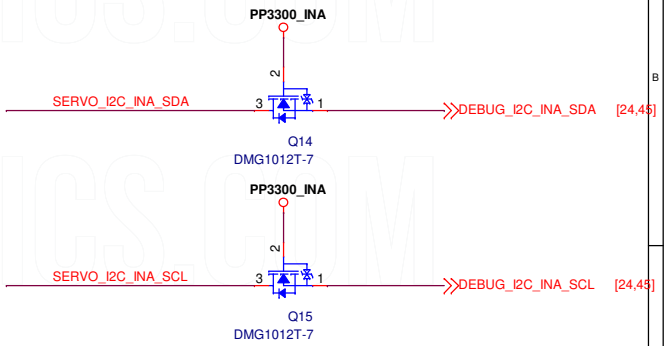
SERVO HEADER



EC POWER FOR FLASHING

[24] UART_H1_TX_SERVO_RX — R744 *Short_0402 — UART_H1_FP_TX_SERVO_RX
[24] UART_H1_RX_SERVO_TX — R746 *Short_0402 — UART_H1_FP_RX_SERVO_TX
[24] H1_RST_ODL — R748 *Short_0402 — H1_FP_RST_ODL
PP3300_H1_G — R225 *Short_0402 — PP3300_H1_FP_UART_PWR

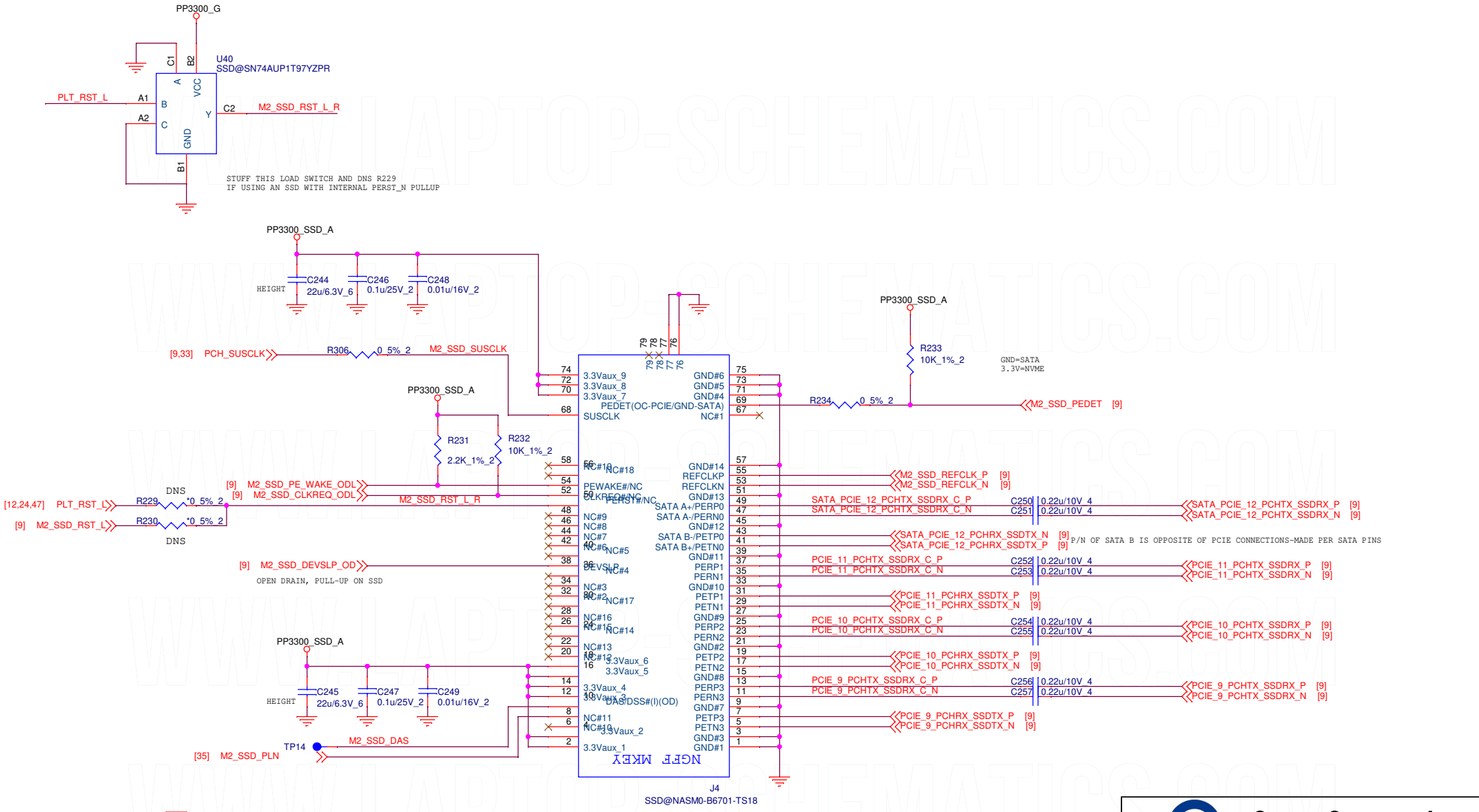
LEAKAGE PROTECTION FROM SERVO



[7,11,23,24,25,29,32,33,35,38,39,40,41,42,43,44,45] PP3300_A
[23,35,44,45,46] PP3300_EC
[27,29,35,39,44,45,46] PP3300_G
[23,24,30,38,44,45] PP3300_H1_G
[45] PP3300_INA
[45] PP3300_INA_SERVO
[23] PP3300_SERVO_PCH_SPI
[30,32,38,39,40,41,42,43] PPVAR_SYS

Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	SERVO DEBUG	1C
Date: Thursday, January 02, 2020	Sheet 26 of 49	



Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: SSD M.2	Rev: 1C
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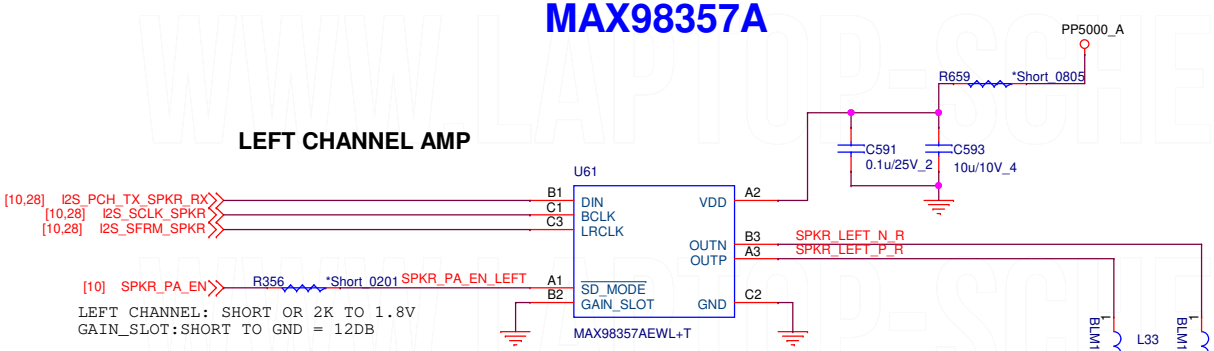
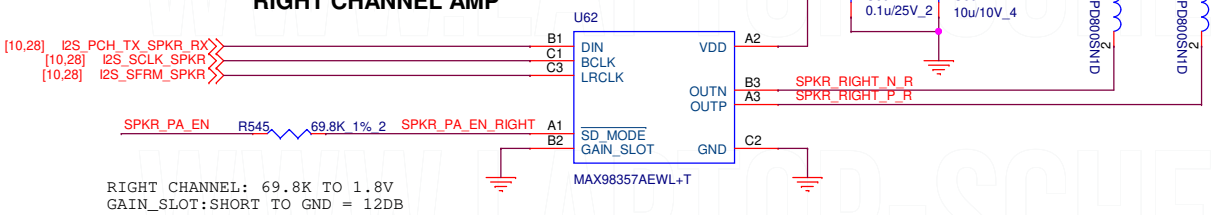
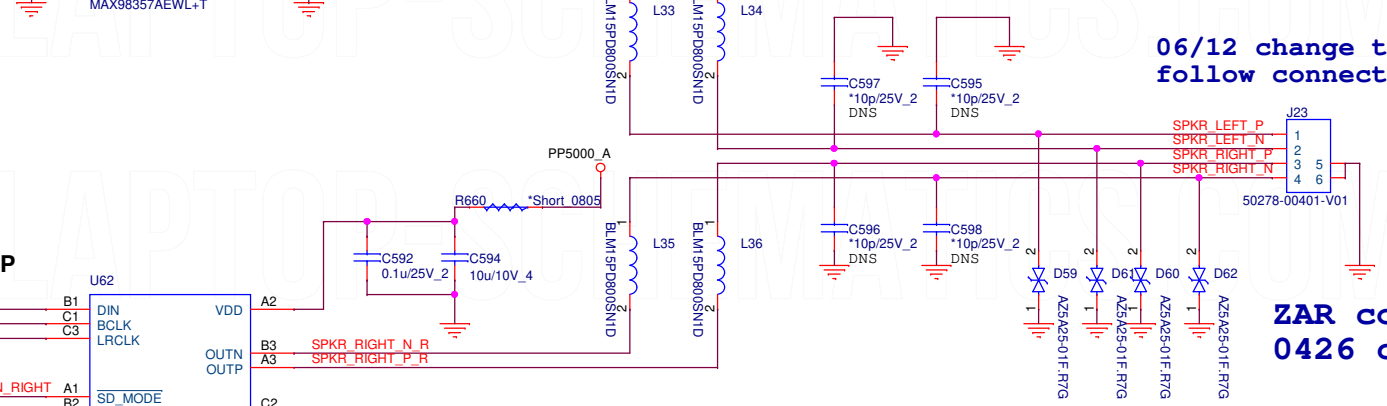
MAX98357A

LEFT CHANNEL AMP



RIGHT CHANNEL AMP





06/12 change to DFHD04MR445
follow connector list

ZAR connector
0426 change P/N

pin define follow ZAT

[24,36,37,39,40,41,44,45,46] PP5000_A

Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: AUDIO SPEAER AMPS	Rev: 1C
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VBAT ON EC RAIL TO REDUCE 60HZ
POWERED SPEAKER NOISE
OTHER POWER ON SOC RAILS TO PREVENT LEAKEGE

HEADPHONE AMP

LAYOUT NOTES

ROUTE HP_RING2 AND HP_RING2_SENSE DIFFERENTIALLY
ROUTE HP_SLEEVE AND HP_SLEEVE_SENSE DIFFERENTIALLY

pin define follow ZAT
0515 ZAR connector

VBAT 2.5~5V
DACREF 1.8V
DBVDD 1.8V
LDO1_IN 1.8B

edited symbol

FINE TUNE RESISTOR STUFFING FOR EMI

Quanta Computer Inc.	PROJECT : ZAR
Size	Document Number: AUDIO HEADPHONE AMP — Rev: 1C
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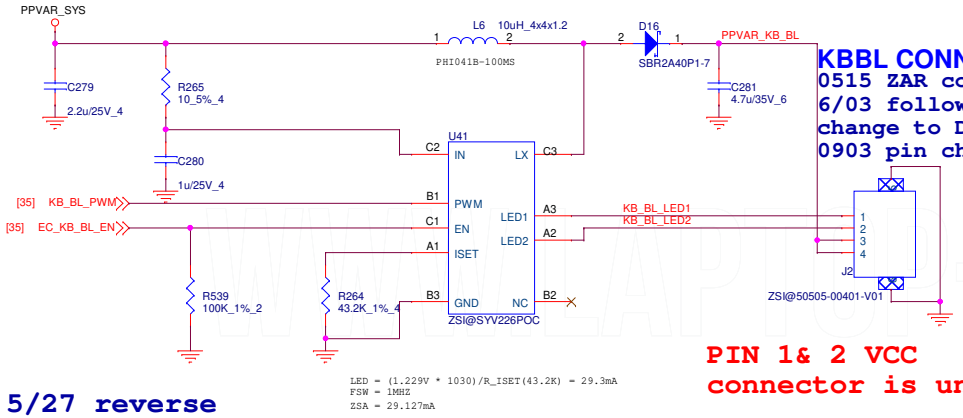
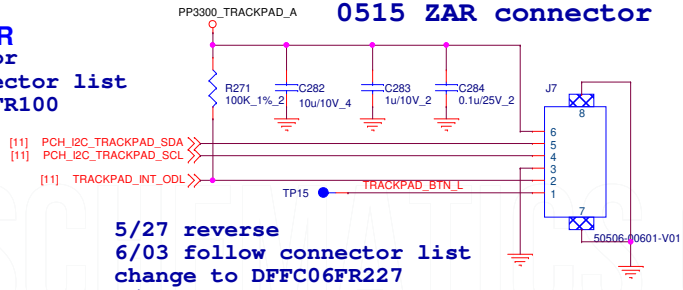


KBBL CONNECTOR
0515 ZAR connector
6/03 follow connector list
change to DFFC04FR100
0903 pin changed



TRACKPAD CONNECTOR
0515 ZAR connector

4.4 Pin Assignment

Pin Assignment and Description

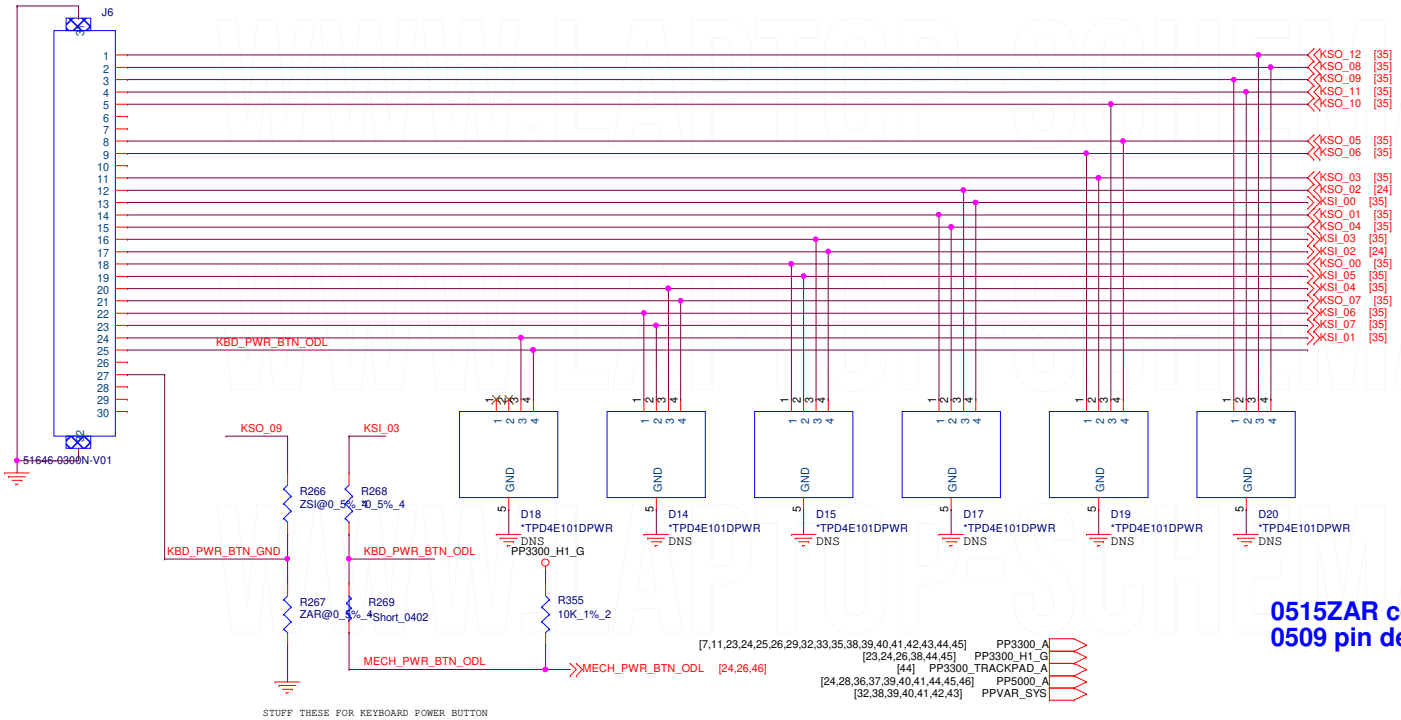
Pin#	Signal	I/O	Description
1	NC		Not connected
2	/INT	O	Slave interrupt, low active Indicates touchpad likes to send data to system (host) when low.
3	GND	GND	Ground
4	I²C_CLK	I/O	I²C clock I_{drive} or I_{sink}: 8 mA max.
5	I²C_DATA	I/O	I²C data. I_{drive} or I_{sink}: 8 mA max.
6	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.

5/27 reverse
6/03 follow connector list
change to DFFC06FR227
6/17 follow connector list
change to DFFC06FR050

pin define follow 0509 AVL ADLB577C009

PIN 1& 2 VCC
connector is under contact

5/27 reverse



KEYBOARD CONNECTOR

1030 follow connector list, change to DFFC30FR199
0603 follow connector list, change to DFFC30FR165
0515 ZAR connector
0509 pin define follow ZSA
0426 change P/N

0515ZAR connector
0509 pin define follow ZSA

	15"
1	KSO12
2	KSO8
3	KSO9
4	KSO11
5	KSO10
6	NC
7	NC
8	KSO5
9	KSO6
10	NC
11	KSO3
12	KSO2
13	KSI0
14	KSO1
15	KSO4
16	KSI3
17	KSI2
18	KSO0
19	KSI5
20	KSI4
21	KSO7
22	KSI6
23	KSI7
24	KSI1
25	POWER_DET
26	NC
27	GND
28	NC
29	NC
30	NC

12" AD1G_C80B

Mem-PIN	Define
1	KSO12
2	KSO8
3	KSO9
4	KSO11
5	KSO 0
6	N.C
7	N.C
8	KSO5
9	KSO6
10	N.C
11	KSO3
12	KSO2
13	KSI0
14	KSO1
15	KSO4
16	KSI3
17	KSI2
18	KSO0
19	KSI5
20	KSI4
21	KSO7
22	KSI6
23	KS I
24	KSI1
25	N.C
26	N.C
27	N.C
28	N.C
29	N.C
30	N.C

13" AL1G_C18BWL

Quanta Computer Inc.
PROJECT : ZAR

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	KB/TP/FAN	1C

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Quanta Computer Inc.

PROJECT : ZAR

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	FINGER PRINT SENSOR(none)	1C
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6 AXIS IMU (MLB)

U59
SDX SCX CSB OSDO OSCB INT2 VDD
SDO ASDx ASCx INT1 VDDIO GNDIO GND
[35,46] EC_I2C_SENSOR_SDA
[35,46] EC_I2C_SENSOR_SCL
PP3300_PP1800_SENSOR_A
TP33
IMU_INT_L2
BASE_SIXAXIS_INT_L [35]
PP3300_PP1800_SENSOR_A
C298 0.1u/25V_2
C299 1u/10V_2
ZSI@BMI160

8 BIT ADDRESS: 0XD0

STUFF FOR DMIC TUNING

[10,32] LID_CAM_DMIC_CLK
C691 *0.01u/16V_2 DNS

C691 intel suggest change to CLK

EDP SIGNALS

PPVAR_SYS
F1 1210L075/24PR/0.75A/24V_1210
C501 22u/25V_8
C7900 0.1u/16V_4
PP3300_TOUCHSCREEN_DX
R9310 *Short_0402

[8] EDP_AUX_N C301 0.1u/25V_2 EDP_AUX_C_N
[8] EDP_AUX_P C300 0.1u/25V_2 EDP_AUX_C_P
[8] EDP_TX0_N C297 0.1u/25V_2 EDP_TX0_C_N
[8] EDP_TX0_P C296 0.1u/25V_2 EDP_TX0_C_P
[8] EDP_TX1_N C294 0.1u/25V_2 EDP_TX1_C_N
[8] EDP_TX1_P C295 0.1u/25V_2 EDP_TX1_C_P
[8] EDP_TX2_N C292 0.1u/25V_2 EDP_TX2_C_N
[8] EDP_TX2_P C293 0.1u/25V_2 EDP_TX2_C_P
[8] EDP_TX3_N C290 0.1u/25V_2 EDP_TX3_C_N
[8] EDP_TX3_P C291 0.1u/25V_2 EDP_TX3_C_P

PP3300_A R9320 *0_5%_4
PP1800_A R9308 Short_0402
PP3300_PANEL_DX C7901 0.1u/16V_4
C7902 0.1u/16V_4
PP3300_CAM_A R9309 *Short_0402
MIC_PWR
CCD_PWR

PP3300_TOUCHSCREEN_DX
C1194 180P/50V_4
R5168 33_1%_2
[8] SOC_EDP_HPD
[35] EDP_BKLTEN_OD
EDP_BKLTEN_OD
[8] SOC_EDP_BKL_PWM

USI TOUCH PANEL

C344 4.7u/10V_4
C345 1u/10V_2
R9341 ZSI@10K_5%_4
[11] USI_INT
USI_RST_Q_ODL
R273 ZAR@1M_1%_2
[11] USI_REPORT_EN
PCH_I2C_USI_Q_SCL
PCH_I2C_USI_Q_SDA
USI INT ZAR: pull down 1M ohm
ZSI: pull high 10K ohm

CAM
W/DMIC

L7 DLP11SA900HL2L
[9] USB2_CAM_N USB2_CAM_CMC_N
[9] USB2_CAM_P USB2_CAM_CMC_P
[10] LID_CAM_DMIC_DATA R289 33_1%_2 LID_CAM_DMIC_DATA_R
[10,32] LID_CAM_DMIC_CLK

J11
51540-04001-V01

BACKLIGHT ENABLE CONTROL

PP3300_PANEL_DX
R286 10K_1%_2
D1 RB751S40
[8] SOC_EDP_BKLTEN
EDP_BKLTEN_OD

RESERVE GMR

0515 ZAR connector pin define follow ZSA

PP3300_TOUCHSCREEN_DX
R293 2.2K_1%_2
[11] PCH_I2C_USI_SDA
PCH_I2C_USI_Q_SDA
Q21
DMG1012T-7

PP3300_TOUCHSCREEN_DX
R294 2.2K_1%_2
[11] PCH_I2C_USI_SCL
PCH_I2C_USI_Q_SCL
Q22
DMG1012T-7

PP3300_TOUCHSCREEN_DX
R287 100K_1%_2
[11] USI_RST_L
USI_RST_Q_ODL
Q51
DMG1012T-7

[7,11,23,24,25,26,29,33,35,38,39,40,41,42,43,44,45] PP3300_A
[10,11,14,29,33,39,41,44,45,47] PP1800_A
[44] PP3300_CAM_A
[44,45] PP3300_PANEL_DX
[30,38,39,40,41,42,43] PPVAR_SYS

For panel T11 timing

PP3300_PANEL_DX
PPVAR_SYS
R9344 22_5%_8
R9342 1M_1%_2
Q55 2N7002K
R9343 1M_1%_2
[8,44] EN_PP3300_EDP_DX
Q501 DDTC144EUA-7-F

Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: LID, EDP, CAM, TOUCH, PEN	Rev: 1C
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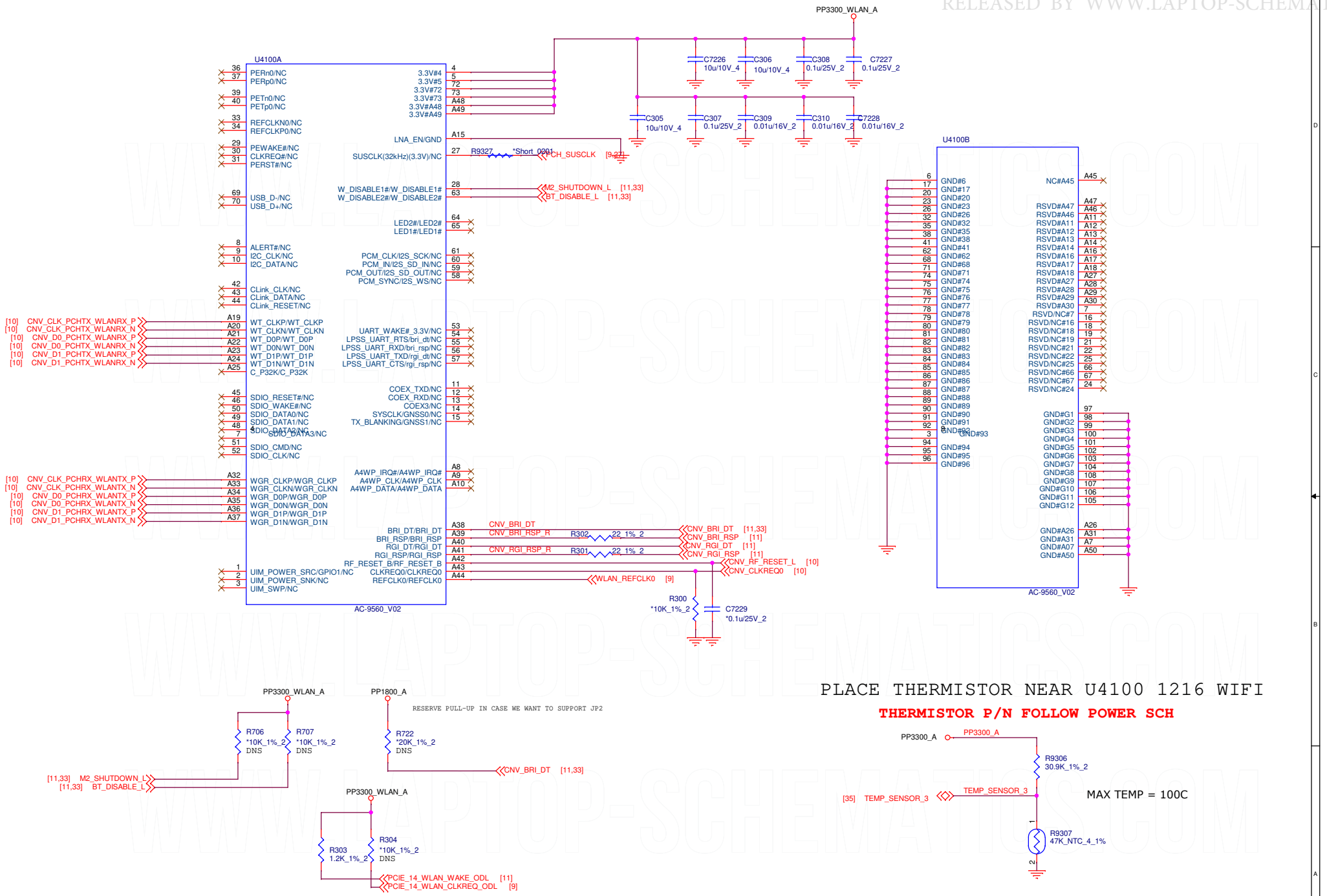

Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: WIFI	Rev: 1C
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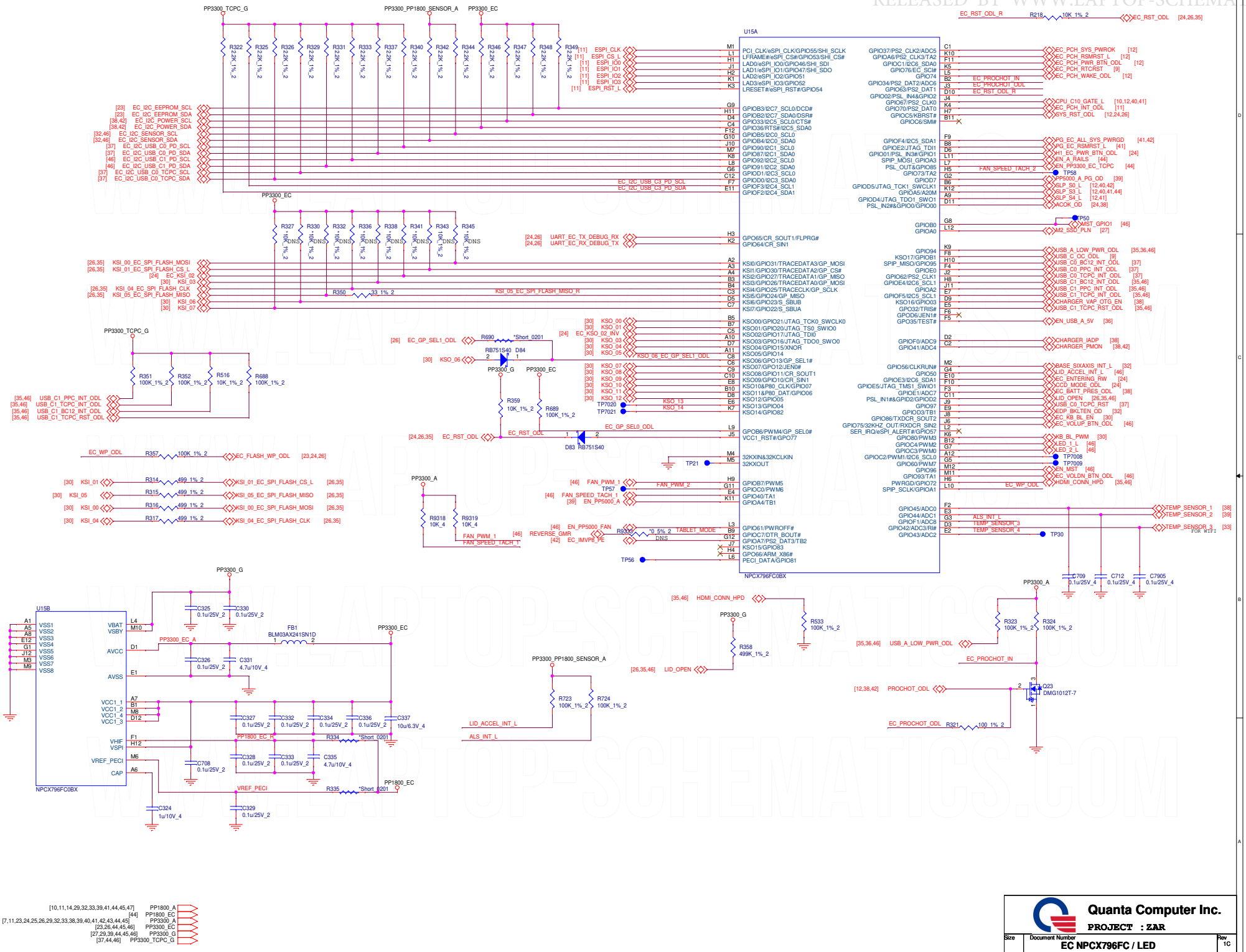
Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	LTE(none)	1C

Date: Thursday, January 02, 2020 Sheet 34 of 49



Quanta Computer Inc.			
PROJECT : ZAR			
Size	Document Number		Rev
	EC NPCX796FC / LED		1C
Date: Thursday, January 02, 2020	Sheet 35 of 49		

TYPE-A: PORT 0

PP5000_A

C338 22u/10V_6

R361 100K_1%_2

U16

VIN

DM_OUT

DP_OUT

CTL1

CTL2

CTL3

EN

ILIM_SEL

ILIM_L

ILIM_H

VOUT

DM_IN

DP_IN

STATUS

FAULT

EPAD GND

SLGC55545VTR

[9] USB2_A0_N

[9] USB2_A0_P

USB2_A0_U_N

USB2_A0_U_P

USB_A0_STATUS_L [46]

USB_A_OC_ODL [9]

[35] EN_USB_A_5V

USB_A0_ILIM_SEL

USB_A0_ILIM_LO

USB_A0_ILIM_HI

[35,46] USB_A_LOW_PWR_ODL

Q24 PJA138K

R362 48.7K_1%_2

R363 29.4K_1%_2

IF USING TPS2546, R362=51.1K, R363=30.9K
LO LIMIT: 912-1055 MA
HI LIMIT: 1516-1737MA

PP5000_USB_A0_VBUS

0527
follow connector list

C343 150u/6.3V_3528H1.9

[9] USB3_A0_RX_N

[9] USB3_A0_RX_P

L4 NFP0QHB542HS2D

USB3_A0_RX_N

USB3_A0_RX_P

USB3_A0_RX_L_N

USB3_A0_RX_L_P

L3 NFP0QHB542HS2D

USB2_A0_U_P

USB2_A0_U_N

USB2_A0_L_P

USB2_A0_L_N

[9] USB3_A0_TX_N

[9] USB3_A0_TX_P

C340 0.22u/10V_2

C339 0.22u/10V_2

L5 NFP0QHB542HS2D

USB3_A0_TX_C_N

USB3_A0_TX_C_P

USB3_A0_TX_L_N

USB3_A0_TX_L_P

CN1

Shield

StdA_SSRX-

GND

StdA_SSRX+

D+

GND_Drain

D-

StdA_SSTX-

VBUS

StdA_SSTX+

2UB4024-002111F

0827 modify SMT footprint

D28

Line-1

Line-2

GND#1

Line-3

Line-4

NC#4

NC#3

NC#2

NC#1

AZ1043-04F.R7G

USB3_A0_TX_L_P

USB3_A0_TX_L_N

USB3_A0_RX_L_P

USB3_A0_RX_L_N

D89 PESD5V0H1BSF

D90 PESD5V0H1BSF

USB2_A0_L_N

USB2_A0_L_P

MICRO SD CARD
*IF NOT ON MLB, USB TO SD INTERFACE MUST BE USED

PP3300_SD_DX

C341 4.7u/10V_4

C342 0.1u/25V_2

0527 follow connector list

J16 158-1000902625

SD_DAT3

GND

VSS

VDD

CLK

DAT0

DAT1

DAT2

CD

GND1

GND2

GND4

GND3

GND5

[10] SD_DATA3

[10] SD_CMD

[10] SD_CLK

[10] SD_DATA0

[10] SD_DATA1

[10] SD_DATA2

[10] SD_CD_ODL

R367 22_1%_2

R368 22_1%_2

R635 *Short_0201

R364 22_1%_2

R365 22_1%_2

R366 22_1%_2

R5237 *Short_0201

SD_DATA3_R

SD_CMD_R

SD_CLK_R

SD_DATA0_R

SD_DATA1_R

SD_DATA2_R

Reserve for NC or NO

D25 D26 D27 D22 D23 D24 D63 TPD1E6B06DPLR

[44] PP3300_SD_DX

[24,28,37,39,40,41,44,45,46] PP5000_A

Quanta Computer Inc.

PROJECT : ZAR

Size	Document Number	Rev
	USB A/SD CARD	1C
Date: Thursday, January 02, 2020	Sheet 36 of 49	

PORT 0:TCPPC

CSD87501L --> MOQ 3K
CSD87501LT --> MOQ 250
CSD87501L = CSD87501LT

06/20
EMI reserve

ADDRESS (HEX, 8 BIT): 0XBE

THERM PAD 1 MUST BE CONNECTED TO ISOLATED THERMAL PAD

ADDRESS (HEX, 8 BIT): 0X80

IF TCPC IS NOT ANALOGIX, MUST STUFF
PULL-UP/PULL-DOWN RESISTORS ON
DDI1_AUX_P AND DDI_AUX_N

AVDD33 SHOULD TURN ON FIRST
DVDD_IO SHOULD TURN ON WITHIN 2MS OF AVDD33

PORT 0:TCPC

DEFAULT I2C ADDRESSES (HEX, 8-BIT)

TCPC: 0X58
SPI: 0X7E
EMTB: 0X7A
EMRB: 0X84
DEBUG1: 0X72
DEBUG2: 0X70

ESD DIODES TO PROTECT H1

DFHS24FR477
8/27 EVT changed

[35,44,46] PP3300_TCPC_G
[24,28,36,39,40,41,44,45,46] PP5000_A
[38,46] PPVAR_VBUS_IN

Quanta Computer Inc.
PROJECT : ZAR

Size	Document Number	Rev
	USB C0	1C

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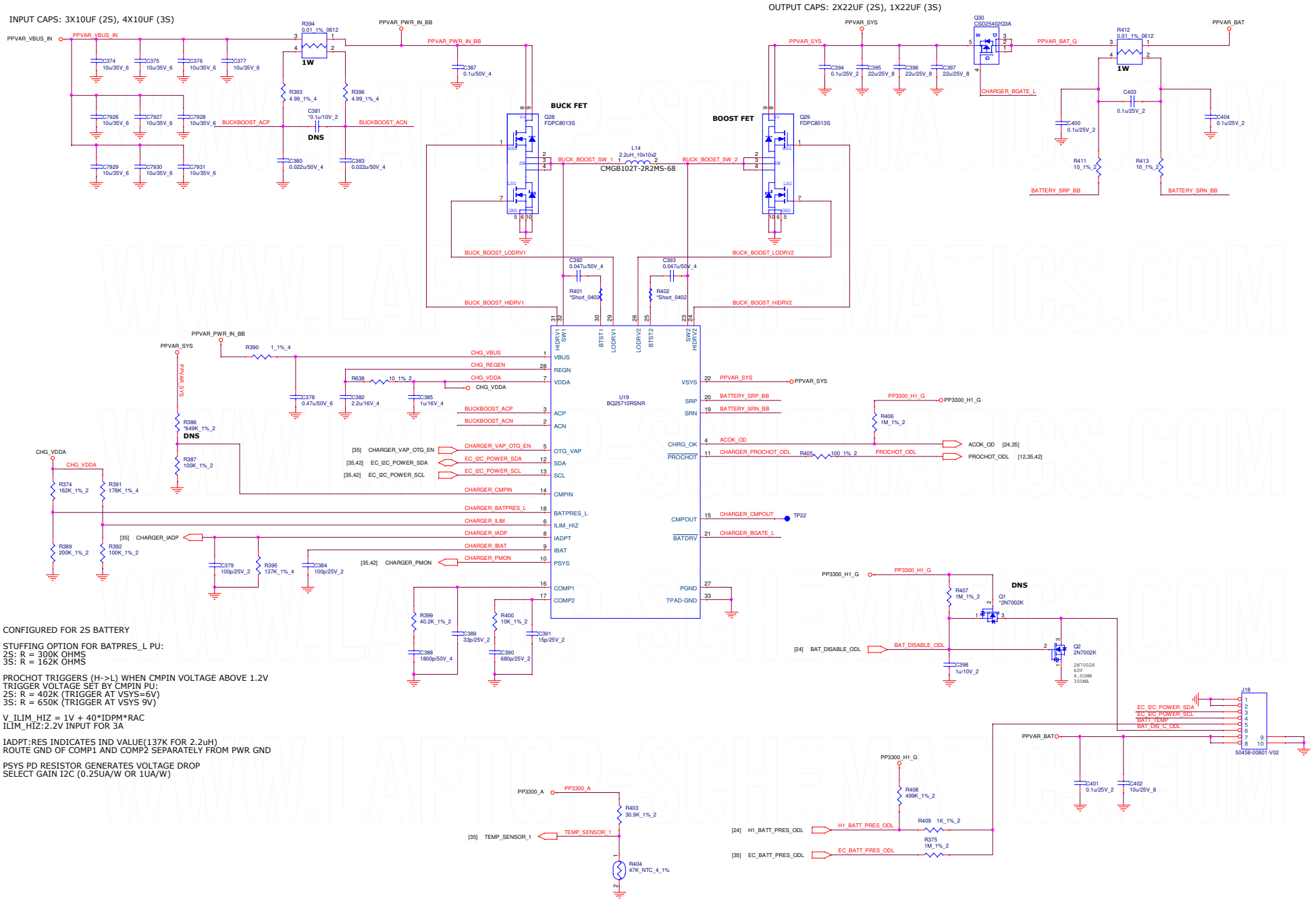

CONFIGURED FOR 2S BATTERY

STUFFING OPTION FOR BATPRES_L PU:
2S: R = 300K OHMS
3S: R = 162K OHMS

PROCHOT TRIGGERS (H->L) WHEN CMPIN VOLTAGE ABOVE 1.2V
TRIGGER VOLTAGE SET BY CMPIN PU:
2S: R = 402K (TRIGGER AT VSYS=6V)
3S: R = 650K (TRIGGER AT VSYS 9V)

V_ILIM_HIZ = 1V + 40*IDPM*RAC
ILIM_HIZ:2.2V INPUT FOR 3A

IADPT:RES INDICATES IND VALUE(137K FOR 2.2uH)
ROUTE GND OF COMP1 AND COMP2 SEPARATELY FROM PWR GND

PSYS PD RESISTOR GENERATES VOLTAGE DROP
SELECT GAIN I2C (0.25UA/W OR 1UA/W)

MAX TEMP = 100C
PLACE THERMISTOR NEAR CHARGING INDUCTOR

Quanta Computer Inc.	
PROJECT :	
Size	Document Number: POWER: BATTERY CHARGER — Rev: 1C
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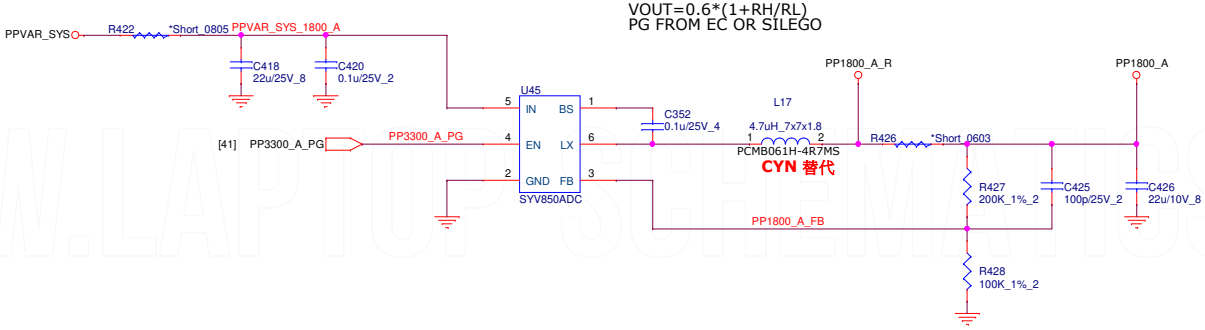
PP1800_A

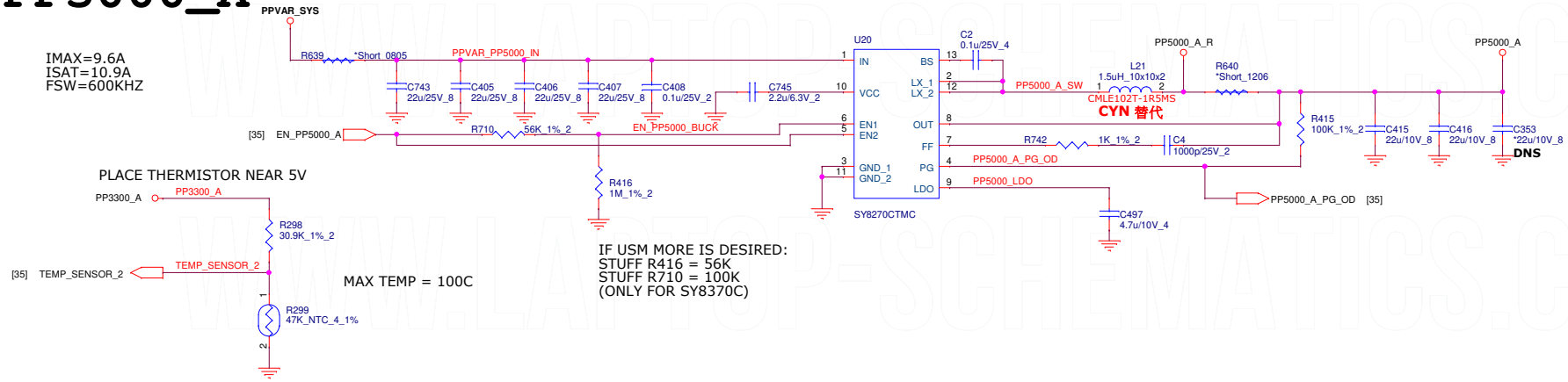
IMAX = 0.2A
ISAT = 0.2A
FSW = 500KHZ

VOUT=0.6*(1+RH/RL)
PG FROM EC OR SILEGO



PP5000_A

IMAX=9.6A
ISAT=10.9A
FSW=600KHZ



PLACE THERMISTOR NEAR 5V

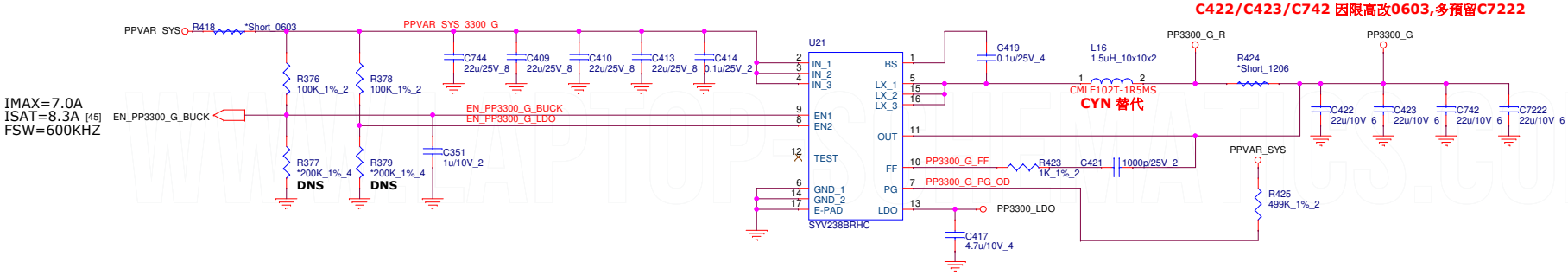
MAX TEMP = 100C

IF USM MORE IS DESIRED:
STUFF R416 = 56K
STUFF R710 = 100K
(ONLY FOR SY8370C)

PP3300_G

C422/C423/C742 因限高改0603,多預留C7222

IMAX=7.0A
ISAT=8.3A [45]
FSW=600KHZ



Quanta Computer Inc.		
PROJECT :		
Size	Document Number	Rev
	POWER: 5V, 3.3V, 1.8V	1C
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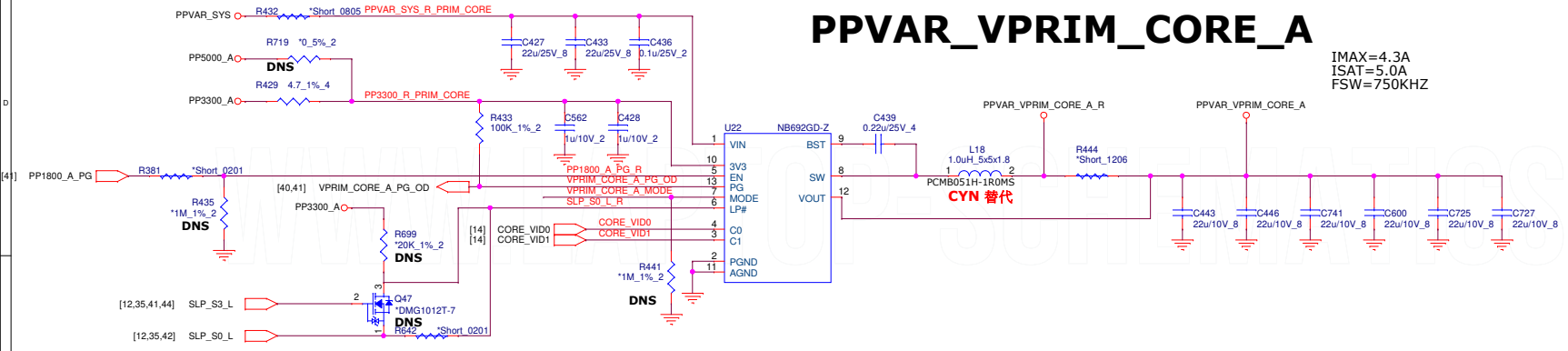
SETTINGS 40

PPVAR_VPRIM_CORE_A

IMAX=4.3A
ISAT=5.0A
FSW=750KHZ



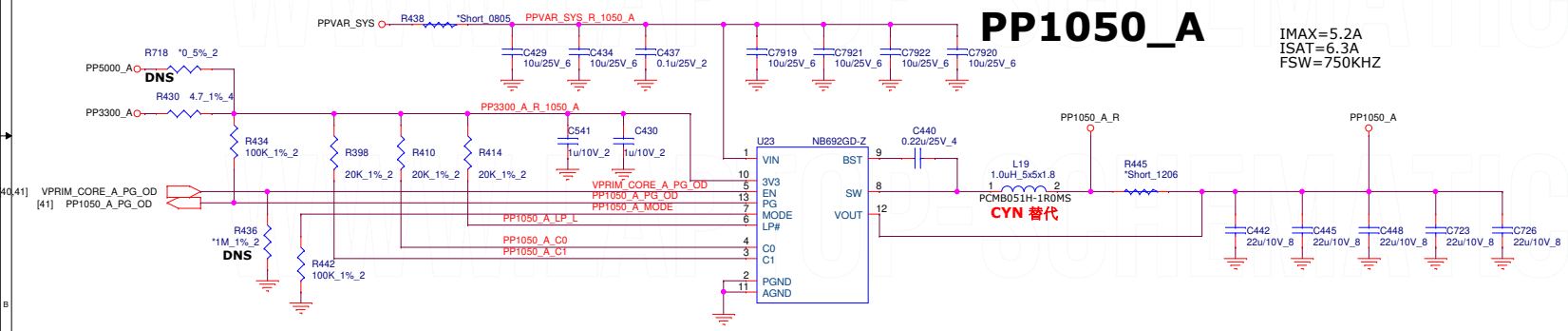
	VOUT	LP_L	C0	C1
PPVAR_VPRIM_CORE_A	0.75	0	x	x
	0.9	1	0	0
	0.95	1	0	1
	1.00	1	1	1
	1.05	1	1	1
PP1050_A	1.05	1	1	1
PP950_VCCIO	0.95	1	0	1

*LP_L, C0, C1 PULLED HIGH INTERNALLY

RAIL	MODE PIN PD RES
PPVAR_VPRIM_CORE_A	FLOAT OR >230K
VCCOPC/V1.0A/EOPIO	100K
VCCIO	0

PP1050_A

IMAX=5.2A
ISAT=6.3A
FSW=750KHZ

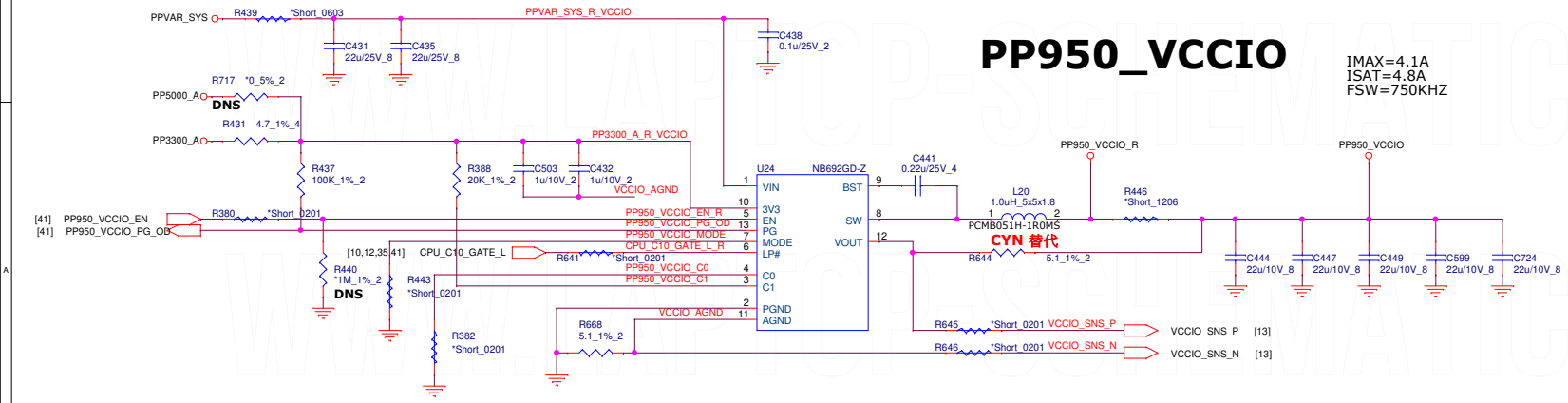


OPERATING MODE	EN PIN VOLTAGE [V]
ULTRASONIC (USM)	1.3 - 1.7
NORMAL	> 2.3

*EN PIN HAS 800K INTERNAL PU

PP950_VCCIO

IMAX=4.1A
ISAT=4.8A
FSW=750KHZ



Quanta Computer Inc.
PROJECT :

Size	Document Number	Rev
	VCCPRIM_CORE, 1.05, VCCIO	1C

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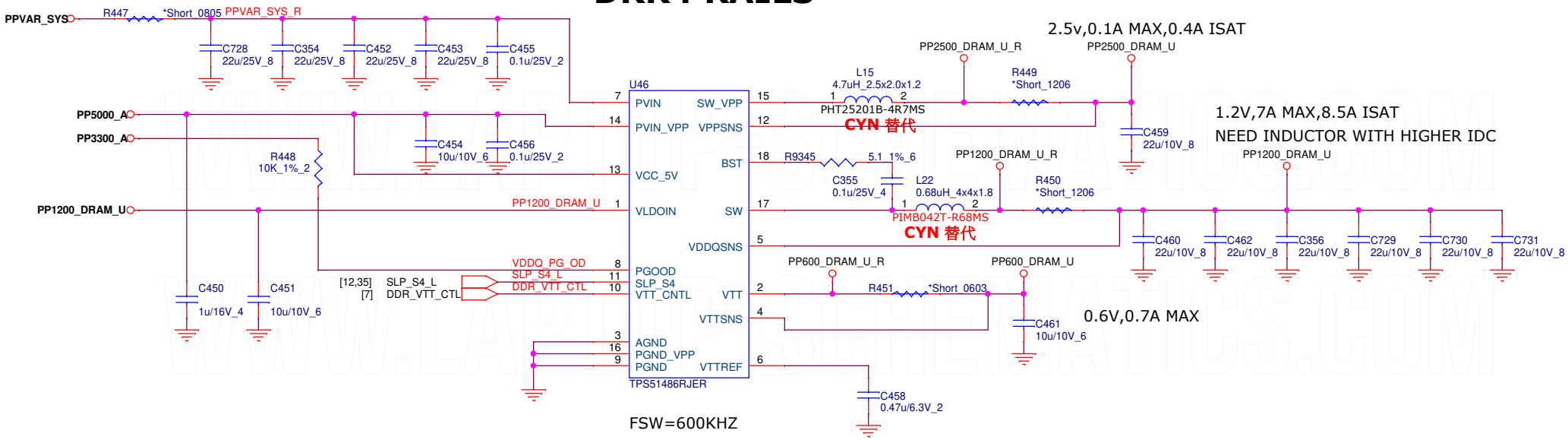
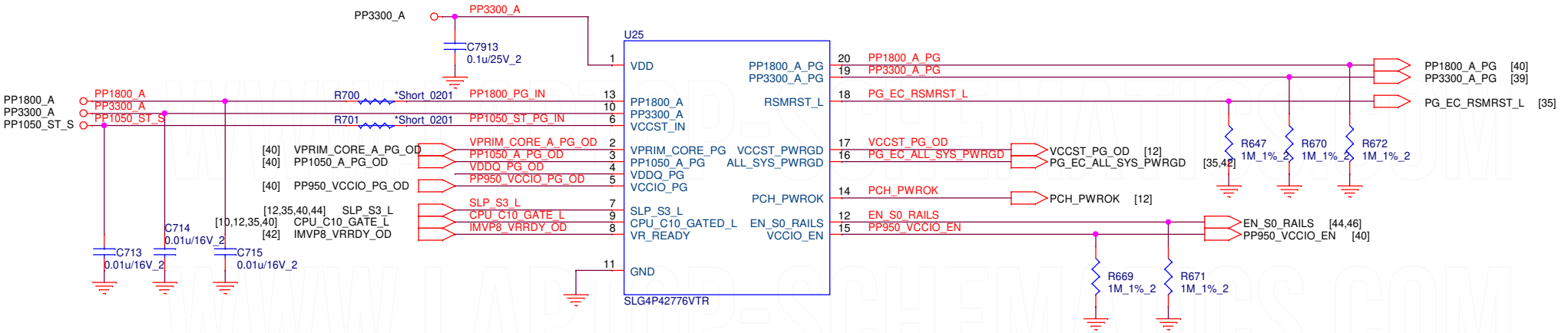
DRR4 RAILS



POWER GOOD GENERATION



Quanta Computer Inc.		
PROJECT :		
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	POWER: VDDQ, PG CHIP	1C
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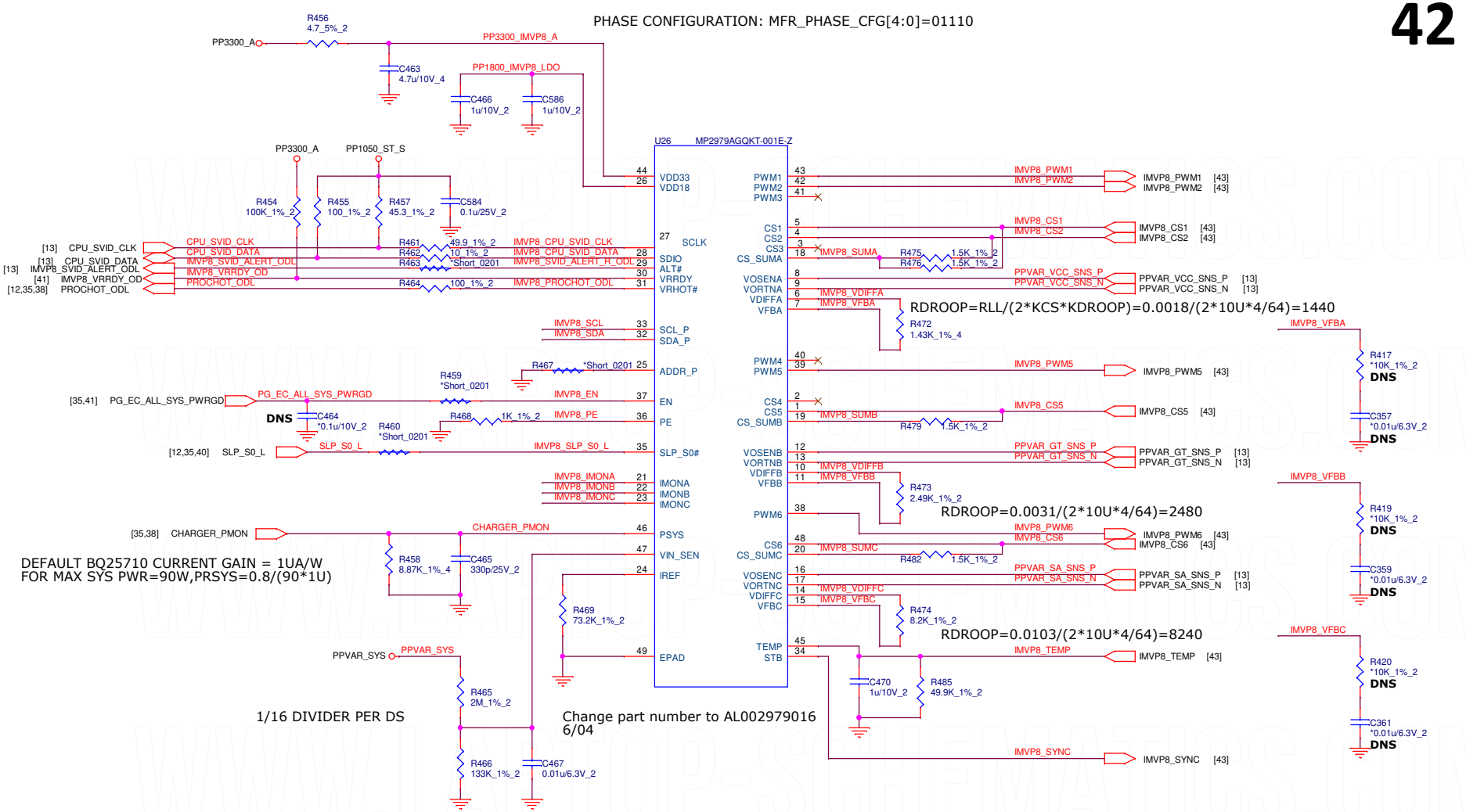
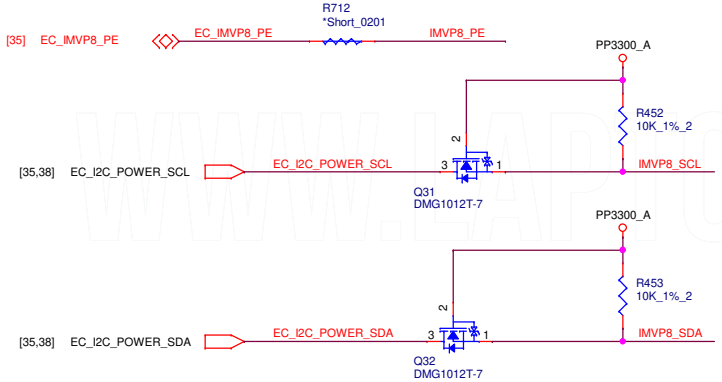
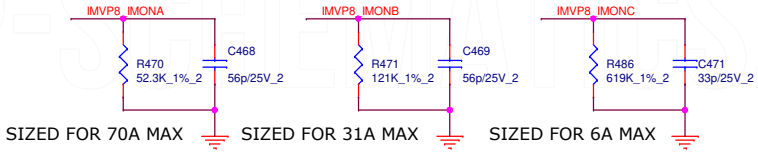
PHASE CONFIGURATION: MFR_PHASE_CFG[4:0]=01110





RIMON=32*VIMON_MAX/(ICCMAX*KCS), WHERE VIMON_MAX=1.1636, KCS=10U



Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	POWER: IMVP8	1C
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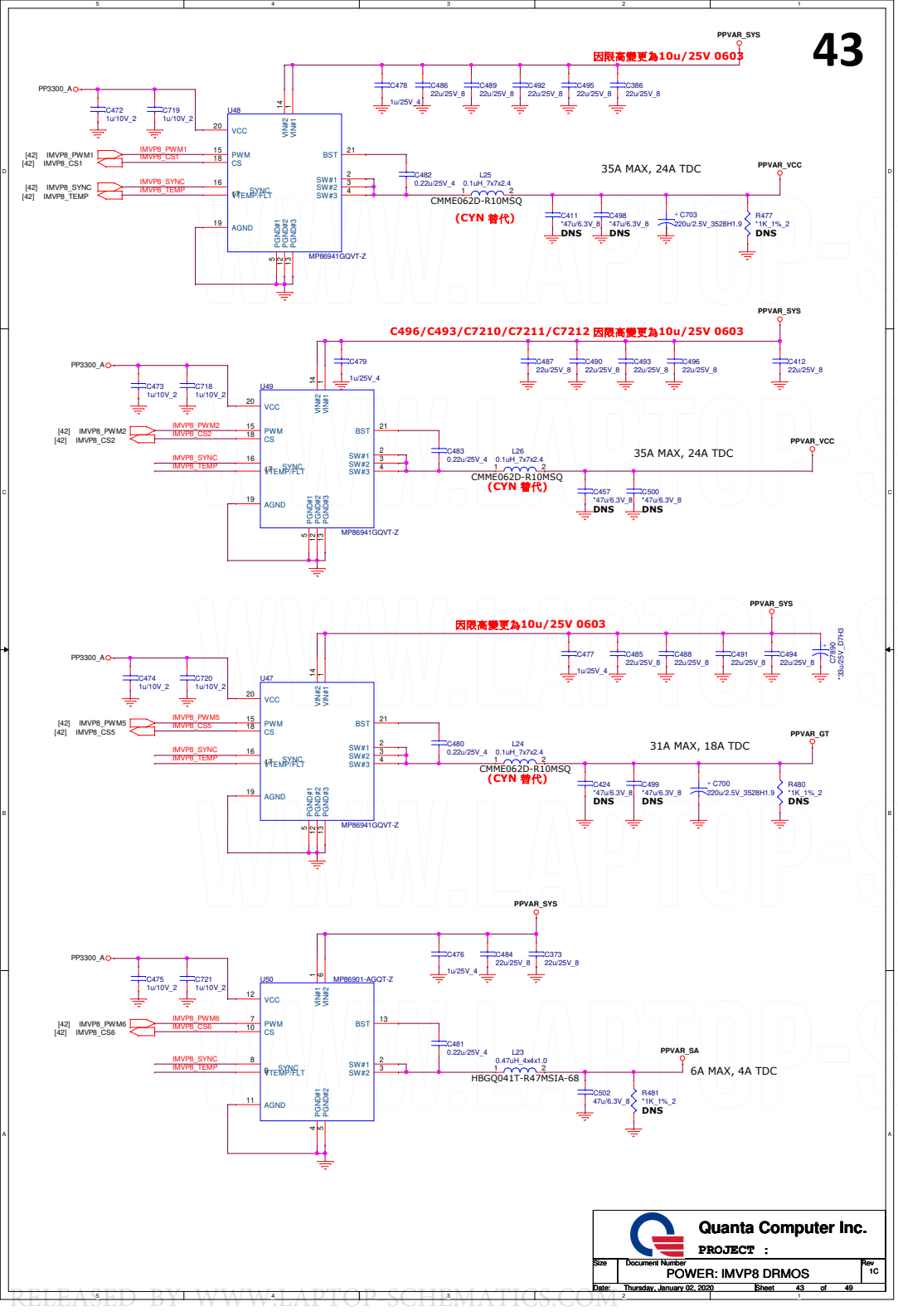

Quanta Computer Inc.

PROJECT :

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	POWER: IMVP8 DRMOS	1C

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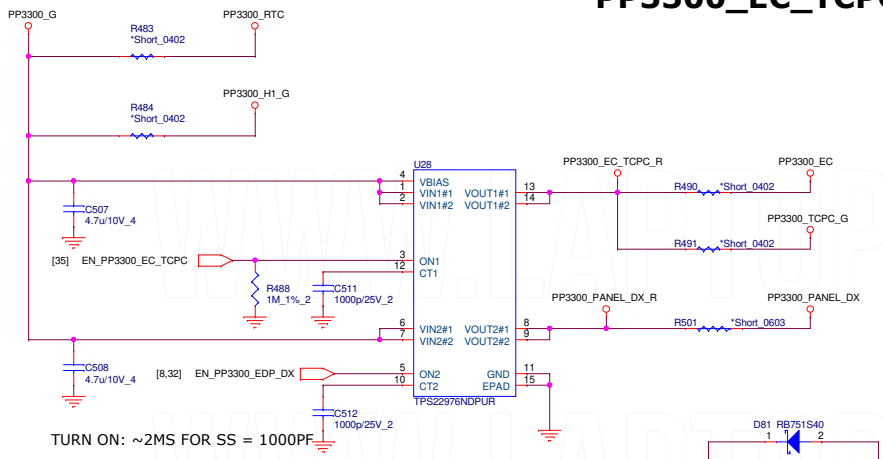
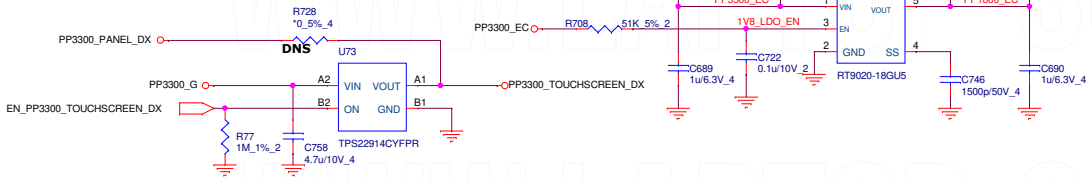
PP3300_EC_TCPC

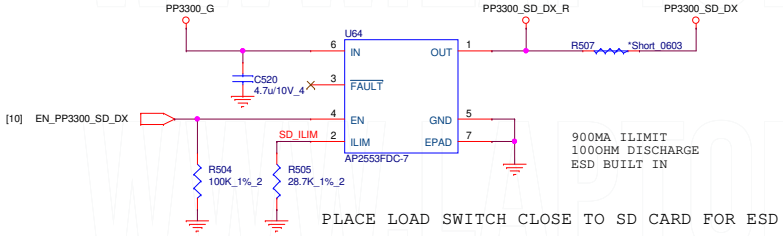


TURN ON: ~2MS FOR SS = 1000PF

FIXED 1.8V LDO



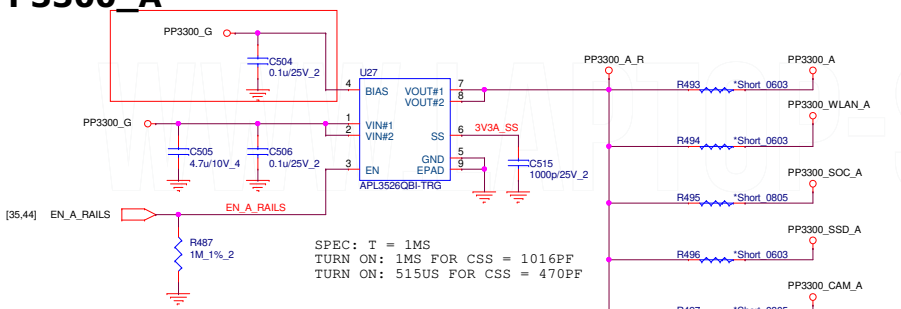
PP3300_SD_DX



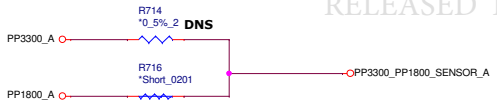
900MA ILIMIT
100OHM DISCHARGE
ESD BUILT IN

PLACE LOAD SWITCH CLOSE TO SD CARD FOR ESD

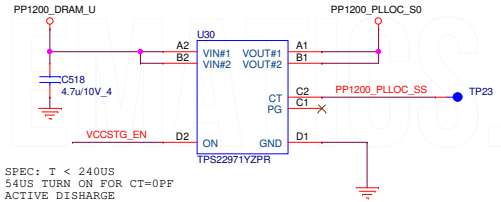
PP3300_A



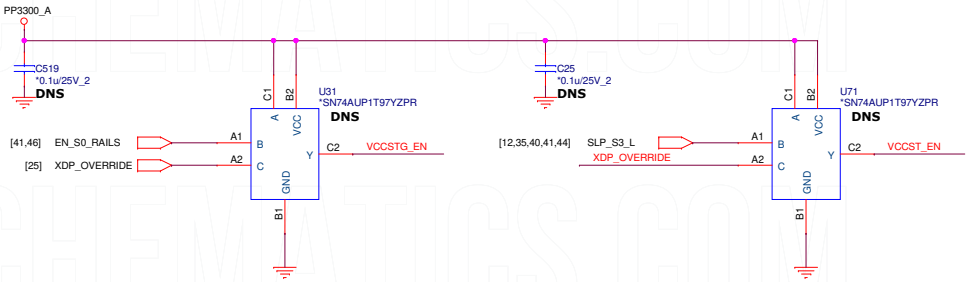
SPEC: T = 1MS
TURN ON: 1MS FOR CSS = 1016PF
TURN ON: 515US FOR CSS = 470PF



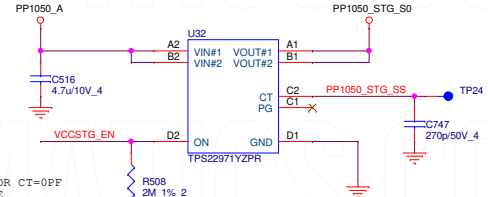
PP1200



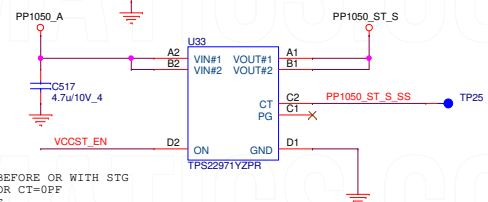
SPEC: T < 240US
54US TURN ON FOR CT=0PF
ACTIVE DISHARGE



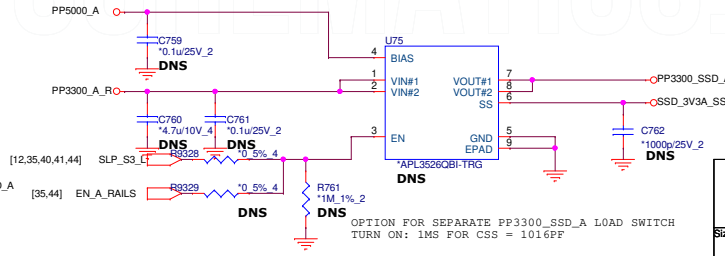
PP1050



SPEC: T < 65US
54US TURN ON FOR CT=0PF
ACTIVE DISHARGE



SPEC: COME UP BEFORE OR WITH STG
54US TURN ON FOR CT=0PF
ACTIVE DISHARGE



OPTION FOR SEPARATE PP3300_SSD_A LOAD SWITCH
TURN ON: 1MS FOR CSS = 1016PF

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	POWER: LOAD SWITCH	1C
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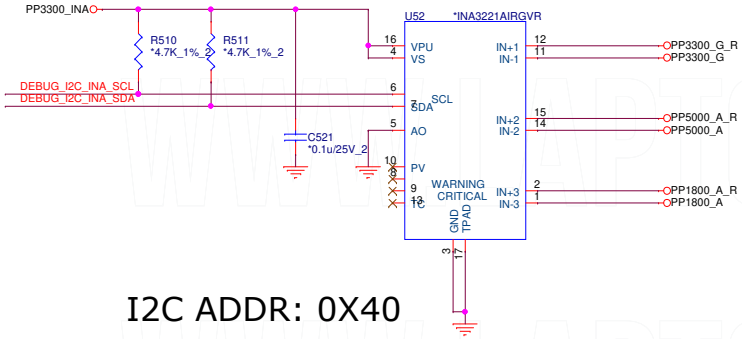
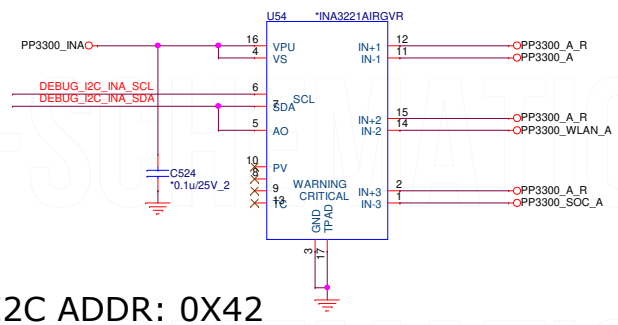
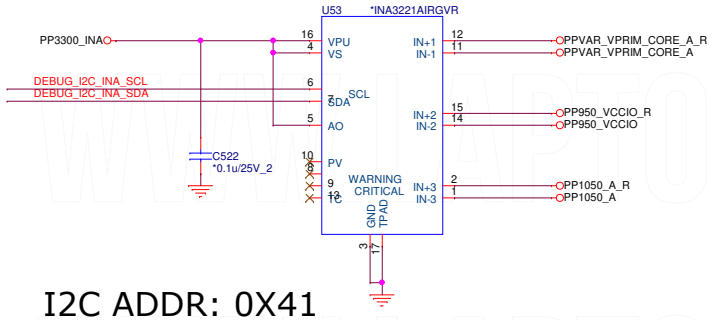
[24,26] DEBUG_I2C_INA_SCL
[24,26] DEBUG_I2C_INA_SDA



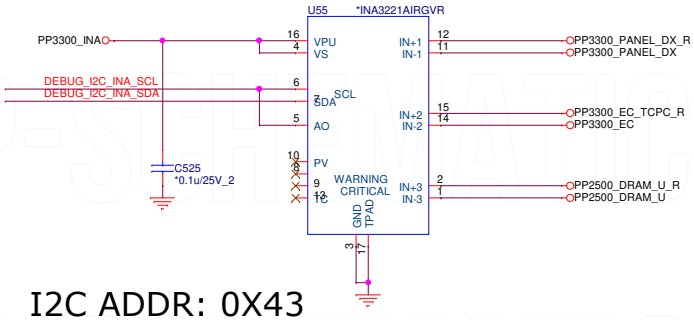
I2C ADDR: 0X40



I2C ADDR: 0X42



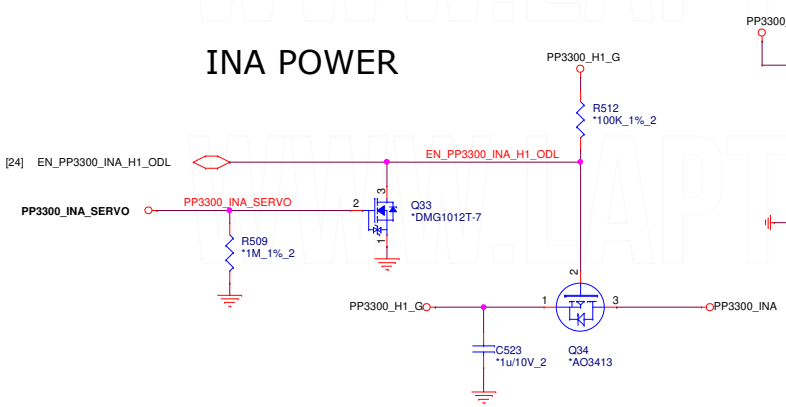
I2C ADDR: 0X41

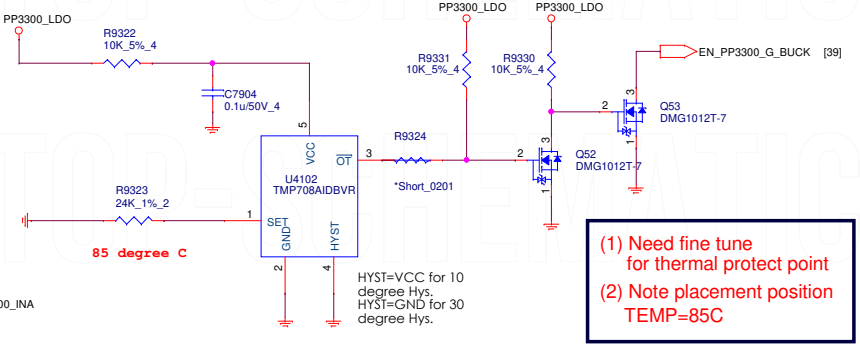


I2C ADDR: 0X43

Thermal protection

INA POWER





(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=85C

Quanta Computer Inc.		
PROJECT :		
Size	Document Number: INAS / Thermal	Rev 1C
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PP5000_A
R354 100K_1%_2
[36] USB_A0_STATUS_L
R339 0_5%_2
[35,36] USB_A_LOW_PWR_ODL
Q25 PJA138K

PEN_GARAGE_DET_L
TP7022

5/27 reverse

[8] DDI2_TX0_P
[8] DDI2_TX0_N
[8] DDI2_TX1_P
[8] DDI2_TX1_N
[8] DDI2_TX2_P
[8] DDI2_TX2_N
[8] DDI2_TX3_P
[8] DDI2_TX3_N
[9] USB3_C1_TX_P
[9] USB3_C1_TX_N
[9] USB3_C1_RX_P
[9] USB3_C1_RX_N
[9] USB2_C1_P
[9] USB2_C1_N
[8] DDI2_AUX_P
[8] DDI2_AUX_N
PP5000_A
PPVAR_VBUS_IN
Main:DFFC45FR053
2nd: DFFC45FR057
FH34SRJ-45S-0.5SH
J9

5/27 reverse

FH34SRJ-40S-0.5SH50
CN2
PP3300_PP1800_SENSOR_A
PP3300_EC
[35] LID_ACCEL_INT_L
[32,35] EC_I2C_SENSOR_SDA
[32,35] EC_I2C_SENSOR_SCL
[35] EN_PP5000_FAN
[35] FAN_PWM_1
[35] FAN_SPEED_TACH_1
[8] DDI2_HPD_ODL
[35] LED_1_L
[35] LED_2_L
MECH_PWR_BTN_ODL
[24,26,30] MECH_PWR_BTN_ODL
[35] HDMI_CONN_HPD
[35] EN_MST
[35] MST_GPIO1
[35] EC_VOLUP_BTN_ODL
[35] EC_VOLDN_BTN_ODL
[26,35] LID_OPEN
REVERSE_GMR
[35] REVERSE_GMR
[35] EC_I2C_USB_C1_PD_SCL
[35] EC_I2C_USB_C1_PD_SDA
[35] USB_C1_TCPC_INT_ODL
[35] USB_C1_PPC_INT_ODL
[35] USB_C1_BC12_INT_ODL
[35] USB_C1_TCPC_RST_ODL
[10,11] PEN_GARAGE_DET_L
[11] PCH_I2C_SAR0_MST_SCL
[11] PCH_I2C_SAR0_MST_SDA
[41,44] EN_S0_RAILS
[11,44] EN_PP3300_TOUCHSCREEN_DX
R9332 0_5%_2
PP3300_G
PP3300_TCPC_G

ZAR connector
0426 change P/N

[27,29,35,39,44,45] PP3300_G
[35,37,44] PP3300_TCPC_G
[24,28,36,37,39,40,41,44,45] PP5000_A
[37,38] PPVAR_VBUS_IN

ZAR connector
0426 P/N check OK

For unuse Board ID

TP7024
Board_ID
R7500 1K_1%_2

[CLIP]

CLIP1 CLIP2 CLIP3 CLIP4
CLIP5 CLIP6 CLIP7 CLIP8
CLIP9 CLIP10 CLIP11 CLIP12
CLIP13 CLIP14 CLIP15 CLIP16
EMI@CLIP-39X35-100X18-3P

HOLE1 *H-C362D217P2
HOLE2 *H-ZARAX-9
HOLE3 *H-C362D217P2
HOLE4 *H-C295D98P2
HOLE5 *H-O193X126D169X102P2
HOLE6 *H-TBC362IC217D217P2
HOLE7 ZAR@H-TC236IC142BC165D142P2
HOLE9 *H-ZARAX-1
HOLE10 *H-C134D102P2

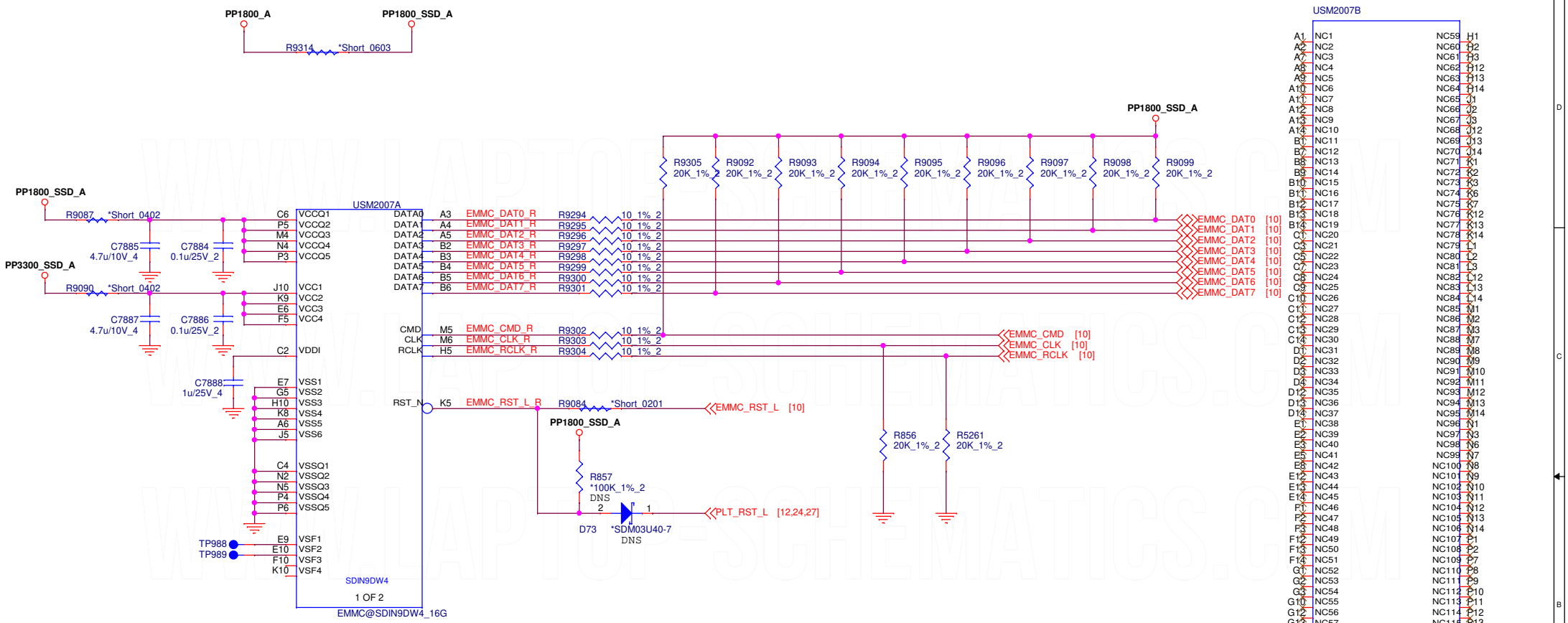
SPAD3
*SPAD-ZARAX-1
HOLE20 *SPAD-C276

Check

PPVAR_VCC PAD14 *SPAD-RE326X47
PPVAR_VCC PAD15 *SPAD-RE293X42
PPVAR_VCC PAD16 *SPAD-RE204X46

2Dbarcode1 *2D-BARCODE-8X8-S
2Dbarcode *2D-BARCODE-6X6-S
HOLE21 *H-R157X157D157X157N
HOLE16 *H-O185X166D165X146P2
HOLE17 *H-O185X166D165X146P2
HOLE18 *H-C166D146P2
HOLE19 *H-C166D146P2

Quanta Computer Inc.
PROJECT : ZAR
Size | Document Number: BTN / SUB BOARD CONNECTOR | Rev: 1C
Date: Thursday, January 02, 2020 | Sheet 46 of 49



Quanta Computer Inc.		
PROJECT : ZAR		
Size	Document Number: eMMC	Rev: 1C
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Model	Version	CHANGE LIST
	1A	1. First release
	1B	1. page 22: Delete C599,C600 on DDR CLK lines, these are being removed from CML PDG 2. page 35: Move PD resistors on HDMI_CONN_HPD R533 to MLB EC page 3. page 33: Add 10k PU R706,R707 to PP3300_WLAN_A on M2_SHUTDOWN_L and also BT_DISABLE_L 4. page 11: Change PU on R499 to 1.8V 5. page 10: Move MEM_CH_SEL to GPP_F2 6. page 9: Move WiFi M.2 USB from SoC port 5 to port 10 7. page 41: U25, Use Silego part with new firmware with adjusted tolerances (BOM change) 8. page 35: USB_C0_TCPC_RST_ODL to USB_C0_TCPC_RST and remove R687 9. page 35: Remove TCPC_USB_C1_HPD from EC 10. page 35: Move EC_VOLDN_BTN_ODL to GPIO93 on EC 11. page 35: swap FAN_SPEED_TACH_2 on GPIOA4 with EN_PP5000_A on GPIO73 12. page 30,35: Moved DS1, DS2, R629, R630, R631, R632, D21 (power LED) from EC page to Base page 13. page 44: VIN of U63 change to PP3300_G. Add a 10K/0.1uF RC delay (R708, C722) to the enable of U63 and have it enabled by PP3300_EC 14. page 39: Changed PU on R415 to PP5000_A 15. page 10: Add a 100K PU R709 on GPP_F23 to 1.8V 16. page 24: Q44,Q43 bodydiode pointed to the wrong way should be towards USB_C0_SBU1_U and USB_C0_SBU2_U 17. page 39: U21+Others, Replace PU2 (SYV886) with NB690 to allow for higher current output. 18. page 40: U22, Add 4 22uF output caps (6 output caps total) 19. page 40: U23, Add 2 22uF output caps (5 output caps total) 20. page 40: U24, Add 3 22uF output caps (5 output caps total) 21. page 41: U46, Add 3 22uF output caps (6 output caps total) and Add another 22uF input cap (4 input caps total). Change inductor to 0.68uH instead of 1uH. Need Isat > 8.5A and Idc>7A 22. page 45: Q33 set to STUFF 23. page 42: Change R468 to 1K ohms. Add a 0 ohm resistor between the PE signal (Pin 36) and GPIOA7 of the EC. Name the net EC_IMVP8_PE on the EC side and IMVP8_PE on the MPS side 24. page 11: Remove R60, R63 25. page 32: Remove Q19, Q20, R291, R292. Remove PCH_I2C_PEN_SDA/SCL_Q nets from J25 connector 26. page 37: DNS resistors R637, R636 27. page 11,32: PCH_I2C_TOUCHSCREEN_SDA/SCL change to PCH_I2C_USI_SDA/SCL. Change on both sides of FETs. 28. page 11,32: TOUCHSCREEN_RST_L rename as USI_RSL_L. Change on both sides of FET 29. page 11,32: TOUCHSCREEN_INT_L rename as USI_INT_H. Remove PU and add 1M pull-down 30. page 11,32: TOUCHSCREEN_DIS_L rename as USI_REPORT_EN 31. page 39: Ignore line items 36-40. Replace U20 with SY8270C. There should be 4x22uF input caps and 2x22uF output caps. Inductor should be 1.5uH with Idc > 9.6A and Isat > 10.9A. Add a voltage divider to the EN signal. Divider is just a place holder for now. When SY8370C is used R1 = 100K, R2 = 56K (refer to google schematic) 32. page 39: Replace U21 with SYV238B. There should be 4x22uF input caps and 3x22uF output caps. The inductor should be 1.5uH with Idc > 7A and Isat > 8.3A 33. page 44: Replace U63 with RT9020 34. page 44: Add 270pF C747 cap to GND 35. page 17: Reduce to C94 22uF instead of 47uF 36. page 27: Add control circuit for PLT_RST_L with EC_PCH_RSMRST_L control. Follow Google's schematic 37. page 2(on USB DB): Add schottky diode D79 clamps the AUX line to the 3.3V rail to limit overshoot problems: DP_MST_AUX_C_N to PP3300_TCPC 38. page 35: Reduce C335 from 10uF to 4.7UF 39. page 37: Add schottky diode D80 clamps the AUX line to the 3.3V rail to limit overshoot problems:DDI1_AUX_N_C to PP3300_TCPC 40. page 37, 2(on USB DB): Add a 0 ohm resistor between PP5000_A from VCONN Power and DNS it on both U60 and U65 41. page 44: R708 should be ~51K. C746 should be at least 1500pF. Input to LDO should be PP3300_EC 42. page 42: Change R469 to 73.2kOhm 43. page 14: Added C734 - a 1uF cap to be placed near BV2. Added C733 - a 1uFcap to be placed near BV12 44. page 27,35: Added M2_SSD_PLN net to pin 8 of the SSD connector and connected this to GPIOA0 on the EC 45. page 11,34: Changed the name WWAN_RADIO_DISABLE_1V8_ODL to WWAN_RADIO_DISABLE_1V8. Change the name WWAN_RADIO_DISABLE_1V8_Q_ODL to WWAN_RADIO_DISABLE_1V8_ODL. Replaced fet Q52 with diode D82 46. page 12: Add a test point to XDP_BPM<0> 47. page 33: Add a DNS PU R722 to 1.8V on CNV_BRI_DT 48. page 32: Added ALS_INT_L on page 32 49. page 44: Created PP3300_PP1800_SENSOR_A (default to PP1800_A) so that we can switch the sensor power rail to 3.3V if desired 50. page 32, 35, 1(on G sensor DB): Changed PP1800_A to PP3300_PP1800_SENSOR_A EC_I2C_SENSOR_1V8_SCL to EC_I2C_SENSOR_SCL EC_I2C_SENSOR_1V8_SDA to EC_I2C_SENSOR_SDA 51. page 35: Added R723, R724 100K pullups to PP3300_PP1800_SENSOR_A on LID_ACCEL_INT_L and ALS_INT_L 52. page 39: Changed inductor L16 and L21 to CMME102T-1R5MS
	rev 2_1	1. page 11,35: Add a PU R725 to EC_PCH_INT_L and change name to _ODL 2. page 32: On all the touchscreen and pen devices, pull them up(PP3300_PANEL_DXPCH_I2C_USI_SDA/SCL, USI_RST_L) to PP3300_TOUCHSCREEN_DX instead 3. page 11,32: Rename USI_INT_H to USI_INT 4. page 11, 34: Rename WWAN_RADIO_DISABLE_1V8 to WWAN_RADIO_DISABLE_1V8_L 5. page 11: Rename EMR_GARAGE_DET to PEN_GARAGE_DET_L on BY30 6. page 11: Change BV30 from unused PEN_RESET_L to FPMCU_BOOT1 7. page 16: Remove TP38, TP44-TP49 8. page 26: Add 100K R726 PD to Pins 26 on servo(J3) 9. page 31: Remove SLP_S4_L and SLP_SUS_L going to FP connector 10. page 23: Change the SPI ROM to a 16MB part 11. page 35: Pull up R359 to PP3300_G, Connect EC_RST_ODL to PSL4 , Move SYS_RST_ODL to pin GPIOC5/KBRST_L 12. page 35: Add a diode D83 with annode connected to GPIO77 and cathode connected to EC_RST_ODL before R359 13. page 23: Move R198 closer to the SPI ROM and DNS it with a note that the resistor should be close to the SPI ROM to reduce the stub 14. page 26: Remove U40 and related components, ADD R744~R751 15. page 4(on USB DB): Move D79 to be in parallel with R506 16. page 31: Add straps, PUs, and PDs to MCU signals 17. page 31: Option for PDs on SPI CS signals 18. page 46, 1(USB DB): move power button switch (SW1)to USB DB 19. page 47: add eMMC page 20. page 33: change WIFI from M.2 type to solder down type 21. page 30, 5(USB DB): move LED and Fan to DB 22. page 31: remove finger print function 22. page 34: remove LTE function 23. page 10: Move MEM_STRAPs to match eMMC schematic 24. page 2,3: update block diagram 25. page 32: update edp pin define 26. page 46: add pen detect circuit and pen charge circuit. 27. page 9: delete TP7010-7013, TP7018-7019, TP7022-7029, TP7036-TP7041 28. page 34: delete R311,R627,R628(LTE) 29. page 11: delete TP7030-7035,TP7020, TP7021 30. page 31: delete finger print circuit 31. page 11, 46: delete PEN_PDCT_ODL, PEN_RESET_ODL,PEN_INT_ODL NET 32. page 33: M2_SHUTDOWN_L connect to wifi pin 28 ,BT_DISABLE_L connect to wifi pin 63 33. page 12: stuff R101 33. page 25: delete TP128~TP133, delete R201,R203,R205,R207,R209,R9282 34. page 23: delete R165,Q9, U38 PIN 9 change to NC. 35. page 47: stuff 49084, unstuff R857 , add R9314
	rev 2_2	1. page 11: Removed TRACKPAD_INT_ODL from GPP_D21 2. page 11: Change R74 to 4.7K 3. page 25: DNSed all XDP components 4. page 11: Removed WWAN_CONFIG_0/1/2/3 and R95/R96/R97/R98 5. page 11: Removed TP16,TP26,TP27,TP37 and R20,R21,R72 6. page 10: Added R9325 100k ohm to GPP_F23 and stuff, DNS R709

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	1C	1.Down size of some cap and res footprint.(C1205,C7835,C7836,R857,R721,R720,R46,R47,R680,R681,R5118,R5168,R9058,R9059,R9316, C290,C291,C292,C293,C294,c295,C296,C297,C300,C301). To optimize routing. 2.Del J24. (colay keyboard connector no use in future) . 3.Adjust PPVAR_SYS Cap quantity and value of U47,U48 and U49. New placement without high limit, we change back to follow CRB design. 4.Del pen function (J25,J26,U4101 relative sch).Customer remove this function form feature list. 5.Change CN1,J16,J17 connector type for new ID. 6.Colay SPI ROM socket 7.Reverse J6,J7,J9,CN2,pin define for placement 8.Change to EC_PROCHOT_IN_OD to EC_PROCHOT_IN(Clarity for firmware) 9.R303 Change to 1.2k (Reduce rise time < 100ns on WAKE signal) 10.R231 Change to 2.2k (Reduce rise time < 100ns on WAKE signal) 11.Q46 Gate of this transistor should be connected to PP3300_H1_G 12.Change connector PN follow connector list.(J17,J6,J2,Page30,37) 13. Adjust PPVAR_SYS_R_VCCIO CAP (2x 22U -->6x10u, due to layout high limit,Page 40) 14. Change this circuit to match Nami CCD circuit (Q46, Q18, R538,Page 24) 15. Adjust cap of PPVAR_VPRIM_CORE_A and PP1050_A (due to high limit, Page40) 16. Del reserve GMR function on MB (Page32) 17. Add power net name between D2 and U37 (Page23) 18. R5237 chnage to 0201 size (Page36) 19. Down size of res and cap (EMMC)(Page47).To optimize routing. 20. Modify sch of thermal detected.(Page45) 21. Change J23 PN follow connector list .(Page28) 22. Down size of cap (TX/RX cap)(Page37).To optimize routing. 23. Change ESD solution (Page37).To optimize routing. 24. Add screw hole (Page46) 25. Swap L10,L3,L4,L5,L9 pin connection.(Page36) To optimize routing. 26. Change USB typeA ESD solution D28,D87 (Page36) 27. Add screw hole (Page46) 28. Change U63 PN to RT9020-18GU5. Output Voltage should be 1.8V not 3.3V (Page44) 29. Change J7 PN follow connector list (Page30) 30. Swap L4,L5 pin connection.(Page36) To optimize routing. 31. Add EMI solution. C7923,C7924,C7925,L29,L30,L31,L32,L33,L34,L35,L36(Page10,Page28,Page29,Page37) For EMI reserve. 32. Add connection to CN2 for PEN.(Page46) 33. Del TP103,TP105,TP113,TP111,TP114,TP115,TP104,TP112,TP118,TP106,TP110,TP116,TP109,TP108,TP135,TP134,TP120,TP107.(Page16) 34. Change USB typeA / typeC ESD solution add D66,D88,D89,D90 & Del D86,D87(page 36,37) for Intel Feedback add F2 for safety request(page 36) 35. Change hole9/hole10 footprint and add 2 clip (Page46) 36. DNS R711, C349 (Page37) VCONN for Port 0 is sourced from U44 37. Add DNS buffer powered from PP3300_G to isolate PLT_RST_L from M2_SSD_RST_L_R (in parallel with R229). Add note that it is only needed for SSDs that have an internal pull-up. (Page27) Internal pull-up on some SSDs can cause glitch on PLT_RST_L after the AP stops driving it, causing CR50 to think that AP is still on. 38. Change R362 to 48.7k, and add note that if using TI BC1.2 part, value should be 51.1k, Change R363 to 29.4k, and add note that if using TI BC1.2 part, value should be 30.9k (Page36) 39. Add a schematic note next to this signal that describes when this signal is needed.Need to make this clear to OEMs(Page11) 40.Add DNS 200pF caps near TCPC.May need to add capacitance in order to meet USB PD cReceiver minimum spec(Page37) 41.Add TABLET_MODE signal to GPIOC7 pin on EC.This will be used in systems that have GMR sensor instead of hall effect (Page35) 42.Change C302, C303 to 0 ohm(Page8).we mount cap on USB board. 43.Modify Hole2 Hole3 Hole4 footprint. (Page46) 44.Modify J4 J5 footprint. (Page27,29). Follow connector list. 45.Modify XDP connection. (Page12,25). To optimize routing. 46.Modify PAD footprint. (Page46). 47. Change C55,C98,C86,C91,C73,C118,C29,C37,C193,C144,C186,C211,C203,C152 PN(Page17). Without high limitation, change to another one. 48. Change R490 to 0.1 ohm (Page44). 49. Change clip PN for ME request (Page46). 50. Change Hole7,Hole8 footprint (Page46). 51. Change D66,D88,D89,D90 PN (Page36,37). USB+- should use ESD component with 5v tolerance.

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	1D	1.Page 12,25 : Modify XDP connection. For intel issue tracker JTAG connection. Stuff these resistors R202, R203, R204 R205, R206, R207, R208, R209, R210, R211. 2. page 30 : J2 pin define upside down(JIM) 3. page 36 : remove F2 on PP3300_SD_DX. Due to U64 already had safety function. 4. page 11 : Change R75 pull up to be PP1800_A. GPP_A8 Dual-route signal to GPP_A16 5. page 32: Remove "USI INT IS ACTIVE HIGH" note. 6. page 11: Change R771 pull up to be PP1800_A. GPP_A8 Dual-route signal to GPP_A16 7. page 8, USB D/B page 4: Move diode D79 to DDI2_AUX_N on page 8 (cathode connected to PP3300_SOC_A) 8. page 25 : reserved R667 for DCI. 9. page 10 : unstuff C7924 for SD_CLK EMI suggestion, after EMI test, we can remove it and signal will be more positive. 10. page 10 : Add R9340 damping R for CNV_CLKREQ 11. page 29 : Add R773,R772 option for output crosstalk tuning 12. page 11 : DNS series resistors R20, R21 and R72 on unused PCH SPI1 interface 13. page 35 : Put diode D84 in series with signal KSO_06, cathode connecting to EC and anode connecting to the keyboard connector. Remove R691 499 ohm series resistor.
	ZAR DVT ZSI EVT	1.Page 37(Follow Hatch change list) : add FB4 between AVDD and DVDD rails of ANX3447. add C764, C765, C766 for DVDD rails. 2.Page 32: add Q55,Q501,R9342,R9343,R9344 for panel T11 timing tuning. 3.USB D/B : modify R629 to 3.3k and modify R630 to 1.8k for LED current setting 4.USB D/B : R9390 change from 1k to 620 ohm to prevent OCP (Fan Iset up to 0.9A) 5.MLB : add layout test point for factory request 6.Page 37(Follow Hatch change list): Connect DVDD_IO to PP3300_TCPC_AVDD through a 0 ohm resistor R775 7.Page 37(Follow Hatch change list): connect pull-up R319 to PP3300_TCPC_AVDD because ROLE_SEL needs to be pulled up to AVDD33 8.Page 37(Follow Hatch change list): add note stating that 100K pull-up / pull-down is 'no-stuff' only for ANX3447 because of bug b:/124410548 9.Page 37(Follow Hatch change list): add 10K series resistor R218 at output of GPIO2/PSL_IN4 to Improper isolation of EC_RST_ODL on some NPCX79nx designs 9.Page 29: add C7932, C7933 for PP1800_A power rail
	V3.0	1.Page 23(Follow Hatch change list) : R163 change from 100k to 4.7k because Input impedance on EC EEPROM WC# pin is too low, so pullup is too large. Static "high" voltage only reaches 1.15V when it should be ~3.3V, resulting in unprotected EC EEPROM
	V3.1	1. Page X : Change to shortpad : Location : 0201 : R132,R133,R194,R202,R203,R204,R205,R206,R207,R208,R209,R210,R211,R223,R241,R242,R254,R255,R26,R261,R262,R28,R30,R33,R334,R335,R356,R371,R384,R5237, R635,R65,R661,R676,R690,R772,R773,R9084,R9327,R9334,R9335 0402 : R225,R5238,R744,R746,R748,R9087,R9090,R9308,R9309,R9310,R9340 0603 : R137,R138,R235,R236,R237,R683 0805 : R659,R660 2.Page 23 : (1) Remove U3 (BIOS socket) (2) Reserved U4104 for shortage issue. (3) Add R9348 for realtek recommend . (3) Remove soundwires straps : R244,R245,R246,R247,R248,R249,R250,R251,R252,R253 for realtek recommend . 3.Page 10 : (1) Remove C7925 for realtek recommend (2) Change R40 from 33 ohm to 0ohm for realtek recommend 4.Page 7 : Add. R9347 ,Reserved Q502 ,Q503 & Del. Q49 for reduce glitch 5.Page 29 : (1) Add C7934 for realtek recommend (2) Unstuff C7932,C7933 5.Page 44 : Change U27.4 BIAS pin from PP5000_A to PP3300_G for PP5000_A glitch

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