# Octopus_A_Yorp_DVT

SCH: 650-01771-03-SCH
ASSY:650-01771-03
PCB: 651-01771-03

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**TABLE OF CONTENTS**



BITLAND Bitland Information Technology Co.,Ltd.

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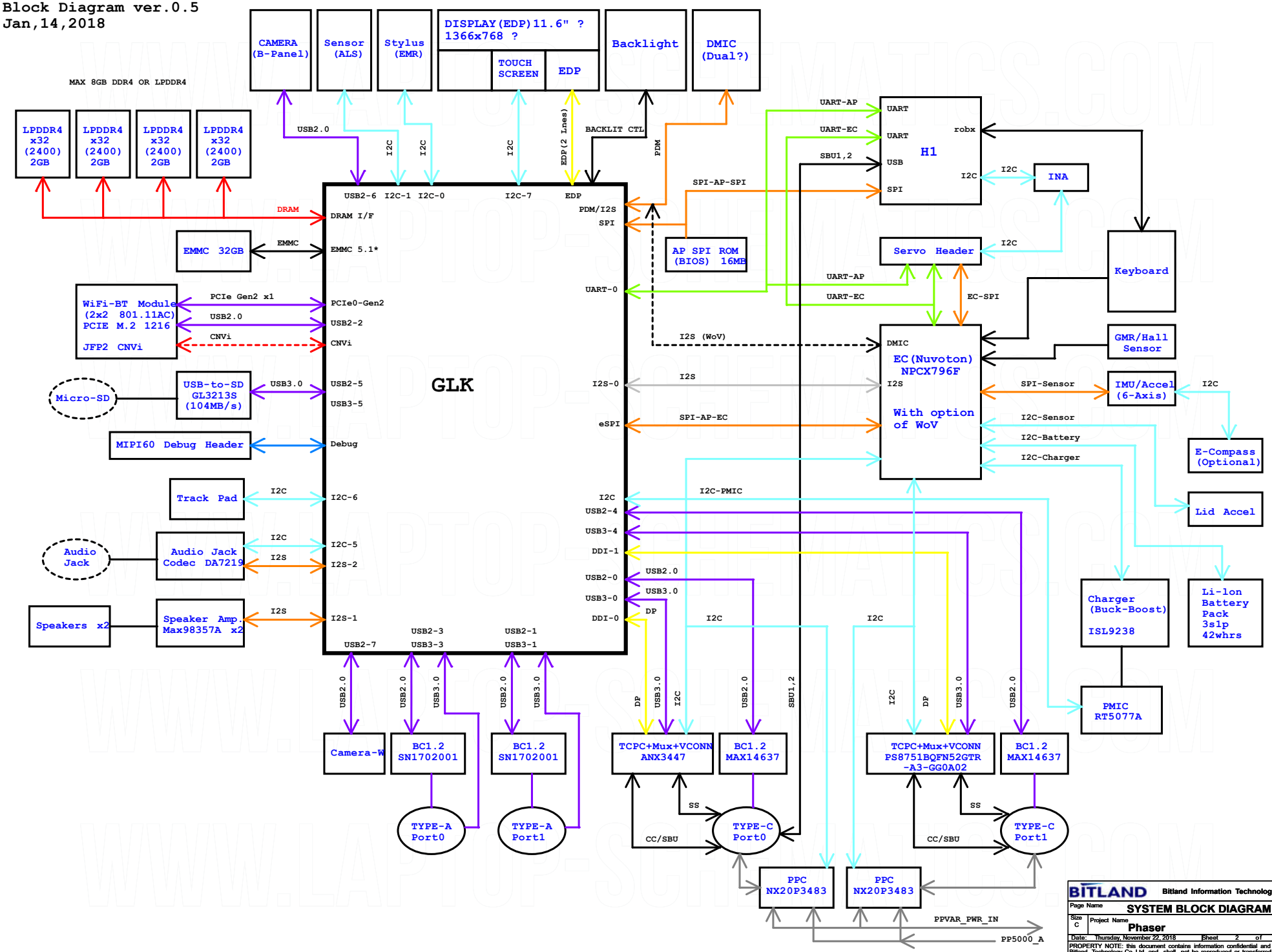
# Octopus(Gemini Lake) Block Diagram ver.0.5 Jan,14,2018

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Page Name: SYSTEM BLOCK DIAGRAM

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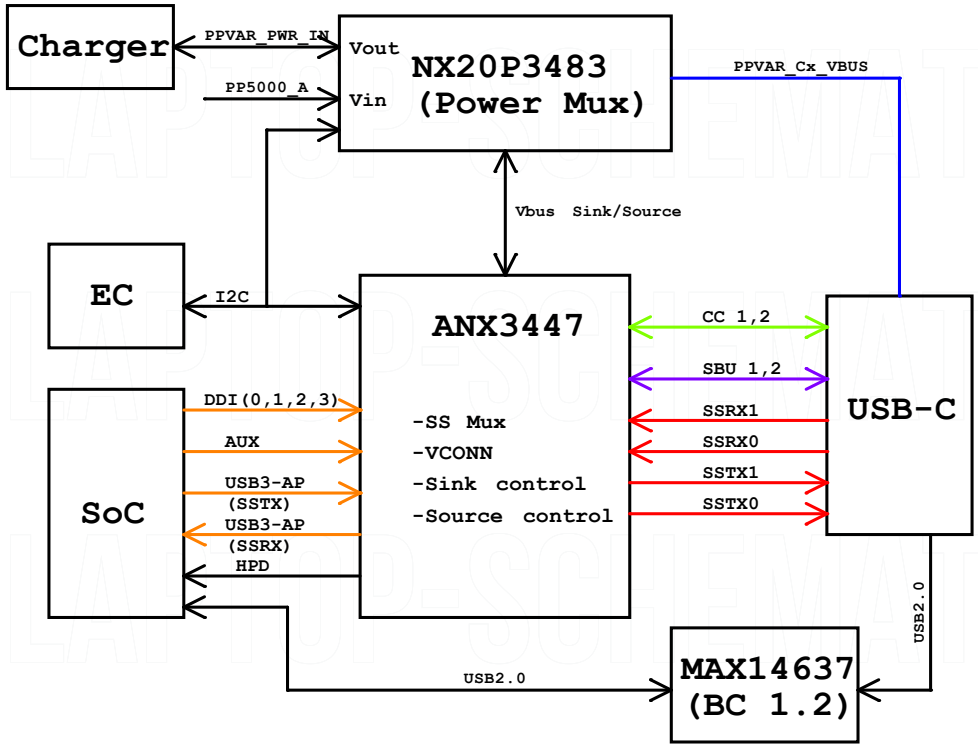


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Page Name: USB TYPE-C BLOCK DIAGRAM

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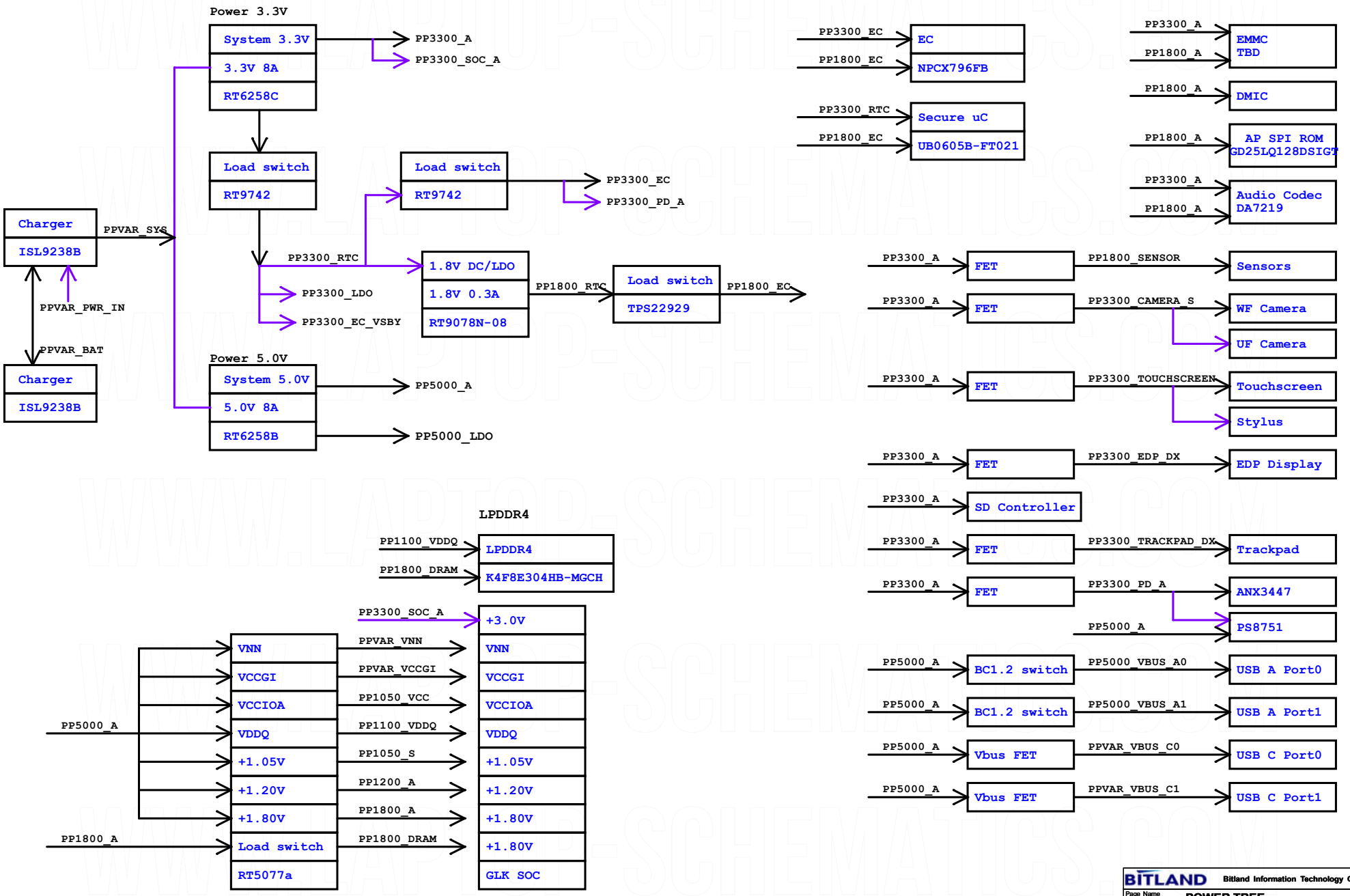
# Power Tree

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Page Name: POWER TREE

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| Master | Port | Net Name | Slave Device(S) | Speed |
|---|---|---|---|---|
| EC | I2C0 0 | EC_I2C_BATTERY_3V3 | BATTERY(TBD) | 100KHz |
| EC | I2C1 0 | EC_I2C_USB_C0_MUX | ANX7447,NX20P3483 | 100KHz |
| EC | I2C2 0 | EC_I2C_USB_C1_MUX | PS8751B | 100KHz |
| EC | I2C3 0 | EC_I2C_EEPROM | M34E02 | 100KHz |
| EC | I2C4 1 | EC_I2C_CHARGER_3V3 | ISL8238B | 100KHz |
| EC | I2C5 0 | - | | |
| EC | I2C7 0 | EC_I2C_SENSOR_U | LSM6DS3TR, LIS2DE12TR | 400KHz |
| AP | LPSS I2C0 | PCH_I2C_PEN | STYLUS(TBD) | 400KHz |
| AP | LPSS I2C1 | - | - | |
| AP | LPSS I2C2 | - | | |
| AP | LPSS I2C3 | DBG_PCH_I2C | TBD | TBD |
| AP | LPSS I2C4 | PCH_I2C_H1 | UR0605B | 100KHz |
| AP | LPSS I2C5 | PCH_I2C_AUDIO | DA7219 | 100KHz |
| AP | LPSS I2C6 | PCH_I2C_TRACPAD | TRACPAD(TBD) | 100KHz |
| AP | LPSS I2C7 | PCH_I2C_TOUCHSCREEN | TOUCHSCREEN (TBD) | 100KHz |
| AP | PMC I2C | PCH_PMIC_I2C | RT5077A | 100KHz |



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Page Name: I2C MAP

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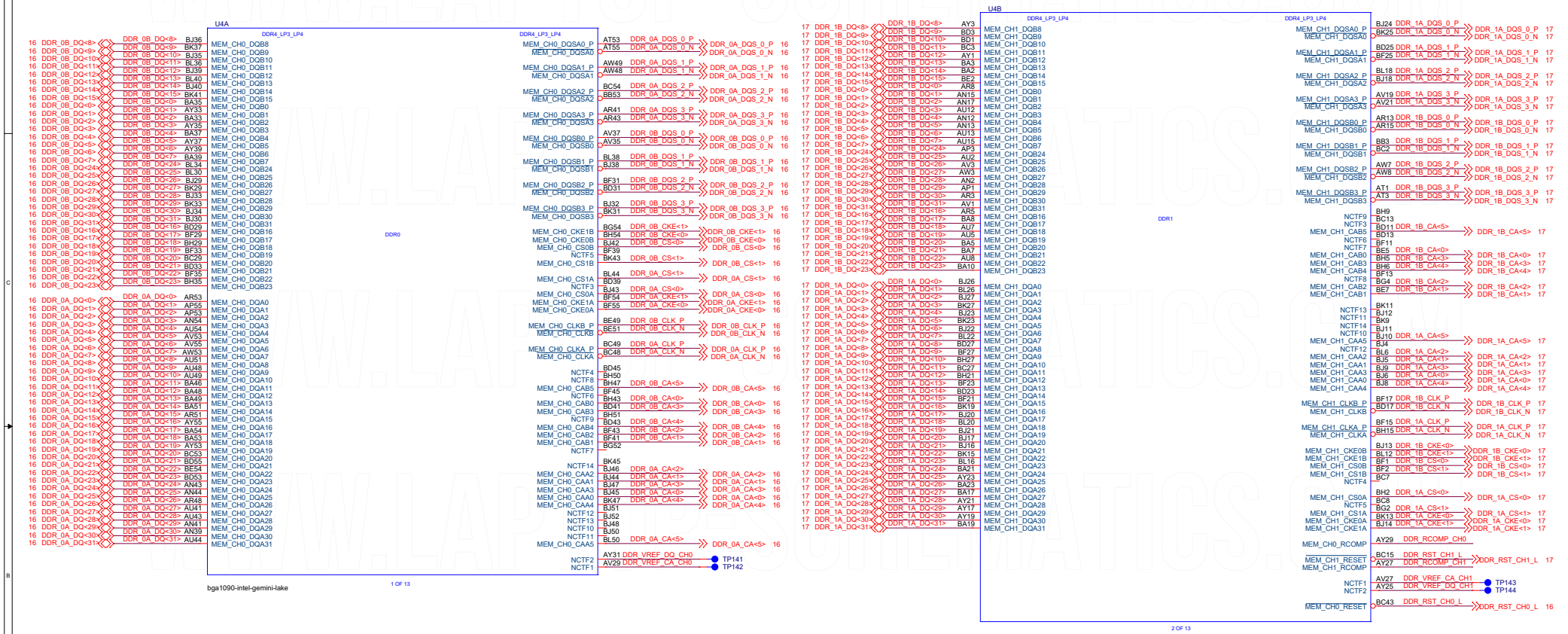


PLACE AS CLOSE TO SOC AS POSSIBLE

| | |
|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. |
| Page Name | SOC DRAM I/F |
| Size C | Project Name: Phaser |
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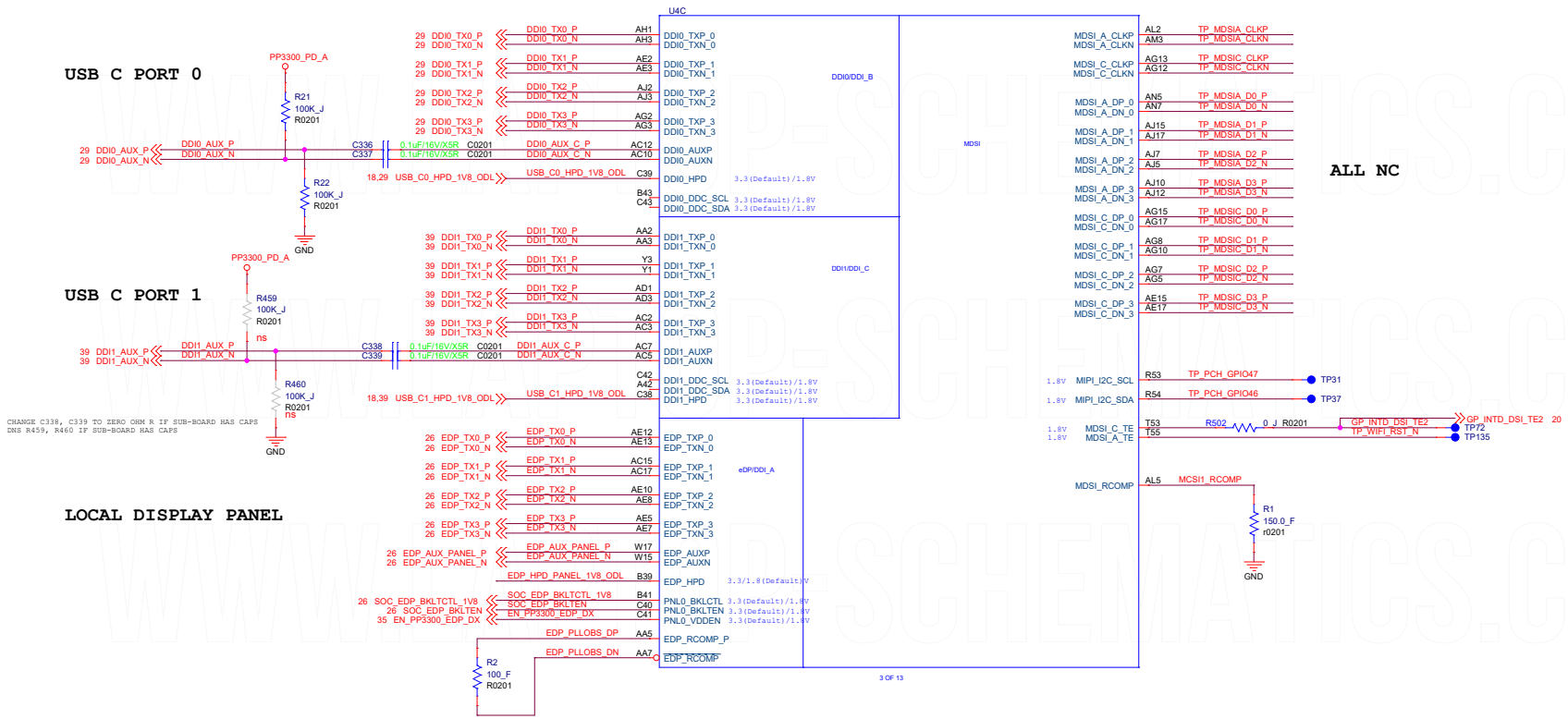


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|---|---|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. | | |
| Page Name | SOC EDP/MIPI/DDI | | |
| Size C | Project Name Phaser | | Rev 1.3 |
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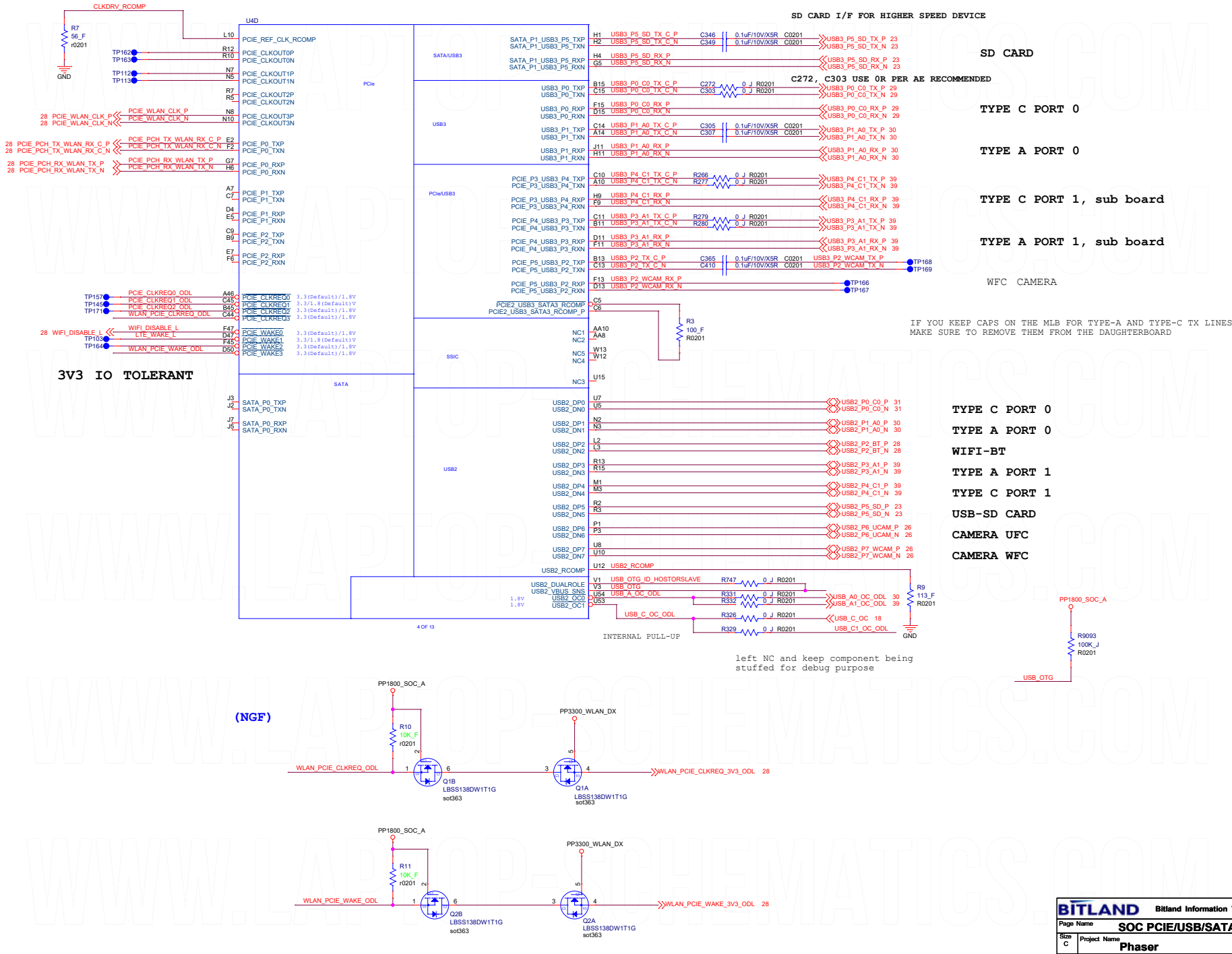


| | |
|---|---|
| Bitland Information Technology Co.,Ltd. | |
| Page Name | SOC PCIE/USB/SATA |
| Size C | Project Name: Phaser |
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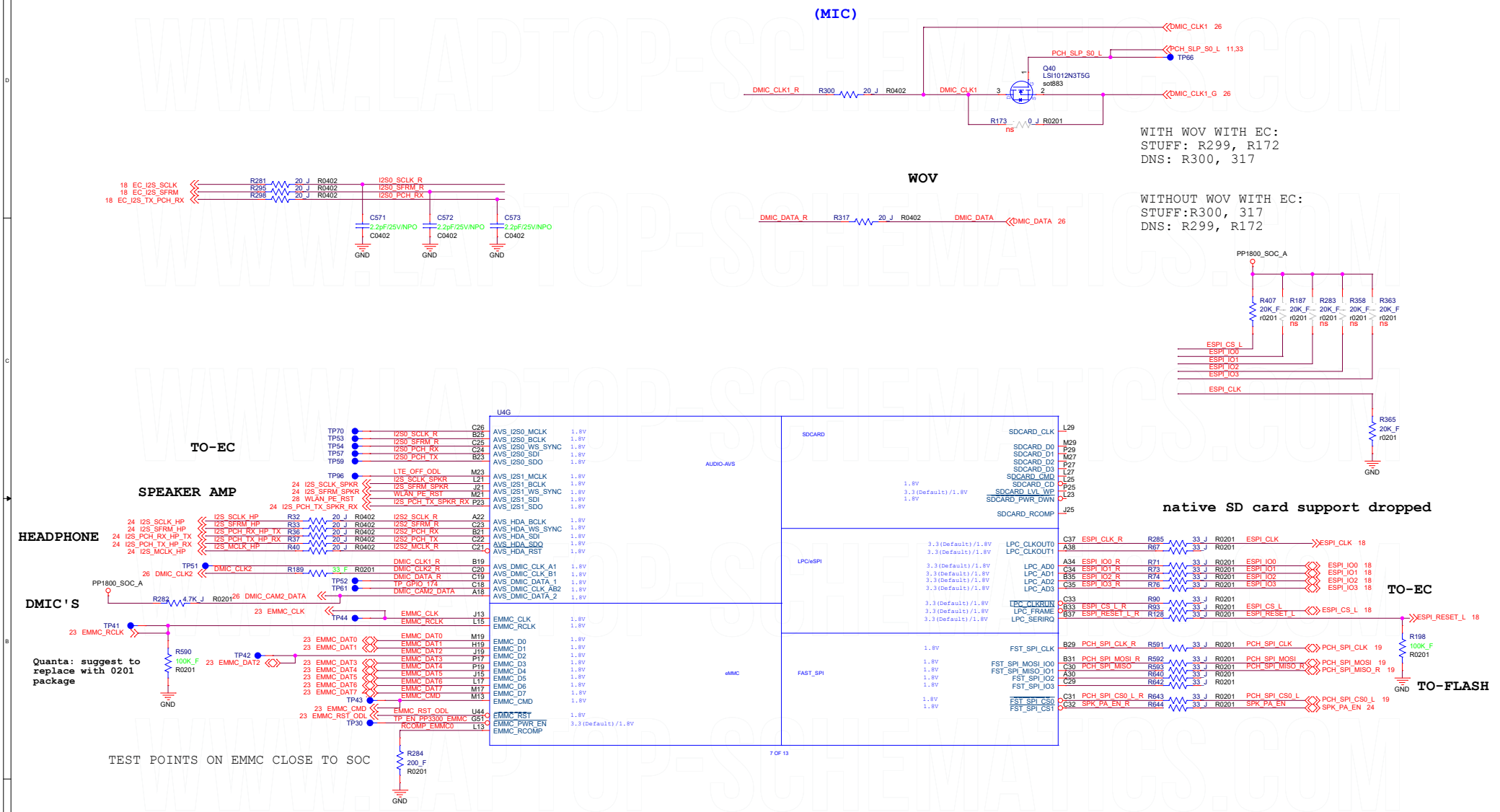
(MIC)
DMIC_CLK1 26
PCH_SLP_S0_L
PCH_SLP_S0_L 11,33
TP66
Q40
LSI1012N3T5G
sot883
DMIC_CLK1_R
R300
20_J R0402
DMIC_CLK1
DMIC_CLK1_G 26
R173
ns
0_J R0201
WITH WOV WITH EC:
STUFF: R299, R172
DNS: R300, 317
WOV
WITHOUT WOV WITH EC:
STUFF:R300, 317
DNS: R299, R172
DMIC_DATA_R
R317
DMIC_DATA
DMIC_DATA 26
18 EC_I2S_SCLK
18 EC_I2S_SFRM
18 EC_I2S_TX_PCH_RX
R281
R295
R298
I2S0_SCLK_R
I2S0_SFRM_R
I2S0_PCH_RX
C571
C572
C573
2.2pF/25V/NPO
C0402
GND
PP1800_SOC_A
R407
R187
R283
R358
R363
20K_F
r0201
ESPI_CS_L
ESPI_IO0
ESPI_IO1
ESPI_IO2
ESPI_IO3
ESPI_CLK
R365
TO-EC
SPEAKER AMP
HEADPHONE
DMIC'S
native SD card support dropped
U4G
AUDIO-AVS
SDCARD
LPC/eSPI
eMMC
FAST_SPI
7 OF 13
TP70
TP53
TP54
TP57
TP59
TP96
I2S0_SCLK_R
I2S0_SFRM_R
I2S0_PCH_RX
I2S0_PCH_TX
LTE_OFF_ODL
I2S_SCLK_SPKR
I2S_SFRM_SPKR
WLAN_PE_RST
I2S_PCH_TX_SPKR_RX
I2S_SCLK_HP
I2S_SFRM_HP
I2S_PCH_RX_HP_TX
I2S_PCH_TX_HP_RX
I2S_MCLK_HP
I2S2_SCLK_R
I2S2_SFRM_R
I2S2_PCH_RX
I2S2_PCH_TX
I2S2_MCLK_R
TP51
DMIC_CLK2
R189
33_F R0201
DMIC_CLK1_R
DMIC_CLK2_R
DMIC_DATA_R
TP_GPIO_174
DMIC_CAM2_DATA
TP52
TP61
PP1800_SOC_A
R282
4.7K_J R0201
26 DMIC_CAM2_DATA
23 EMMC_CLK
TP44
EMMC_CLK
EMMC_RCLK
TP41
23 EMMC_RCLK
R590
100K_F
R0201
Quanta: suggest to replace with 0201 package
TP42
23 EMMC_DAT2
EMMC_DAT0
EMMC_DAT1
EMMC_DAT2
EMMC_DAT3
EMMC_DAT4
EMMC_DAT5
EMMC_DAT6
EMMC_DAT7
EMMC_CMD
TP43
23 EMMC_CMD
23 EMMC_RST_ODL
EMMC_RST_ODL
TP_EN_PP3300_EMMC_G51
TP30
RCOMP_EMMC0
R284
200_F
R0201
TEST POINTS ON EMMC CLOSE TO SOC
AVS_I2S0_MCLK
AVS_I2S0_BCLK
AVS_I2S0_WS_SYNC
AVS_I2S0_SDI
AVS_I2S0_SDO
AVS_I2S1_MCLK
AVS_I2S1_BCLK
AVS_I2S1_WS_SYNC
AVS_I2S1_SDI
AVS_I2S1_SDO
AVS_HDA_BCLK
AVS_HDA_WS_SYNC
AVS_HDA_SDI
AVS_HDA_SDO
AVS_HDA_RST
AVS_DMIC_CLK_A1
AVS_DMIC_CLK_B1
AVS_DMIC_DATA_1
AVS_DMIC_CLK_AB2
AVS_DMIC_DATA_2
EMMC_CLK
EMMC_RCLK
EMMC_D0
EMMC_D1
EMMC_D2
EMMC_D3
EMMC_D4
EMMC_D5
EMMC_D6
EMMC_D7
EMMC_CMD
EMMC_RST
EMMC_PWR_EN
EMMC_RCOMP
SDCARD_CLK
SDCARD_D0
SDCARD_D1
SDCARD_D2
SDCARD_D3
SDCARD_CMD
SDCARD_CD
SDCARD_LVL_WP
SDCARD_PWR_DWN
SDCARD_RCOMP
LPC_CLKOUT0
LPC_CLKOUT1
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_CLKRUN
LPC_FRAME
LPC_SERIRQ
FST_SPI_CLK
FST_SPI_MOSI_IO0
FST_SPI_MISO_IO1
FST_SPI_IO2
FST_SPI_IO3
FST_SPI_CS0
FST_SPI_CS1
ESPI_CLK_R
ESPI_IO0_R
ESPI_IO1_R
ESPI_IO2_R
ESPI_IO3_R
ESPI_CS_L_R
ESPI_RESET_L_R
PCH_SPI_CLK_R
PCH_SPI_MOSI_R
PCH_SPI_MISO
PCH_SPI_CS0_L_R
SPK_PA_EN_R
ESPI_CLK 18
ESPI_IO0 18
ESPI_IO1 18
ESPI_IO2 18
ESPI_IO3 18
ESPI_CS_L 18
ESPI_RESET_L 18
PCH_SPI_CLK 19
PCH_SPI_MOSI 19
PCH_SPI_MISO_R 19
PCH_SPI_CS0_L 19
SPK_PA_EN 24
R198
100K_F
R0201
TO-FLASH
No external PU/PD on GPIO_174, using internal PD for setting VDD2 to 1.2v (GPIO_174)
R282 is for strapping high to enable eSPI mode (GPIO_175)
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Page Name
SOC AUDIO/EMMC/LPC/SPI
Size C
Project Name
Phaser
Rev 1.3
Date: Thursday, November 22, 2018
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I2C MAY BE PROBLEM IF THE I2C PULL-UP VOLTAGE IS TURNED OFF WHEN DEVICE IS OFF

MODE SELECTION: PULL HI =1.8V

PLACE R573 NEAR M.2

STEST CONNECTION

PLACEMENMT OF THE LEVEL SHIFTERS AND PULL-UPS DON'T NEED TO BE NEAR AP

(TSN)

(TPD)

(PEN)

| | |
|---|---|
| Bitland Information Technology Co.,Ltd. | |
| Page Name | SOC I2C/CNVI/UART/SPI |
| Size C | Project Name: Phaser |
| Rev | 1.3 |
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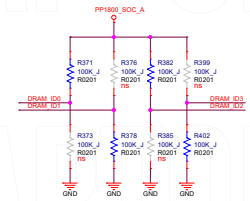
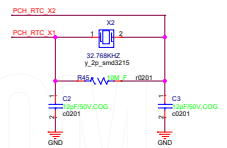
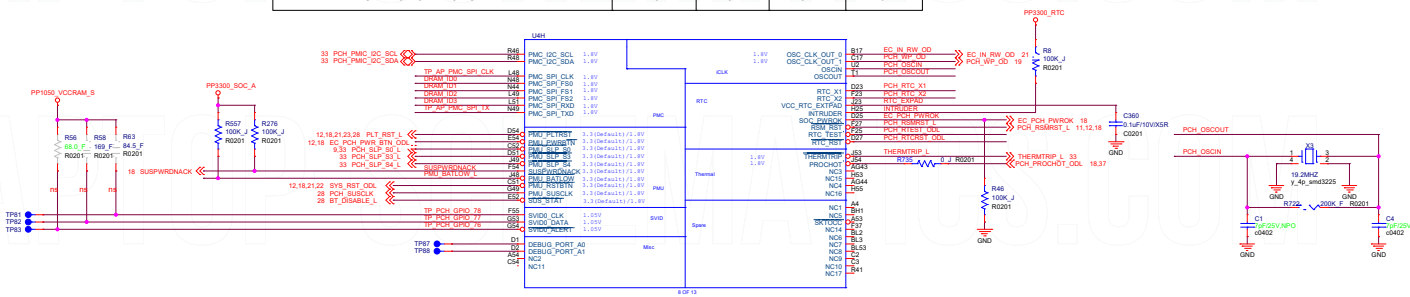
| RAM_ID | DRAM_ID3 | | DRAM_ID2 | | DRAM_ID1 | | DRAM_ID0 | |
|---|---|---|---|---|---|---|---|---|
| | R399 | R402 | R382 | R385 | R376 | R378 | R371 | R373 |
| 0 | DNS | Stuff | DNS | Stuff | DNS | Stuff | DNS | Stuff |
| 1 | DNS | Stuff | DNS | Stuff | DNS | Stuff | Stuff | DNS |
| 2 | DNS | Stuff | DNS | Stuff | Stuff | DNS | DNS | Stuff |
| 3 | DNS | Stuff | DNS | Stuff | Stuff | DNS | Stuff | DNS |
| 4 | DNS | Stuff | Stuff | DNS | DNS | Stuff | DNS | Stuff |
| 5 | DNS | Stuff | Stuff | DNS | DNS | Stuff | Stuff | DNS |
| 6 | DNS | Stuff | Stuff | DNS | Stuff | DNS | DNS | Stuff |
| 7 | DNS | Stuff | Stuff | DNS | Stuff | DNS | Stuff | DNS |
| 8 | Stuff | DNS | DNS | Stuff | DNS | Stuff | DNS | Stuff |
| 9 | Stuff | DNS | DNS | Stuff | DNS | Stuff | Stuff | DNS |
| 10 | Stuff | DNS | DNS | Stuff | Stuff | DNS | DNS | Stuff |
| 11 | Stuff | DNS | DNS | Stuff | Stuff | DNS | Stuff | DNS |
| 12 | Stuff | DNS | Stuff | DNS | DNS | Stuff | DNS | Stuff |
| 13 | Stuff | DNS | Stuff | DNS | DNS | Stuff | Stuff | DNS |
| 14 | Stuff | DNS | Stuff | DNS | Stuff | DNS | DNS | Stuff |
| 15 | Stuff | DNS | Stuff | DNS | Stuff | DNS | Stuff | DNS |

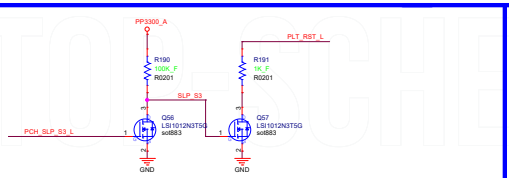
| RAM_ID | Memory | Speed | Rank Density | Dual Rank | Ch0 | Ch0 | Part Number |
|---|---|---|---|---|---|---|---|
| 0 | 4GiB | 2400MHz | 8Gb | N | Y | Y | MT53B256M32D2NP-053 /H9HCNNNBPUMLHR-NME |
| 1 | 8GiB | 2400MHz | 16Gb | N | Y | Y | MT53B512M32D2NP-046 /H9HCNNNBPUMLHR-NME |
| 2 | 8GiB | 2400MHz | 8Gb | Y | Y | Y | |
| 3 | 4GiB | 2400MHz | 16Gb | N | Y | N | |
| 4 | 4GiB | 2400MHz | 8Gb | Y | Y | N | |
| 5 | 4GiB | 2400MHz | 16Gb | N | N | Y | |
| 6 | 4GiB | 2400MHz | 8Gb | Y | N | Y | |

| MEMORY TYPE | CONFIG3 | CONFIG2 | CONFIG1 | CONFIG0 |
|---|---|---|---|---|
| SAMSUNG 8GB K4F6E3S4HM-MGCJ | 0 | 0 | 0 | 1 |
| SAMSUNG 4GB K4F8E304HB-MGCJ | 0 | 0 | 0 | 0 |
| SAMSUNG 8GB K4F6E304HB-MGCJ | 0 | 0 | 1 | 0 |
| MICRON 8GB MT53E512M32D2NP-046 | 0 | 0 | 0 | 1 |
| MICRON 4GB MT53B256M32D1NP-053 | 0 | 0 | 0 | 0 |
| MICRON 8GB MT53B512M32D2NP-062 | 0 | 0 | 1 | 0 |
| HYNIX 8GB H9HCNNNBPUMLHR-NME | 0 | 0 | 1 | 0 |
| HYNIX 4GB H9HCNNN8KUMLHR-NME | 0 | 0 | 0 | 0 |



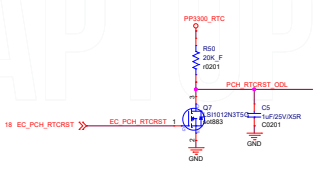



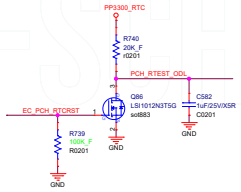



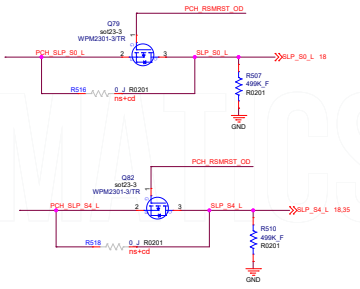


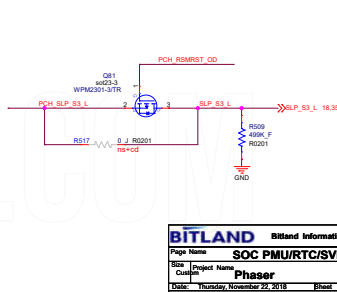
**CHECK RTCRST SIGNAL**




**CHECK RTCRST SIGNAL**

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Page Name: SOC PMU/RTC/SVID/THERMAL/MISC

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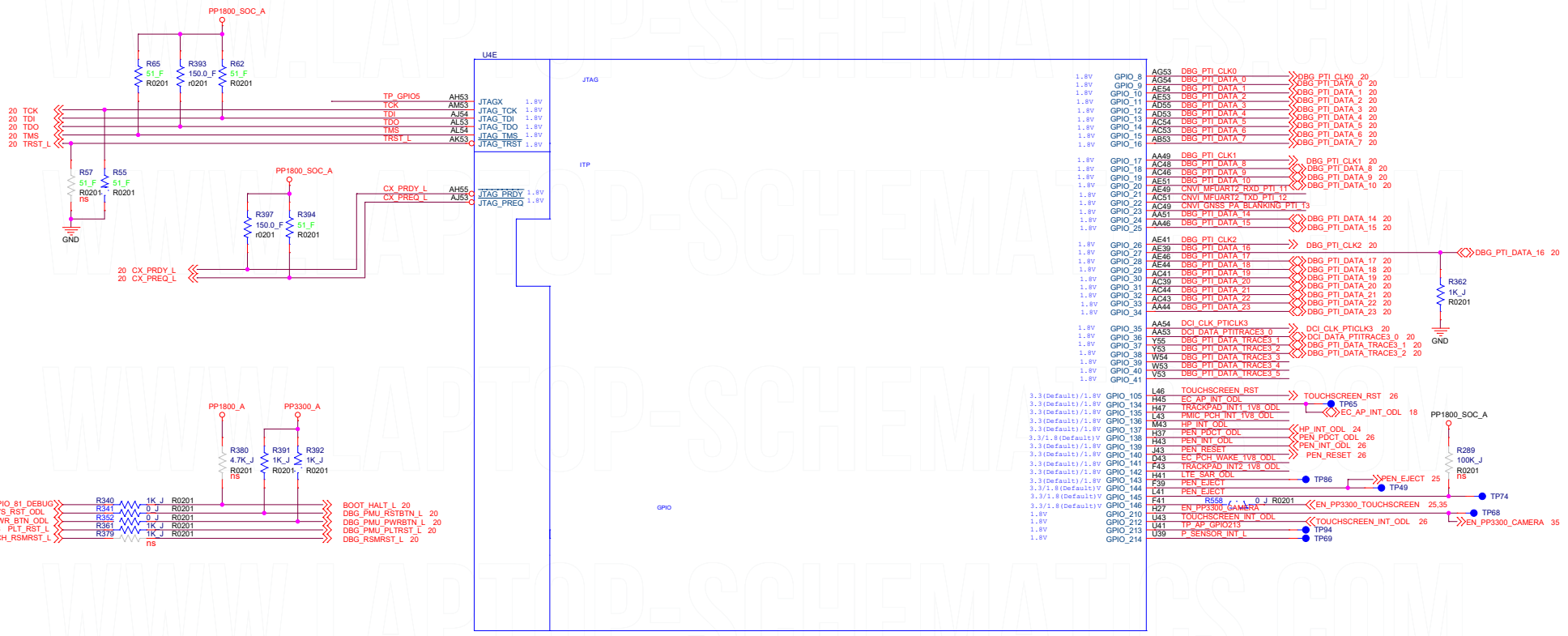
**LAYOUT NOTE: PLACE THE R62, 65, 55, 57, R393 WITHIN 1" OF J5 MIPI60 CONNECTOR.**

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Page Name: **SOC JTAG/GPIO/ITP**

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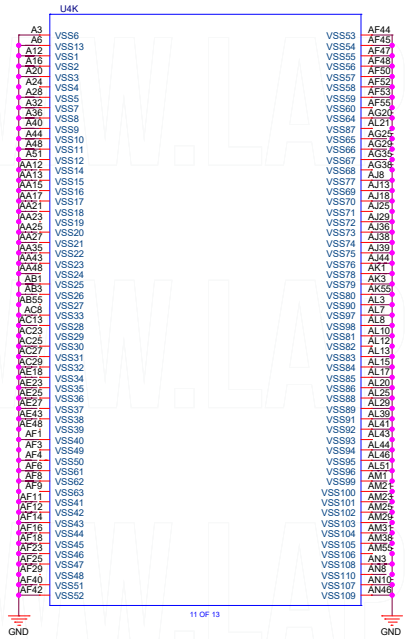


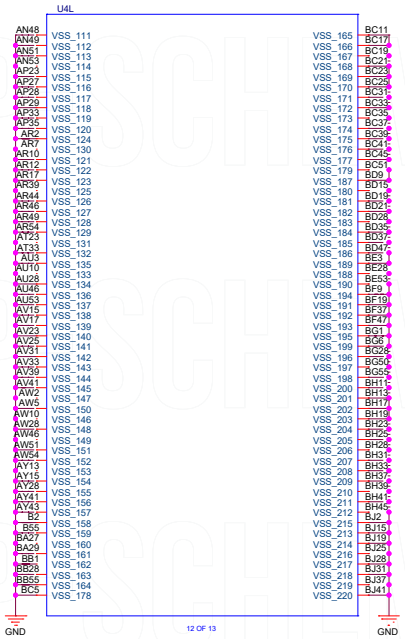


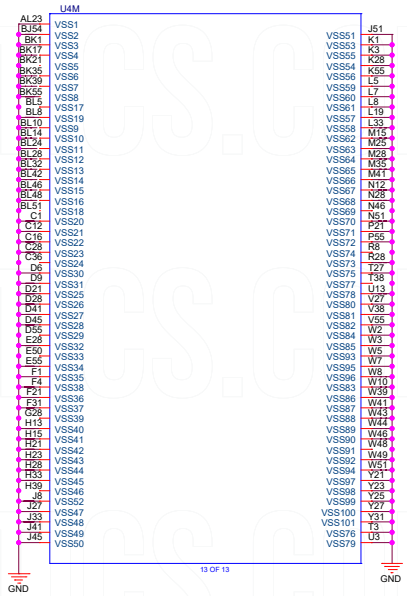


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Page Name: SOC GROUND

Size: C | Project Name: Phaser | Rev: 1.3

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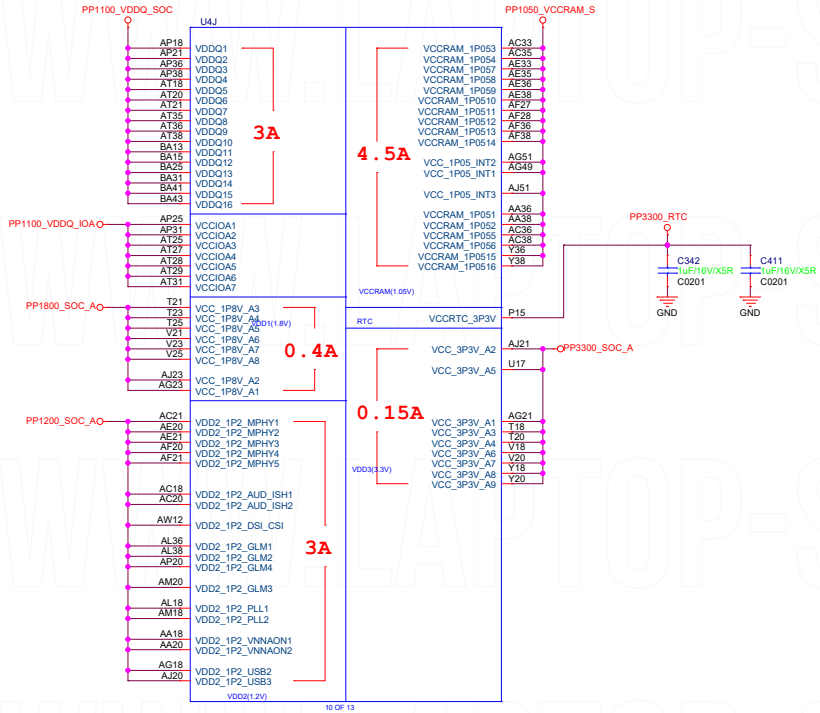
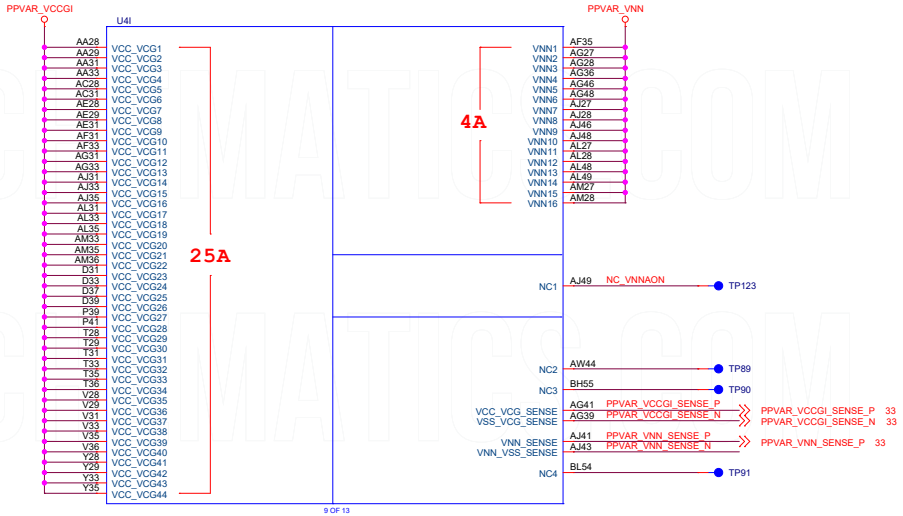
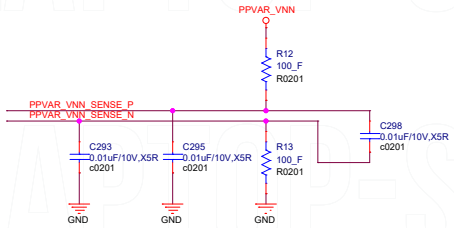
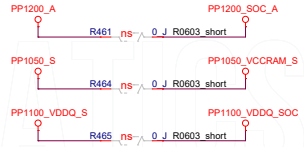
SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION



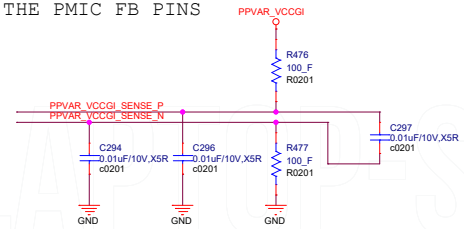




SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION




PLEASE THESE COMPONENTS NEAR THE PMIC FB PINS

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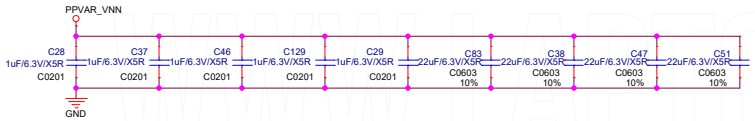
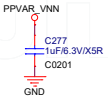
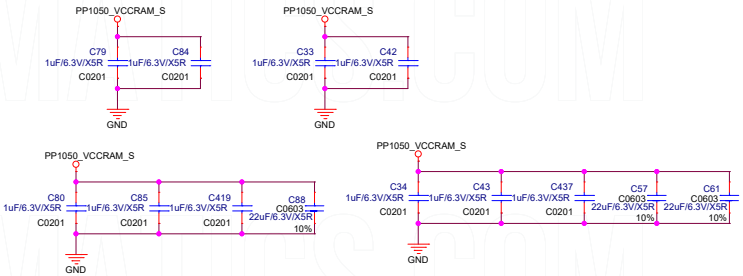
DECOUPLING VALUES AND NUMBER BASED ON THE REFERENCE DOC

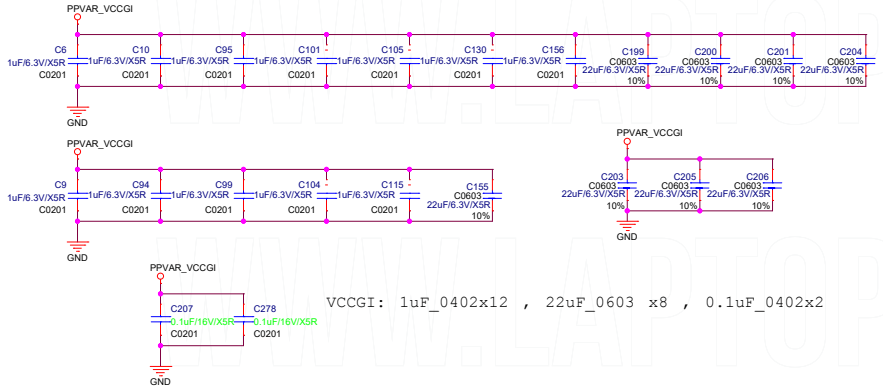



VNN: 1uF_0402x5 , 22uF_0603 x4

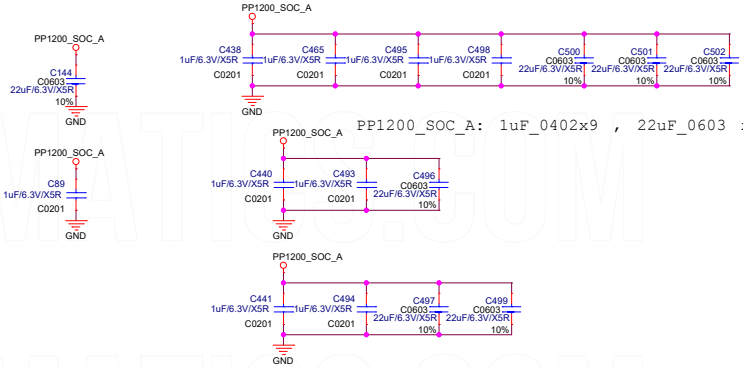



PP1050_VCCRAM_S: 1uF_0402x10 , 22uF_0603 x3



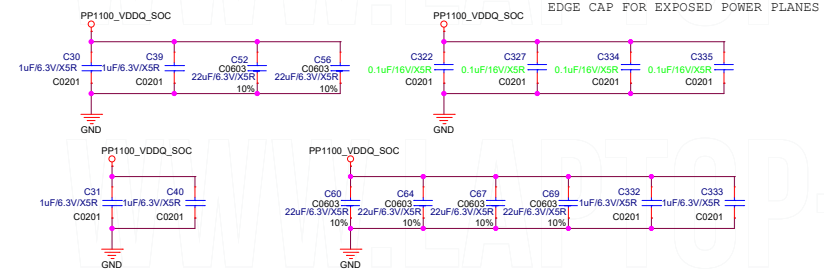




VCCGI: 1uF_0402x12 , 22uF_0603 x8 , 0.1uF_0402x2



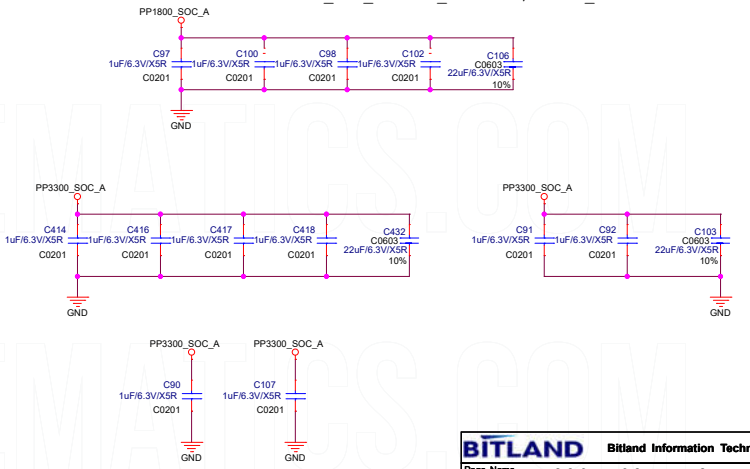

PP1200_SOC_A: 1uF_0402x9 , 22uF_0603 x7

EDGE CAP FOR EXPOSED POWER PLANES




VDDQI: 1uF_0402x9 , 22uF_0603 x9 , 0.1uF_0402x4

PP1800_SOC_A: 1uF_0402x4 , 22uF_0603 x1




PP3300_SOC_A: 1uF_0402x8 , 22uF_0603 x2

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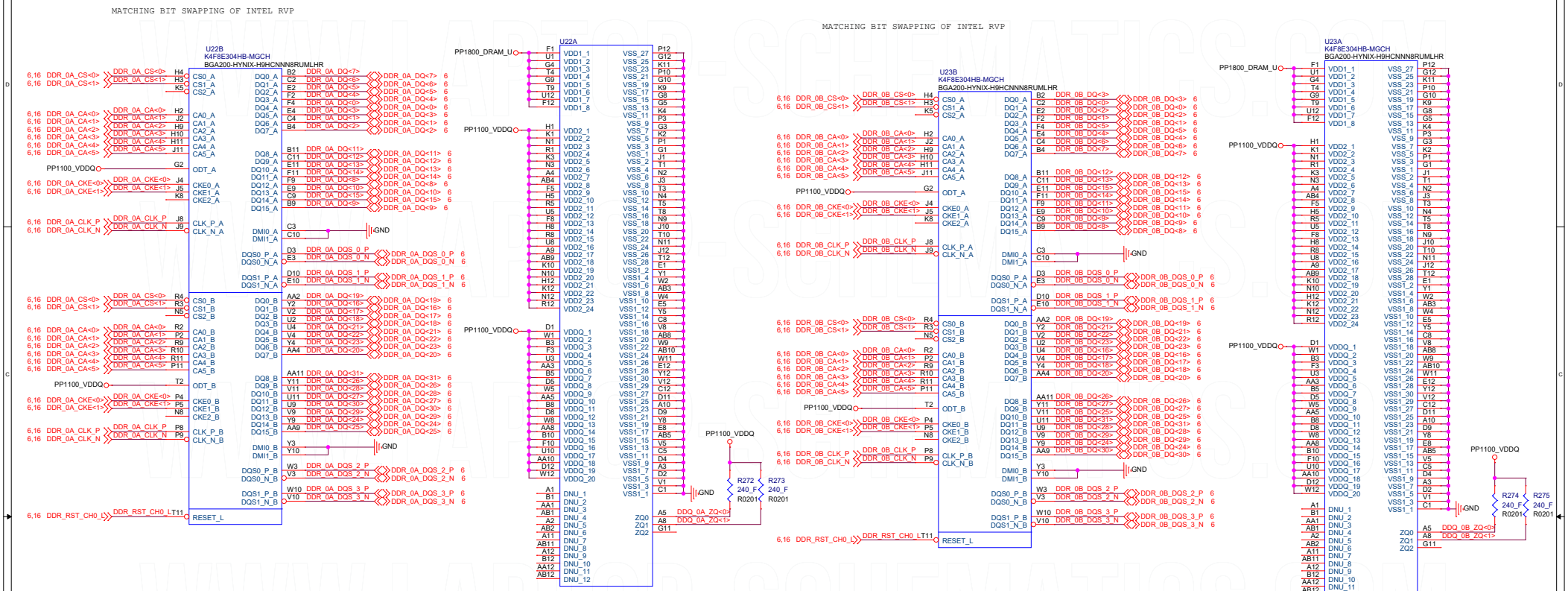
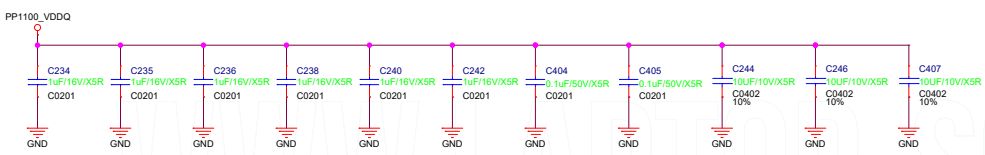
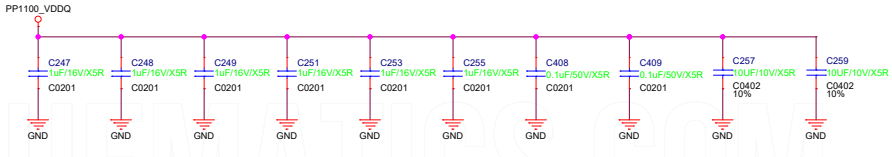
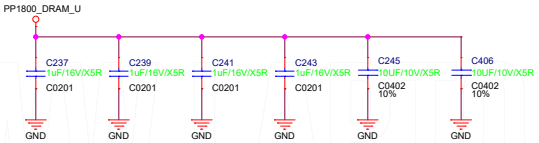


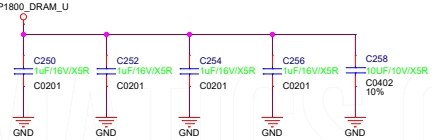

U22 VDD caps:1uFx6, 0.1uFx2, 10uFx3




U23 VDD caps:1uFx6, 0.1uFx2, 10uFx2




U22 VDD caps:1uFx4, 10uFx2




U23 VDD caps:1uFx4, 10uFx1

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Page Name: MEMORY CH 00/01 LPDDR4

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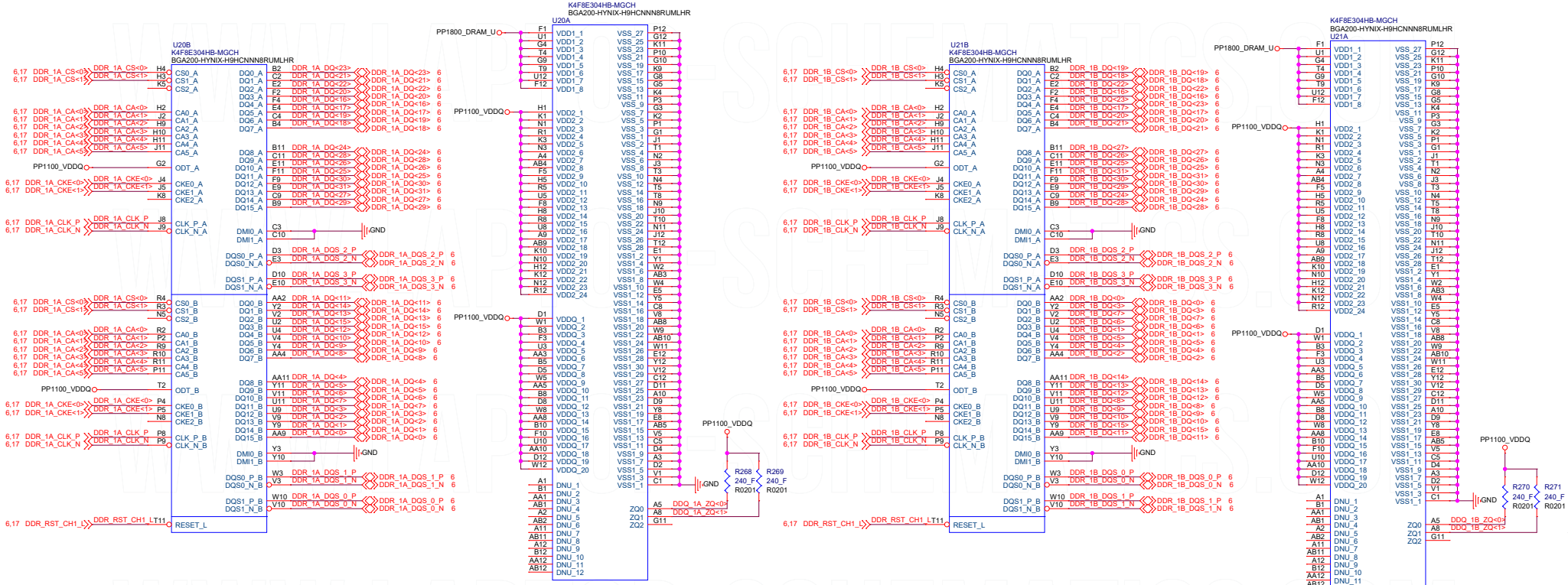
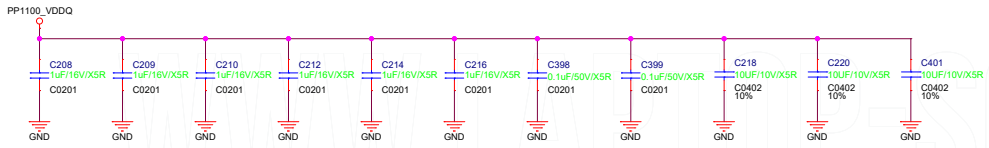
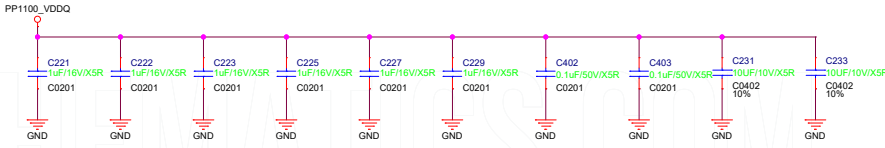
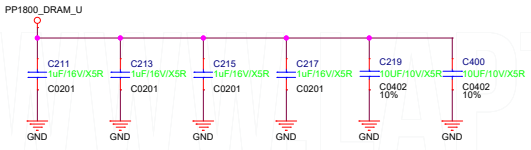


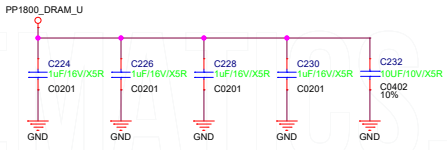

U20 VDD caps:1uFx6, 0.1uFx2, 10uFx3




U21 VDD caps:1uFx6, 0.1uFx2, 10uFx2




U20 VDD caps:1uFx4, 10uFx2




U20 VDD caps:1uFx4, 10uFx1

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Page Name: MEMORY CH 10/11 LPDDR4

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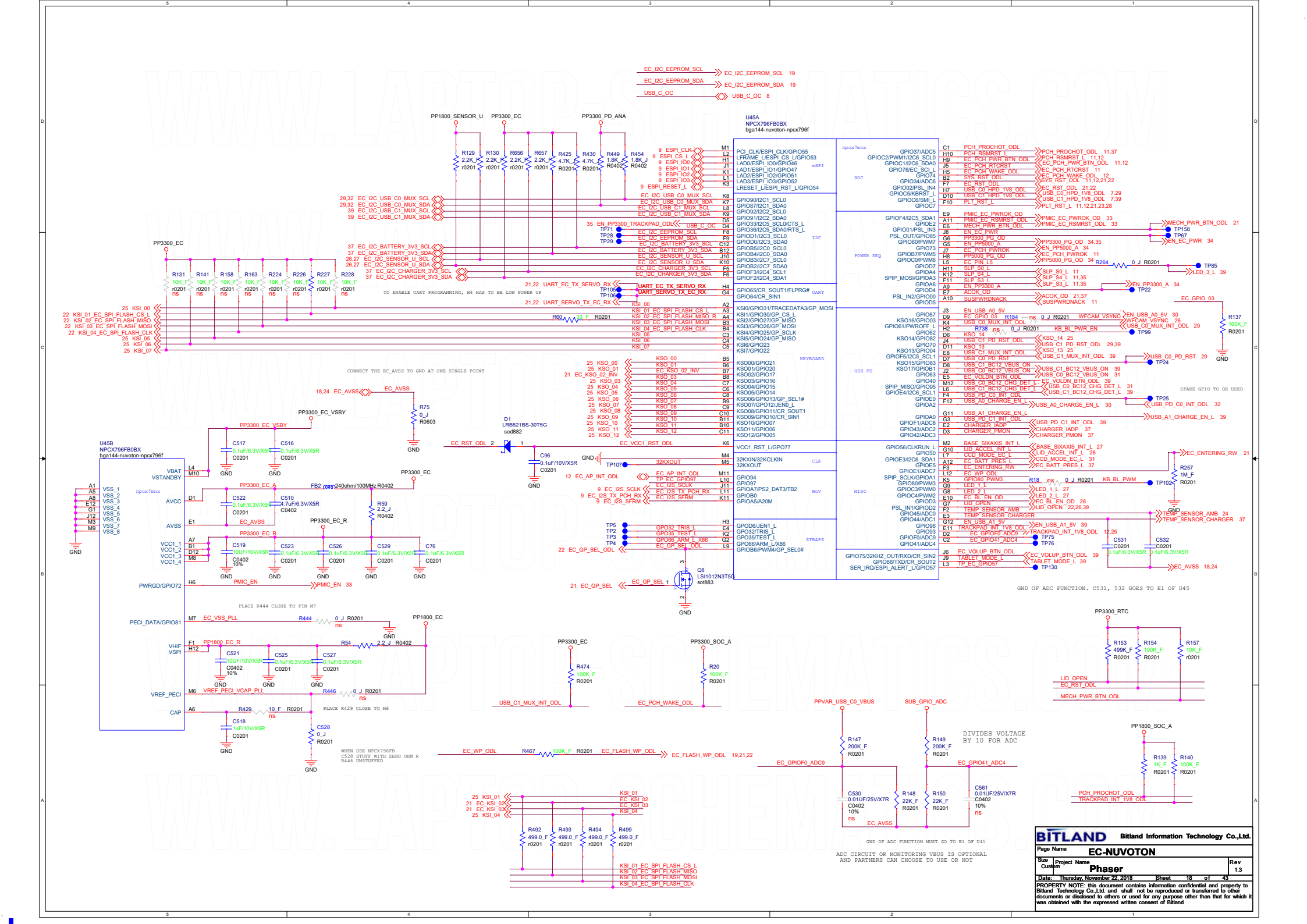
EC_I2C_EEPROM_SCL
EC_I2C_EEPROM_SDA
USB_C_OC
PP1800_SENSOR_U
PP3300_EC
PP3300_PD_ANA
U45A
NPCX796FB0BX
bga144-nuvoton-npcx796f
PP3300_EC
PP3300_EC_VSBY
PP3300_EC_A
PP3300_EC_R
PP1800_EC
U45B
NPCX796FB0BX
bga144-nuvoton-npcx796f
CONNECT THE EC_AVSS TO GND AT ONE SINGLE POINT
TO ENABLE UART PROGRAMMING, H4 HAS TO BE LOW POWER UP
PLACE R444 CLOSE TO PIN M7
PLACE R429 CLOSE TO M6
WHEN USE NPCX796FB
C528 STUFF WITH ZERO OHM R
R446 UNSTUFFED
D1
LRB521BS-30T5G
sod882
Q8
LSI1012N3T5G
sot883
PP3300_RTC
PP1800_SOC_A
PP3300_SOC_A
DIVIDES VOLTAGE
BY 10 FOR ADC
ADC CIRCUIT OR MONITORING VBUS IS OPTIONAL
AND PARTNERS CAN CHOOSE TO USE OR NOT
GND OF ADC FUNCTION MUST GO TO E1 OF U45
GND OF ADC FUNCTION. C531, 532 GOES TO E1 OF U45
SPARE GPIO TO BE USED
BITLAND
Bitland Information Technology Co.,Ltd.
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EC-NUVOTON
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Custom
Project Name
Phaser
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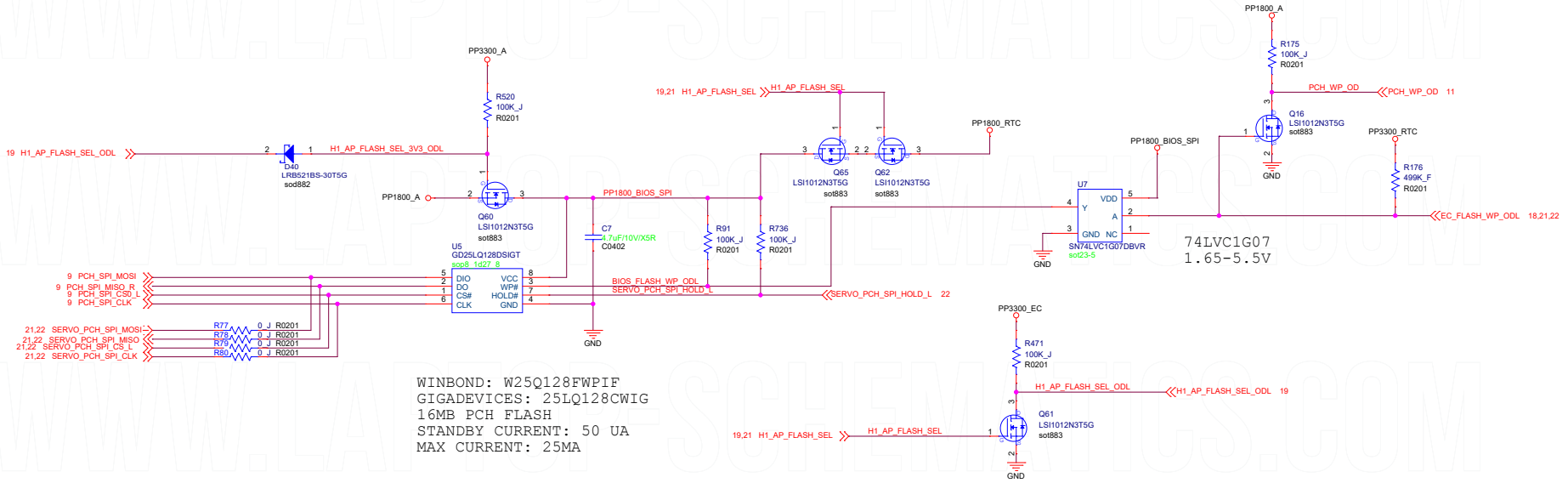
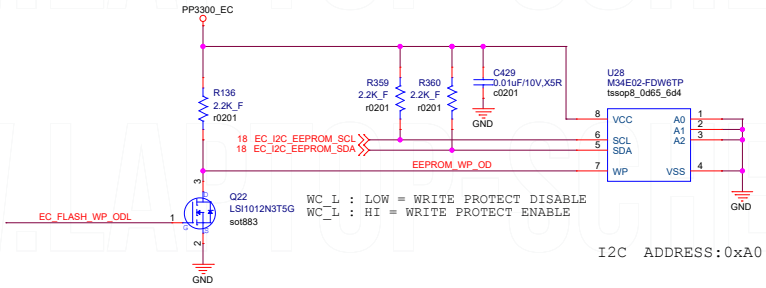
## PCH SPI FLASH




WINBOND: W25Q128FWPIF
GIGADEVICES: 25LQ128CWIG
16MB PCH FLASH
STANDBY CURRENT: 50 UA
MAX CURRENT: 25MA

## EC EEPROM




WC_L : LOW = WRITE PROTECT DISABLE
WC_L : HI = WRITE PROTECT ENABLE

I2C ADDRESS:0xA0

SKU EEPROM

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| | | |
|---|---|---|
| Page Name | SPI ROM | |
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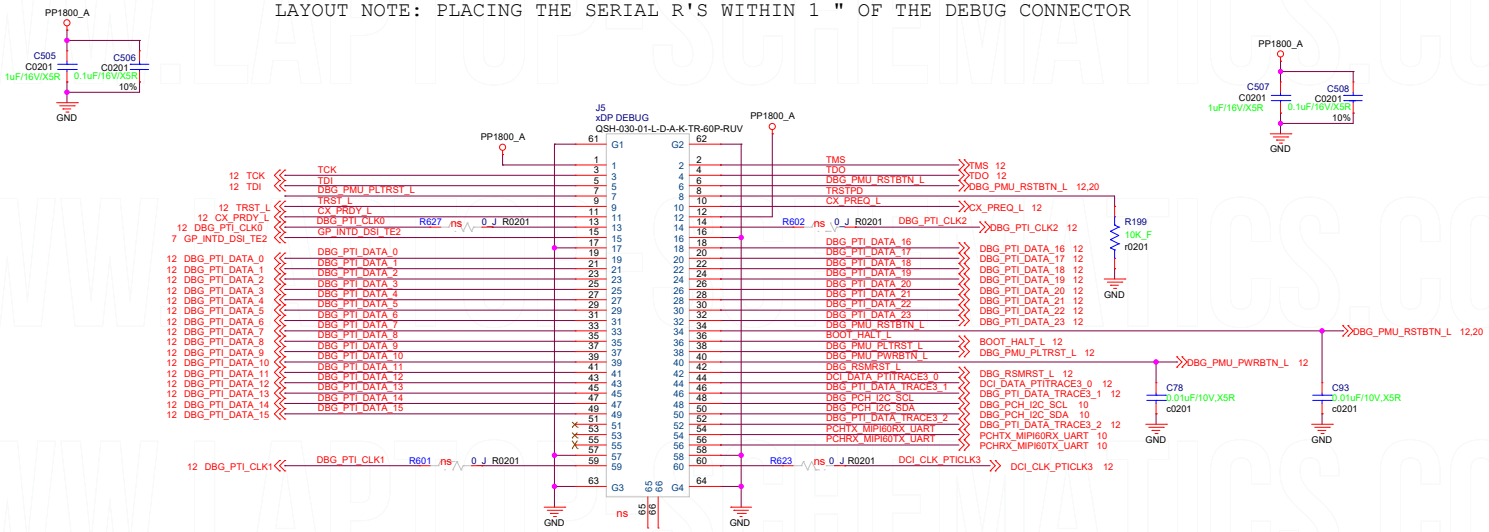
LAYOUT NOTE: PLACING THE SERIAL R'S WITHIN 1 " OF THE DEBUG CONNECTOR




PRODUCTION NOTE: DNS J5, R627, R602, R623, R601

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Page Name: MIPI60 DEBUG HEADER

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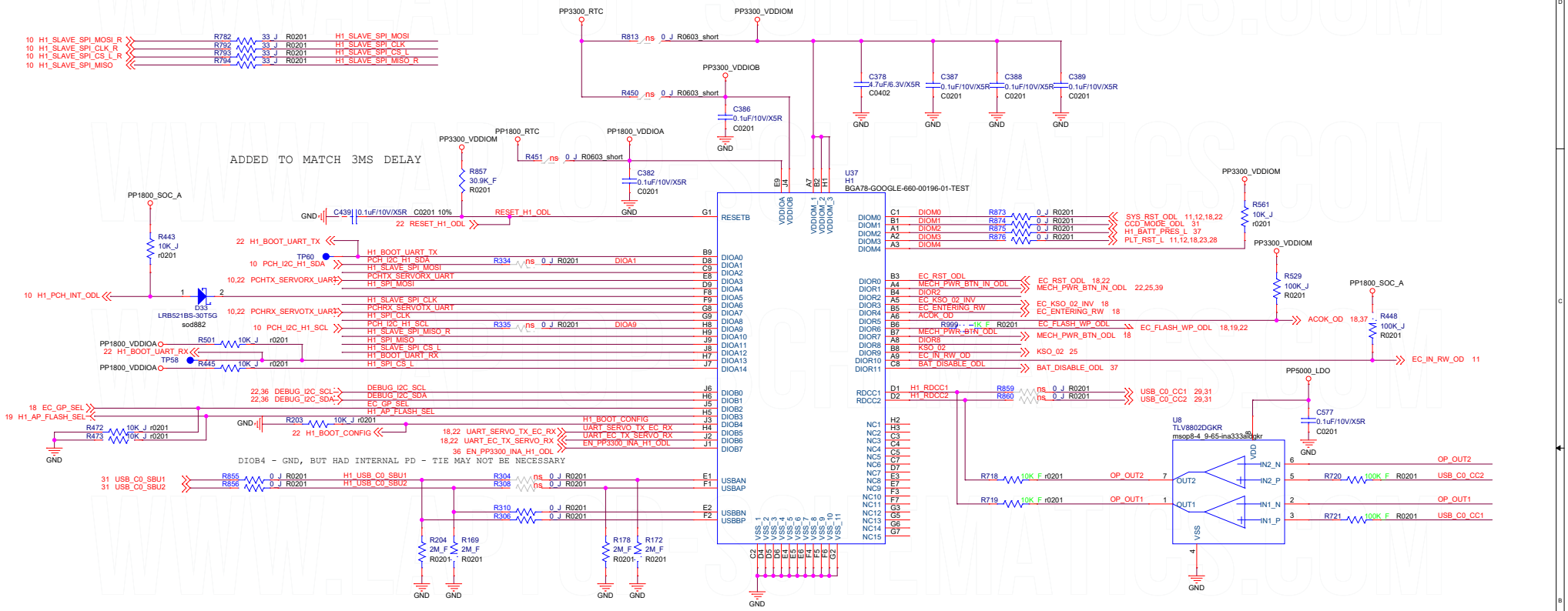
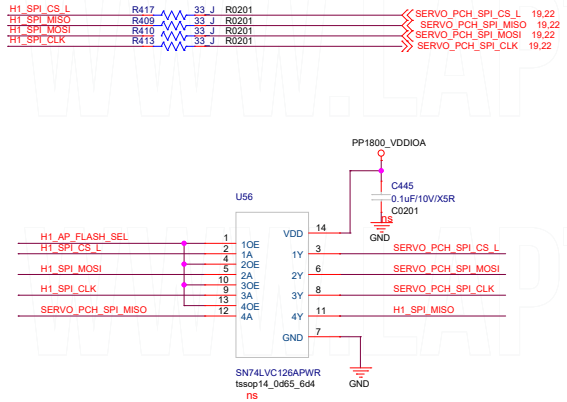
KEEP NEAR TPM/SPI ROM TO MINIMIZE SPI STUBS
PLACE TERMINATION NEAR DIVIDE

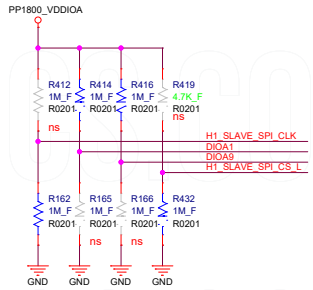
## (H1C)




FOR EC FLASH PROGRAMMING



STRAPS : SPI FOR CONVERTIBLE/CLAMPSHELL



| | | |
|---|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. | |
| Page Name | H1 SECURE MICROCONTROLLER | |
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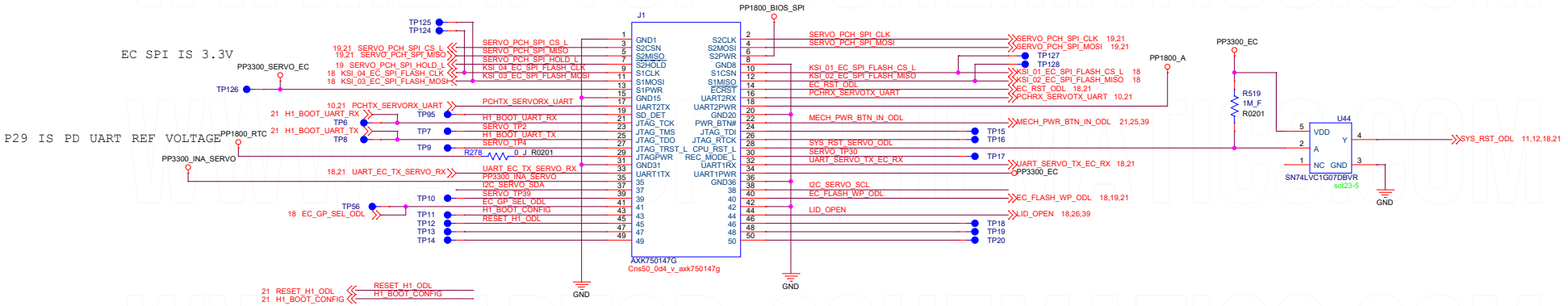
(GOG)

P18 IS PCH UART REF VOLTAGE
P34 IS EC UART REF VOLTAGE
CAN REMOVE U44, R519 IF J1 IS DNS

PCH SPI IS 1.8V

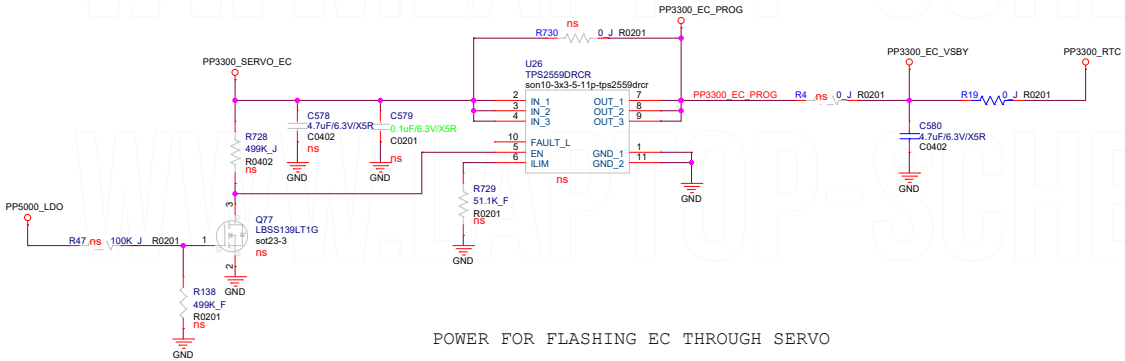
EC SPI IS 3.3V

P29 IS PD UART REF VOLTAGE



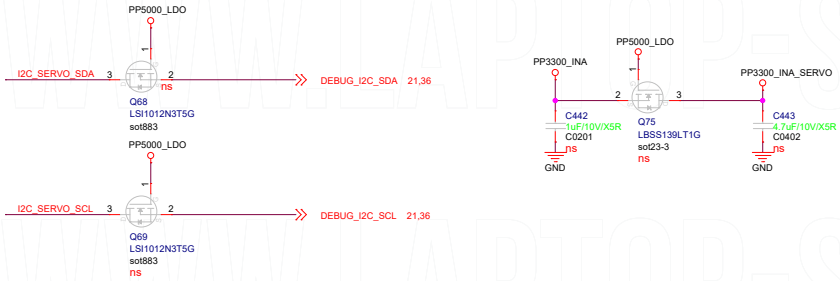

## SERVO HEADER

CAN REMOVE U44, U26, Q77, C578, C579, R128, R47, R138 R519 IF J1 IS DNS



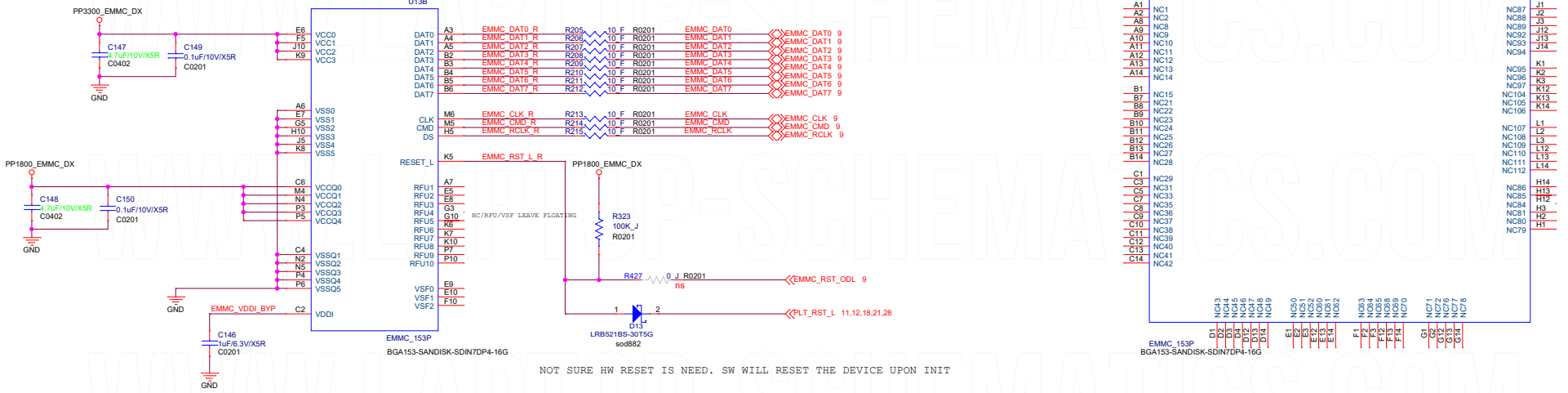

POWER FOR FLASHING EC THROUGH SERVO

CAN REMOVE Q68, Q69 IF J1 IS DNS



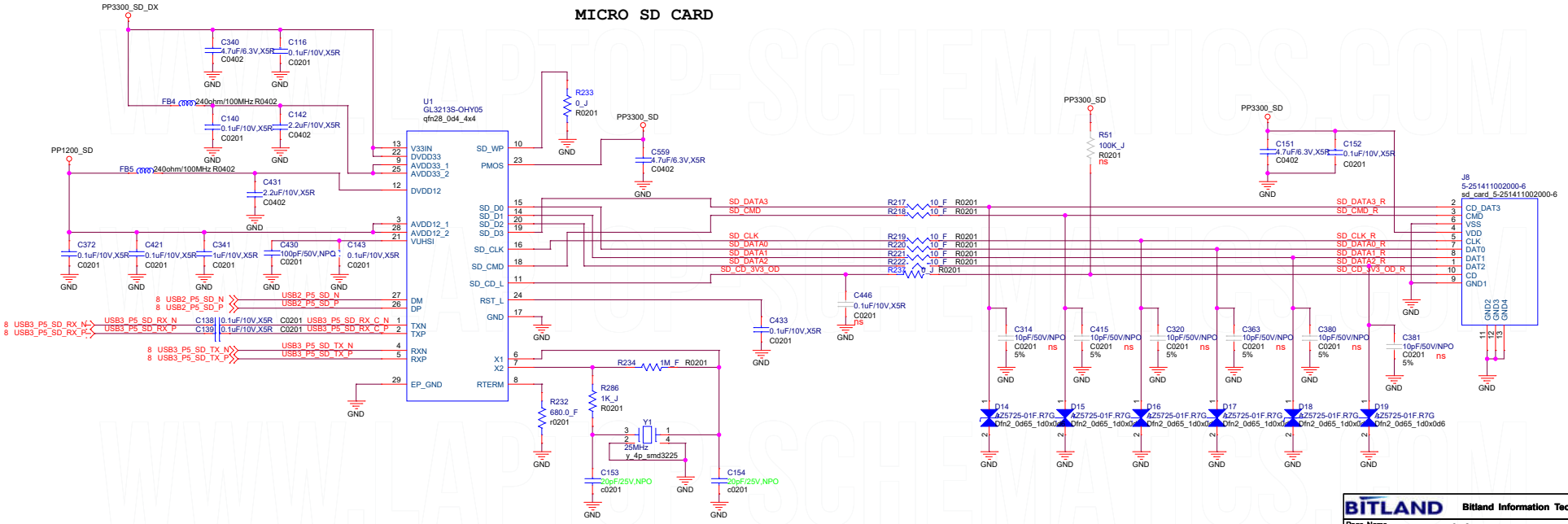
# 32 GB EMMC STORAGE

150 UA SLEEP CURRENT




NOT SURE HW RESET IS NEED. SW WILL RESET THE DEVICE UPON INIT

## MICRO SD CARD




| | |
|---|---|
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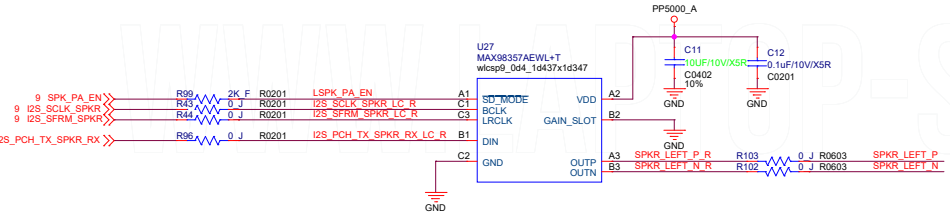
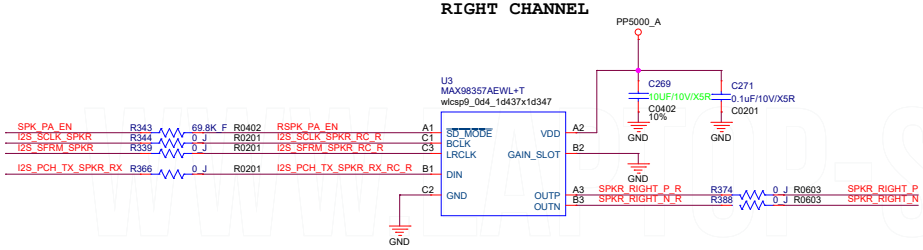
## (AMP)

### LEFT CHANNEL



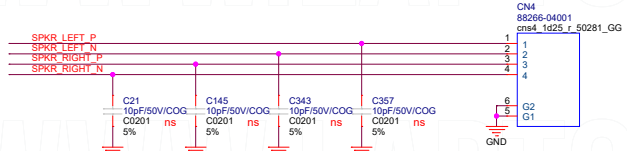

LEFT CHANNEL = SHORT (OR 2K FOR SAFETY) TO 1.8V
GAIN_SLOT: 100K TO GND = 15 DB GAIN
GAIN_SLOT: UNCONNECTED = 9 DB GAIN
GAIN_SLOT: 0 TO VDD = 6 DB GAIN
GAIN_SLOT: 0 TO GND = 12 DB GAIN
GAIN_SLOT: 100K TO VDD = 3 DB GAIN

### RIGHT CHANNEL

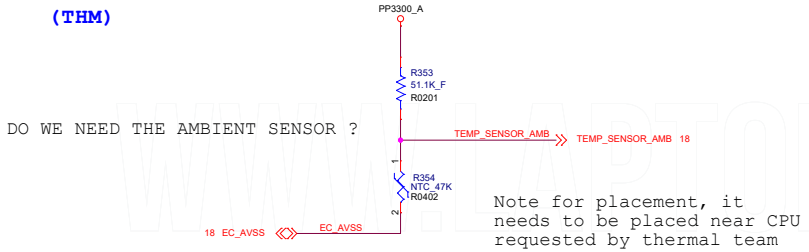



RIGHT CHANNEL = 69.8K TO 1.8V
GAIN_SLOT: GND = 12 DB GAIN

## (ADO)




## (THM)



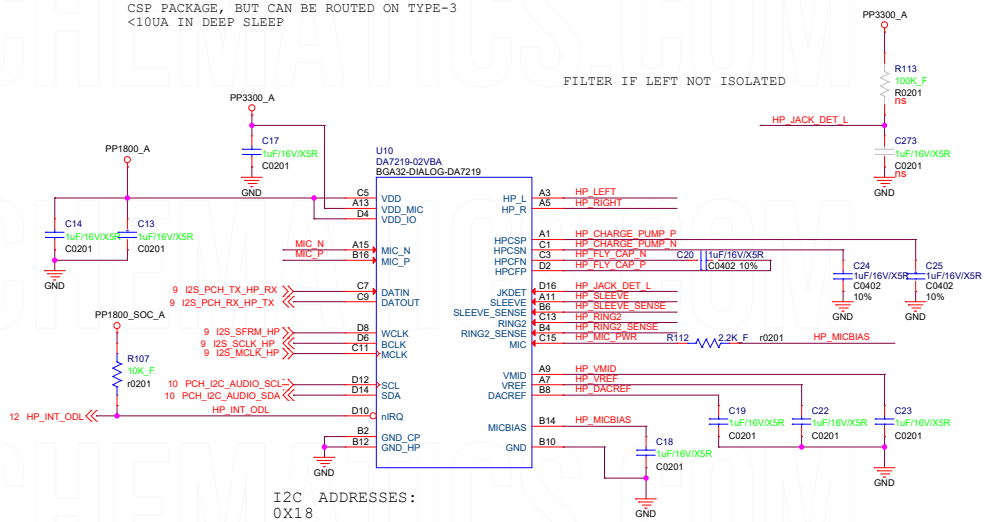

DO WE NEED THE AMBIENT SENSOR ?

Note for placement, it needs to be placed near CPU requested by thermal team

## (AMP)

CSP PACKAGE, BUT CAN BE ROUTED ON TYPE-3 <10UA IN DEEP SLEEP

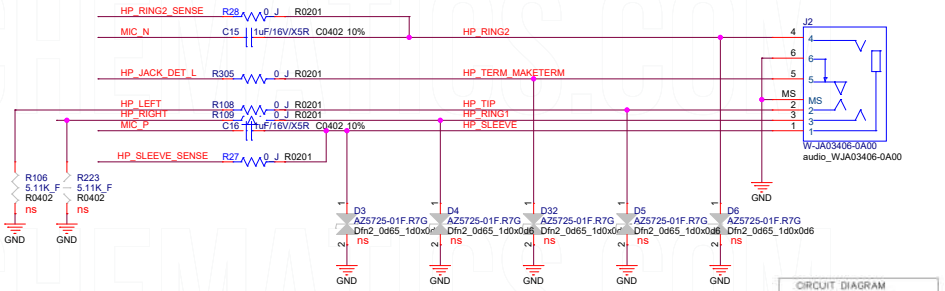
FILTER IF LEFT NOT ISOLATED

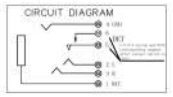



I2C ADDRESSES:
0X18
0X19
0X1A (DEFAULT)
0X1B

## (ADO)

5K TO FILTER LEFT IF NOT ISOLATED




CHANGED MIC SERIES CAPS TO 1UF TO MATCH 10HZ 3DB
FREQUENCY RECOMMENDED IN THE DA7219 DATASHEET

THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL
THE SAME APPLIES TO HP SLEEVE AND HP SLEEVE SENSE SIGNALS
ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

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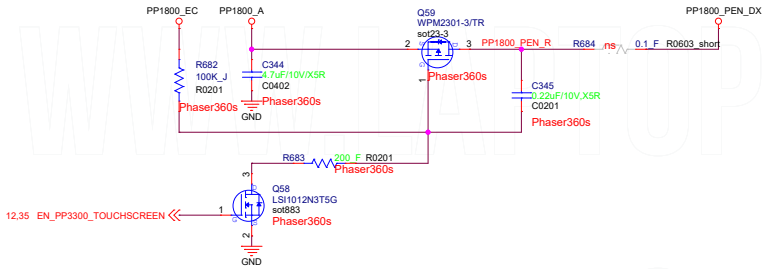
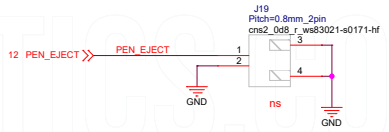
## TOUCHSCREEN AND PEN/STYLUS POWER TOGETHER

TOUCHSCREEN + STYLUS ( IF AVAILABLE )




**PEN/STYLUS CONNECTOR (MOVE TO PAGE26)**

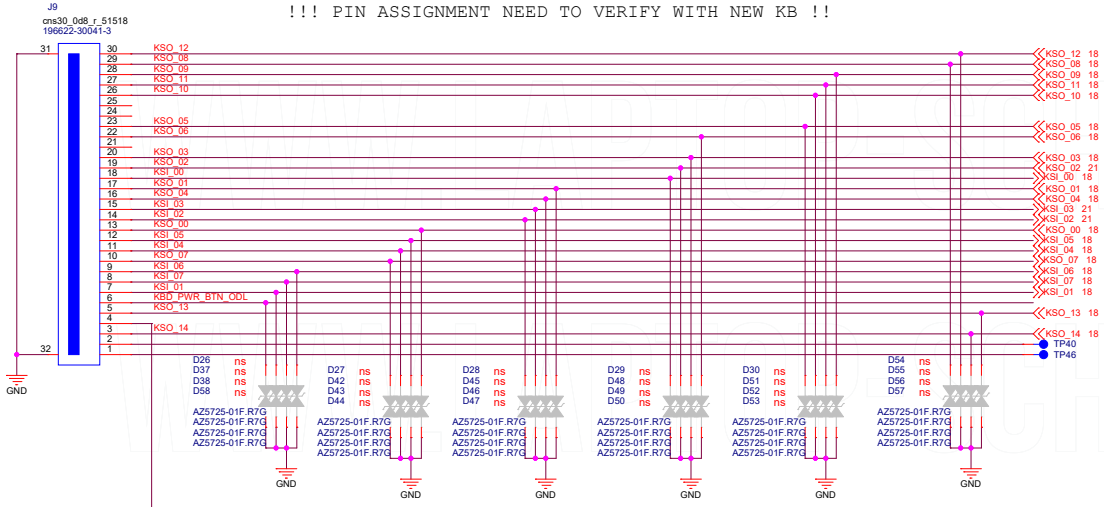



PEN_EJECT FOR GARAGED STYLUS. IT WILL BE A WAKE SOURCE

## KEYBOARD

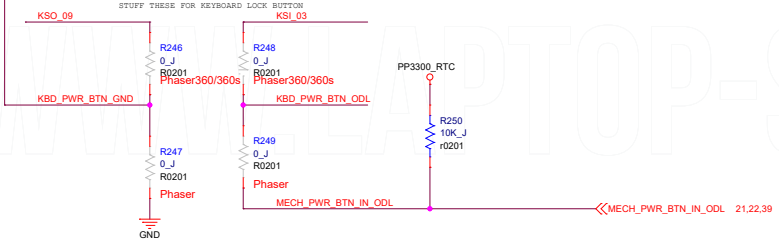
ADDED KSO13,14 FOR THE NUMPAD
CM TO CHOOSE CONNECTOR- THIS ONE WILL SUPPORT THE KEYPAD SO THE PINOUT MAY NEED TO CHANGE

!!! PIN ASSIGNMENT NEED TO VERIFY WITH NEW KB !!



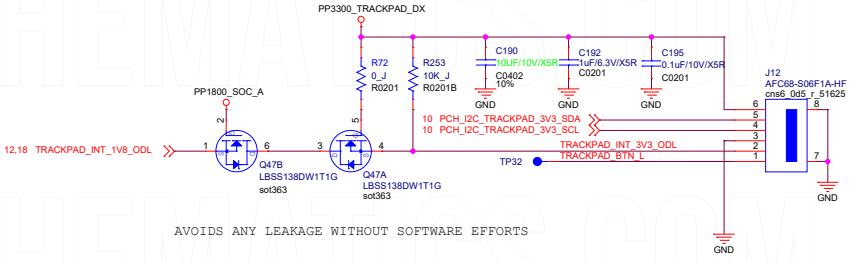

## KEYBOARD BACKLIGHT CONN

STUFF THESE FOR KEYBOARD LOCK BUTTON




## TRACKPAD CONNECTOR

CM TO CHOOSE CONNECTOR




THE PURPOSE OF THIS CIRCUIT IS TO ALLOW A SINGLE KEYBOARD MATRIX FOR BOTH A CONVERTIBLE AND CLAMSHELL SKU

STUFF THESE FOR KEYBOARD POWER BUTTON

AVOIDS ANY LEAKAGE WITHOUT SOFTWARE EFFORTS

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| | | |
|---|---|---|
| Page Name | KB, TPD | |
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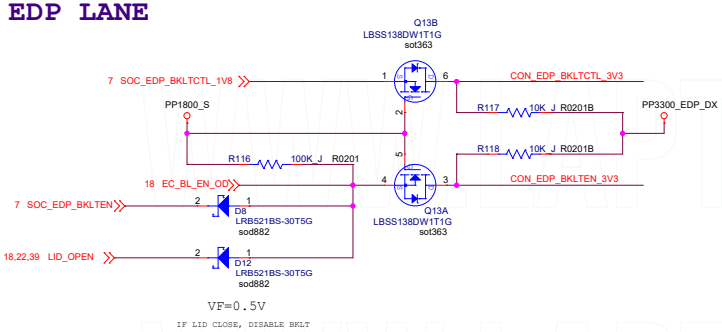
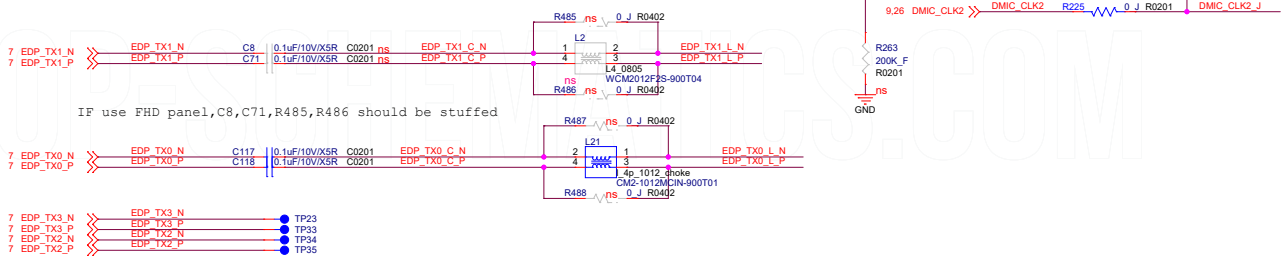
## EDP LANE

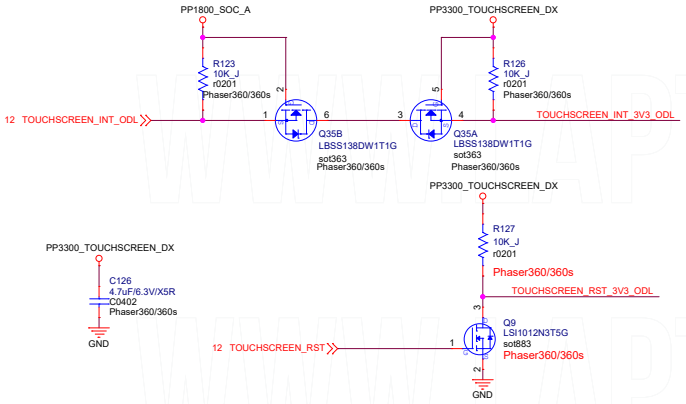



EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR

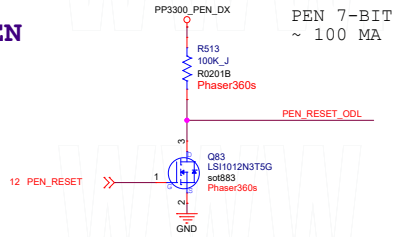



## LID ACCEL-CORAL (MOVE TO PAGE40)

## TOUCHSCREEN




## PEN

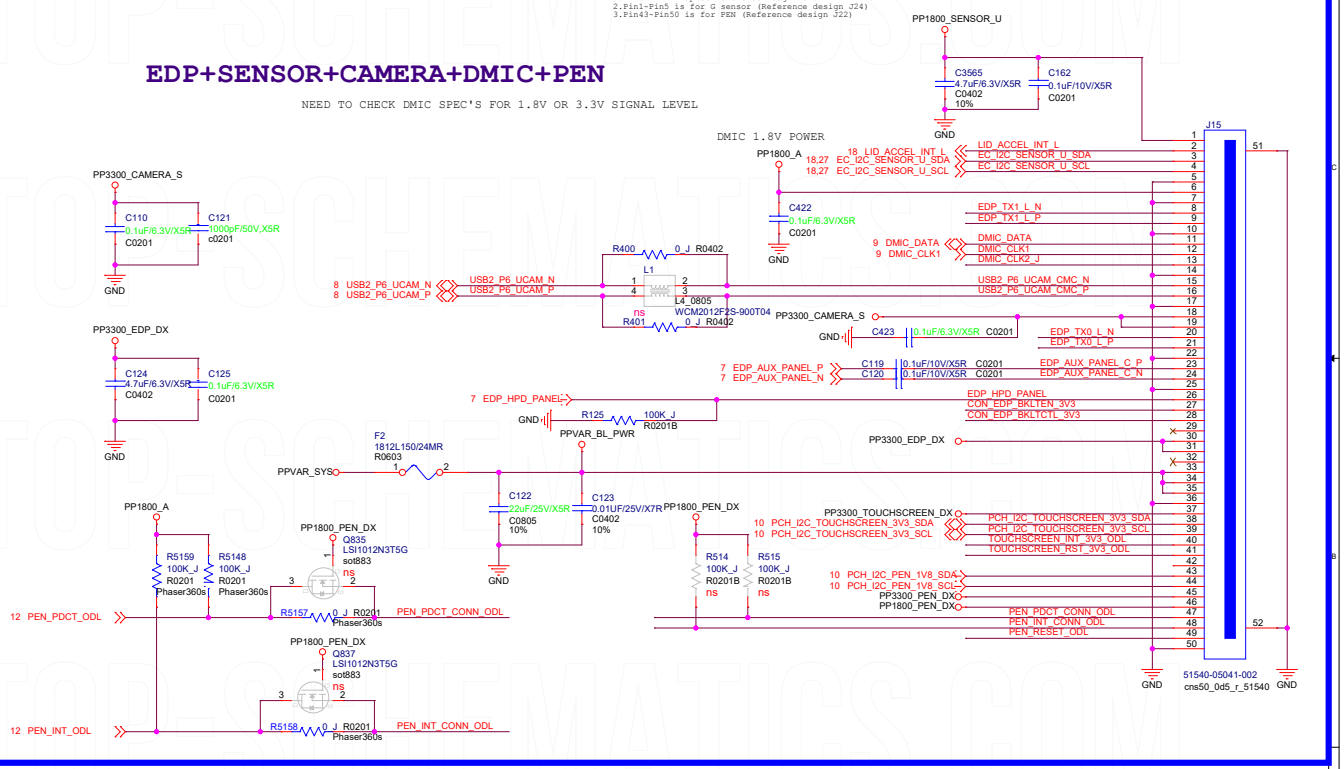



## EDP+SENSOR+CAMERA+DMIC+PEN

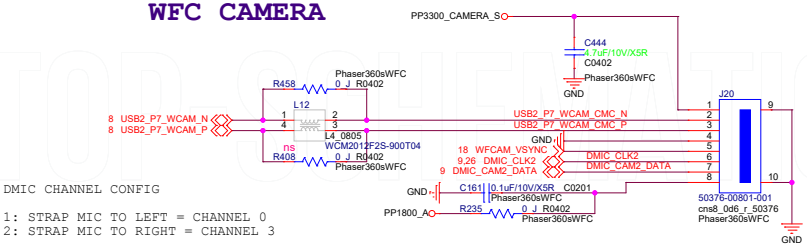
NOTE:
1.Pin6~Pin42 map to Reference Desgin J15 Pin1~Pin40
2.Pin1~Pin5 is for G sensor (Reference design J24)
3.Pin43~Pin50 is for PEN (Reference design J22)

NEED TO CHECK DMIC SPEC'S FOR 1.8V OR 3.3V SIGNAL LEVEL

DMIC 1.8V POWER




## WFC CAMERA




PREFERRED DMIC CHANNEL CONFIG

INTERFACE 1: STRAP MIC TO LEFT = CHANNEL 0
INTERFACE 2: STRAP MIC TO RIGHT = CHANNEL 3

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Page Name: LID: eDP, CAM, TOUCH, SENSOR

Size: C | Project Name: Phaser | Rev: 1.3

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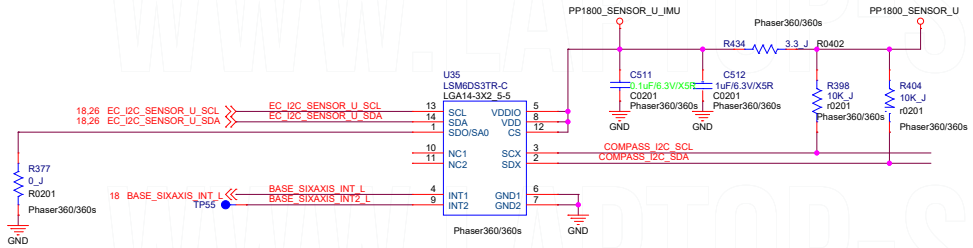
IMU WILL NOT BE STUFFED IF WFCAM IS STUFFED




## IMU (6-AXIS)

MODE 2 (SLAVE TO EC, MASTER TO MAG)

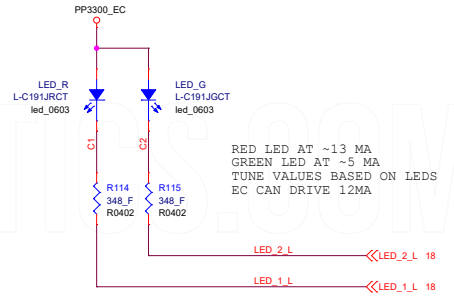
I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 0X6A (LSB SET BY SD0/SA0)

For Phaser no need Magnetometer, remove it----0426

## GMR SENSOR MOVED TO PAGE39

## CHARGE/BATTERY LED

Change LED color from orange/blue to red/green.
LED_1_L controls LED_RED and LED_2_L controls LED_GREEN.
This is the same as robo.

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Page Name: SENSOR: COMPASS, GYRO (OPTION 1)

Size: C | Project Name: Phaser | Rev: 1.3

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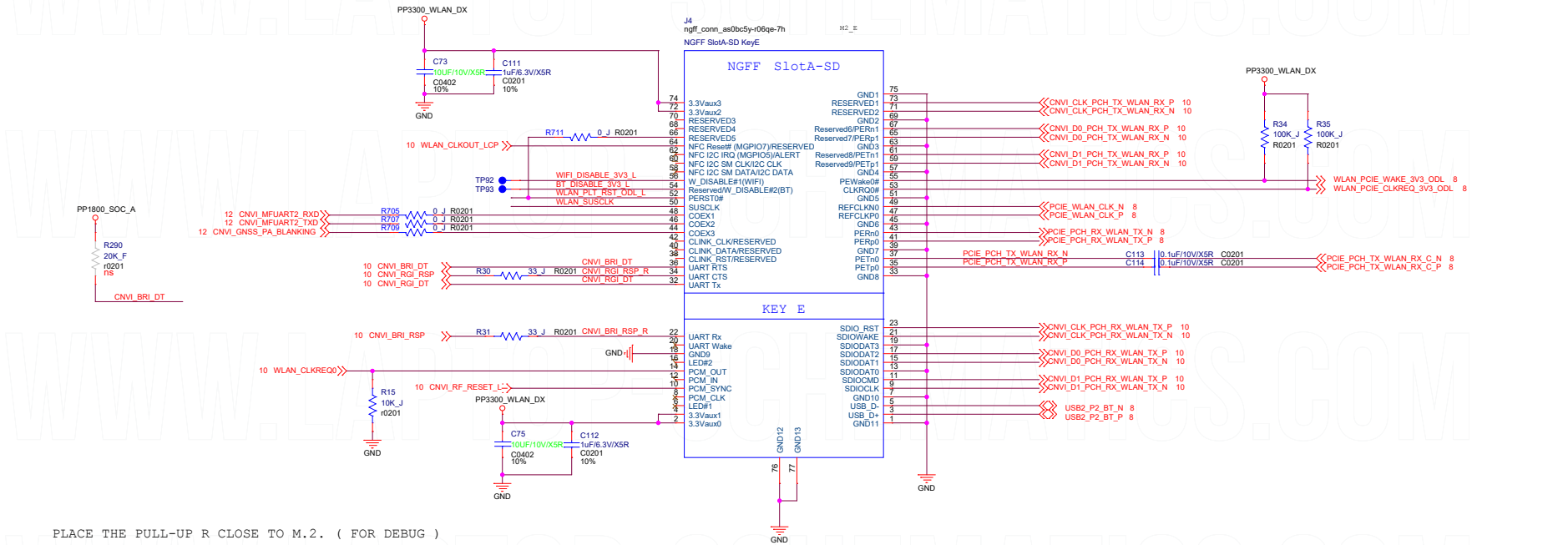
# WIFI

CM TO CHOOSE CONNECTOR

**(NGF)**




PLACE THE PULL-UP R CLOSE TO M.2. ( FOR DEBUG )

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| | | |
|---|---|---|
| Page Name | WIFI/BT CONNECTOR | |
| Size C | Project Name Phaser | Rev 1.3 |
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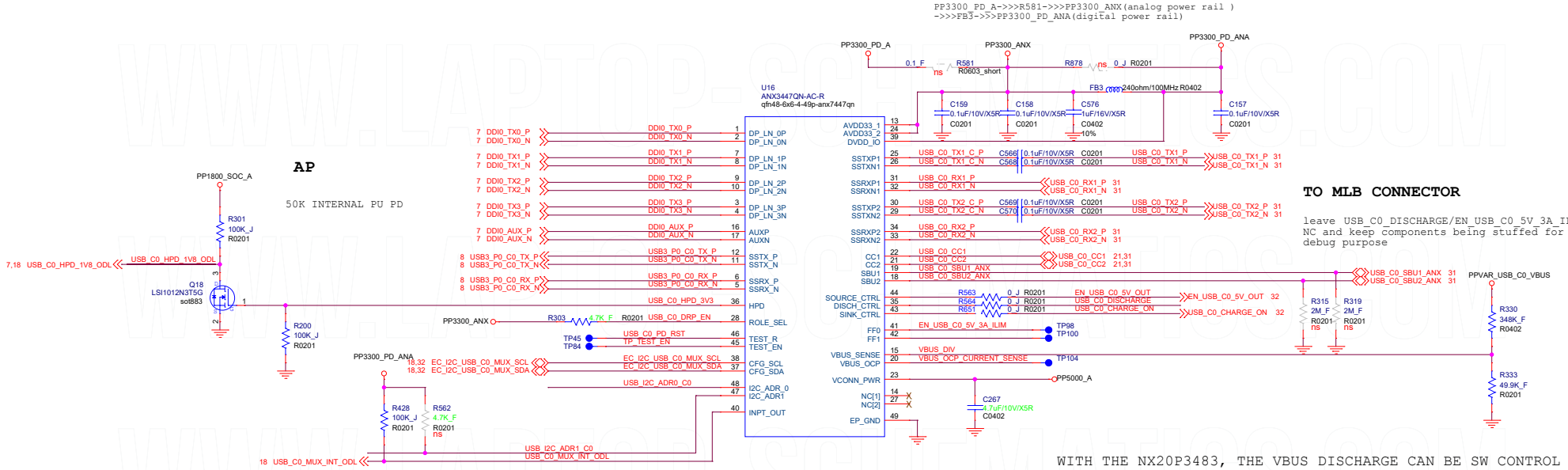
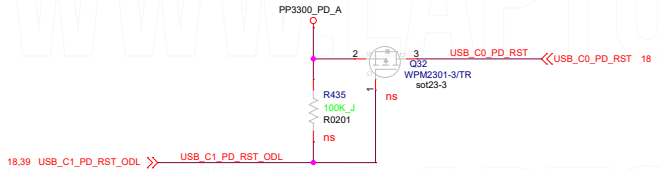
## FOR USB-C PORT 0




DEFAULT I2C ADDRESS: 0X58
IF ADR1 IS PULLED UP: 0X7C

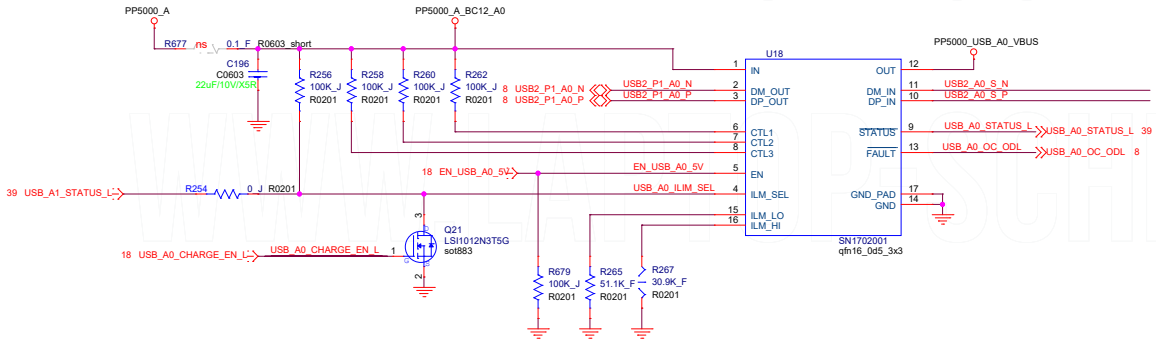
WITH THE NX20P3483, THE VBUS DISCHARGE CAN BE SW CONTROL



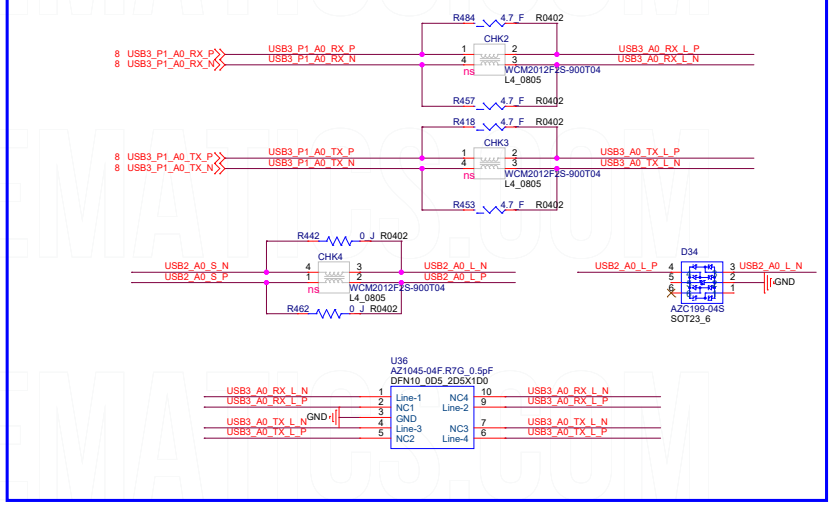

USB_C0_PD_RST IS ACTIVE HIGH WITH 100K INTERNAL PD

| | | |
|---|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. | |
| Page Name | USB C TCPC/MUX (OPTION 2) | |
| Size C | Project Name Phaser | Rev 1.3 |
| Date: Thursday, November 22, 2018 | Sheet 29 of 43 | |

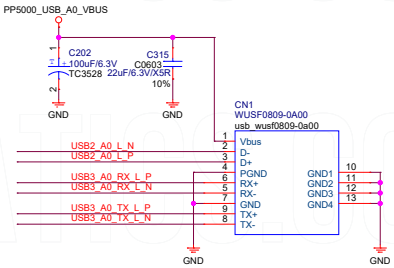
## BC 1.2 FOR THE TYPE-A PORT A0




Deviation
Change L5(PCMF3USB3S) to discrete EMI filter and ESD----0315




CM TO CHOOSE CONNECTOR

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Page Name: USB A CONNECTIONS (MLB)

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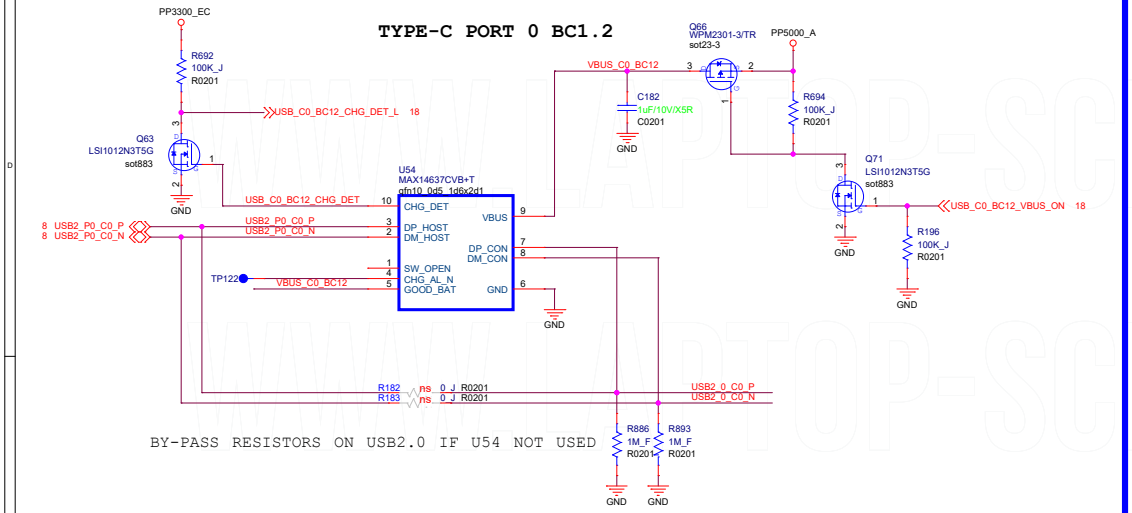
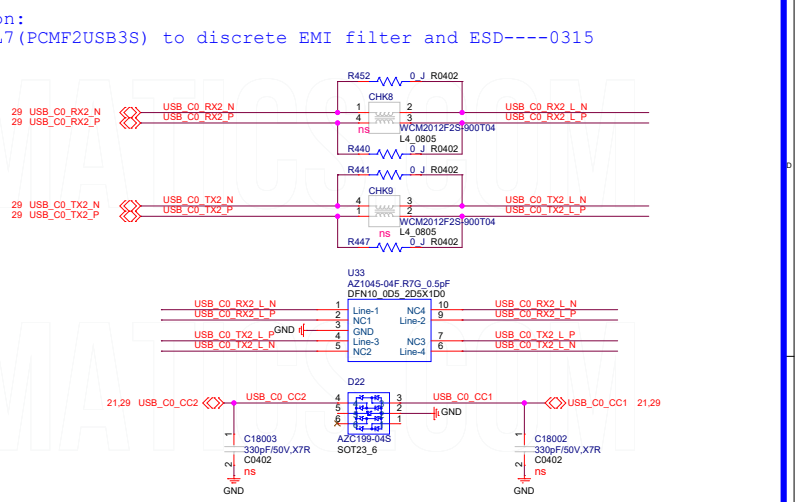
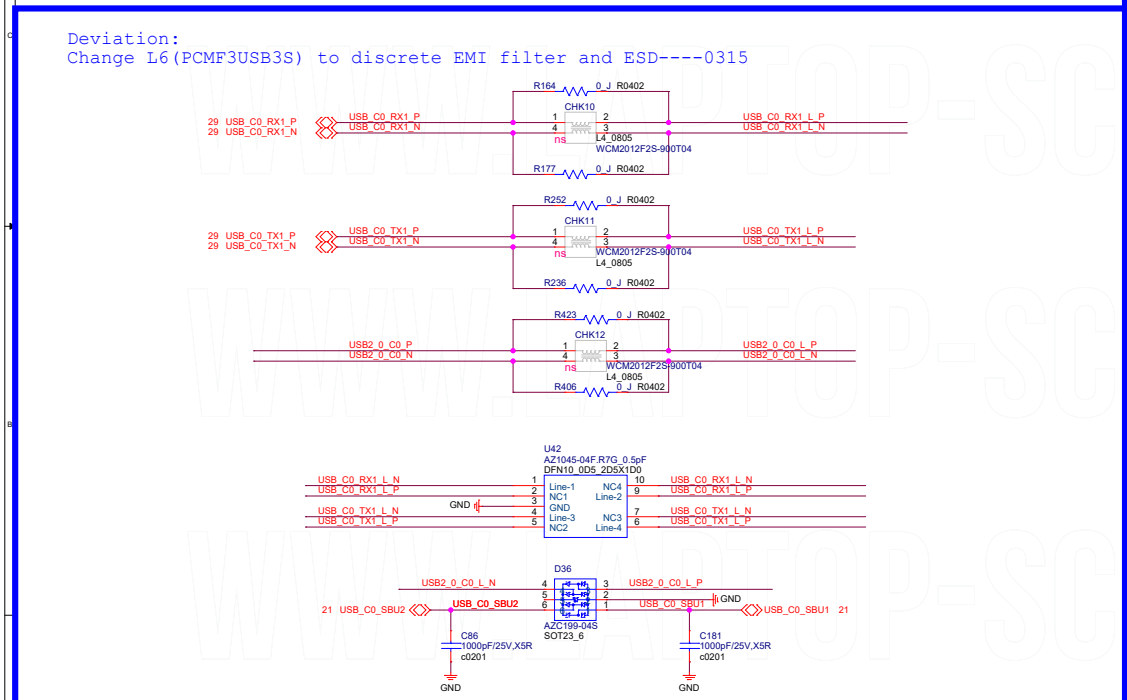
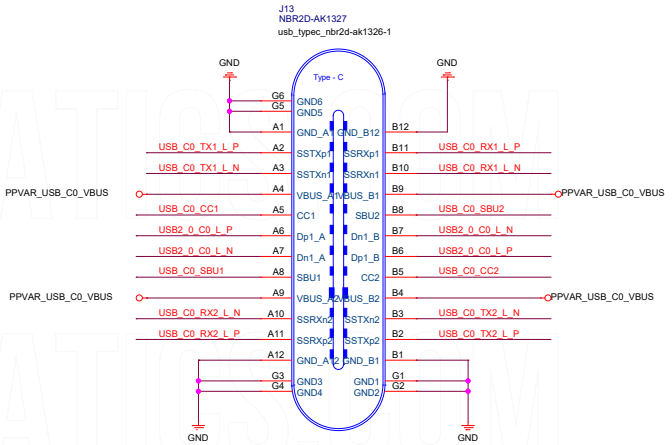
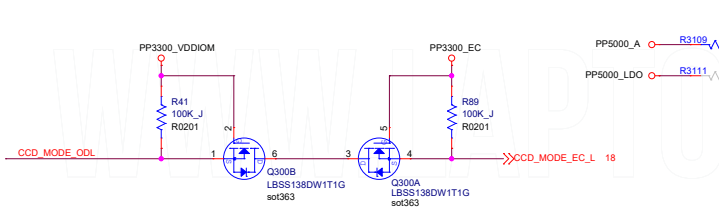


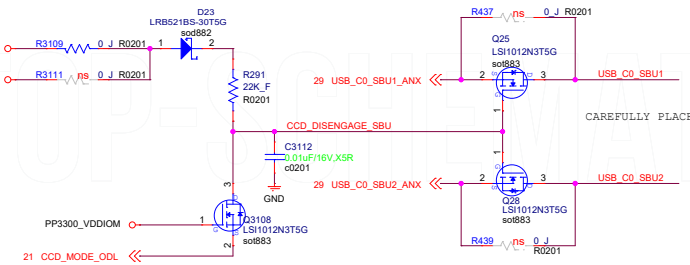




Note, for proto, stuffing maxim to TI land pattern should be ok, but for EVT, it is required to update particular footprint created for maxim's use

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| | | | |
|---|---|---|---|
| Page Name | USB C CONNECTOR ( MLB ) | | |
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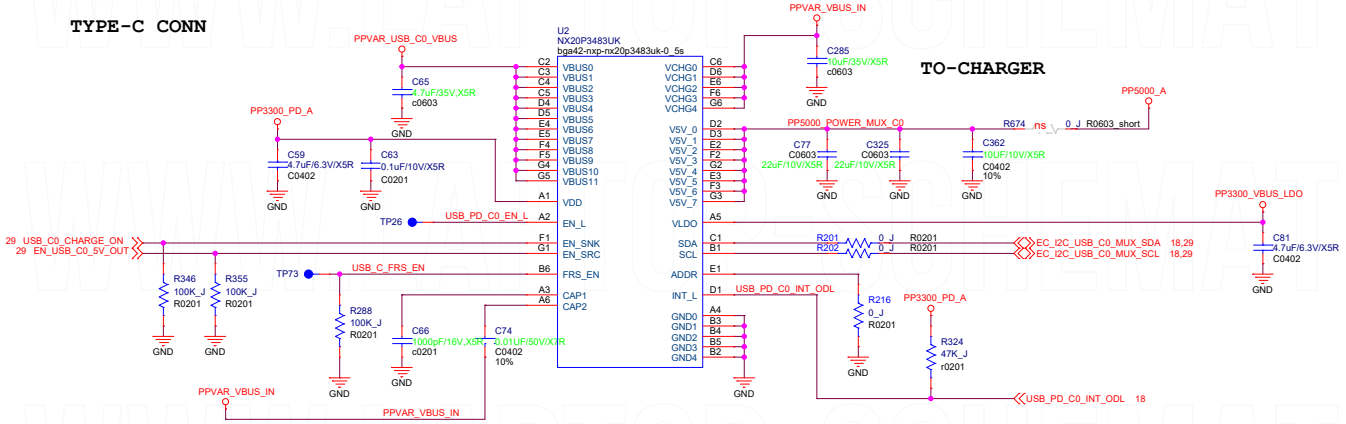
| Date: Friday, November 23, 2018 | Sheet 31 of 43 | | |

# PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR




| | | |
|---|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. | |
| Page Name | USB C VBUS CONTROL | |
| Size C | Project Name Phaser | Rev 1.3 |
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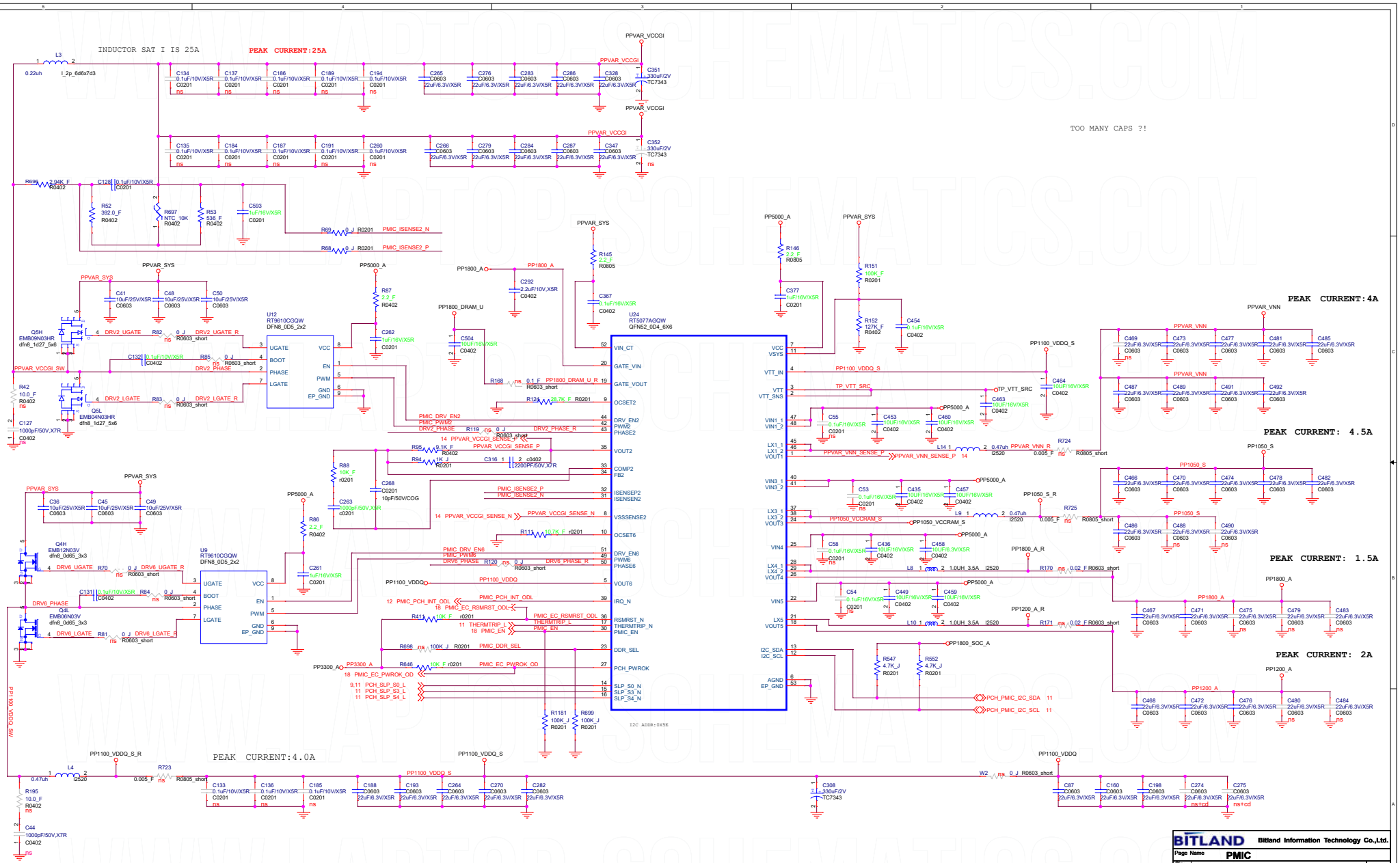
INDUCTOR SAT I IS 25A
PEAK CURRENT:25A
TOO MANY CAPS ?!
PEAK CURRENT:4A
PEAK CURRENT: 4.5A
PEAK CURRENT: 1.5A
PEAK CURRENT: 2A
PEAK CURRENT:4.0A
PPVAR_VCCGI
PPVAR_SYS
PP5000_A
PP1800_A
PP1800_DRAM_U
PPVAR_VNN
PP1050_S
PP1200_A
PP1100_VDDQ_S
PP1100_VDDQ
PP3300_A
U12 RT9610CGQW DFN8_0D5_2x2
U9 RT9610CGQW DFN8_0D5_2x2
U24 RT5077AQGW QFN62_0D4_6X6
Q5H EMB09N03HR dfn8_1d27_5x6
Q5L EMB04N03HR dfn8_1d27_5x6
Q4H EMB12N03V dfn8_0d65_3x3
Q4L EMB06N03V dfn8_0d65_3x3
I2C ADDR:0X5E
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Size Custom
Project Name Phaser
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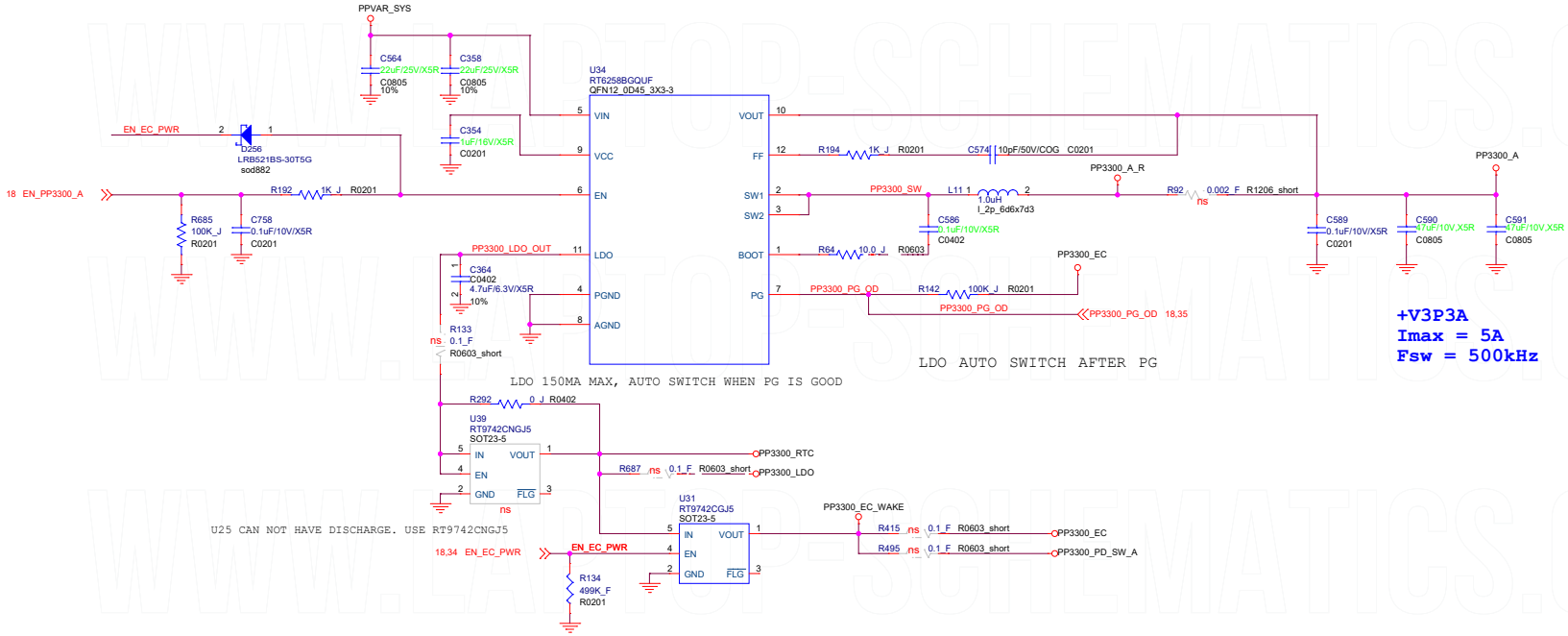
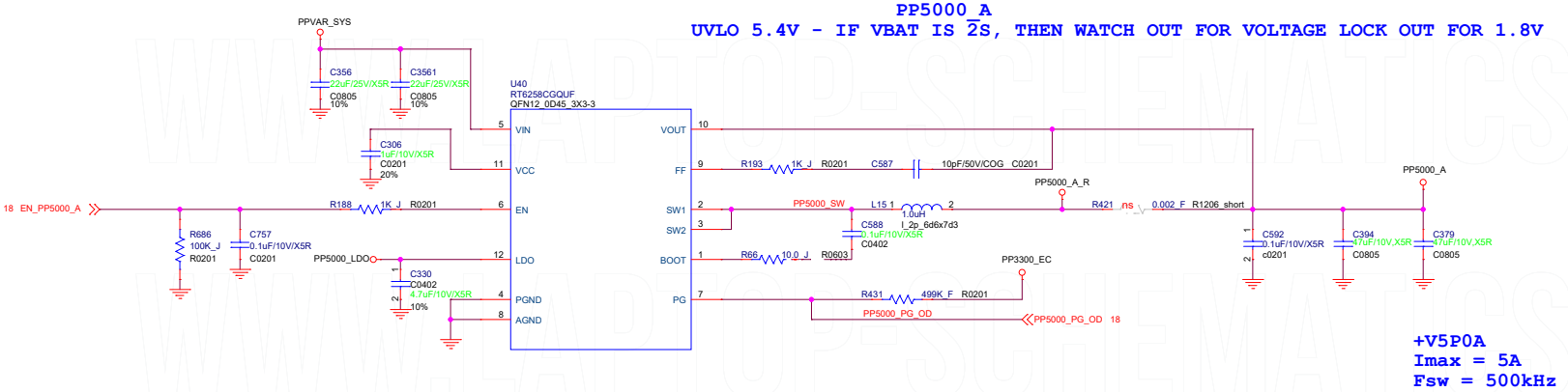
## PP3300_A
## UVLO 4.5V- IF VBAT IS 2S, THEN WATCH OUT.




## PP5000_A
## UVLO 5.4V - IF VBAT IS 2S, THEN WATCH OUT FOR VOLTAGE LOCK OUT FOR 1.8V

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Page Name: POWER:1.8V(EC) 3.3V AND 5V

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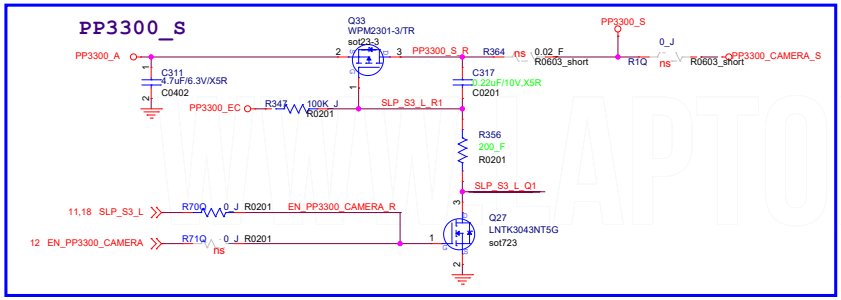
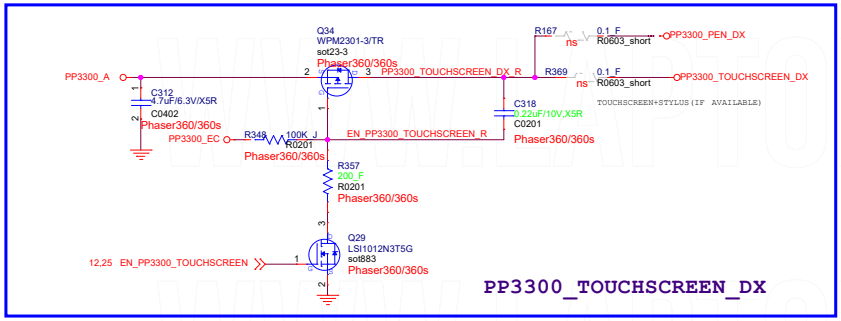
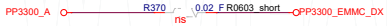
## PP3300_S



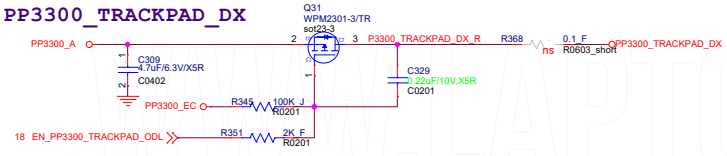

## PP3300_TOUCHSCREEN_DX




## PP3300_EMMC_DX

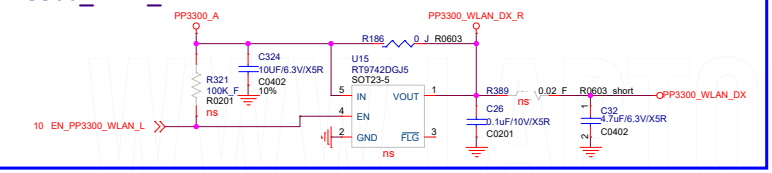



## PP3300_TRACKPAD_DX

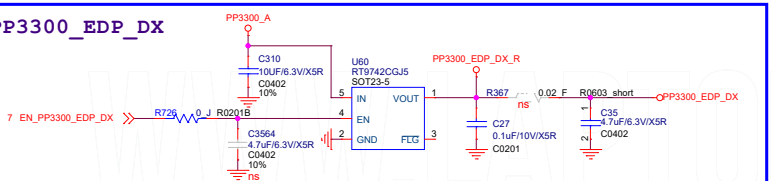



## PP3300_WLAN_DX

FOR CNVI MODULE, DNS U15 AND BYPASS WITH RESISTOR.

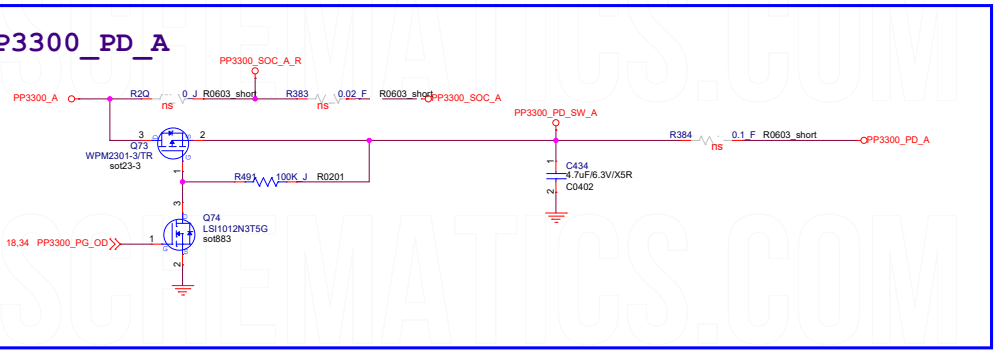



## PP3300_EDP_DX

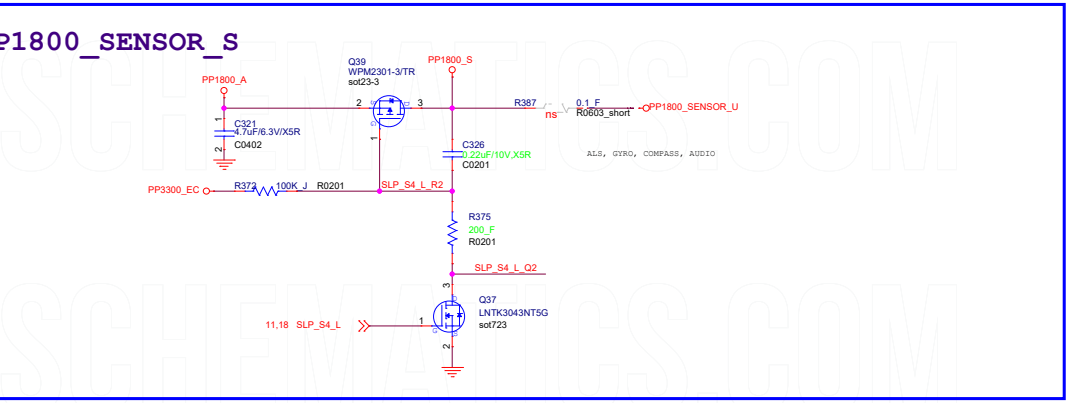



## PP3300_SD_DX


## PP3300_PD_A

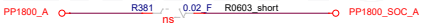



## PP1800_SENSOR_S




## PP1800_EMMC_DX


## PP1800_SOC_A

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Page Name: POWER-LOAD SWITCH

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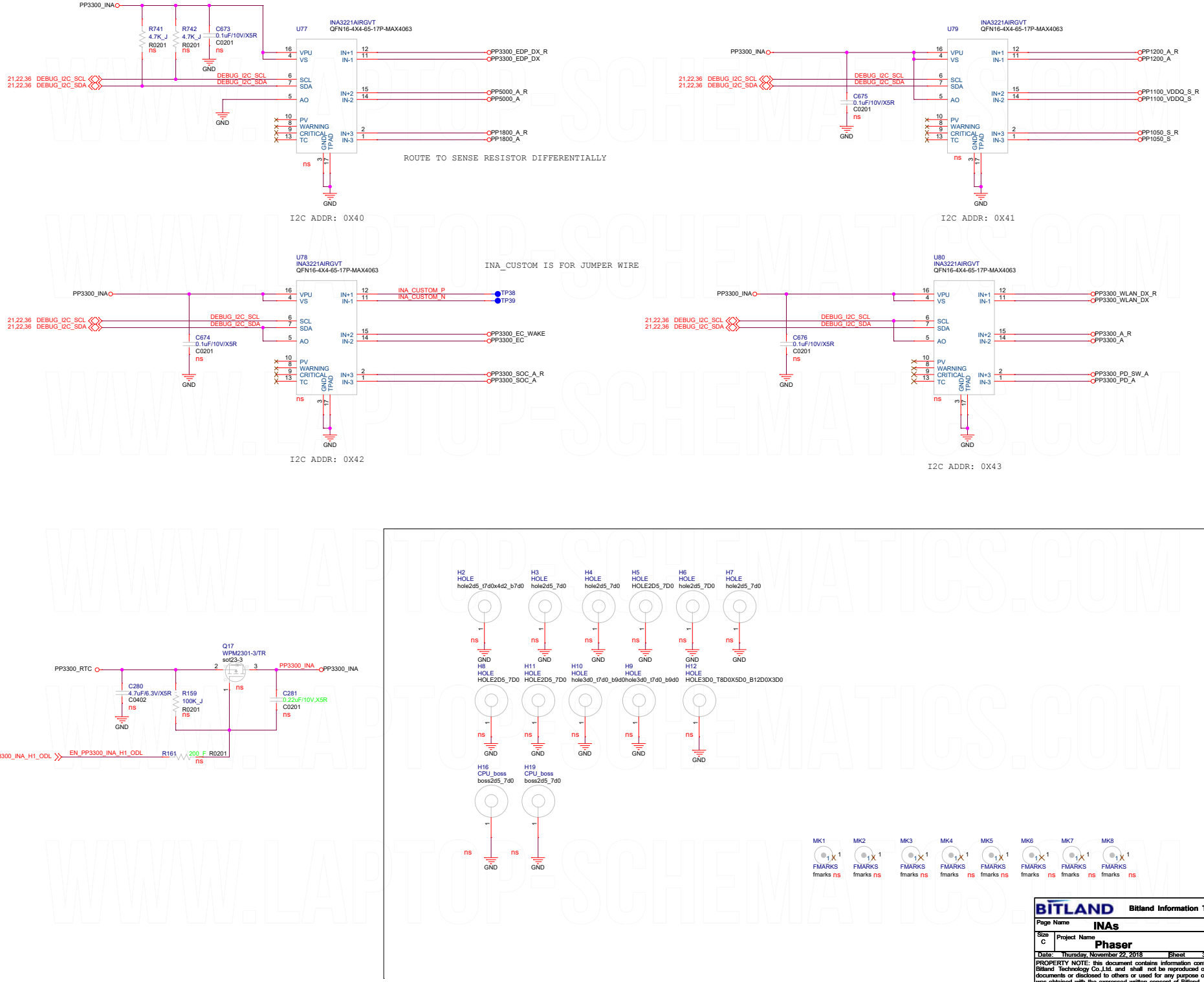


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| | | |
|---|---|---|
| Page Name | INAs | |
| Size C | Project Name Phaser | Rev 1.3 |
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INCREASE OR ADD POSCAPS IF AUDIBLE NOISE IS HEARD

RECOMMENDED VALUE FROME DATASHEET

RC SNUBBER REQUIRED?

BUCK LEG

BOOST LEG

ISL9238

ISL9238HRTZ-T QFN32_0D4_4X4

C541 GND PIN SHOULD GOES TO PIN E1 AVSS OF U45

I2C ADDR: 0X09

BATGONE LOW INDICATES BATTERY PRESENT

FOR 0.476A ADAPTER CURRENT LIMIT AND 733KHZ SWITCHING FREQUENCY:
2 CELL: 93.1K
3 CELL: 105K
3 CELL: 162K (AUTONOMOUS CHARGING)

PLACE NEAR HOTSPOT OF THE CHARGER

CV: 12.6V
3S1P Battery

| BAT_DISABLE_OD | C299 | Q55 | Q10 |
|---|---|---|---|
| FLOAT* ACTIVE LOW | STUFF DNS | STUFF DNS | DNS STUFF |

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Page Name: BATTERY CHARGER

Size C | Project Name: Phaser | Rev 1.3

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## GPIO for LTE

Coral sub board
-LTE_SAR_ODL has pullup to PP1800_DX_LTE
-LTE_OFF_OFL has pullup to PP1800_DX_LTE
-LTE_WAKE_L has pullup to PP1800_SOC_A, R773 still needs
to be stuffed if sub board is not attached

**LTE has been removed-0426**

LEVERAGING CORAL BOARD!

## STEST

**STEST has been removed-0426**

## P-SENSOR

**P-SENSOR has been removed-0426**



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Page Name: LTE, STEST

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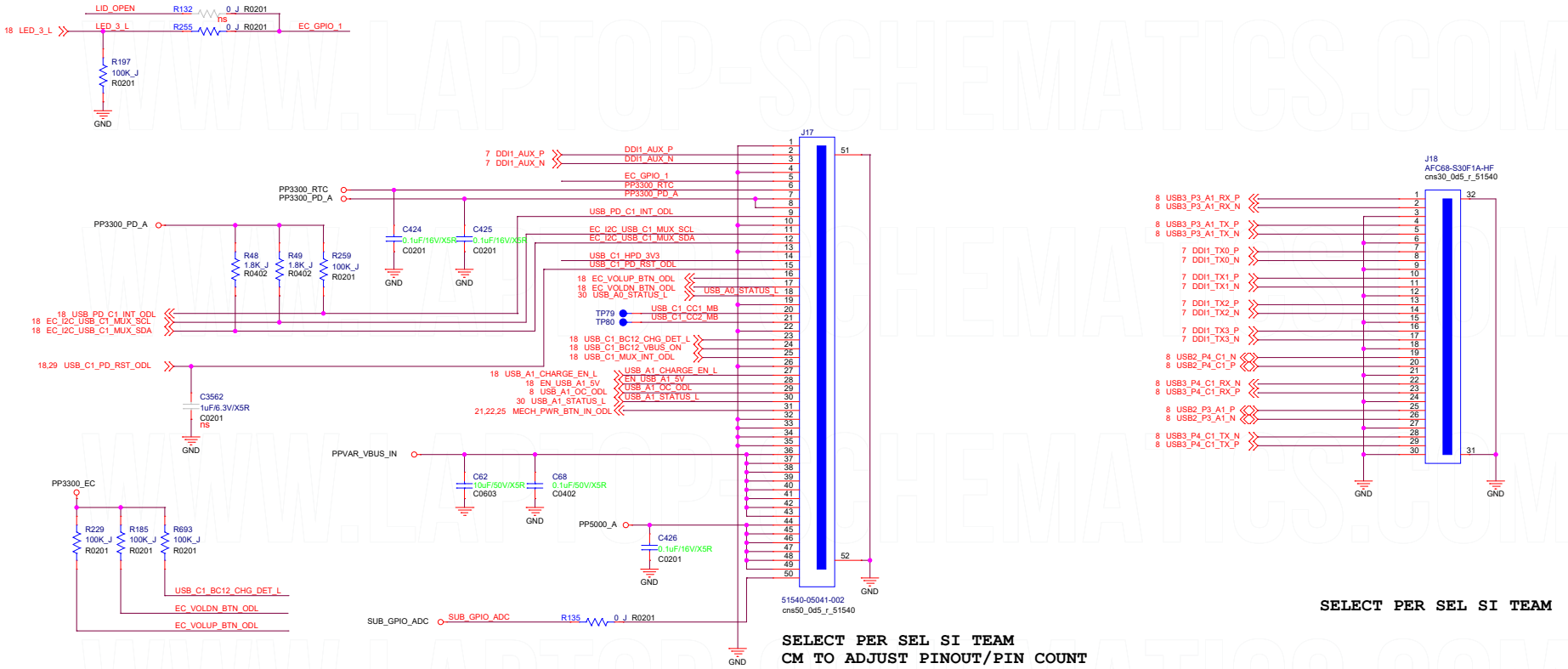
EC_GPIO_1, 2 CAN BE USED FOR CONNECTING THE GMR SENSOR ON THE SUB-BOARD
OR IT CAN BE USED TO CONNECT TO AN SPARE EC GPIO PINS FOR ADDITIONAL CONTROL FROM EC

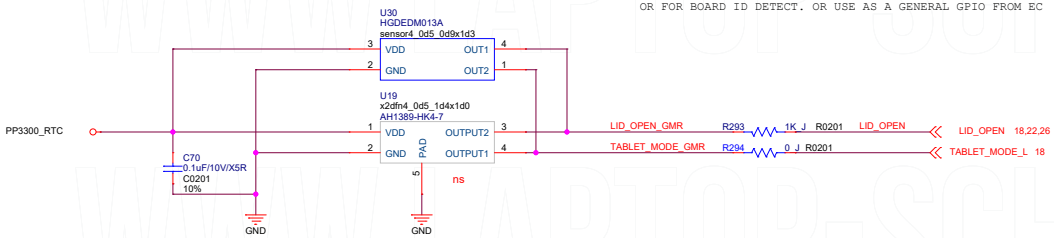


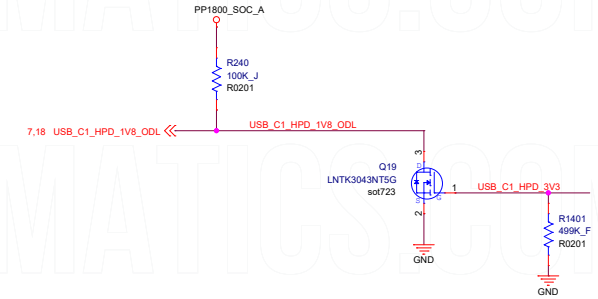

SELECT PER SEL SI TEAM
CM TO ADJUST PINOUT/PIN COUNT




SELECT PER SEL SI TEAM

SUB_GPIO_ADC GOES TO AN ADC PIN OF EC
WITH STUFFING OPTIONS, THE PIN CAN BE USED FOR VBUS DETECT
OR FOR BOARD ID DETECT. OR USE AS A GENERAL GPIO FROM EC




# MOTHER BOARD INTERFACE

| | |
|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. |
| Page Name | CONNECTORS TO SUB BOARD |
| Size C | Project Name: Phaser |
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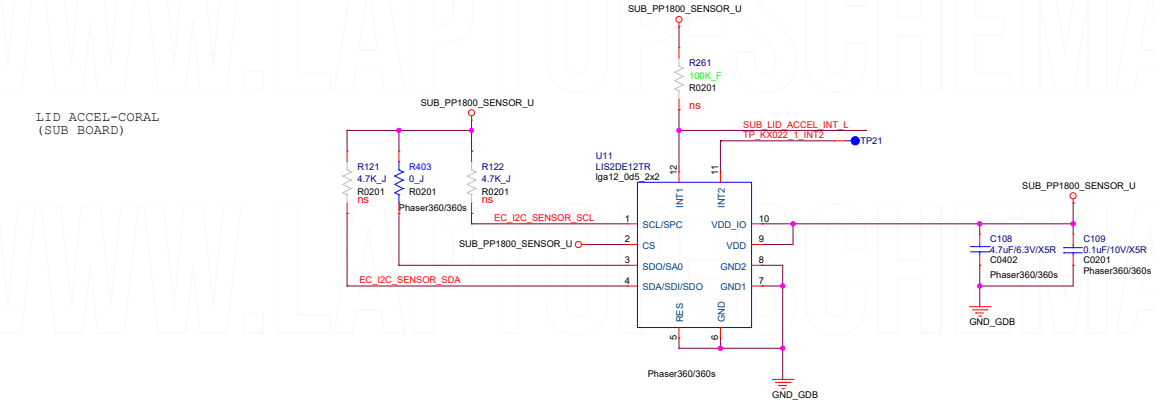
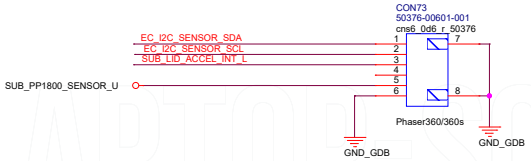



I2C MODE: ( SET BY NCS TIE TO VDDIO )
I2C ADDRESS: 0X18 (SDO_ADDR = GND), 0X1F (SDO_ADDR = VDDIO)
I2C MAX SPEED = 3.4MHZ

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| | | |
|---|---|---|
| Page Name | SUB:G sensor DB | |
| Size C | Project Name Phaser | Rev 1.3 |
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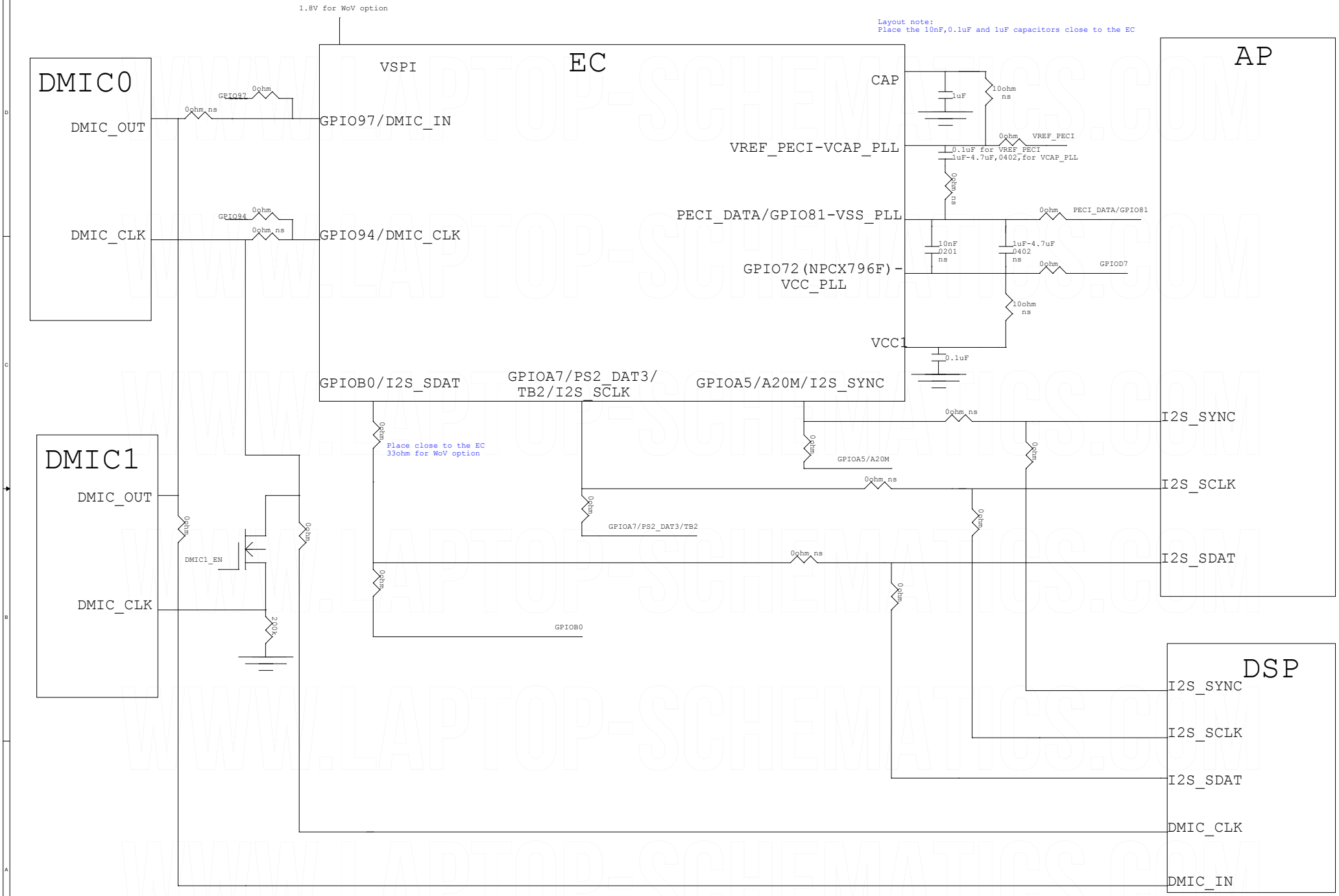




| | | |
|---|---|---|
| BITLAND | Bitland Information Technology Co.,Ltd. | |
| Page Name | WOV DIAGRAM | |
| Size C | Project Name Phaser | Rev 1.3 |
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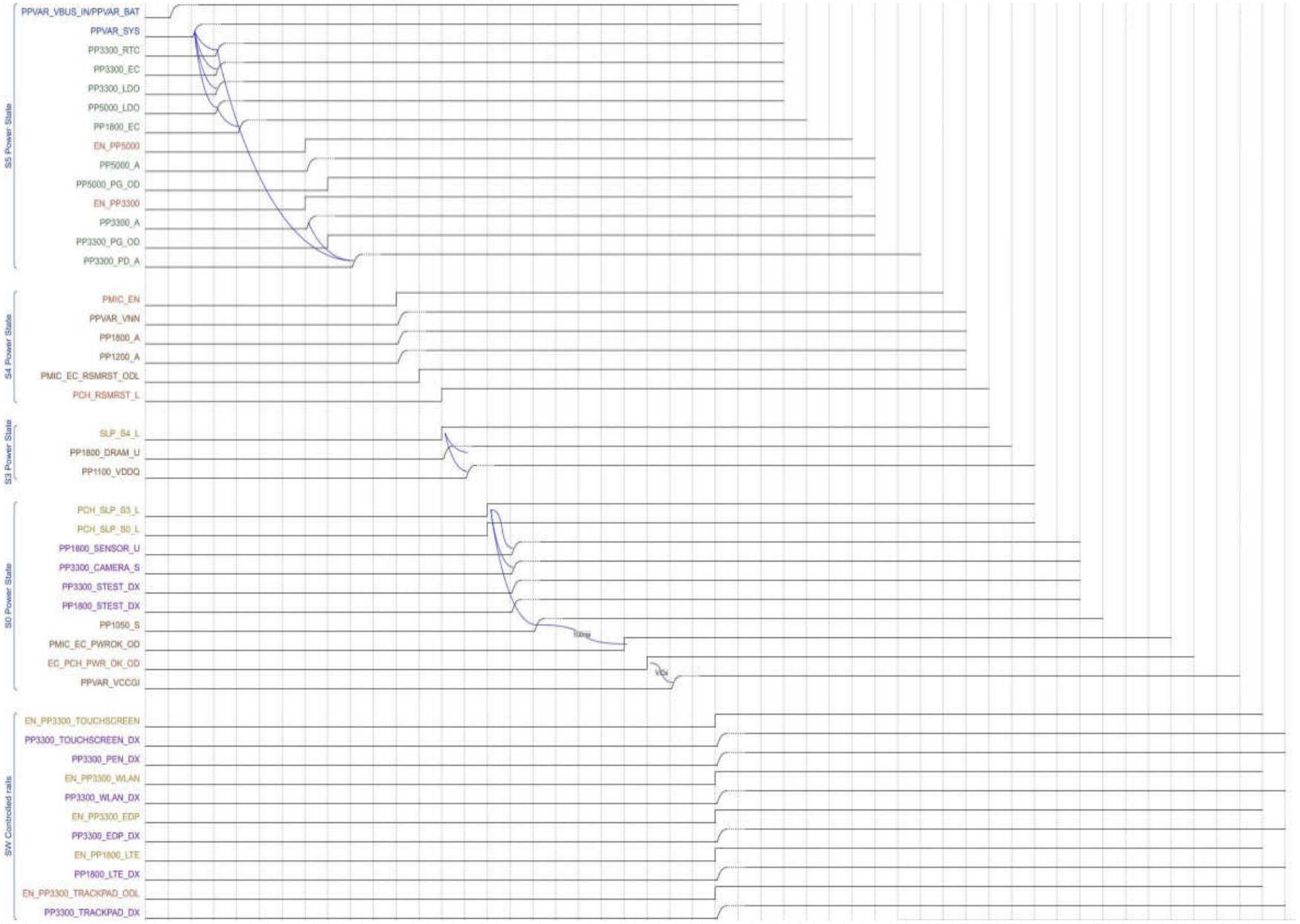




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Page Name **POWER SEQUENCE**

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| GPIO # | Bump Name | Voltage | Bootstrap Termination | Default Termination | Bootstrap Purpose | Bootstrap Usage | Bootstrap | Octopus Signal Name |
|---|---|---|---|---|---|---|---|---|
| GPIO 27 | GPIO 27 | 1.8V | 20K PU | 1K PD | Allow eMMC as a boot source | 1=enable(default)<br>0=disable | eMMC Boot | DBG_PTI_DATA_16 |
| GPIO 28 | GPIO 28 | 1.8V | 20K PU | 20K PU | Allow SPI as a boot source | 1=enable(default)<br>0=disable | SPI Boot | DBG_PTI_DATA_17 |
| GPIO 42 | MDSI_A_TE | 1.8V | 20K PD | 20K PD | Flash Descriptor override | 1=Override<br>0=No Override(default) | Flash Descriptor | TP_WIFI_RST_N,TP135 |
| GPIO 43 | MDSI_C_TE | 1.8V | 20K PU | 20K PU | RSVD | 1=Disable(default)<br>0=Do Not Use | RSVD | GP_INTD_DSI_TE2 |
| GPIO 44 | USB2_OC0_N | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=Disable(default) | RSVD | USB_A_OC_ODL |
| GPIO 45 | USB2_OC1_N | 1.8V | 20K PD | 20K PD | Top swap override | 1=enable<br>0=disable(default) | Top Swap | USB_C_OC_ODL |
| GPIO 61 | SIO_UART0_TXD | 1.8V | 20K PD | 20K PD | Enable TXE ROM Bypass | 1=enable bypass<br>0=disable bypass(default) | TXE ROM Bypass | PCHTX_MIPI60RX_UART |
| GPIO 62 | SIO_UART0_RTS_N | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=Disable(default) | RSVD | STEST_INT_L |
| GPIO 65 | SIO_UART2_TXD | 1.8V | 20K PD | 20K PD | Force DNX FW Load | 1=Force DnX<br>0=Do not force(default) | DnX FW Load | PCHTX_UART2 |
| GPIO 66 | SIO_UART2_RTS_N | 1.8V | 20K PD | 20K PD | LPC boot BIOS strap | 1=boot from LPC<br>0=do not boot from LPC(default) | LPC Boot | TP172 |
| GPIO 79 | SIO_SPI_0_CLK | 1.8V | 20K PD | 1M PD | RSVD | 1=Do Not Use<br>0=Normal Operation | RSVD | H1_SLAVE_SPI_CLK_R |
| GPIO 80 | SIO_SPI_0_FS0 | 1.8V | 20K PD | 1M PD | RSVD | 1=Do Not Use<br>0=No halt(default) | RSVD | H1_SLAVE_SPI_CS_L_R |
| GPIO 81 | SIO_SPI_0_FS1 | 1.8V | 20K PU | 20K PU | RSVD | 1=Disable(default)<br>0=Do Not Use | RSVD | GPIO_81_DEBUG |
| GPIO 83 | SIO_SPI_0_TXD | 1.8V | 20K PU [Pre-ES and ES]<br>20K PD [ES21 and QS] | 4.7K PU | LPC 1.8V/3.3V mode select | 1=1.8V mode<br>0=3.3V mode(default) | LPC Voltage select | H1_SLAVE_SPI_MOSI_R |
| GPIO 84 | SIO_SPI_2_CLK | 1.8V | 20K PU | 3.3K PD | Allow SPI as a boot source | 1=don't boot from SPI(default)<br>0=boot from SPI(debug) | SPI Boot Source | STEST_SPI1_CLK_R |
| GPIO 85 | SIO_SPI_2_FS0 | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=Disable(default) | RSVD | STEST_SPI_CS_L_R |
| GPIO 86 | SIO_SPI_2_FS1 | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=enable(default) | RSVD | STEST_CNTRL |
| GPIO 87 | SIO_SPI_2_FS2 | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=default | RSVD | TP_PCH_GPIO_87_PD DURING RSMRST |
| GPIO 89 | SIO_SPI_2_TXD | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=default | RSVD | STEST_SPI1_MOSI_R |
| GPIO 159 | AVS_I2S0_SDI | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=default | RSVD | I2S0_PCH_RX |
| GPIO 163 | AVS_I2S1_WS_SYNC | 1.8V | 20K PU [Pre-ES and ES]<br>20K PD [ES21 and QS] | 20K PU [Pre-ES and ES]<br>20K PD [ES21 and QS] | SMBus 1.8V/3.3V mode select | 1=1.8V mode<br>0=3.3V mode(default) | Buffers 1.8V/3.3V | I2S_SFRM_SPKR |
| GPIO 164 | AVS_I2S1_SDI | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=default | RSVD | WLAN_PE_RST |
| GPIO 168 | AVS_HDA_SDI | 1.8V | 20K PU [Pre-ES and ES]<br>20K PD [ES21 and QS] | 20K PU [Pre-ES and ES]<br>20K PD [ES21 and QS] | PMU 1.8V/3.3V mode select | 1=1.8V mode<br>0=3.3V mode(default) | PMU 1.8V/3.3V | I2S2_PCH_RX |
| GPIO 172 | AVS_M_CLK_B1 | 1.8V | 20K PD | 20K PD | SMBus No Reboot | 1=Enable<br>0=Disable (default) | SMBus Reboot | DMIC_CLK2_R |
| GPIO 174 | AVS_M_CLK_AB2 | 1.8V | 20K PD | 20K PD | VDD2 1.24V vs 1.2V select | 1=VDD2 is 1.24V<br>0=VDD2 is 1.20V(default) | VDD2 Voltage | TP_GPIO_174 |
| GPIO 175 | AVS_M_DATA_2 | 1.8V | 20K PD | 4.7K PU | eSPI vs LPC | 1=eSPI mode<br>0=LPC mode(default) | eSPI/LPC mode | DMIC_CAM2_DATA |
| GPIO 177 | SMB_CLK | 3.3V(Default)<br>/1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=default | RSVD | TP_PCH_SMB_CLK,TP160 |
| GPIO 191 | CNV_BRI_DT | 1.8V | 20K PD | 20K PD | eSPI Flash Sharing Mode | 1=slave attached<br>0=master attached(default) | Flash Sharing | CNVI_BRI_DT_R |
| GPIO 192 | CNV_BRI_RSP | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=Normal Operation | RSVD | CNVI_BRI_RSP |
| GPIO 193 | CNV_RGI_DT | 1.8V | 20K PU | 20K PU | RSVD | 1=Do Not Use<br>0=Normal Operation | RSVD | CNVI_RGI_DT_R |
| GPIO 194 | CNV_RGI_RSP | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=Normal Operation | RSVD | CNVI_RGI_RSP |
| GPIO 195 | CNV_RF_RESET_N | 1.8V | 20K PD | 20K PD | RSVD | 1=Do Not Use<br>0=Normal Operation | RSVD | CNVI_RF_RESET_L |
| GPIO 196 | XTAL_CLKREQ | 1.8V | 20K PD | 10K PD | RSVD | 1=Do Not Use<br>0=Normal Operation | RSVD | WLAN_CLKREQ0 |

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