# ZBC_DROID_BLORB

## TABLE OF CONTENTS

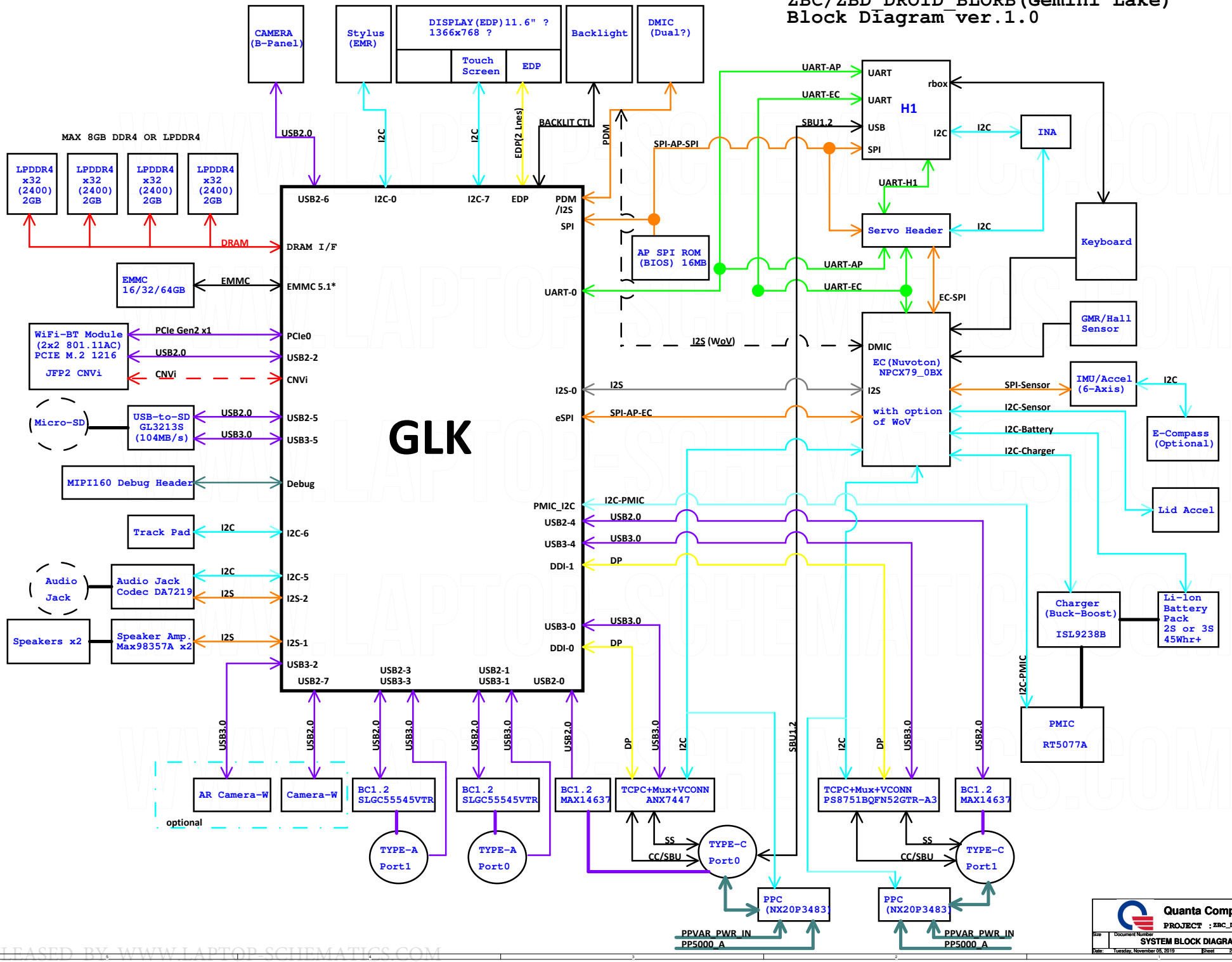


## TABLE OF CONTENTS

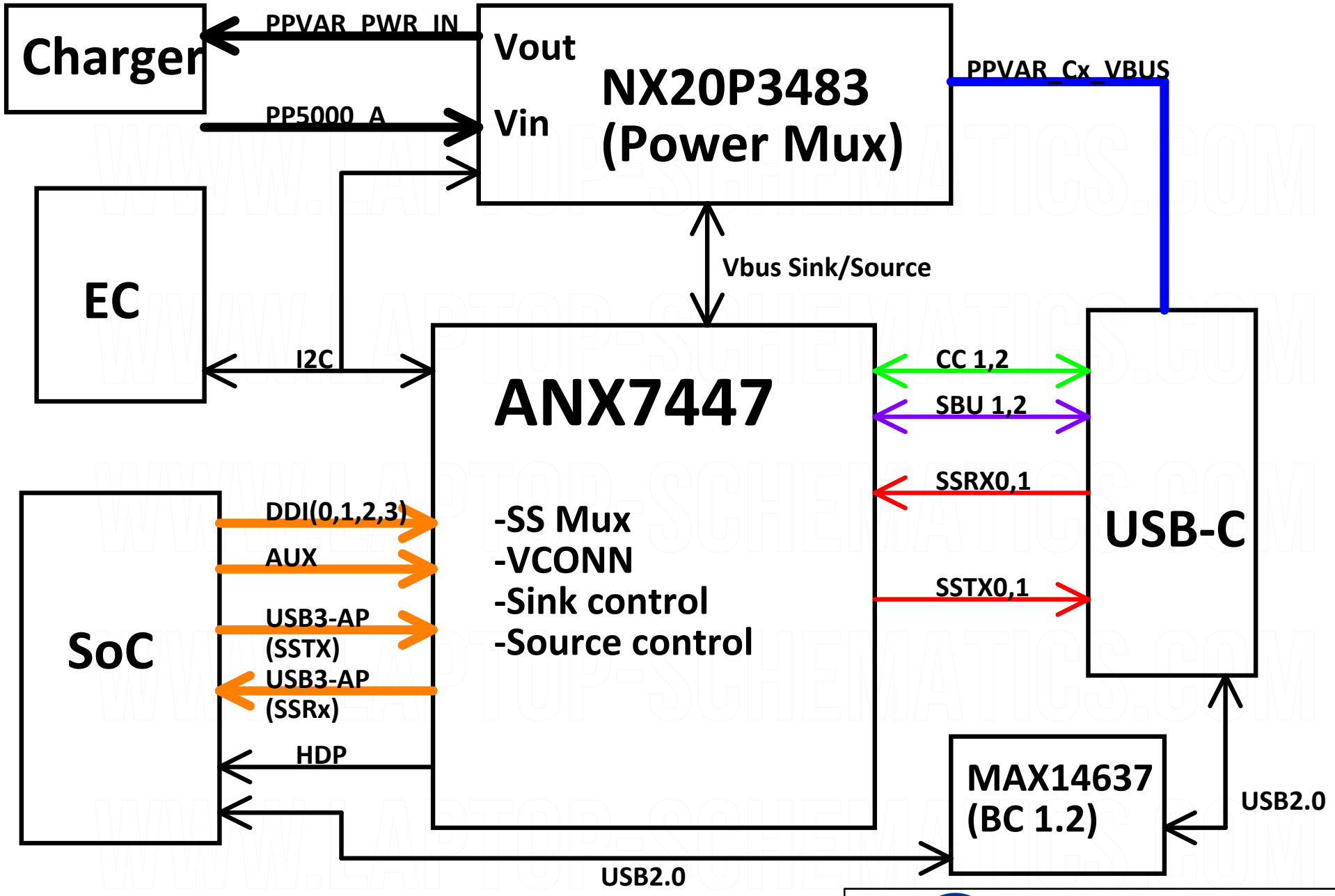



Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB
Size | Document Number: TABLE OF CONTENTS | Rev 1A
Date: Tuesday, November 05, 2019 | Sheet 1 of 45

# ZBC/ZBD_DROID_BLORB(Gemini Lake)
# Block Diagram ver.1.0




Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB
SYSTEM BLOCK DIAGRAM
Rev 1A
Tuesday, November 05, 2019
Sheet 2 of 45

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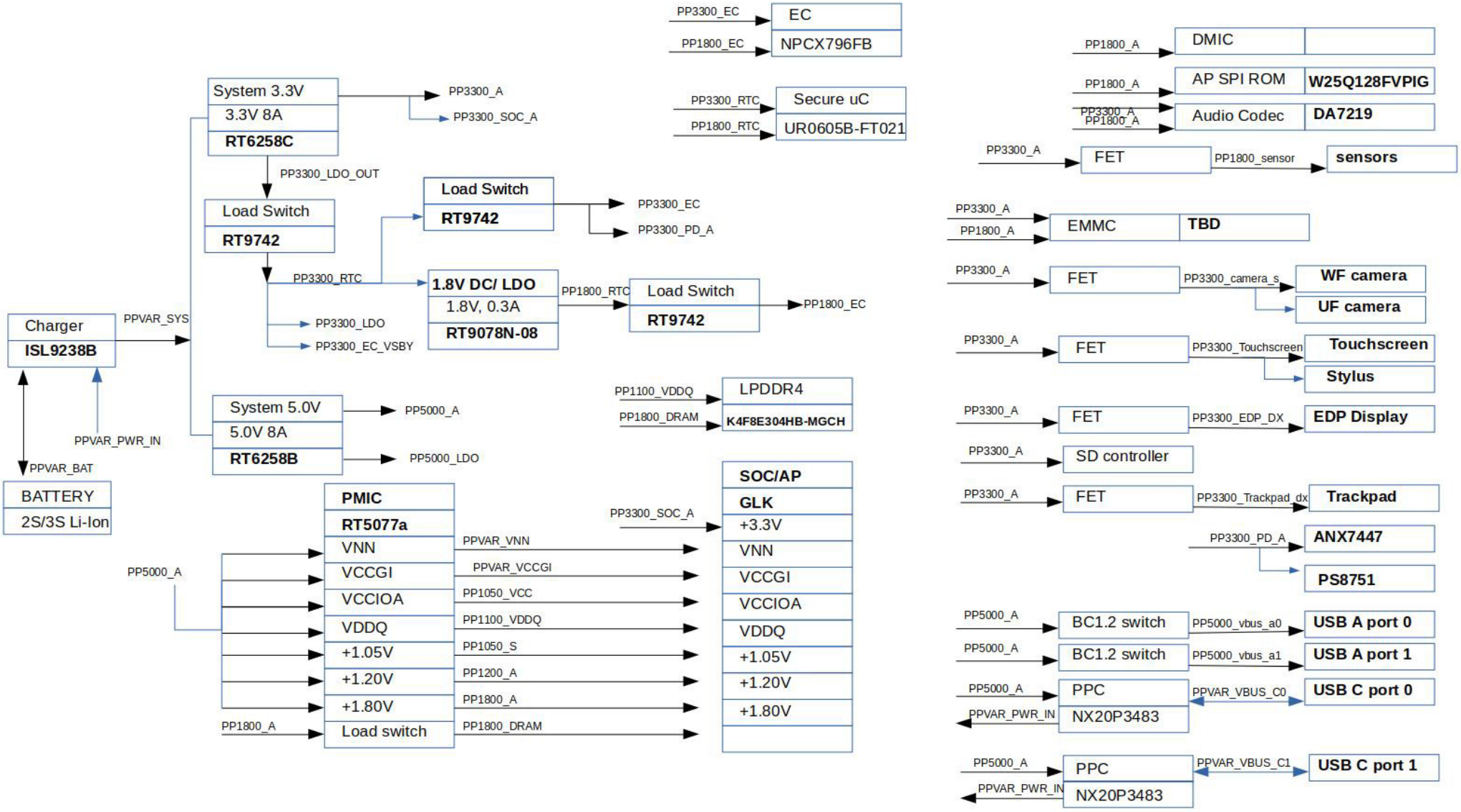
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | USB TYPE-C BLOCK DIAGRAM | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 3 of 45 | |

# Power Tree

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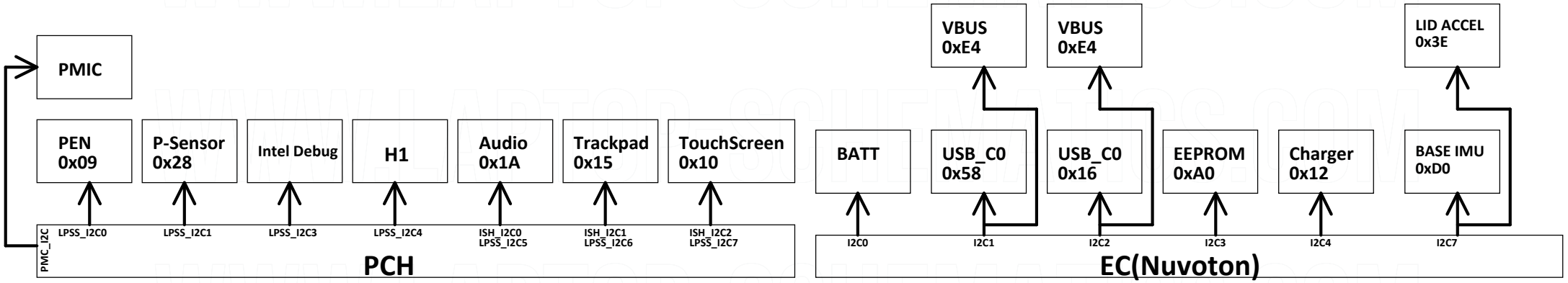
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | Power Tree | 1A |

Date: Tuesday, November 05, 2019 Sheet 4 of 45

| Master | Port | Net Name | Slave Device(S) | Speed |
|---|---|---|---|---|
| EC | I2C0_0 | EC_I2C_BATTERY_3V3 | BATTERY ( TBD ) | 100KHZ |
| EC | I2C1_0 | EC_I2C_USB_C0_MUX | ANX7447, NX20P3483 | 100KHZ |
| EC | I2C2_0 | EC_I2C_USB_C1_MUX | *Check subboard* | 100KHZ |
| EC | I2C3_0 | EC_I2C_EEPROM_SCL | M34E02 | 100KHZ |
| EC | I2C4_1 | EC_I2C_CHARGER_3V3 | ISL9238B | 100KHZ |
| EC | I2C5_0 | - | | |
| EC | I2C7_0 | EC_I2C_SENSOR_U | LSM6DS3TR, LIS2MDLTR | 400KHZ |
| AP | LPSS_I2C0 | PCH_I2C_PEN | STYLUS (TBD ) | 400KHZ |
| AP | LPSS_I2C1 | PCH_I2C_P_SENSOR | TBD | 100KHZ |
| AP | LPSS_I2C2 | - | | |
| AP | LPSS_I2C3 | DBG_PCH_I2C | TBD | TBD |
| AP | LPSS_I2C4 | PCH_I2C_H1 | H1 ( not used ) | 100KHZ |
| AP | LPSS_I2C5 | PCH_I2C_AUDIO | DA7219 | 100KHZ |
| AP | LPSS_I2C6 | PCH_I2C_TRACKPAD | TRACKPAD (TBD ) | 100KHZ |
| AP | LPSS_I2C7 | PCH_I2C_TOUCHSCREEN | TOUCHSCREEN ( TBD ) | 100KHZ |
| AP | PMC_I2C | PCH_PMIC_I2C | RT5077A | 100KHZ |

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PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | I2C MAP | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 5 of 45 | |

## (CPU)


| Quanta Computer Inc. | | | |
|---|---|---|---|
| PROJECT : ZBC_DROID_BLORB | | | |
| Size | Document Number: SOC DRAM I/F | | Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 6 of 45 | | |

# Gemini lake (DISPLAY,eDP)

(CPU)

## USB C PORT 0

PP3300_PD_A

R21 100K_5%_2

(29) DDI0_AUX_P
(29) DDI0_AUX_N

C336 0.1u/16V_4
C337 0.1u/16V_4

R22 100K_5%_2

C84Q *10p/25V_2

(18,29) USB_C0_HPD_1V8_ODL

(29) DDI0_TX0_P
(29) DDI0_TX0_N
(29) DDI0_TX1_P
(29) DDI0_TX1_N
(29) DDI0_TX2_P
(29) DDI0_TX2_N
(29) DDI0_TX3_P
(29) DDI0_TX3_N

## USB C PORT 1

PP3300_PD_A

R459 *2AC@100K_5%_2

(39) DDI1_AUX_P
(39) DDI1_AUX_N

C338 *Short_0201
C339 *Short_0201

R460 *2AC@100K_5%_2

(18,39) USB_C1_HPD_1V8_ODL

(39) DDI1_TX0_P
(39) DDI1_TX0_N
(39) DDI1_TX1_P
(39) DDI1_TX1_N
(39) DDI1_TX2_P
(39) DDI1_TX2_N
(39) DDI1_TX3_P
(39) DDI1_TX3_N

1228_Q_Changed C338/C339 to a short pad

## LOCAL DISPLAY PANEL

(26) EDP_TX0_P
(26) EDP_TX0_N
(26) EDP_TX1_P
(26) EDP_TX1_N
(26) EDP_TX2_P
(26) EDP_TX2_N
(26) EDP_TX3_P
(26) EDP_TX3_N
(26) EDP_AUX_PANEL_P
(26) EDP_AUX_PANEL_N

EDP_HPD_PANEL_1V8_ODL

(26) SOC_EDP_BKLTCTL_1V8
(26) SOC_EDP_BKLTEN
(35) EN_PP3300_EDP_DX

R2 100_1%_2

U4C

DDI0_TXP_0 AH1
DDI0_TXN_0 AH3
DDI0_TXP_1 AE2
DDI0_TXN_1 AE3
DDI0_TXP_2 AJ2
DDI0_TXN_2 AJ3
DDI0_TXP_3 AG2
DDI0_TXN_3 AG3
DDI0_AUXP AC12
DDI0_AUXN AC10
DDI0_HPD C39
DDI0_DDC_SCL B43
DDI0_DDC_SDA C43
DDI0/DDI_B
1.8V/3.3V

DDI1_TXP_0 AA2
DDI1_TXN_0 AA3
DDI1_TXP_1 Y3
DDI1_TXN_1 Y1
DDI1_TXP_2 AD1
DDI1_TXN_2 AD3
DDI1_TXP_3 AC2
DDI1_TXN_3 AC3
DDI1_AUXP AC7
DDI1_AUXN AC5
DDI1_DDC_SCL C42
DDI1_DDC_SDA A42
DDI1_HPD C38
DDI1/DDI_C
1.8V/3.3V

EDP_TXP_0 AE12
EDP_TXN_0 AE13
EDP_TXP_1 AC15
EDP_TXN_1 AC17
EDP_TXP_2 AE10
EDP_TXN_2 AE8
EDP_TXP_3 AE5
EDP_TXN_3 AE7
EDP_AUXP W17
EDP_AUXN W15
EDP_HPD B39
PNL0_BKLTCTL B41
PNL0_BKLTEN C41
PNL0_VDDEN C40
eDP/DDI_A
1.8V/3.3V
EDP_RCOMP_P AA5
EDP_RCOMP AA7

GLK_SOC_RVP2
3 OF 13

MDSI_A_CLKP AL2
MDSI_A_CLKN AM3
MDSI_C_CLKP AG13
MDSI_C_CLKN AG12
MDSI_A_DP_0 AN5
MDSI_A_DN_0 AN7
MDSI_A_DP_1 AJ15
MDSI_A_DN_1 AJ17
MDSI_A_DP_2 AJ7
MDSI_A_DN_2 AJ5
MDSI_A_DP_3 AJ10
MDSI_A_DN_3 AJ12
MDSI_C_DP_0 AG15
MDSI_C_DN_0 AG17
MDSI_C_DP_1 AG8
MDSI_C_DN_1 AG10
MDSI_C_DP_2 AG7
MDSI_C_DN_2 AG5
MDSI_C_DP_3 AE15
MDSI_C_DN_3 AE17
MDSI

TP_MDSIA_CLKP
TP_MDSIA_CLKN
TP_MDSIC_CLKP
TP_MDSIC_CLKN
TP_MDSIA_D0_P
TP_MDSIA_D0_N
TP_MDSIA_D1_P
TP_MDSIA_D1_N
TP_MDSIA_D2_P
TP_MDSIA_D2_N
TP_MDSIA_D3_P
TP_MDSIA_D3_N
TP_MDSIC_D0_P
TP_MDSIC_D0_N
TP_MDSIC_D1_P
TP_MDSIC_D1_N
TP_MDSIC_D2_P
TP_MDSIC_D2_N
TP_MDSIC_D3_P
TP_MDSIC_D3_N

## ALL NC

MIPI_I2C_SCL R53 TP_PCH_GPIO47 TP31
MIPI_I2C_SDA R54 TP_PCH_GPIO46 TP37
1.8V

MDSI_C_TE T53
MDSI_A_TE T55

R502 *0_5%_2
GP_INTD_DSI_TE2 TP72
GP_INTD_DSI_TE2 (20)
TP_WIFI_RST_N TP135

MDSI_RCOMP AL5 MCSI1_RCOMP
R1 150_1%_2

(LDS)

PP1800_SOC_A

R731 100K_5%_2

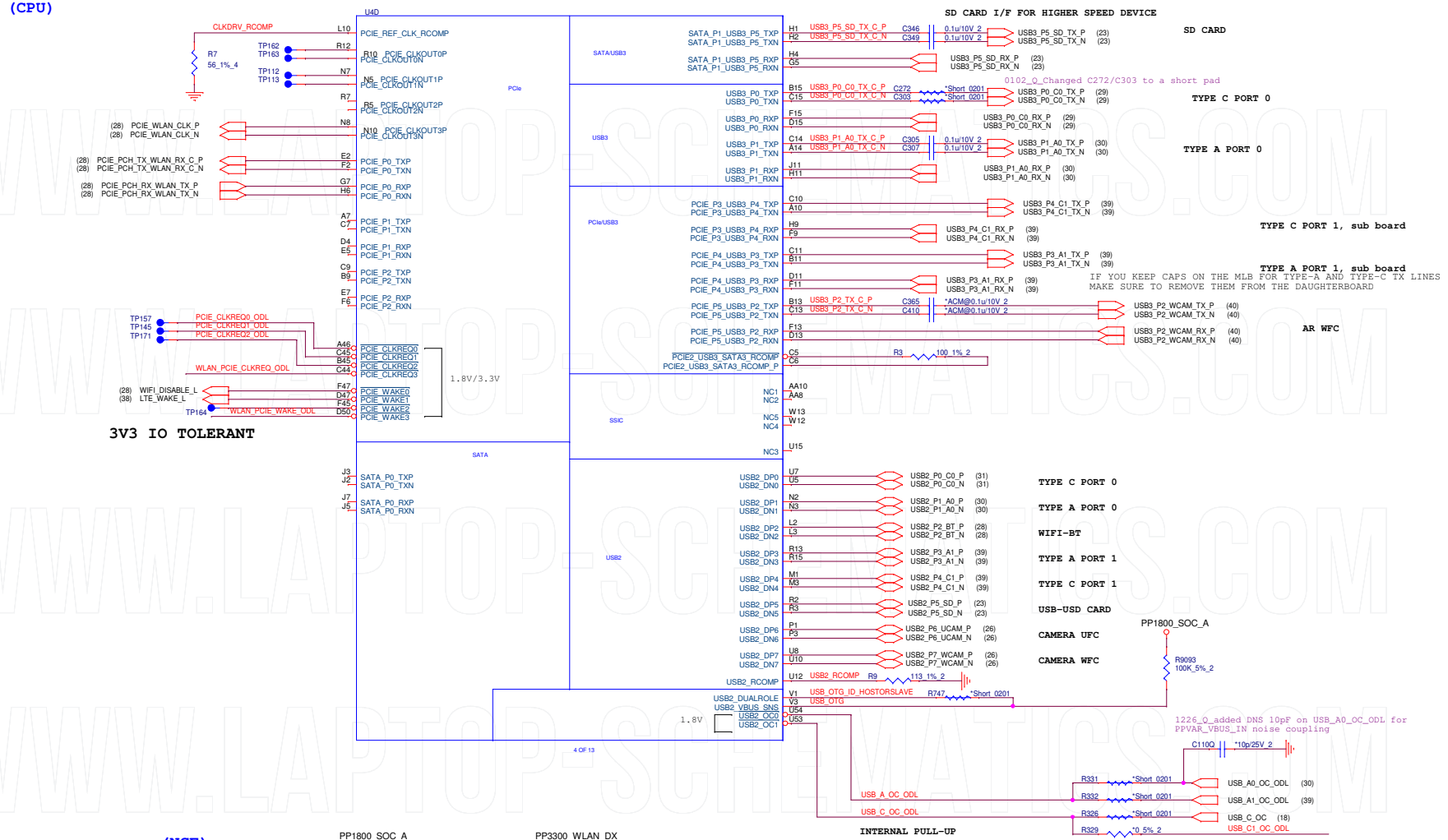
EDP_HPD_PANEL_1V8_ODL

(26) EDP_HPD_PANEL

Q78 PJE138K

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZBC_DROID_BLORB | | |
| Size | Document Number: SOC EDP/MIPI/DDI | Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 7 of 45 | |

# Gemini lake (SATA , ODD, CLK ,USB,PCIE)




Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | SOC PCIE/USB/SATA | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 8 of 45 | |

# Gemini lake (EMMC/LPC/I2C/GPIO/HDA)

(CPU)

(18) EC_I2S_SCLK — R281 20_1%_2 — I2S0_SCLK_R
(18) EC_I2S_SFRM — R295 20_1%_2 — I2S0_SFRM_R
(18) EC_I2S_TX_PCH_RX — R298 20_1%_2 — I2S0_PCH_RX

C571 2.2p/25V_2 | C572 2.2p/25V_2 | C573 2.2p/25V_2

(MIC)

DMIC_CLK1 (26) — TP66
PCH_SLP_S0_L (11,33)
Q40 PMZ370UNE
DMIC_CLK1_R — R300 20_1%_2 — DMIC_CLK1_G (26)
WOV
R173 *0_5%_2
DMIC_DATA_R — R317 20_1%_2 — DMIC_DATA (26)

(CPU)

TO-EC

SPEAKER AMP

HEADPHONE

DMIC'S

TEST POINTS ON EMMC CLOSE TO SOC

TP70 TP53 TP54 TP57 TP59 — I2S0_SCLK_R, I2S0_SFRM_R, I2S0_PCH_RX, I2S0_PCH_TX

(38) LTE_OFF_ODL
(24) I2S_SCLK_SPKR
(24) I2S_SFRM_SPKR
(28) WLAN_PE_RST
(24) I2S_PCH_TX_SPKR_RX

(24) I2S_SCLK_HP
(24) I2S_SFRM_HP
(24) I2S_PCH_RX_HP_TX
(24) I2S_PCH_TX_HP_RX
(24) I2S_MCLK_HP

R32 R33 R36 R37 R40 — 20_1%_2 — I2S2_SCLK_R, I2S2_SFRM_R, I2S2_PCH_RX, I2S2_PCH_TX, I2S2_MCLK_R

(26,40) DMIC_CLK2 — R189 33_1%_2 — DMIC_CLK1_R, DMIC_CLK2_R, DMIC_DATA_R, TP_GPIO_174
TP51 TP52 TP61

PP1800_SOC_A — R282 4.7K_5%_2 — (40) DMIC_CAM2_DATA

(23) EMMC_RCLK
(23) EMMC_CLK — TP44 TP41
R590 100K_1%_6
(23) EMMC_DAT0 (23) EMMC_DAT1 (23) EMMC_DAT2 (23) EMMC_DAT3 (23) EMMC_DAT4 (23) EMMC_DAT5 (23) EMMC_DAT6 (23) EMMC_DAT7 — TP42
(23) EMMC_CMD — TP43
(23) EMMC_RST_ODL — TP30
TP_EN_PP3300_EMMC
RCOMP_EMMC0
R284 200_1%_2

U4J

AVS_I2S0_MCLK AVS_I2S0_BCLK AVS_I2S0_WS_SYNC AVS_I2S0_SDI AVS_I2S0_SDO
AVS_I2S1_MCLK AVS_I2S1_BCLK AVS_I2S1_WS_SYNC AVS_I2S1_SDI AVS_I2S1_SDO
AVS_HDA_BCLK AVS_HDA_WS_SYNC AVS_HDA_SDI AVS_HDA_SDO AVS_HDA_RST
AVS_DMIC_CLK_A1 AVS_DMIC_CLK_B1 AVS_DMIC_DATA_1 AVS_DMIC_CLK_AB2 AVS_DMIC_DATA_2
1.8V
AUDIO-AVS

EMMC_CLK EMMC_RCLK
EMMC_D0 EMMC_D1 EMMC_D2 EMMC_D3 EMMC_D4 EMMC_D5 EMMC_D6 EMMC_D7 EMMC_CMD
EMMC_RST EMMC_PWR_EN EMMC_RCOMP
1.8V
1.8V/3.3V
eMMC

RSVD
RSVD6 RSVD5 RSVD7 RSVD8 RSVD9 RSVD3 RSVD4 RSVD2 RSVD10 RSVD1
RSVD

LPC/eSPI
LPC set 3.3V
LPC_CLKOUT0 LPC_CLKOUT1 LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_CLKRUN LPC_FRAME LPC_SERIRQ
1.8V/3.3V

FAST_SPI
FST_SPI_CLK FST_SPI_MOSI_IO0 FST_SPI_MISO_IO1 FST_SPI_IO2 FST_SPI_IO3 FST_SPI_CS0 FST_SPI_CS1
1.8V

7 OF 13

PP1800_SOC_A
R407 20K_1%_2 | R187 *20K_1%_2 | R283 *20K_1%_2 | R358 *20K_1%_2 | R363 *20K_1%_2
ESPI_CS_L ESPI_IO0 ESPI_IO1 ESPI_IO2 ESPI_IO3 ESPI_CLK
R365 20K_1%_2

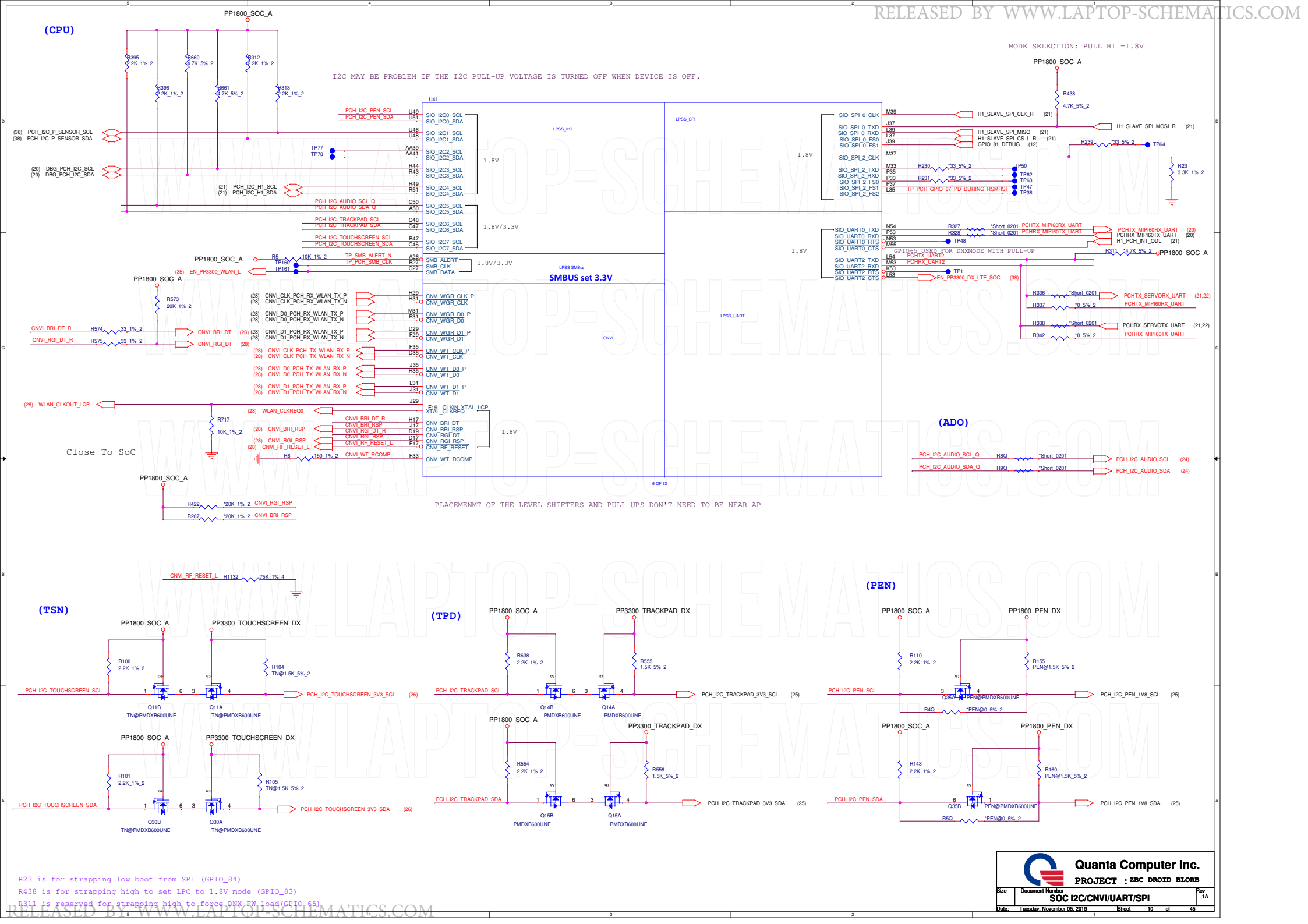
native SD card support dropped

ESPI_CLK_R — R285 33_5%_2 — ESPI_CLK (18)
R67 *33_5%_2
ESPI_IO0_R R71 ESPI_IO0 (18)
ESPI_IO1_R R73 ESPI_IO1 (18)
ESPI_IO2_R R74 ESPI_IO2 (18)
ESPI_IO3_R R76 ESPI_IO3 (18)
TO-EC
ESPI_CS_L_R R93 ESPI_CS_L (18)
ESPI_RESET_L_R R128 ESPI_RESET_L (18)
R90 *33_5%_2

PCH_SPI_CLK_R R591 PCH_SPI_CLK (19)
PCH_SPI_MOSI_R R592 PCH_SPI_MOSI (19)
PCH_SPI_MISO R593 PCH_SPI_MISO_R (19)
R640 *33_5%_2
R642 *33_5%_2
PCH_SPI_CS0_L_R R643 PCH_SPI_CS0_L (19)
SPK_PA_EN_R R644 SPK_PA_EN (24)
R198 100K_1%_6
TO-FLASH

No extermal PU/PD on GPIO_174, using internal PD for setting VDD2 to 1.2v (GPIO_174)
R282 is for strapping high to enable eSPI mode (GPIO_175)

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB
Size | Document Number: SOC AUDIO/EMMC/LPC/SPI | Rev 1A
Date: Tuesday, November 05, 2019 | Sheet 9 of 45



| Vendor | Dram PartNumber | RAM ID | Memory | Rank Density | Dual Rank |
|---|---|---|---|---|---|
| Micron | MT53B256M32D1NP-062 | 0 (0000) | 4GiB | 8Gb | N |
| Hynix | H9HCNNN8KUMLHR-NME | 0 (0000) | 4GiB | 8Gb | N |
| Samsung | K4F8E304HB-MGCJ | 0 (0000) | 4GiB | 8Gb | N |
| Nanya | NT6AN256T32AV-J2 | 0 (0000) | 4GiB | 8Gb | N |
| Micron | MT53E512M32D2NP-046 | 1 (0001) | 8GiB | 16Gb | N |
| Samsung | K4F6E3S4HM-MGCJ | 1 (0001) | 8GiB | 16Gb | N |
| Kingston | B5116PC2WDGPKR | 1 (0001) | 8GiB | 16Gb | N |
| Micron | MT53B512M32D2NP-062 | 2 (0010) | 8GiB | 8Gb | Y |
| Hynix | H9HCNNNBPUMLHR-NME | 2 (0010) | 8GiB | 8Gb | Y |
| Samsung | K4F6E304HB-MGCJ | 2 (0010) | 8GiB | 8Gb | Y |

(CPU)

PP1800_SOC_A

R371 *100K_5%_2 DRAM_ID0 DRAM_ID1
R376 *100K_5%_2
R382 *100K_5%_2
R399 *100K_5%_2 DRAM_ID3 DRAM_ID2
R373 100K_5%_2
R378 100K_5%_2
R385 100K_5%_2
R402 100K_5%_2

# Gemini lake (PMU/PMIC/RTC)

PP3300_SOC_A

R557 100K_5%_2
R276 100K_5%_2

PP1050_VCCRAM_S

R56 *68_1%_2
R58 *169_1%_4
R63 *84.5_1%_4

(18) SUSPWRDNACK

U4E

(33) PCH_PMIC_I2C_SCL → R46 → PMC_I2C_SCL
(33) PCH_PMIC_I2C_SDA → R48 → PMC_I2C_SDA

TP_AP_PMC_SPI_CLK N48 PMC_SPI_CLK
DRAM_ID0 N44 PMC_SPI_FS0
DRAM_ID1 L49 PMC_SPI_FS1
DRAM_ID2 L51 PMC_SPI_FS2
DRAM_ID3 N49 PMC_SPI_RXD
TP_AP_PMC_SPI_TX PMC_SPI_TXD

1.8V

PLT_RST_L → D54 PMU_PLTRST
(12,18,21,23,28) PLT_RST_L
(12,18) EC_PCH_PWR_BTN_ODL → C52 PMU_PWRBTN
(9,33) PCH_SLP_S0_L → C53 PMU_SLP_S0
(33) PCH_SLP_S3_L → D51 PMU_SLP_S3
(33) PCH_SLP_S4_L → J49 PMU_SLP_S4
SUSPWRDNACK F54 SUSPWRDNACK
PMU_BATLOW_L J48 PMU_BATLOW
(12,18,21,22) SYS_RST_ODL → C51 PMU_RSTBTN
(28) PCH_SUSCLK → G49 PMU_SUSCLK
(28) BT_DISABLE_L → E52 SUS_STAT

PMU set 3.3V

1.8V/3.3V PMU

TP81 TP82 TP83
TP_PCH_GPIO_78 F55 SVID0_CLK
TP_PCH_GPIO_77 G53 SVID0_DATA
TP_PCH_GPIO_76 G54 SVID0_ALERT

1.05V SVID

TP87 TP88
DEBUG_OBS_PORT_A0 D1 DEBUG_PORT_A0
DEBUG_OBS_PORT_A1 D2 DEBUG_PORT_A1
A54 NC2
C54 NC11

Misc

8 OF 13

RTC is 3.3V

1.8V

iCLK
OSC_CLK_OUT_0 B17
OSC_CLK_OUT_1 C17
OSCIN U2 PCH_OSCIN
OSCOUT T1 PCH_OSCOUT

RTC
RTC_X1 D23 PCH_RTC_X1
RTC_X2 F23 PCH_RTC_X2
VCC_RTC_EXTPAD J23 RTC_EXPAD
INTRUDER H25 INTRUDER
SOC_PWROK D25 EC_PCH_PWROK
RSM_RST F25 PCH_RSMRST_L
RTC_TEST F26 PCH_RTEST_ODL
RTC_RST D27 PCH_RTCRST_ODL

Thermal
THERMTRIP J53 THERMTRIP_L (33)
PROCHOT J54 PCH_PROCHOT_ODL (18,37)
NC3 AG43
NC15 H53
NC4 AG44
NC16 H55

Spare
NC1 A4
NC5 BH1
SKTOCC A53
NC14 F37
NC6 BL2
NC7 BL3
NC8 BL53
NC9 C2
NC10 C3
NC17 R41

EC_IN_RW_OD (21) → PCH_WP_OD (19)

PP3300_RTC

R8 100K_5%_2
C360 0.1u/10V_2
R735 *Short_0201
R46 100K_5%_2

SEL BOM: 9H03280012
Quanta suggested 20ppm/12.5pF

PCH_RTC_X2
PCH_RTC_X1
X2 32.768KHZ/20ppm/12.5pF
9H03200031
R45 1M_1%_2
C2 18p/25V_2
C3 18p/25V_2

TXC/9H03200031
2nd source:
EPSON/FC-135

SEL BOM: CS325-19.200MABJ-UT
Quanta suggested 20ppm/12pF

PCH_OSCOUT
PCH_OSCIN
X3 19.2MHZ/20ppm1/12pF
7V19200001
R722 200K_1%_2
C1 15p/25V_2
C4 15p/25V_2

TXC/7V19200001
2nd source:
Hosonic/E3FB19E0X0008E
Interquip/5YEA19200122SF50Q2

PP3300_A

R190 100K_1%_2
R191 1K_1%_2
R120Q *100K_1%_2
C120Q *1u/6.3V_2
PLT_RST_L
PCH_SLP_S3_L → Q56 PJE138K → SLP_S3 → Q57 PJE138K

0109_Q_added DNS resistor/cap on PLT_RST_L for potential issue

PCH_RSMRST_L
R587 100K_1%_2

PP3300_A

R508 499K_1%_2
PCH_RSMRST_OD
PCH_RSMRST_L → Q80 PJE138K
C447 *1u/6.3V_2

## CHECK RTCRST SIGNAL

CHECK RTCRST SIGNAL

PP3300_RTC

R50 20K_1%_2
PCH_RTCRST_ODL
EC_PCH_RTCRST → Q7 PJE138K
C5 1u/25V_4

(18) EC_PCH_RTCRST → EC_PCH_RTCRST
R739 100K_1%_2
Q86 PJE138K
PCH_RTEST_ODL

PP3300_RTC

R740 20K_1%_2
C582 1u/25V_4

PCH_RSMRST_OD

PCH_SLP_S0_L → Q79 PMZB670UPE → SLP_S0_L → SLP_S0_L (18)
R516 *0_5%_2
R507 499K_1%_2

PCH_RSMRST_OD

PCH_SLP_S3_L → Q81 PMZB670UPE → SLP_S3_L → SLP_S3_L (18,35)
R517 *0_5%_2
R509 499K_1%_2

PCH_RSMRST_OD

PCH_SLP_S4_L → Q82 PMZB670UPE → SLP_S4_L → SLP_S4_L (18,35)
R518 *0_5%_2
R510 499K_1%_2

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | SOC PMU/RTC/SVID/THERMAL/MISC | 1A |

Date: Tuesday, November 05, 2019 Sheet 11 of 45

LAYOUT NOTE: PLACE THE R62, 65, 55, 57, R393 WITHIN 1" OF J5 MIPI60 CONNECTOR.

(CPU)

PP1800_SOC_A

R65 51_1%_2 R393 150_1%_2 R62 51_1%_2

TP_GPIO5

(20) TCK (20) TDI (20) TDO (20) TMS (20) TRST_L

U4H

JTAG

AH53 JTAGX
AM53 JTAG_TCK
AJ54 JTAG_TDI
AL53 JTAG_TDO
AL54 JTAG_TMS
AK53 JTAG_TRST

1.8V

ITP

PP1800_SOC_A

R57 *51_1%_2 R55 51_1%_2 R397 150_1%_2 R394 51_1%_2

AH55 JTAG_PRDY
AJ53 JTAG_PREQ

(20) CX_PRDY_L
(20) CX_PREQ_L

PP1800_A PP3300_A

R380 *4.7K_5%_2 R391 1K_5%_2 R392 1K_5%_2

R391,R392,R341,R352 can't be un-stuffed in MP even if removing debugging related stuffs from MP

(10) GPIO_81_DEBUG R340 1K_5%_2 BOOT_HALT_L (20)

(11,18,21,22) SYS_RST_ODL R341 *Short_0201 DBG_PMU_RSTBTN_L (20)

(11,18) EC_PCH_PWR_BTN_ODL R352 *Short_0201 DBG_PMU_PWRBTN_L (20)

(11,18,21,23,28) PLT_RST_L R361 1K_5%_2 DBG_PMU_PLTRST_L (20)

(11,18) PCH_RSMRST_L R379 *1K_5%_2 DBG_RSMRST_L (20)

1.8V

1.8V/3.3V

1.8V

GPIO

5 OF 13

GPIO_8 AG53 DBG_PTI_CLK0 (20)
GPIO_9 AG54 DBG_PTI_DATA_0 (20)
GPIO_10 AE54 DBG_PTI_DATA_1 (20)
GPIO_11 AE53 DBG_PTI_DATA_2 (20)
GPIO_12 AD55 DBG_PTI_DATA_3 (20)
GPIO_13 AD53 DBG_PTI_DATA_4 (20)
GPIO_14 AC54 DBG_PTI_DATA_5 (20)
GPIO_15 AC53 DBG_PTI_DATA_6 (20)
GPIO_16 AB53 DBG_PTI_DATA_7 (20)

GPIO_17 AA49 DBG_PTI_CLK1 (20)
GPIO_18 AC48 DBG_PTI_DATA_8 (20)
GPIO_19 AC46 DBG_PTI_DATA_9 (20)
GPIO_20 AE51 DBG_PTI_DATA_10 (20)
GPIO_21 AE49 CNVI_MFUART2_RXD_PTI_11
GPIO_22 AC51 CNVI_MFUART2_TXD_PTI_12
GPIO_23 AC49 CNVI_GNSS_PA_BLANKING_PTI_13
GPIO_24 AA51 DBG_PTI_DATA_14 (20)
GPIO_25 AA46 DBG_PTI_DATA_15 (20)

GPIO_26 AE41 DBG_PTI_CLK2 (20)
GPIO_27 AE39 DBG_PTI_DATA_16 (20)
GPIO_28 AE46 DBG_PTI_DATA_17 (20)
GPIO_29 AE44 DBG_PTI_DATA_18 (20)
GPIO_30 AC41 DBG_PTI_DATA_19 (20)
GPIO_31 AC39 DBG_PTI_DATA_20 (20)
GPIO_32 AC44 DBG_PTI_DATA_21 (20)
GPIO_33 AC43 DBG_PTI_DATA_22 (20)
GPIO_34 AA44 DBG_PTI_DATA_23 (20)

GPIO_35 AA54 DCI_CLK_PTICLK3 (20)
GPIO_36 AA53 DCI_DATA_PTITRACE3_0 (20)
GPIO_37 Y55 DBG_PTI_DATA_TRACE3_1 (20)
GPIO_38 Y53 DBG_PTI_DATA_TRACE3_2 (20)
GPIO_39 W54 DBG_PTI_DATA_TRACE3_3
GPIO_40 W53 DBG_PTI_DATA_TRACE3_4
GPIO_41 V53 DBG_PTI_DATA_TRACE3_5

GPIO_105 L46
GPIO_134 H45 EC_AP_INT_ODL TOUCHSCREEN_RST (26)
GPIO_135 H47 TRACKPAD_INT1_1V8_ODL TP65 EC_AP_INT_ODL (18)
GPIO_136 L43 PMIC_PCH_INT_1V8_ODL C850 *10p/25V_2
GPIO_137 M43 HP_INT_ODL (24)
GPIO_138 H37 PEN_PDCT_ODL (25) PP1800_SOC_A
GPIO_139 H43 PEN_INT_ODL (25)
GPIO_140 J43 PEN_RESET (25)
GPIO_141 D43 EC_PCH_WAKE_1V8_ODL R289 100K_5_2
GPIO_142 F43 TRACKPAD_INT2_1V8_ODL
GPIO_143 H41 LTE_SAR_ODL (38)
GPIO_144 F39 PEN_EJECT TP49
GPIO_145 L41 PEN_EJECT TP74 PEN_EJECT (25)
GPIO_146 F41 R558 *Short_0201 EN_PP3300_TOUCHSCREEN (25,35)
GPIO_210 R27 TP_GPIO210 TP66 EN_PP3300_CAMERA (35)
GPIO_212 U43 TOUCHSCREEN_INT_ODL (26)
GPIO_213 U41 TP_AP_GPIO213 TP172
GPIO_214 U39 P_SENSOR_INT_L (38)
TP69

1226_Q_made R289 stuffed for no matter internal PU is available or not

PEN_EJECT C860 *10p/25V_2

PP1800_SOC_A

DBG_PTI_DATA_16 R362 1K_5%_2

R28973 20K_1%_2

EC_AP_INT_ODL

(18,25) TRACKPAD_INT_1V8_ODL TRACKPAD_INT_1V8_ODL R524 *Short_0201 TRACKPAD_INT1_1V8_ODL R531 *Short_0201 TRACKPAD_INT2_1V8_ODL

0102_Q_Changed R531 to a short pad

CNVI_GNSS_PA_BLANKING_PTI_13 R14 *Short_0201 CNVI_GNSS_PA_BLANKING (28) R16 *0_5%_2 DBG_PTI_DATA_13 (20)

(PMC)

PP1800_SOC_A

R880 10K_2

PMIC_PCH_INT_1V8_ODL R887 *Short_0201 PMIC_PCH_INT_ODL (33)

CNVI_MFUART2_RXD_PTI_11 R17 *Short_0201 CNVI_MFUART2_RXD (28) R24 *0_5%_2 DBG_PTI_DATA_11 (20)

CNVI_MFUART2_TXD_PTI_12 R25 *Short_0201 CNVI_MFUART2_TXD (28) R61 *0_5%_2 DBG_PTI_DATA_12 (20)

(CPU)

PP1800_SOC_A

R881 *10K_2

EC_PCH_WAKE_1V8_ODL R888 *Short_0201 EC_PCH_WAKE_ODL (18)

R380 is reserved for strapping high (GPIO_81)
R877 is for strapping low to not allow eMMC as a boot source (GPIO_27)
No external PU/PD on GPIO_28, using internal PD for allowing SPI as a boot source

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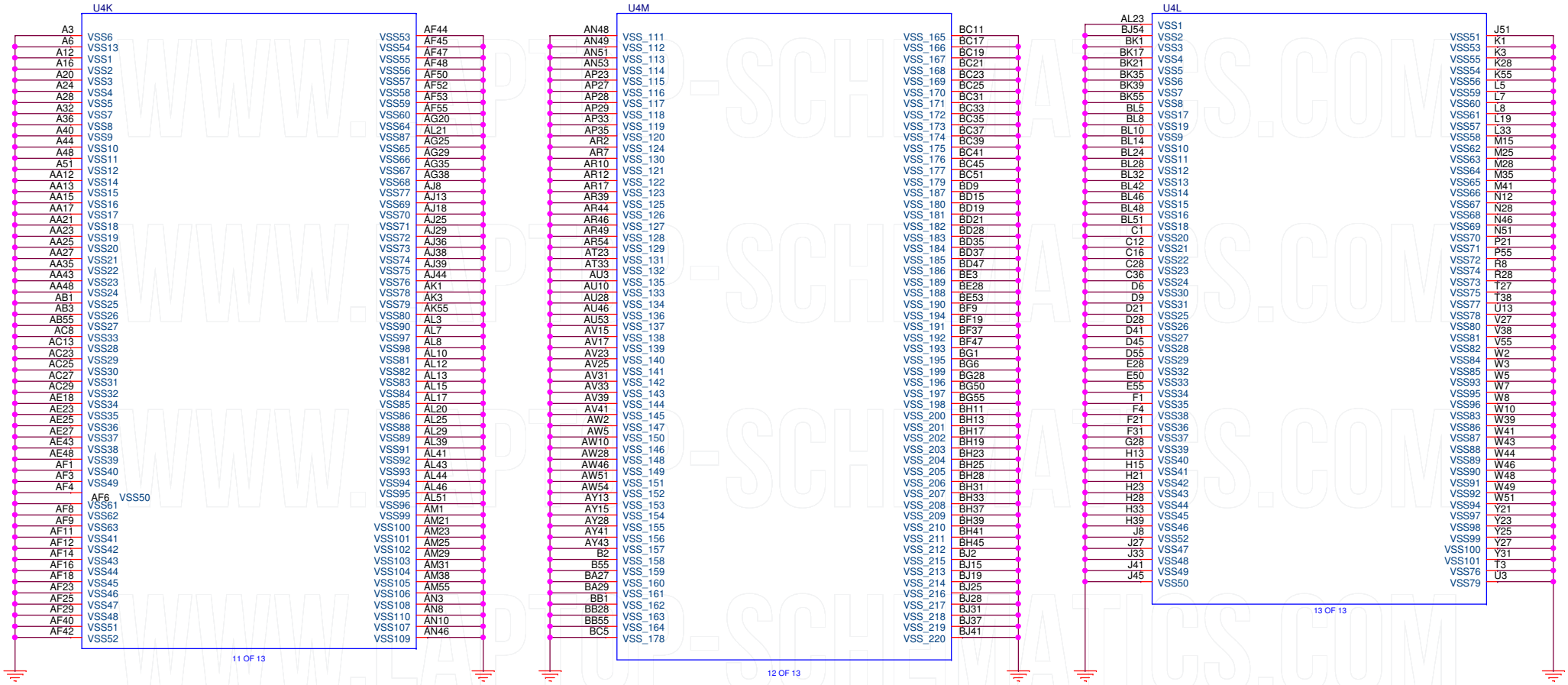
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | SOC JTAG/GPIO/ITP | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 12 of 45 | |

# GLK ULT (GND)

(CPU)



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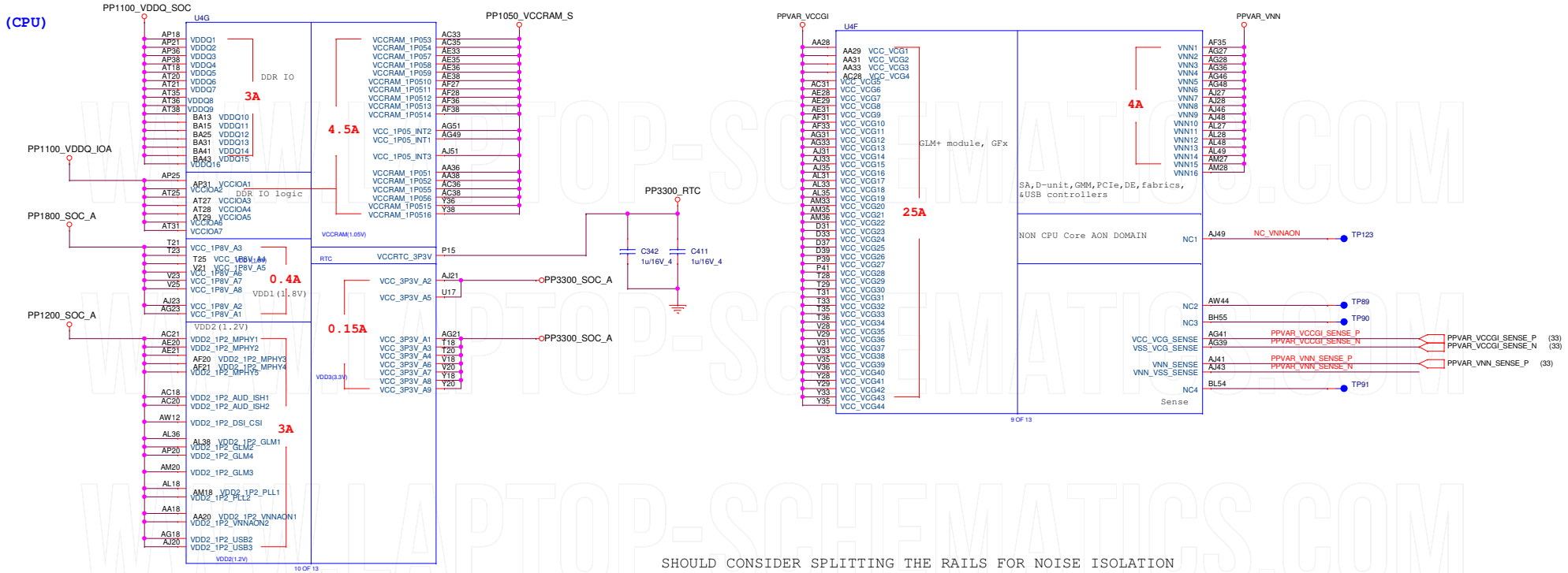
PROJECT : ZBC_DROID_BLORB

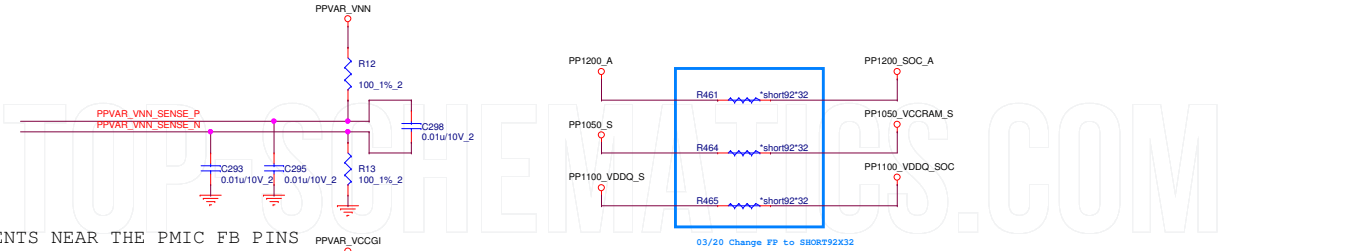
| Size | Document Number | Rev |
|---|---|---|
| | SOC GROUND | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 13 of 45 | |

# Gemini (POWER)

SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION




SHOULD CONSIDER SPLITTING THE RAILS FOR NOISE ISOLATION




PLEASE THESE COMPONENTS NEAR THE PMIC FB PINS


| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZBC_DROID_BLORB | | |
| Size | Document Number: SOC POWER | Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 14 of 45 | |

## (CPU)

PPVAR_VNN

DECOUPLING VALUES AND NUMBER BASED ON THE REFERENCE DOC

C28 1u/6.3V_4, C37 1u/6.3V_4, C46 1u/6.3V_4, C129 1u/6.3V_4, C29 1u/6.3V_4, C83 22u/6.3V_6, C38 22u/6.3V_6, C47 22u/6.3V_6, C51 22u/6.3V_6

PPVAR_VNN: 5 X 1UF_0402_6.3V, 4 X 22UF_0603_6.3V

PPVAR_VNN

C277 1u/6.3V_4

PPVAR_VCCGI

C6 1u/6.3V_4, C10 1u/6.3V_4, C95 1u/6.3V_4, C101 1u/6.3V_4, C105 1u/6.3V_4, C130 1u/6.3V_4, C156 1u/6.3V_4, C199 22u/6.3V_6, C200 22u/6.3V_6, C201 22u/6.3V_6, C204 22u/6.3V_6

PPVAR_VCCGI: 12 X 1UF_0402_6.3V, 8 X 22UF_0603_6.3V, 2 X 0.1UF_0402_16V

PPVAR_VCCGI

C9 1u/6.3V_4, C94 1u/6.3V_4, C99 1u/6.3V_4, C104 1u/6.3V_4, C115 1u/6.3V_4, C155 22u/6.3V_6

PPVAR_VCCGI

C203 22u/6.3V_6, C205 22u/6.3V_6, C206 22u/6.3V_6

PPVAR_VCCGI

C207 0.1u/16V_4, C278 0.1u/16V_4

PP1050_VCCRAM_S

C79 1u/6.3V_4, C84 1u/6.3V_4

PP1050_VCCRAM_S

C33 1u/6.3V_4, C42 1u/6.3V_4

PP1050_VCCRAM_S: 1uF_0402x10 , 22uF_0603 x3

PP1050_VCCRAM_S

C80 1u/6.3V_4, C85 1u/6.3V_4, C419 1u/6.3V_4, C88 22u/6.3V_6

PP1050_VCCRAM_S

C34 1u/6.3V_4, C43 1u/6.3V_4, C437 1u/6.3V_4, C57 22u/6.3V_6, C61 22u/6.3V_6

PP1200_SOC_A

C144 22u/6.3V_6

PP1200_SOC_A

C440 1u/6.3V_4, C493 1u/6.3V_4, C496 22u/6.3V_6

PP1200_SOC_A

C441 1u/6.3V_4, C494 1u/6.3V_4, C497 22u/6.3V_6, C499 22u/6.3V_6

PP1200_SOC_A

C89 1u/6.3V_4

PP1200_SOC_A

C438 1u/6.3V_4, C465 1u/6.3V_4, C495 1u/6.3V_4, C498 1u/6.3V_4, C500 22u/6.3V_6, C501 22u/6.3V_6, C502 22u/6.3V_6

PP1200_SOC_A: 1uF_0402x9 , 22uF_0603 x7

PP1100_VDDQ_SOC

C31 1u/6.3V_4, C40 1u/6.3V_4

PP1100_VDDQ_SOC

EDGE CAP FOR EXPOSED POWER PLANES

C322 0.1u/16V_4, C327 0.1u/16V_4, C334 0.1u/16V_4, C335 0.1u/16V_4

PP1100_VDDQ_SOC

C30 1u/6.3V_4, C39 1u/6.3V_4, C52 22u/6.3V_6, C56 22u/6.3V_6

PP1100_VDDQ_SOC

C60 22u/6.3V_6, C64 22u/6.3V_6, C67 22u/6.3V_6, C69 22u/6.3V_6, C332 1u/6.3V_4, C333 1u/6.3V_4

PP1100_VDDQ_S

W1 *short92*32

PP1100_VDDQ_IOA

C288 1u/6.3V_4, C289 1u/6.3V_4, C291 1u/6.3V_4, C304 22u/6.3V_6, C313 22u/6.3V_6, C319 22u/6.3V_6

03/20 Change FP to SHORT92X32

VDDQI: 1uF_0402x8 , 22uF_0603 x10 , 0.1uF_0402x4

PP1800_SOC_A: 1uF_0402x4 , 22uF_0603 x1

PP1800_SOC_A

C97 1u/6.3V_4, C100 1u/6.3V_4, C98 1u/6.3V_4, C102 1u/6.3V_4, C106 22u/6.3V_6

PP3300_SOC_A

C414 1u/6.3V_4, C416 1u/6.3V_4, C417 1u/6.3V_4, C418 1u/6.3V_4, C432 22u/6.3V_6

PP3300_SOC_A

C90 1u/6.3V_4

PP3300_SOC_A: 1uF_0402x8 , 22uF_0603 x2

PP3300_SOC_A

C91 1u/6.3V_4, C92 1u/6.3V_4, C103 22u/6.3V_6

PP3300_SOC_A

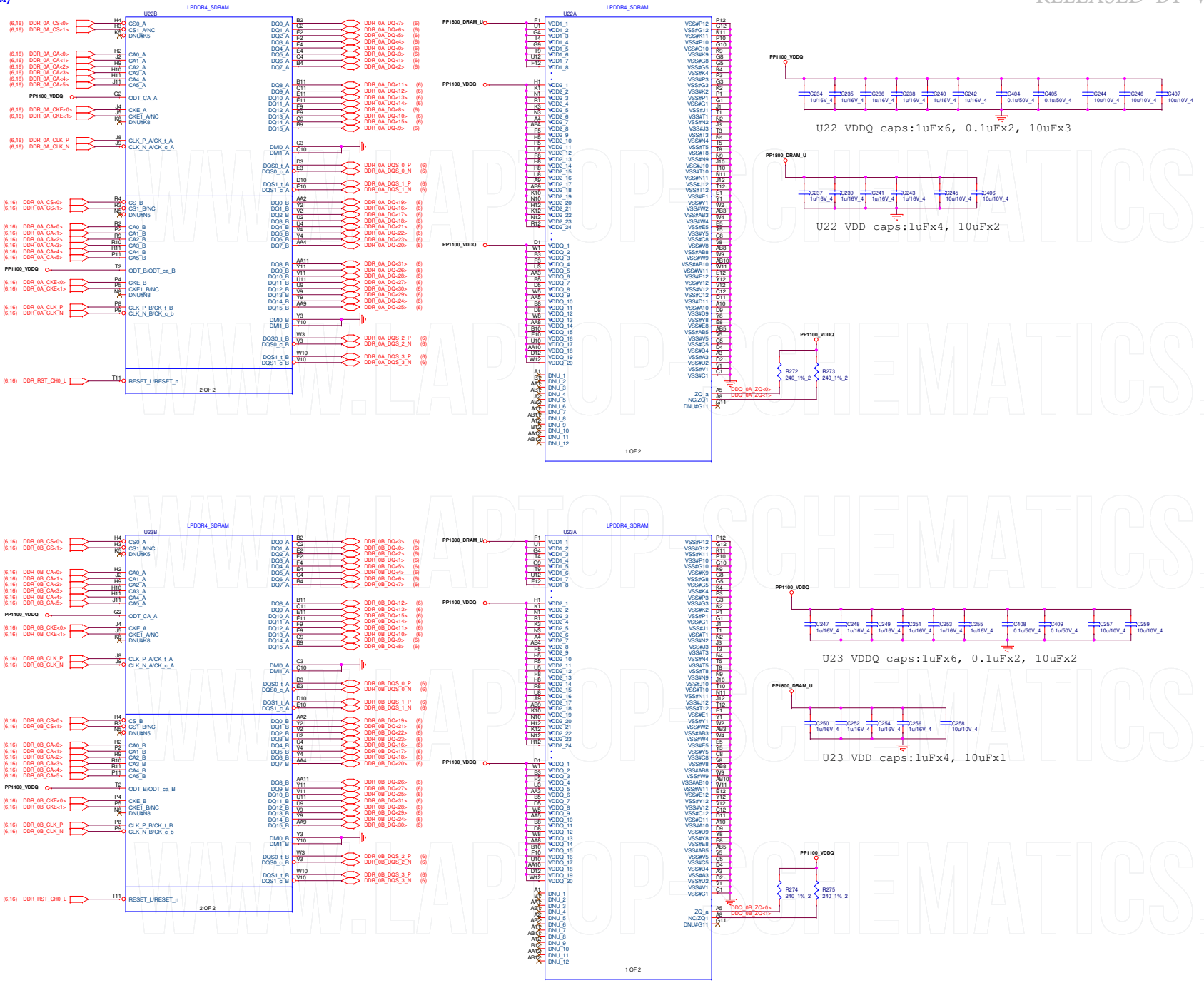
C107 1u/6.3V_4

Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

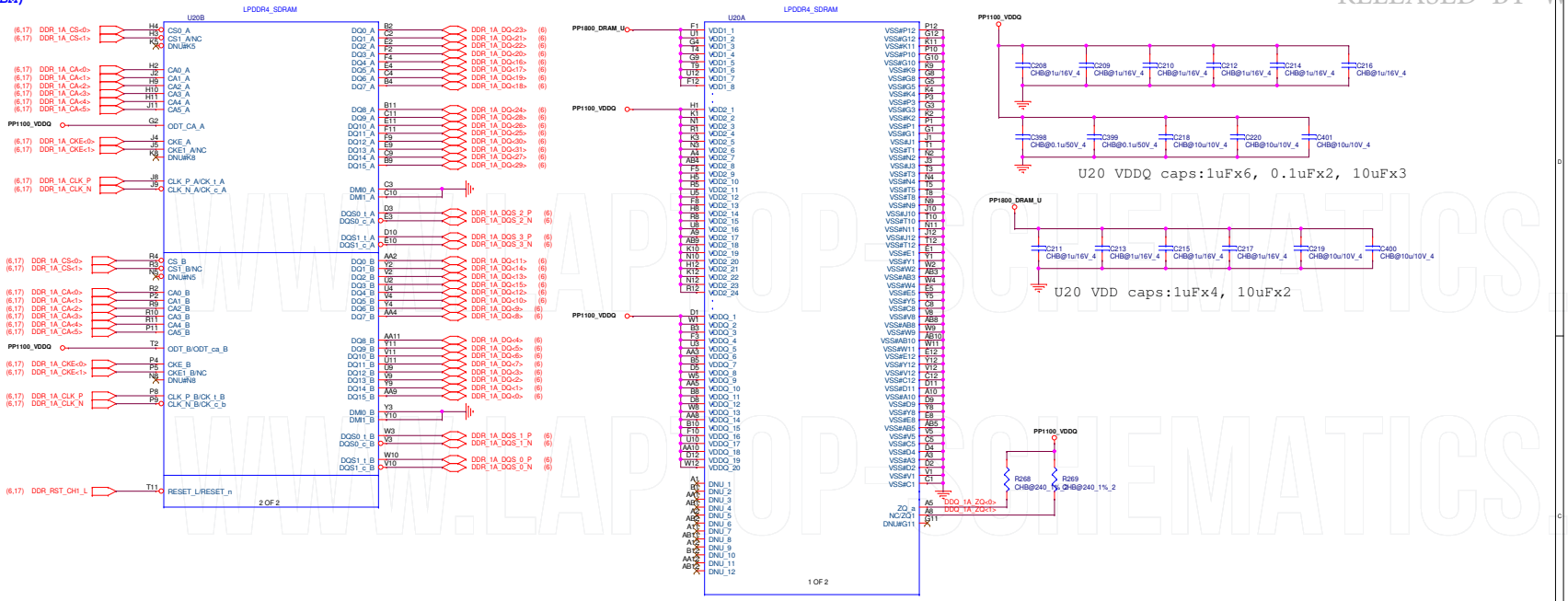
| Size | Document Number | Rev |
|---|---|---|
| | SOC DECOUPLING | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 15 of 45 | |

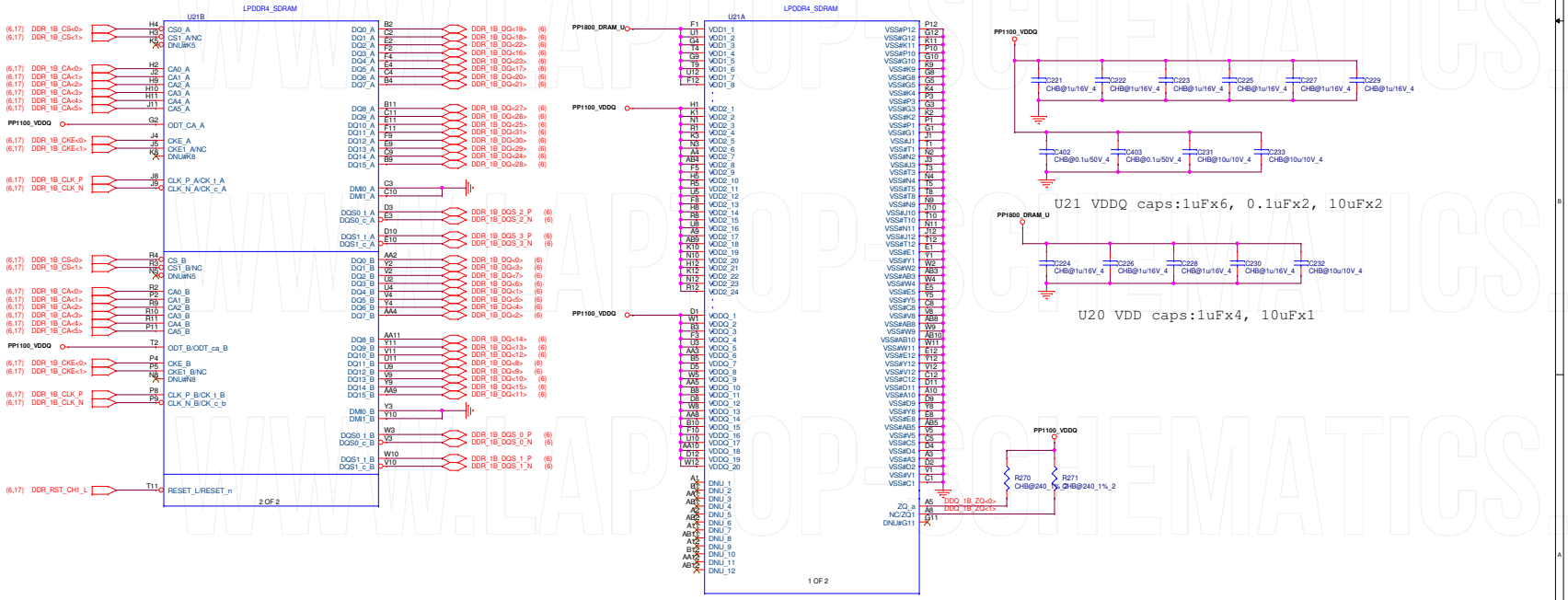
(OBM)




| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : ZBC_DROID_BLORB | |
| Size | Document Number: MEMORY CH 00/01 LPDDR4 — Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 16 of 45 |

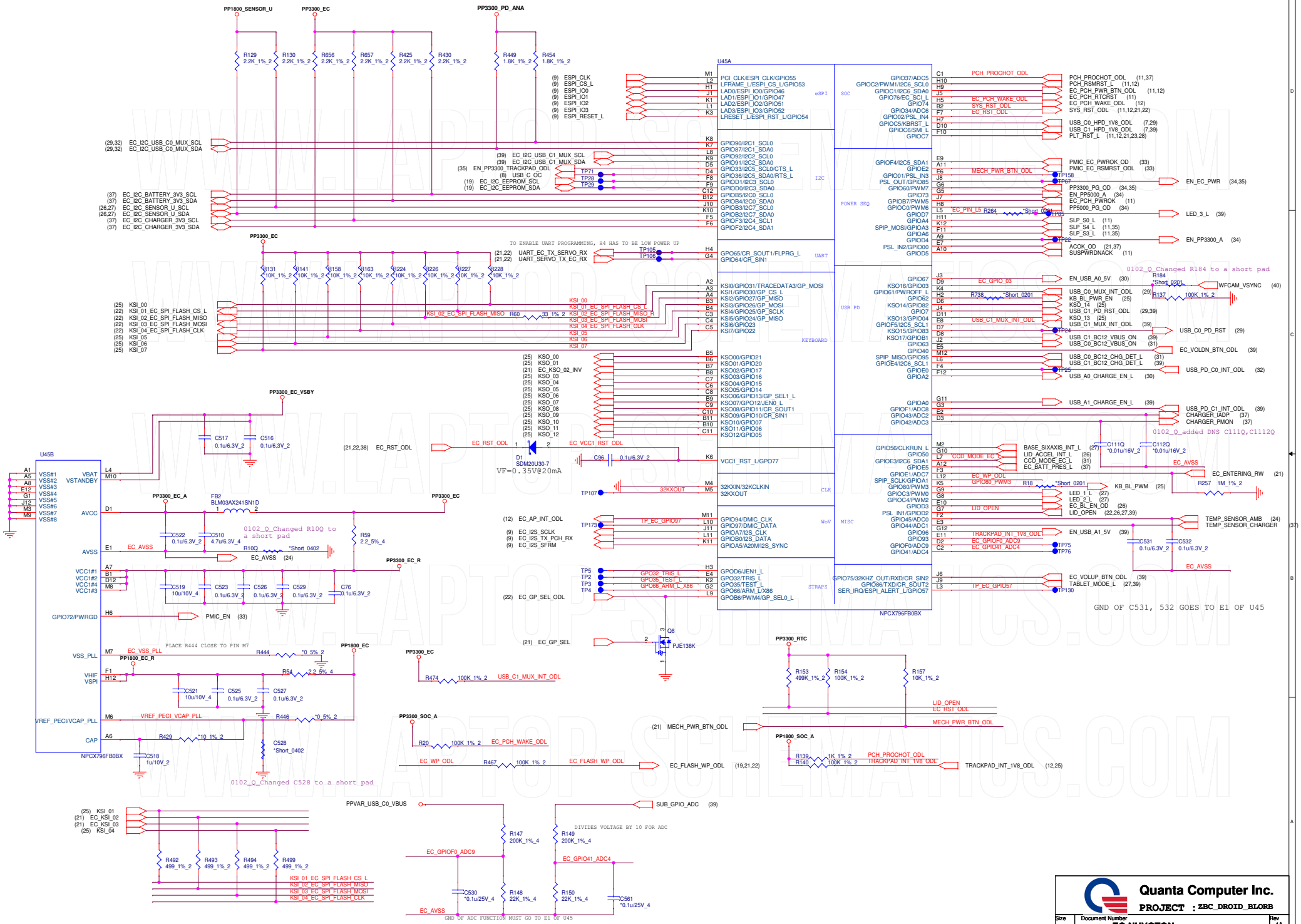
(OBM)



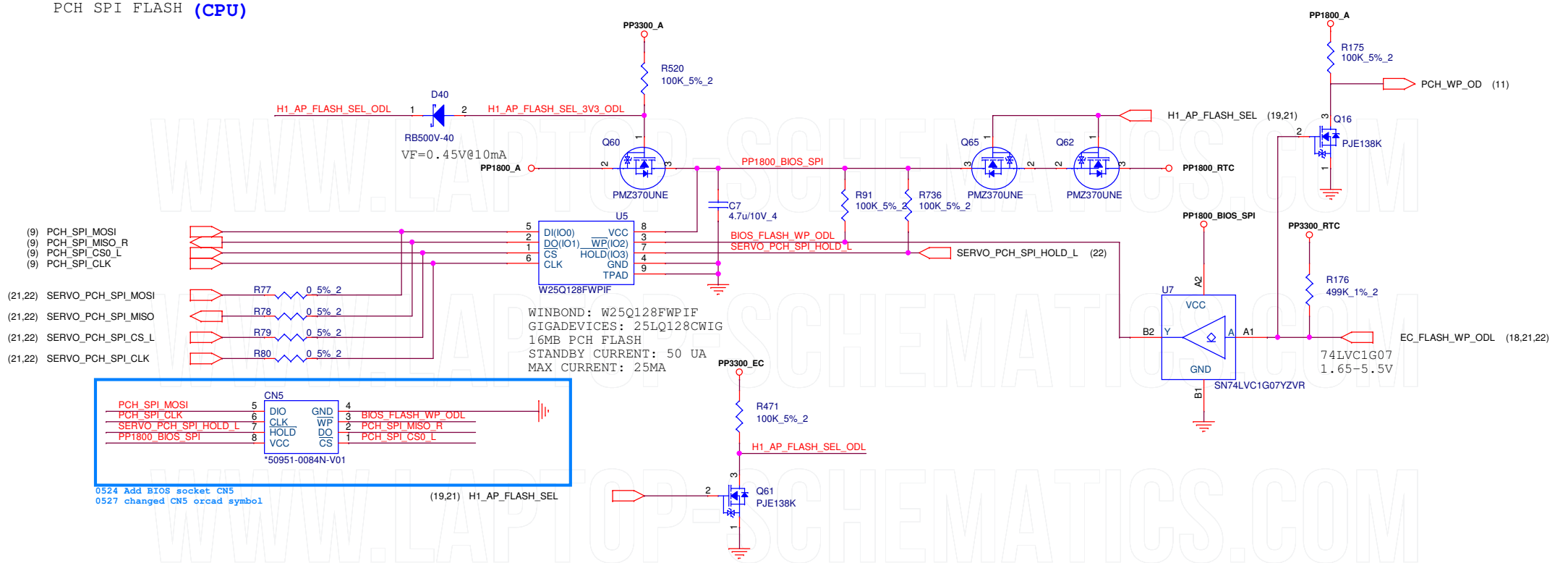




| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : ZBC_DROID_BLORB | | | |
| Size | Document Number | | Rev |
| | MEMORY CH 10/11 LPDDR4 | | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 17 of 45 | | |

(KBC)

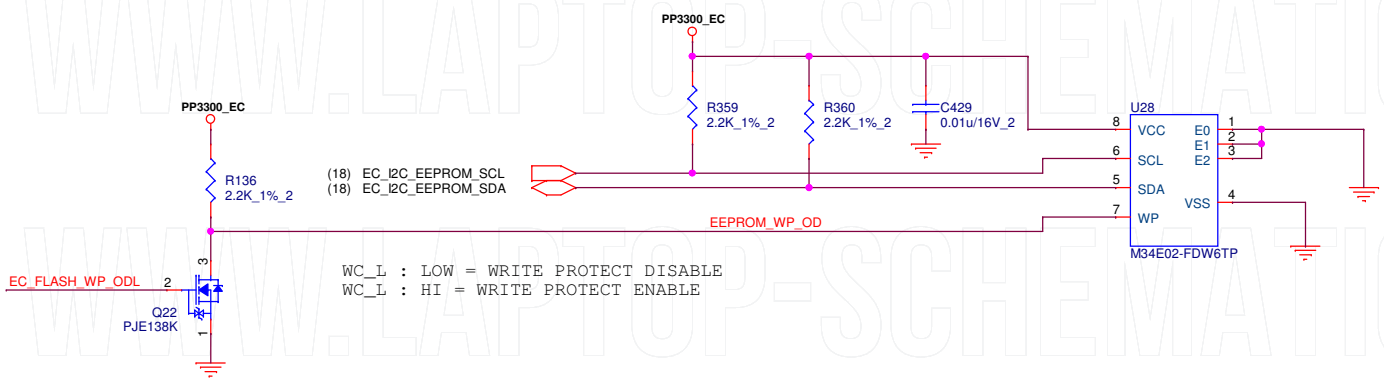


## PCH SPI FLASH (CPU)




## (KBC)

SKU EEPROM




Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | SPI ROM | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 19 of 45 | |

(INT)

PP1800_A

C505 *1u/16V_4

C506 *0.1u/16V_2

LAYOUT NOTE: PLACING THE SERIAL R'S WITHIN 1 " OF THE DEBUG CONNECTOR

PP1800_A

PP1800_A

J5

*QSH-030-01-L-D-A-K-TR

(12) TCK
(12) TDI
(12) TRST_L
(12) CX_PRDY_L
(12) DBG_PTI_CLK0
(7) GP_INTD_DSI_TE2
(12) DBG_PTI_DATA_0
(12) DBG_PTI_DATA_1
(12) DBG_PTI_DATA_2
(12) DBG_PTI_DATA_3
(12) DBG_PTI_DATA_4
(12) DBG_PTI_DATA_5
(12) DBG_PTI_DATA_6
(12) DBG_PTI_DATA_7
(12) DBG_PTI_DATA_8
(12) DBG_PTI_DATA_9
(12) DBG_PTI_DATA_10
(12) DBG_PTI_DATA_11
(12) DBG_PTI_DATA_12
(12) DBG_PTI_DATA_13
(12) DBG_PTI_DATA_14
(12) DBG_PTI_DATA_15
(12) DBG_PTI_CLK1

DBG_PMU_PLTRST_L

R627 *0_5%_2

R601 *0_5%_2

TMS (12)
TDO (12)
DBG_PMU_RSTBTN_L
TRSTPD
CX_PREQ_L (12)
R602 *0_5%_2
DBG_PTI_CLK2 (12)
DBG_PTI_DATA_16 (12)
DBG_PTI_DATA_17 (12)
DBG_PTI_DATA_18 (12)
DBG_PTI_DATA_19 (12)
DBG_PTI_DATA_20 (12)
DBG_PTI_DATA_21 (12)
DBG_PTI_DATA_22 (12)
DBG_PTI_DATA_23 (12)
DBG_PMU_RSTBTN_L (12)
BOOT_HALT_L (12)
DBG_PMU_PLTRST_L (12)
DBG_PMU_PWRBTN_L (12)
DBG_RSMRST_L (12)
DCI_DATA_PTITRACE3_0 (12)
DBG_PTI_DATA_TRACE3_1 (12)
DBG_PCH_I2C_SCL (10)
DBG_PCH_I2C_SDA (10)
DBG_PTI_DATA_TRACE3_2 (12)
PCHTX_MIPI60RX_UART (10)
PCHRX_MIPI60TX_UART (10)
R623 *0_5%_2
DCI_CLK_PTICLK3 (12)

DBG_PMU_RSTBTN_L
DBG_PMU_PLTRST_L
DBG_PMU_PWRBTN_L

PP1800_A

C507 *1u/16V_4

C508 *0.1u/16V_2

R199 *10K_1%_2

DBG_PMU_RSTBTN_L

C93 *0.01u/16V_2

DBG_PMU_PWRBTN_L

C78 *0.01u/16V_2

Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | MIPI60 DEBUG HEADER | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 20 of 45 | |

# (H1C)

KEEP NEAR TPM/SPI ROM TO MINIMIZE SPI STUBS
PLACE TERMINATION NEAR DIVIDE

(10) H1_SLAVE_SPI_MOSI_R — R782 33_5% 2 — H1_SLAVE_SPI_MOSI
(10) H1_SLAVE_SPI_CLK_R — R792 33_5% 2 — H1_SLAVE_SPI_CLK
(10) H1_SLAVE_SPI_CS_L_R — R793 33_5% 2 — H1_SLAVE_SPI_CS_L
(10) H1_SLAVE_SPI_MISO — R794 33_5% 2 — H1_SLAVE_SPI_MISO_R

PP3300_RTC — R813 *Short_0603 — PP3300_VDDIOM
R450 *Short_0603 — PP3300_VDDIOB
PP1800_RTC — R451 *Short_0603 — C386 0.1u/10V_2 — PP1800_VDDIOA
PP3300_VDDIOM — R857 30.9K_1%_2
ADDED TO MATCH 3MS DELAY — C439 0.1u/10V_2

C378 4.7u/6.3V_4 | C387 0.1u/10V_2 | C388 0.1u/10V_2 | C389 0.1u/10V_2

PP3300_VDDIOM — 1226_Q_added 499K PU to PP3300_VDDIOM on H1_BATT_PRES_L as in 2.82 change list
R90Q 499K_1%_2

PP1800_SOC_A — R443 10K_5%_2 — D33 SDM20U30-7 — VF=0.35V@20mA
(10) H1_PCH_INT_ODL

PP1800_VDDIOA — R445 *10K_5%_2 | R501 10K_5%_2
0527 DNS R445 for PP1800_A leakage issue

(22) H1_BOOT_UART_RX

U37 — UR0605B-FT021

(22) RESET_H1_ODL — G1 RESETB

VDD3P3_IOA / VDD3P3_IOB — 1.8V
VDD3P3_IOM_1 / VDD3P3_IOM_2 / VDD3P3_IOM_3 — 1.8V

DIOM0 C1 — R873 *Short_0201 — SYS_RST_ODL (11,12,18,22)
DIOM1 B1 — R874 *Short_0201 — CCD_MODE_ODL (31)
DIOM2 A1 — R875 *Short_0201 — H1_BATT_PRES_L (37)
DIOM3 A2 — R876 *Short_0201 — PLT_RST_L (11,12,18,23,28)
DIOM4 A3

PP3300_VDDIOM — R561 10K_5%_2

DIOA0 B9 — (22) H1_BOOT_UART_TX — TP60
DIOA1 D8 — (10) PCH_I2C_H1_SDA — R334 *0_5%_2 — DIOA1
DIOA2 C9 — H1_SLAVE_SPI_MOSI
DIOA3 E8 — (10,22) PCHTX_SERVORX_UART
DIOA4 D9 — H1_SPI_MOSI
DIOA5 F8 — H1_PCH_INT_L
DIOA6 F9 — H1_SLAVE_SPI_CLK
DIOA7 G8 — (10,22) PCHRX_SERVOTX_UART
DIOA8 G9 — H1_SPI_CLK
DIOA9 H8 — (10) PCH_I2C_H1_SCL — R335 *0_5%_2 — DIOA9
DIOA10 H9 — H1_SLAVE_SPI_MISO_R
DIOA11 J9 — H1_SPI_MISO
DIOA12 J8 — H1_SLAVE_SPI_CS_L
DIOA13 H7 — H1_BOOT_UART_RX — TP58
DIOA14 J7 — H1_SPI_CS_L

DIOB0 J6 — (22,36) DEBUG_I2C_SCL
DIOB1 H6 — (22,36) DEBUG_I2C_SDA
DIOB2 J5 — EC_GP_SEL
DIOB3 H5 — H1_AP_FLASH_SEL
DIOB4 J3 — H1_BOOT_CONFIG
DIOB5 H4 — (18,22) UART_SERVO_TX_EC_RX
DIOB6 J2 — (18,22) UART_EC_TX_SERVO_RX
DIOB7 J1 — (36) EN_PP3300_INA_H1_ODL

(18) EC_GP_SEL
(19) H1_AP_FLASH_SEL
(22) H1_BOOT_CONFIG
R472 10K_5%_2 | R473 10K_5%_2 | R203 10K_5%_2

DIOB4 - GND, BUT HAD INTERNAL PD - TIE MAY NOT BE NECESSARY

USBAN E1 — R304 *0_5%_2
USBAP F1 — R308 *0_5%_2
USBBN E2 — R310 *Short_0201
USBBP F2 — R306 *Short_0201
(31) USB_C0_SBU1 — R855 *Short_0201 — H1_USB_C0_SBU1
(31) USB_C0_SBU2 — R856 *Short_0201 — H1_USB_C0_SBU2
0102_Q_Changed R306,R310 to a short pad

R169 2M_1%_2 | R204 2M_1%_2 | R172 2M_1%_2 | R178 2M_1%_2

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11

DIOR0 A4 — EC_RST_ODL (18,22,38)
DIOR1 B4 — DIOR2 — MECH_PWR_BTN_IN_ODL (22,25)
DIOR2 A5
DIOR3 B5 — EC_KSO_02_INV (18)
DIOR4 A6 — ACOK_OD — EC_ENTERING_RW (18)
DIOR5 B6 — R999 1K_1%_2
DIOR6 B7 — EC_FLASH_WP_ODL (18,19,22)
DIOR7 A8 — DIOR8 — MECH_PWR_BTN_ODL (18)
DIOR8 B8
DIOR9 A9 — EC_IN_RW_OD — KSO_02 (25)
DIOR10 B9
DIOR11 C8 — BAT_DISABLE_ODL (37)

PP3300_VDDIOM — R529 100K_1%_2 — ACOK_OD (18,37)
PP1800_SOC_A — R448 100K_5%_2 — EC_IN_RW_OD (11)

RDCC1 D1 — H1_RDCC1 — R859 *0_5%_2 — USB_C0_CC1 — USB_C0_CC1 (29,31)
RDCC2 D2 — H1_RDCC2 — R860 *0_5%_2 — USB_C0_CC2 — USB_C0_CC2 (29,31)

NC#1 H2 | NC#2 D3 | NC#3 C3 | NC#4 D4 | NC#5 C5 | NC#6 D5 | NC#7 C6 | NC#8 D6 | NC#9 C7 | NC#10 D7 | NC#11 D3 | NC#12 C5 | NC#13 D6 | NC#14 D7 | NC#15

PP5000_LDO — C577 0.1u/10V_2

U8 — VDD | OUT2 | OUT1 | VSS | IN2_N | IN2_P | IN1_N | IN1_P — TLV8802DGKR
R718 10K_1%_2 — OP_OUT2 — OP_OUT2
R719 10K_1%_2 — OP_OUT1 — OP_OUT1
R720 100K_1%_2 — USB_C0_CC2
R721 100K_1%_2 — USB_C0_CC1

FOR EC FLASH PROGRAMMING

H1_SPI_CS_L — R417 33_5%_2 — SERVO_PCH_SPI_CS_L
H1_SPI_MISO — R409 33_5%_2 — SERVO_PCH_SPI_MISO
H1_SPI_MOSI — R410 33_5%_2 — SERVO_PCH_SPI_MOSI
H1_SPI_CLK — R413 33_5%_2 — SERVO_PCH_SPI_CLK

PP1800_VDDIOA — C445 *0.1u/10V_2

U56 — *SN74LVC126ARGYRG4
H1_AP_FLASH_SEL — 1OE
H1_SPI_CS_L — 1A — 1Y — SERVO_PCH_SPI_CS_L — SERVO_PCH_SPI_CS_L (19,22)
2OE
H1_SPI_MOSI — 2A — 2Y — SERVO_PCH_SPI_MOSI — SERVO_PCH_SPI_MOSI (19,22)
3OE
H1_SPI_CLK — 3A — 3Y — SERVO_PCH_SPI_CLK — SERVO_PCH_SPI_CLK (19,22)
4OE
(19,22) SERVO_PCH_SPI_MISO — SERVO_PCH_SPI_MISO — 4A — 4Y — H1_SPI_MISO
VCC | VIA#1 VIA#2 VIA#3 VIA#4 OE_IO GND

stuffing option for different KB

DIOR2 — R565 0_5%_2 — KSI_02 — KSI_02 (25)
R566 *0_5%_2 — KSI_03 — KSI_03 (25)
EC_KSI_03 — R5671 0_5%_2 — KSI_03
EC_KSI_02 — R567 *0_5%_2 — KSI_02
DIOR8 — R568 0_5%_2 — EC_KSI_02 — EC_KSI_02 (18)
R569 *0_5%_2 — EC_KSI_03 — EC_KSI_03 (18)

PP1800_VDDIOA — R412 *1M_1%_2 | R414 1M_1%_2 | R416 1M_1%_2 | R419 *4.7K_1%_2
H1_SLAVE_SPI_CLK — DIOA1
DIOA9 — H1_SLAVE_SPI_CS_L
R162 1M_1%_2 | R165 *1M_1%_2 | R166 *1M_1%_2 | R432 1M_1%_2
STRAPS : SPI FOR CONVERTIBLE/CLAMPSHELL

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZBC_DROID_BLORB | | |
| Size | Document Number: H1 SECURE MICROCONTROLLER | Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 21 of 45 | |

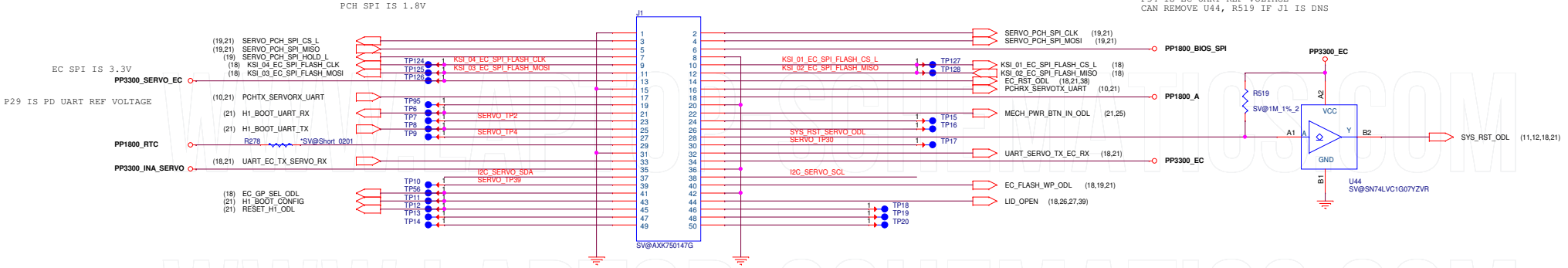
(GOG)

PCH SPI IS 1.8V

P18 IS PCH UART REF VOLTAGE
P34 IS EC UART REF VOLTAGE
CAN REMOVE U44, R519 IF J1 IS DNS

EC SPI IS 3.3V

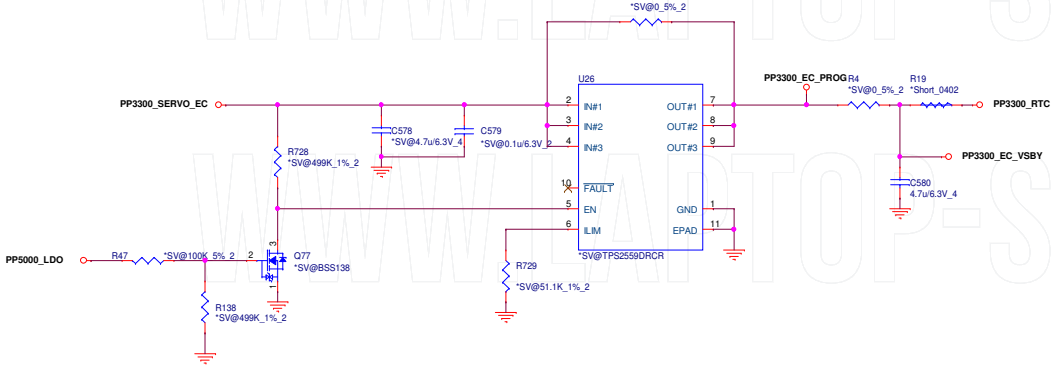
P29 IS PD UART REF VOLTAGE



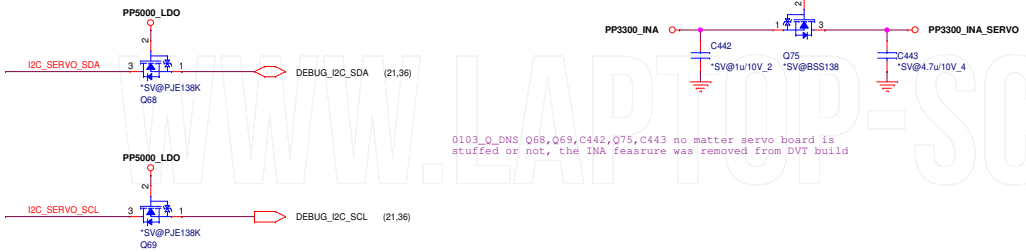

## SERVO HEADER (H1C)

POWER FOR FLASHING EC THROUGH SERVO

CAN REMOVE U44, U26, Q77, C578, C579, R128, R47, R138 R519 IF J1 IS DNS




CAN REMOVE Q68, Q69 IF J1 IS DNS




0103_Q_DNS Q68,Q69,C442,Q75,C443 no matter servo board is stuffed or not, the INA feasrure was removed from DVT build

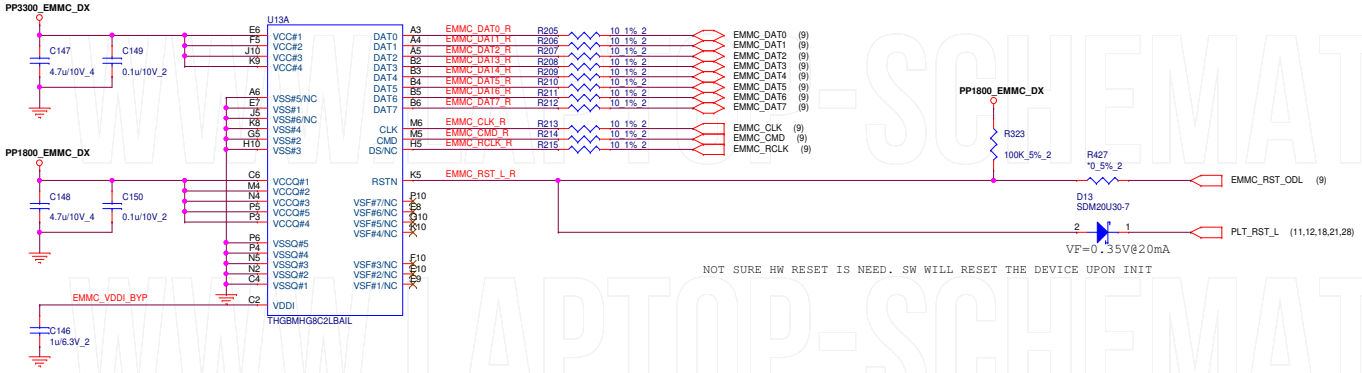
Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

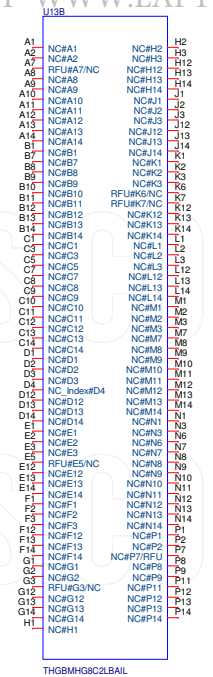
| Size | Document Number | Rev |
|---|---|---|
| | SERVO | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 22 of 45 | |

(MMC)

# 32 GB EMMC STORAGE

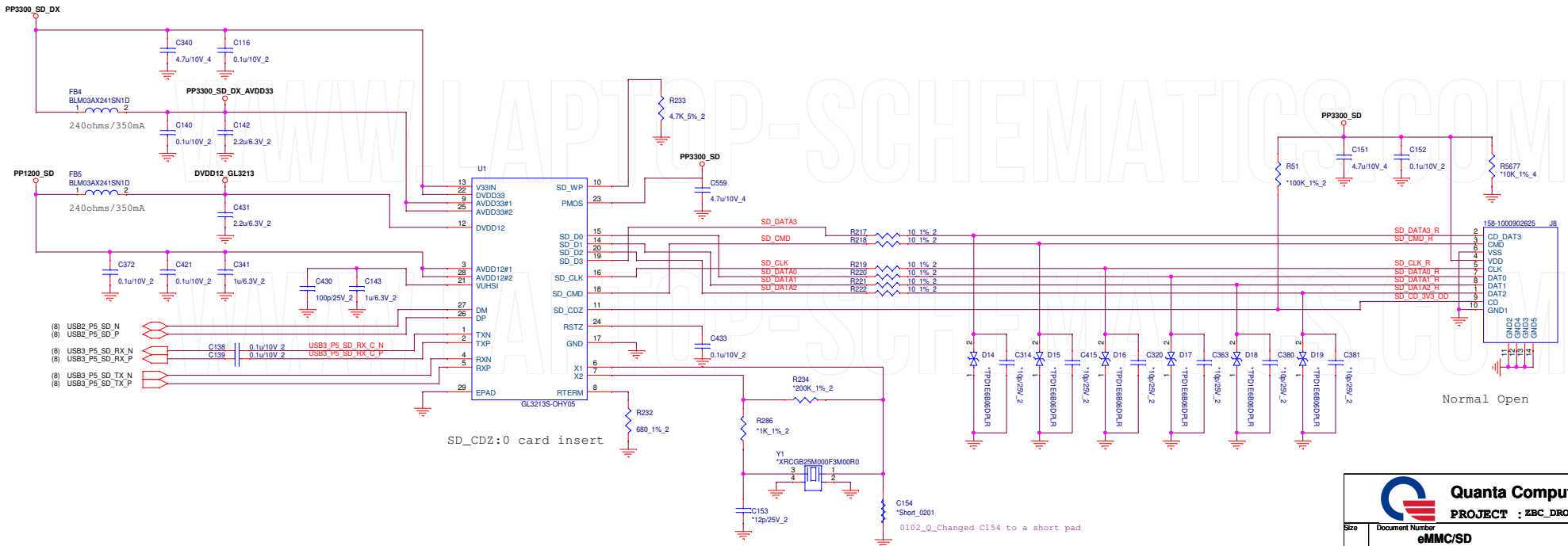
150 UA SLEEP CURRENT




(CRD)

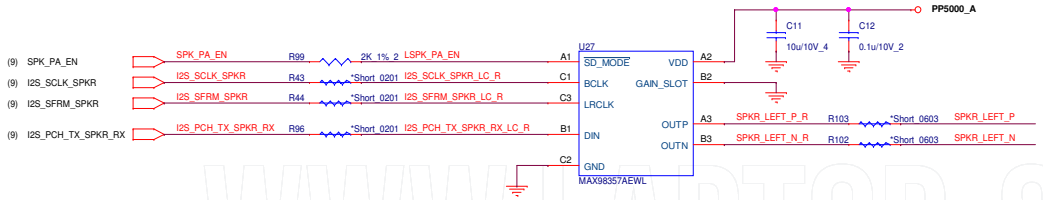
# MICRO SD CARD




| | | | |
|---|---|---|---|
| Quanta Computer Inc. | | | |
| PROJECT : ZBC_DROID_BLORB | | | |
| Size | Document Number | | Rev |
| | eMMC/SD | | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 23 of 45 | | |

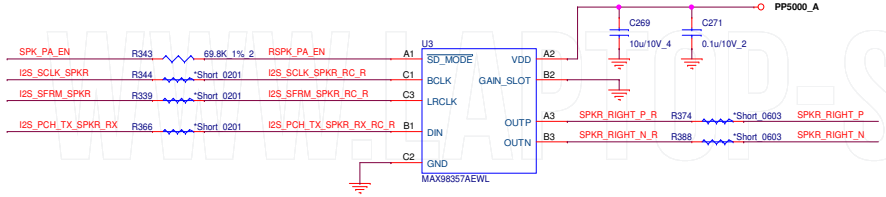
## (AMP)

### LEFT CHANNEL



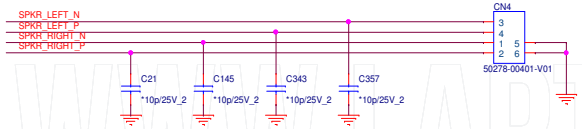

LEFT CHANNEL = SHORT (OR 2K FOR SAFETY) TO 1.8V
GAIN_SLOT: 100K TO GND = 15 DB GAIN
GAIN_SLOT: 0 TO GND = 12 DB GAIN
GAIN_SLOT: UNCONNECTED = 9 DB GAIN
GAIN_SLOT: 0 TO VDD = 6 DB GAIN
GAIN_SLOT: 100K TO VDD = 3 DB GAIN

### RIGHT CHANNEL

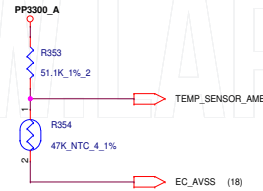



RIGHT CHANNEL = 69.8K TO 1.8V
GAIN_SLOT: GND = 12 DB GAIN

## (ADO)



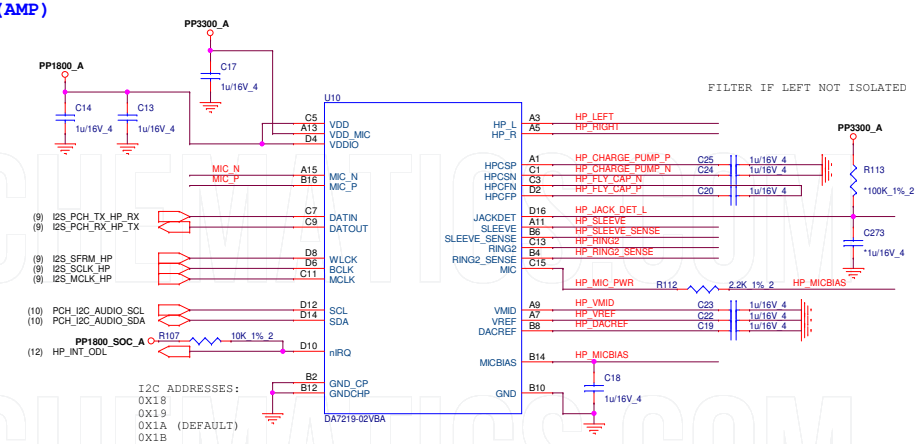

## (THM)




Note for placement, it
needs to be placed near CPU
requested by thermal team

CSP PACKAGE, BUT CAN BE ROUTED ON TYPE-3
<10UA IN DEEP SLEEP

## (AMP)

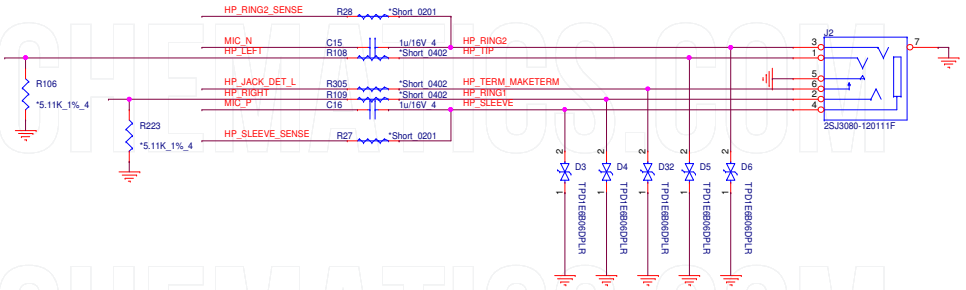



I2C ADDRESSES:
0X18
0X19
0X1A (DEFAULT)
0X1B

FILTER IF LEFT NOT ISOLATED

## (ADO)

5K TO FILTER LEFT IF NOT ISOLATED




| | | | |
|---|---|---|---|
| Audio Jack | 11" ZBA/ZBB | 1st | DFTJ06FRA33 |
| | | 2nd | DFTJ06FRA54 |
| | 14"/15" ZBC/ZBD | 1st | DFTJ06FRA44 |
| | | 2nd | DFTJ06FR985 |

CHANGED MIC SERIES CAPS TO 1UF TO MATCH 10HZ 3DB
FREQUENCY RECOMMENDED IN THE DA7219 DATASHEET

THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL
THE SAME APPLIES TO HP_SLEEVE AND HP_SLEEVE_SENSE SIGNALS
ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | AUDIO | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 24 of 45 | |

# PEN/STYLUS CONNECTOR

TOUCHSCREEN AND PEN/STYLUS POWER TOGETHER

PEN 7-BIT I2C ADDRESS = 0X09
~ 100 MA

(PEN)

TOUCHSCREEN + STYLUS ( IF AVAILABLE )

PP1800_A
PP1800_EC
C344 PEN@4.7u/10V_4
R682 PEN@100K_5%_2
Q59 PEN@AO3415
PP1800_PEN_R
R684 *Short_0.1_1%_4
PP1800_PEN_DX
C345 PEN@0.22u/10V_2
04/15 change to 0.1 ohm
07/18 change to shortpad
R683 PEN@200_1%_2
(12,35) EN_PP3300_TOUCHSCREEN
Q58 PEN@PJE138K

PP1800_A
PP1800_PEN_DX
R5148 100K_5%_2
(12) PEN_PDCT_ODL
PEN_PDCT_CONN_ODL
*PEN@PJE138K Q835
R5157 *PEN@Short_0201
0102_Q_Changed R5157,R5158 to a short pad

PP1800_A
PP1800_PEN_DX
R5159 100K_5%_2
(12) PEN_INT_ODL
PEN_INT_CONN_ODL
*PEN@PJE138K Q837
R5158 *PEN@Short_0201

STUFF R5148,R5159,R5157,R5158 DEFAULT
IF LEAKAGE FOUND, STUFF Q835,Q837,R514,R515
AND DEPOP R5157,R5158,R5148,R5159

PP1800_PEN_DX
R514 *PEN@100K_5%_2
R515 *PEN@100K_5%_2
(10) PCH_I2C_PEN_1V8_SDA
(10) PCH_I2C_PEN_1V8_SCL
J22
PP3300_PEN_DX
PP1800_PEN_DX
PEN_PDCT_CONN_ODL
PEN_INT_CONN_ODL
PEN_RESET_ODL
PEN@50208-00801-V02

PP3300_PEN_DX
R513 PEN@100K_5%_2
(12) PEN_RESET
Q83 PEN@PJE138K

(KBL)

05/02 Change Q90 to AO3409 because of Vgs:11.6V
PPVAR_SYS
PPVAR_SYS_KB_BL_DX_R
R164
PPVAR_SYS_KB_BL_DX
R751 KBL@100K_5%_2
Q90 KBL@AO3409
KBL@0.1_1%_4
(18) KB_BL_PWR_EN
Q89 KBL@PJE138K
R750 KBL@100K_5%_2

(12) PEN_EJECT
J19 PEN@196479-04041-3_PEN_4Pin

PEN_EJECT FOR GARAGED STYLUS. IT WILL BE A WAKE SOURCE

(KBC)

## KEYBOARD

CM TO CHOOSE CONNECTOR- THIS ONE WILL SUPPORT THE KEYPAD SO THE PINOUT MAY NEED TO CHANGE

J9
KSO_12 KSO_08 KSO_09 KSO_11 KSO_10
KSO_05 KSO_06
KSO_03 KSO_02 KSI_00 KSO_01 KSO_04 KSI_03 KSI_02 KSO_00 KSI_05 KSI_04 KSO_07 KSI_06 KSI_07 KSI_01 KBD_PWR_BTN_ODL KSO_13 KSO_14
TP40 TP46
G2 G1 51646-0300N-V01

D26 D27 D28 D25 D30 D29
GND
*TPD4E101DPWR

STUFF THESE FOR KEYBOARD LOCK BUTTON

KSO_09 KSI_03
0 ohm for BOM option
(FSW)
R246 SW@0_5%_2
R248 SW@0_5%_2
KBD_PWR_BTN_GND
KBD_PWR_BTN_ODL
R247 NSW@0_5%_2
R249 NSW@0_5%_2
MECH_PWR_BTN_IN_ODL

THE PURPOSE OF THIS CIRCUIT
IS TO ALLOW A SINGLE KEYBOARD
MATRIX FOR BOTH A CONVERTIBLE
AND CLAMSHELL SKU

(21,22) MECH_PWR_BTN_IN_ODL
STUFF THESE FOR KEYBOARD POWER BUTTON

PP3300_RTC
R250 10K_5%_2
D21 TPD1E6B06DPLR
SW3
SW@NTC316-AD1T-A160T-A

| | |
|---|---|
| Convertible | R246,R248,SW3 STUFF ; R247,R249 NC |
| Clamshell | R247,R249 STUFF ; R246,R248,SW3 NC |

(KBL)

KEYBOARD BACKLIGHT CONN
IF=0.2A, VF=0.3~0.35V @IF=20~40mA

PPVAR_SYS_KB_BL_DX
L17 KBL@22uH_2.5x2.0x1.2
PHT25201B-220MS
D31 KBL@PMEG3002AEL
C583 KBL@1u/25V_4
U30 KBL@TPS61161DRVR
VIN SW FB CTRL COMP TPAD1 TPAD2 GND PAD
(18) KB_BL_PWM
C584 KBL@0.22u/10V_2
C585 KBL@2.2u/50V_6
R754 KBL@4.7_5%_2
KBL@50505-00401-V01
J23

## TRACKPAD CONNECTOR

CM TO CHOOSE CONNECTOR

(TPD)

PP3300_TRACKPAD_DX
0102_Q_Changed R72 to a short pad
R72 *Short_0201
R253 10K_5%_2
C190 10u/10V_4
C192 1u/6.3V_2
C195 0.1u/10V_2
PP1800_SOC_A
(12,18) TRACKPAD_INT_1V8_ODL
Q47B PMDXB600UNE
Q47A PMDXB600UNE
(10) PCH_I2C_TRACKPAD_3V3_SDA
(10) PCH_I2C_TRACKPAD_3V3_SCL
TRACKPAD_INT_3V3_ODL
TRACKPAD_BTN_L
TP32
J12
50506-00601-V01

AVOIDS ANY LEAKAGE WITHOUT SOFTWARE EFFORTS

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | KB, TP, PEN | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 25 of 45 | |

EDP2-EDP3 DOES NOT NEED TO ROUTE TO CONNECTOR

EDP + MIC + SENSOR +CAMERA CONNECTOR

(LDS)

(MIC)

(FCM)

(LDS)

(FCM)

(LDS)

(TSN)

(TSN)

LID ACCEL-CORAL

(ACS)

I2C MODE: ( SET BY NCS TIE TO VDDIO )
I2C 8bit ADDRESS: 0X3E (SDO_ADDR = VDDIO)
I2C MAX SPEED = 3.4MHZ

WFC CAMERA

(RCM)

WFC INTERFACE PINOUT TBD. PENDING CHANGE

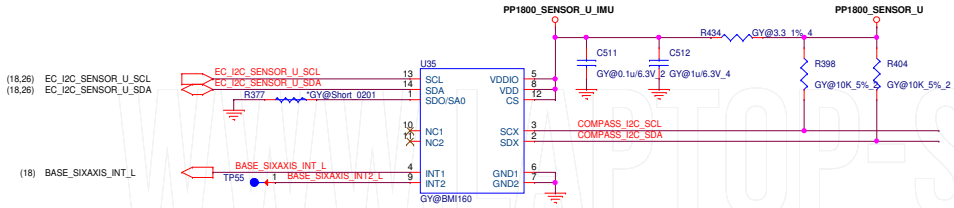
DMIC 1.8V POWER

0102_Q_Changed R225 to a short pad

2nd source:
DK150VPU002/LP-MSM150/24

| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : ZBC_DROID_BLORB | |
| Size | Document Number: LID(eDP/CAM/TOUCH/SENSOR) Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 26 of 45 |

(GRS)




IMU

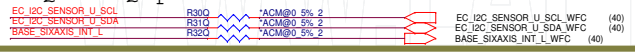
MODE 2 (SLAVE TO EC, MASTER TO MAG)

I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 7'0X68 (LSB SET BY SD0/SA0) -->8'0xD0h

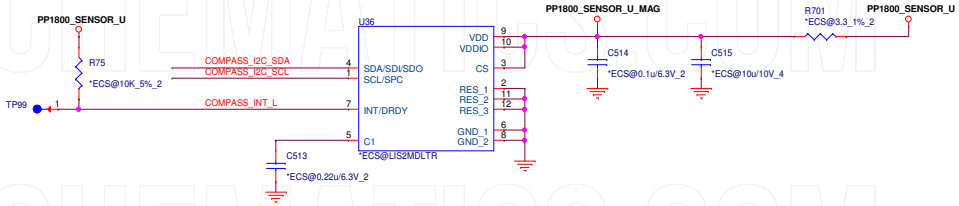
(ACM)

0 ohm for BOM option

R30Q~R32Q place near to IMU U35




(ECS)




MAGNETOMETER

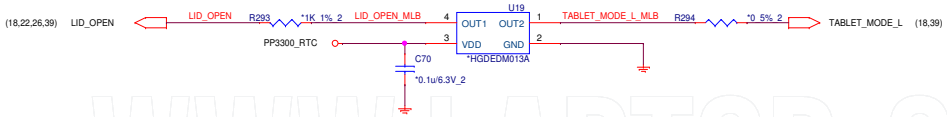
SLAVE TO IMU SENSOR

I2C MODE: SET BY CS PIN TO HI
I2C ADDR: 0X1E

for AR Camera, IMU can be DNS, but R30Q,R31Q,R32Q need to be stuffed

GMR SENSOR (RESERVED FOR ON BOARD SITUATIOM

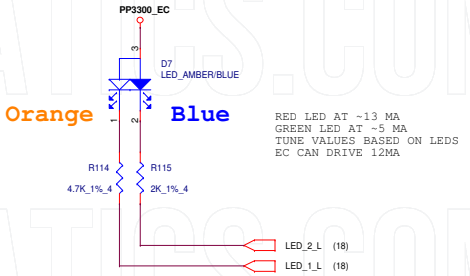
(GMR_MLB) For on board GMR




MAKE SURE TO CHECK THE POLARITY OF MAGNET TO ASSIGN THE PIN LID-OPEN AND TABLET-MODE
IF THE GMR SENSOR IS NOT PLACED ON THE MLB, PLEASE CAREFULLY PLAN THE PINOUT ON THE SUB-BOARD INTERFACE.

(UIF)

CHARGE/BATTERY LED




RED LED AT ~13 MA
GREEN LED AT ~5 MA
TUNE VALUES BASED ON LEDS
EC CAN DRIVE 12MA

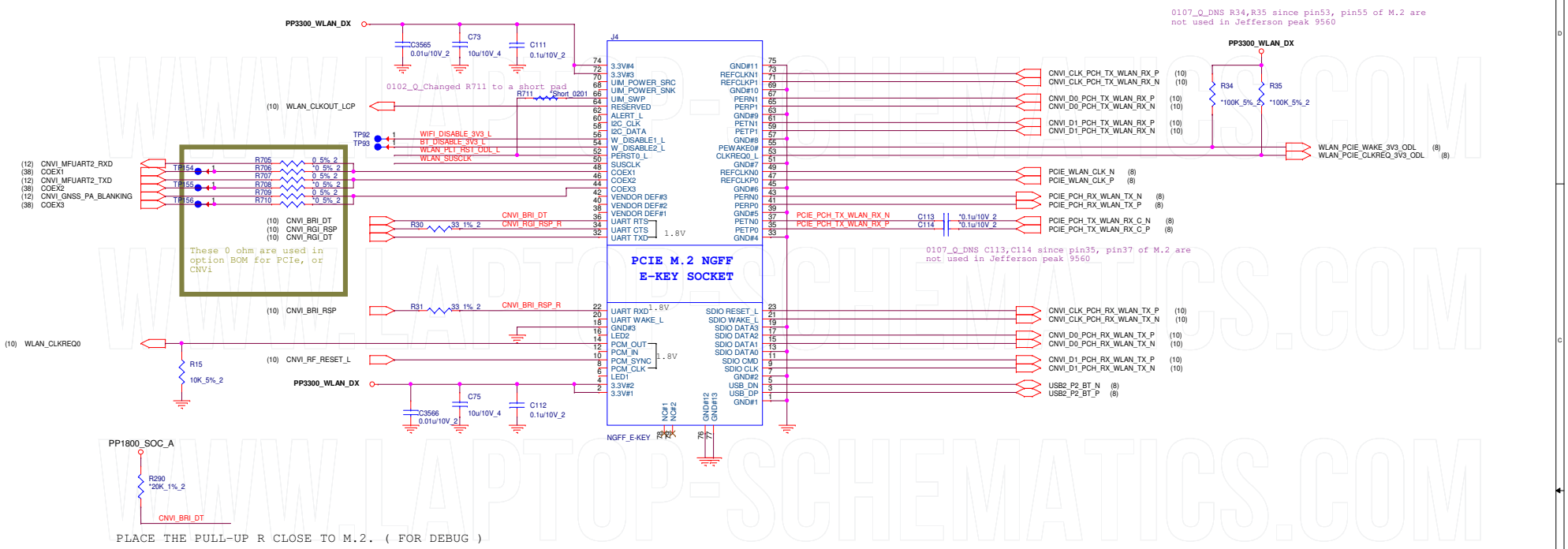
Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

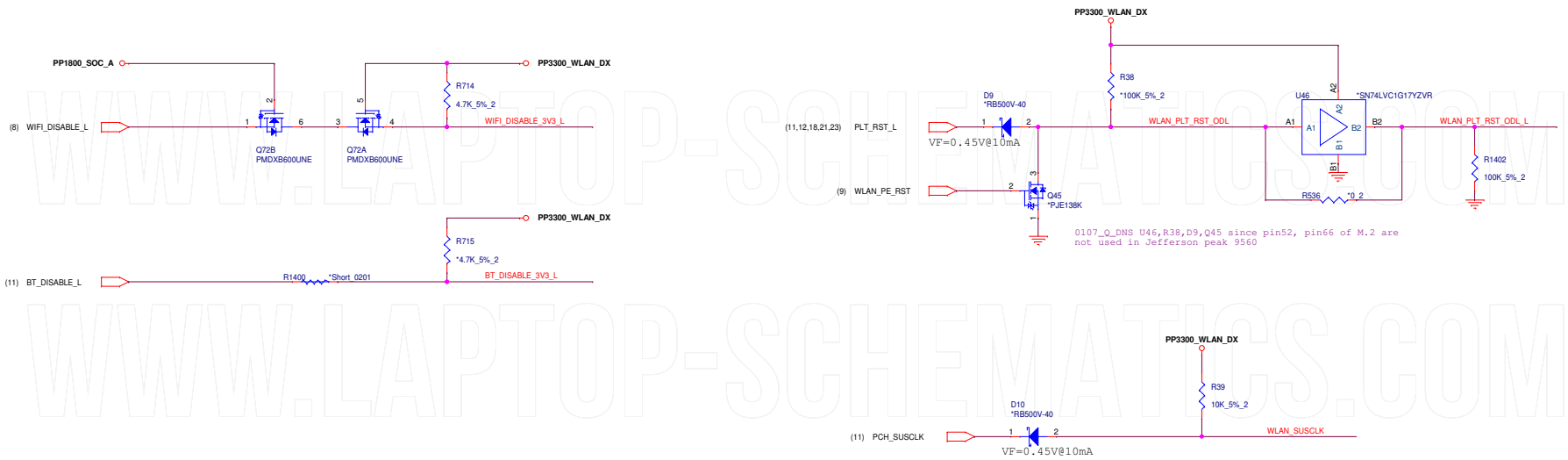
| Size | Document Number | Rev |
|---|---|---|
| | SENSOR(COMPASS/GYRO)(OP1) | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 27 of 45 | |

# WIFI

CM TO CHOOSE CONNECTOR

**(NGF)**



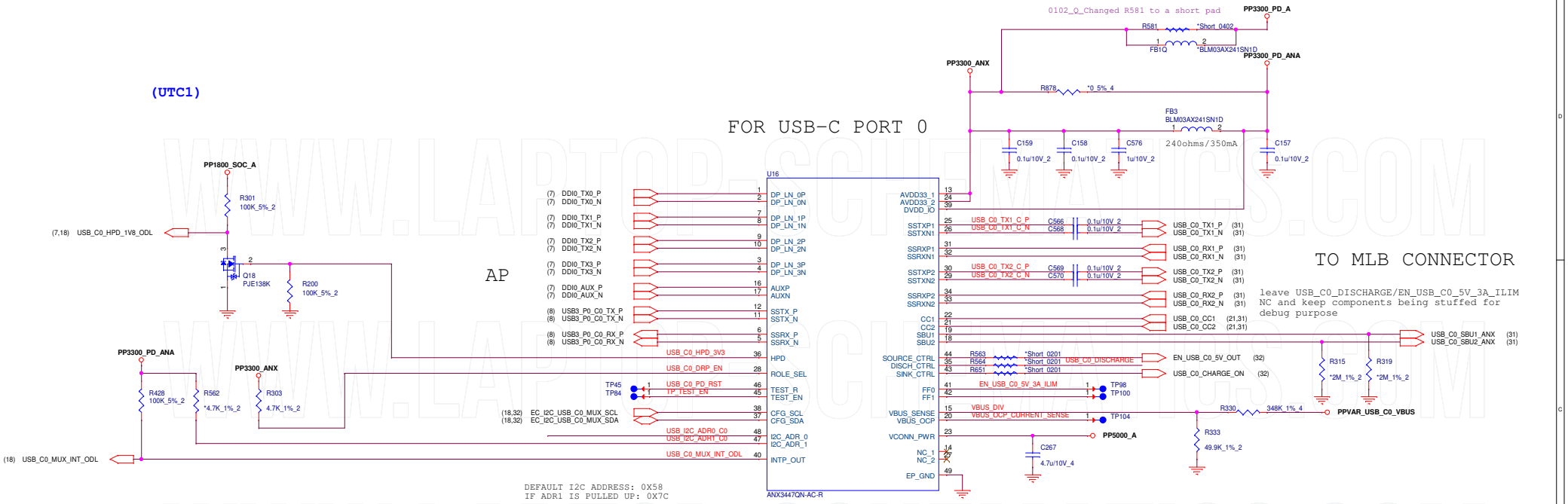




U46,R38,D9,Q45,C113,C114,R34,R35,Q1,Q2 need to be stuffed for WiFi flexible design

| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZBC_DROID_BLORB | | |
| Size | Document Number: WIFI/BT CONNECTOR | Rev 1A |
| Date: Tuesday, November 05, 2019 | Sheet 28 of 45 | |

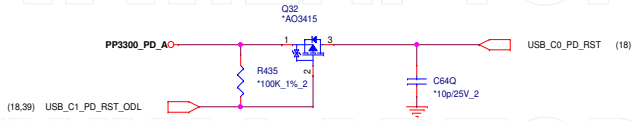
(UTC1)

FOR USB-C PORT 0




DEFAULT I2C ADDRESS: 0X58
IF ADR1 IS PULLED UP: 0X7C

WITH THE NX20P3483, THE VBUS DISCHARGE CAN BE SW CONTROL



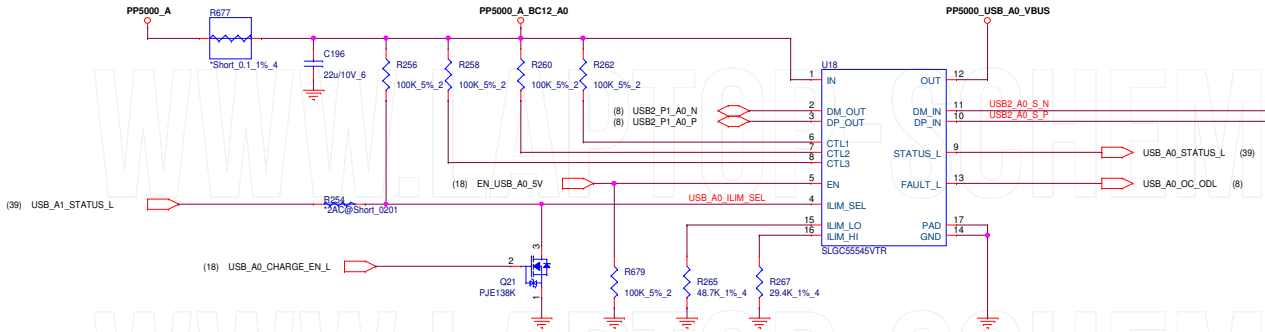

USB_C0_PD_RST IS ACTIVE HIGH WITH 100K INTERNAL PD

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | USB C TCPC/MUX(OP2) | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 29 of 45 | |

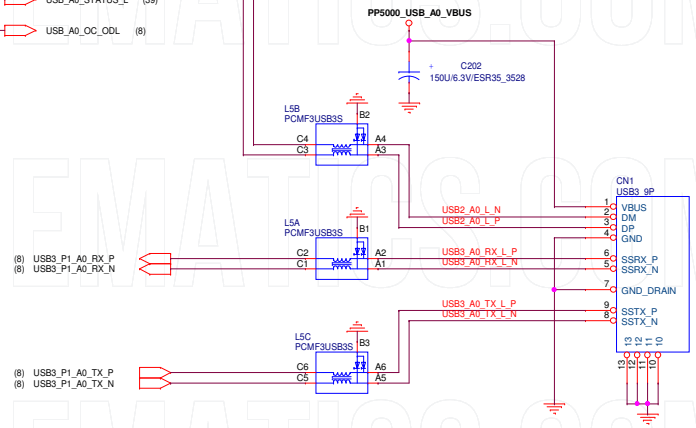
# BC 1.2 FOR THE TYPE-A PORT A0

(UBC1)




(UB31)

CM TO CHOOSE CONNECTOR




| | | | |
|---|---|---|---|
| USB3.0 Type-A conn | 11" ZBA/ZBB | 1st | DFHS09FR780 |
| | | 2nd | DFHS09FR790 |
| | 14" ZBC | 1st | DFHS09FR937 |
| | | 2nd | DFHS09FR936 |
| | 15" ZBD | 1st | DFHS09FRB05 |
| | | 2nd | DFHS09FRB06 |
| | | 3rd | DFHS09FRB07 |



Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | USB A CONNECTIONS(MLB) | 1A |

Date: Tuesday, November 05, 2019 Sheet 30 of 45

(UTC1)

# TYPE-C PORT 0 BC1.2

PP3300_EC
R692 100K_5%_2
USB_C0_BC12_CHG_DET_L
USB_C0_BC12_CHG_DET_L (18)
Q63 PJE138K
PP5000_A
Q66 BSS84AKM
C82 1u/10V_2
R694 100K_5%_2
Q71 PJE138K
USB_C0_BC12_VBUS_ON
USB_C0_BC12_VBUS_ON (18)
R196 100K_5%_2
U54
CHG_DET
VBUS
DP_HOST
DM_HOST
DP_CON
DM_CON
SW_OPEN
CHG_AL_N
GOOD_BAT
GND
MAX14637CVB+T
USB_C0_BC12_CHG_DET
VBUS_C0_BC12
USB2_P0_C0_P
USB2_P0_C0_N
(8) USB2_P0_C0_P
(8) USB2_P0_C0_N
R5678 *100K_5%_2
TP122
R182 *0_5%_4
R183 *0_5%_4
USB2_0_C0_P
USB2_0_C0_N
R886 1M_1%_2
R893 1M_1%_2
L6A
L6B
L6C
PCMF3USB3S
L7A
L7B
PCMF2USB3S
(29) USB_C0_RX1_N
(29) USB_C0_RX1_P
(29) USB_C0_TX1_N
(29) USB_C0_TX1_P
(29) USB_C0_RX2_N
(29) USB_C0_RX2_P
(29) USB_C0_TX2_N
(29) USB_C0_TX2_P
PPVAR_USB_C0_VBUS
C82Q *10u/35V_6
(21,29) USB_C0_CC1
(21,29) USB_C0_CC2
(21) USB_C0_SBU1
(21) USB_C0_SBU2
J13
VBUS1
VBUS2
VBUS3
VBUS4
CC1
CC2
RFU1
RFU2
DM1
DP1
DM2
DP2
SSRX1_N
SSRX1_P
SSTX1_N
SSTX1_P
SSRX2_N
SSRX2_P
SSTX2_N
SSTX2_P
GND1
GND2
GND3
GND4
GND5
GND6
SHIELD1
SHIELD2
NC#1
NC#2
AUSB0295-P007A
0102_Q_Changed J13 Footprint

PP3300_VDDIOM
PP3300_EC
R41 100K_5%_2
R89 100K_5%_2
(21) CCD_MODE_ODL
CCD_MODE_ODL
CCD_MODE_EC_L (18)
Q300B PMDXB600UNE
Q300A PMDXB600UNE

ONLY TIME CCD_DISENGAGE_SBU IS HIGH WHEN CCD_MODE IS INACTIVE AN THERE IS POWER TO THE TCPC

0102_Q_Changed R3109 to a short pad
PP5000_A
PP5000_LDO
R3109 *Short_0201
R3111 *0_5%_2
D23 RB500V-40
R291 22K_1%_4
C3112 0.01u/16V_2
CCD_DISENGAGE_SBU
R437 *0_5%_2
Q25 PMZ370UNE
(29) USB_C0_SBU1_ANX
USB_C0_SBU1
(29) USB_C0_SBU2_ANX
USB_C0_SBU2
Q28 PMZ370UNE
R439 *0_5%_2
PP3300_VDDIOM
Q3108 PJE138K
CCD_MODE_ODL

CAREFULLY PLACE THE FETS, AVOID LONG STUB

(UTC1)

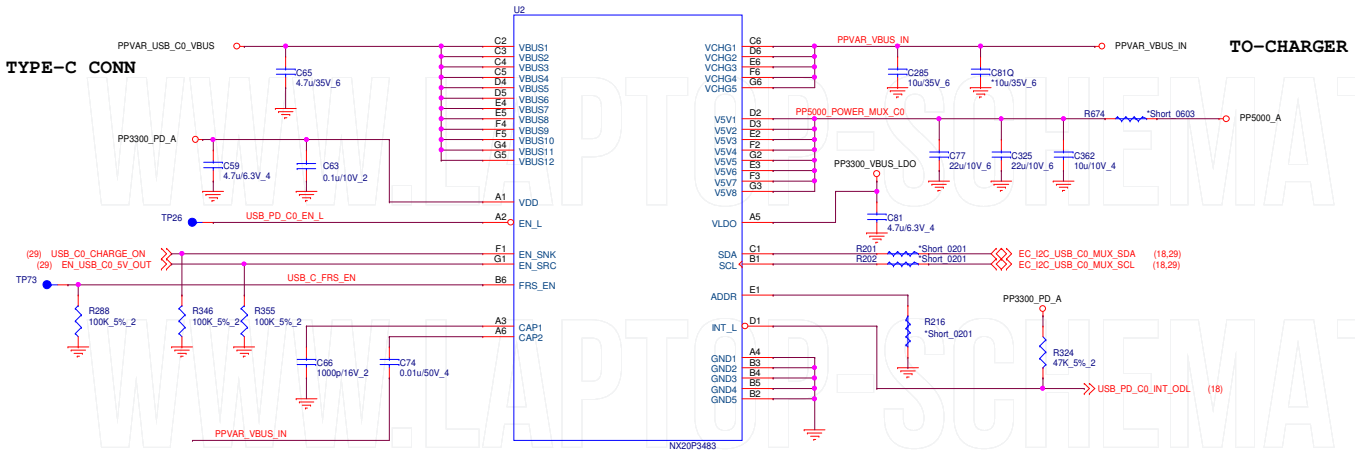
USB_C0_CC1
USB_C0_CC2
USB_C0_SBU1
USB_C0_SBU2
D22 TPD4E101DPWR
C86 1000p/25V_2
C181 1000p/25V_2
C18002 *330p/50V_4
C18003 *330p/50V_4

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB
Size
Document Number
USB C CONNECTOR ( MLB )
Rev 1A
Date: Tuesday, November 05, 2019
Sheet 31 of 45

## PORT 0

PROVIDES ESD PROTECTION, PLACE CLOSE TO CONNECTOR

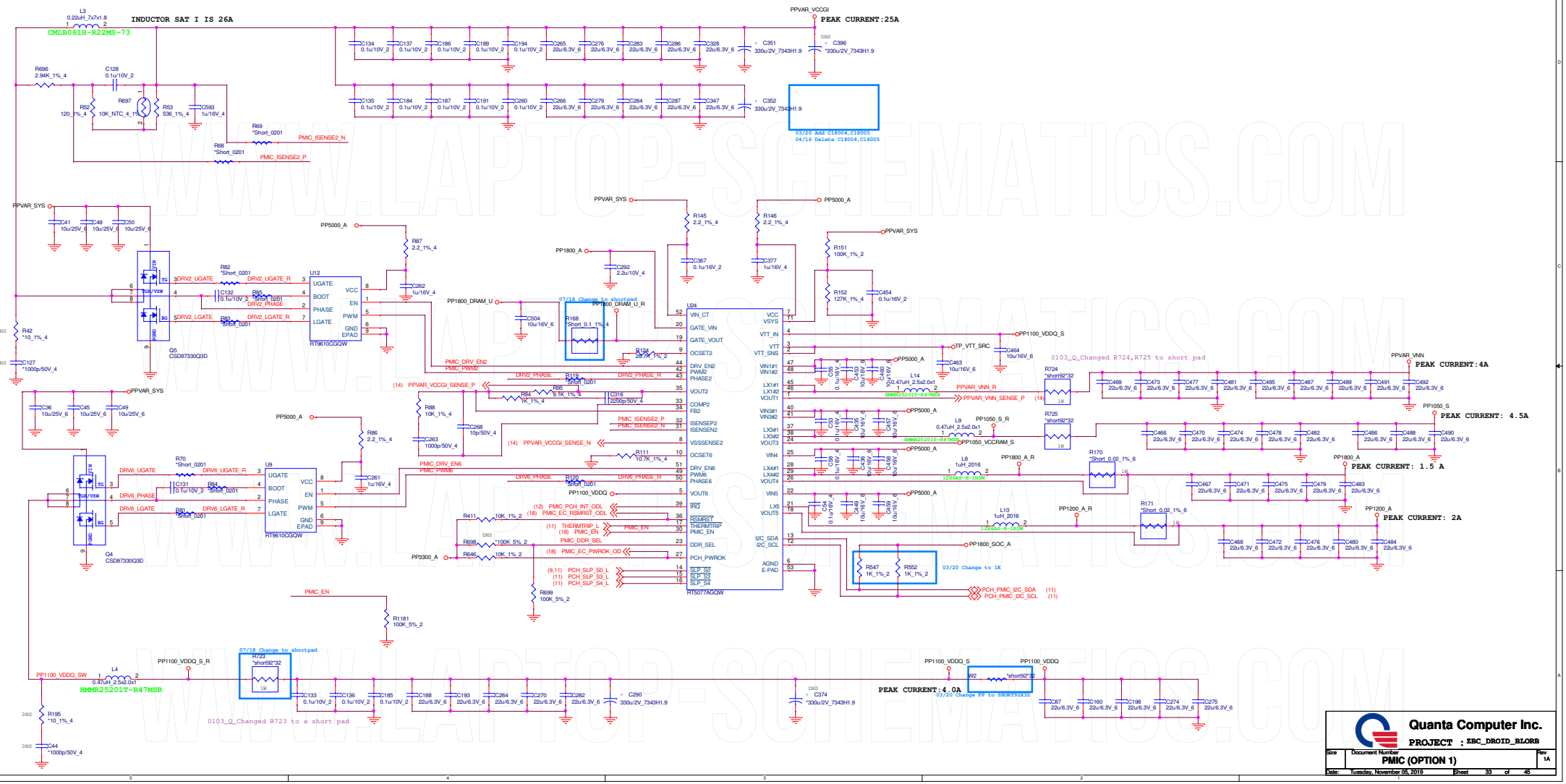
(PUB1)






| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZBC_DROID_BLORB | | |
| Size | Document Number: USB C VBUS CONTROL | Rev: 1A |
| Date: Tuesday, November 05, 2019 | Sheet 32 of 45 | |

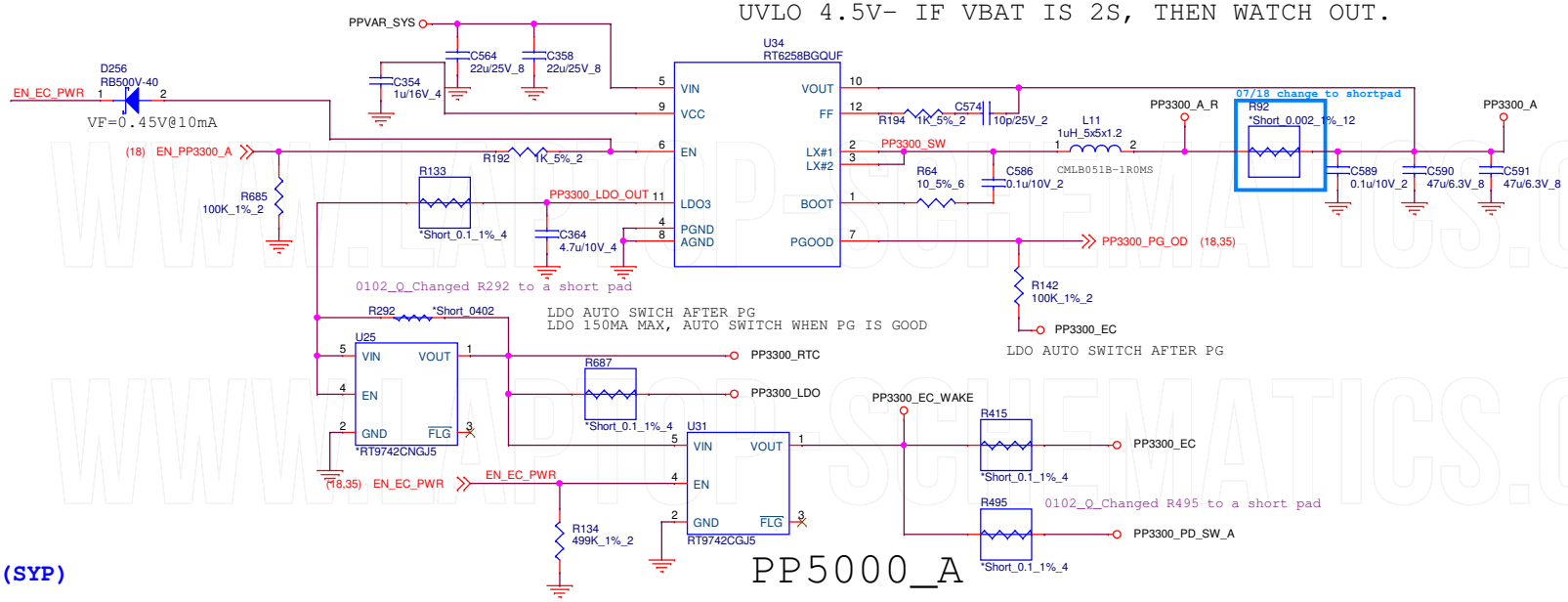
(PMC)



(SYP)

# PP3300_A

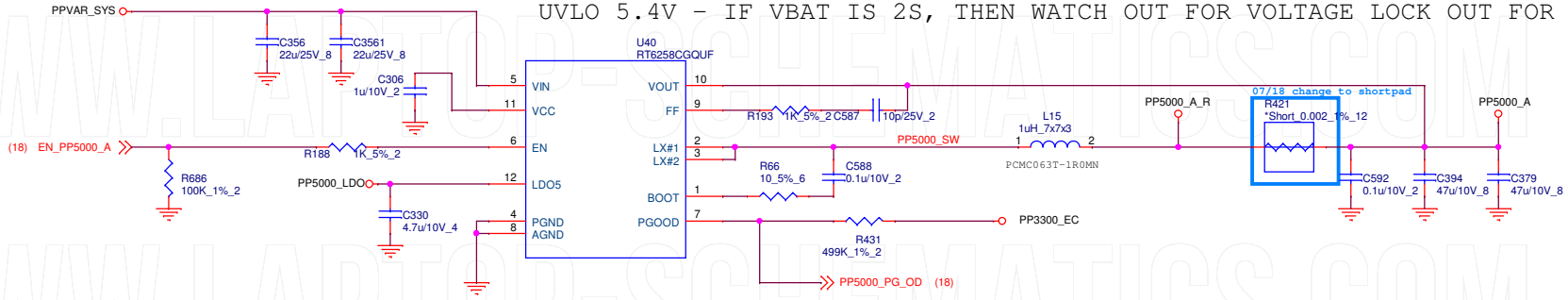
UVLO 4.5V- IF VBAT IS 2S, THEN WATCH OUT.




(SYP)

# PP5000_A

UVLO 5.4V - IF VBAT IS 2S, THEN WATCH OUT FOR VOLTAGE LOCK OUT FOR 1.8V



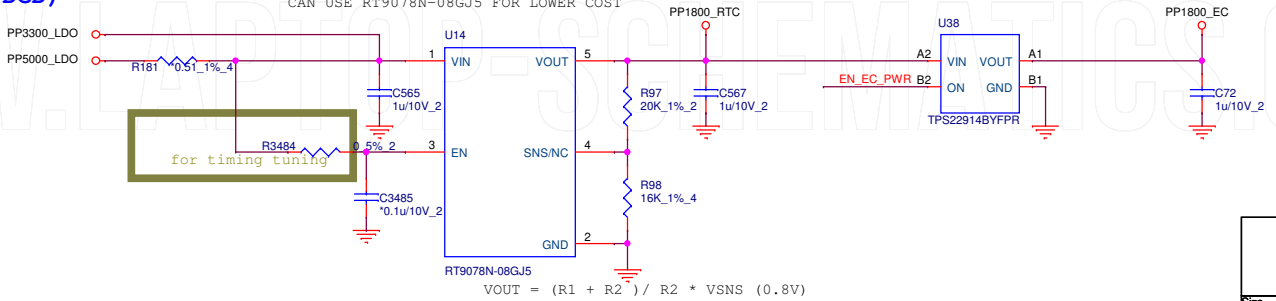

# PP1800_RTC, PP1800_EC

(DCD)

PP1800_RTC CAN BE GENERATED BY A SEPARATE DC-DC R

CAN USE RT9078N-08GJ5 FOR LOWER COST

PP1800_EC CAN BE GENERATED BY A SEPARATE REGULATOR

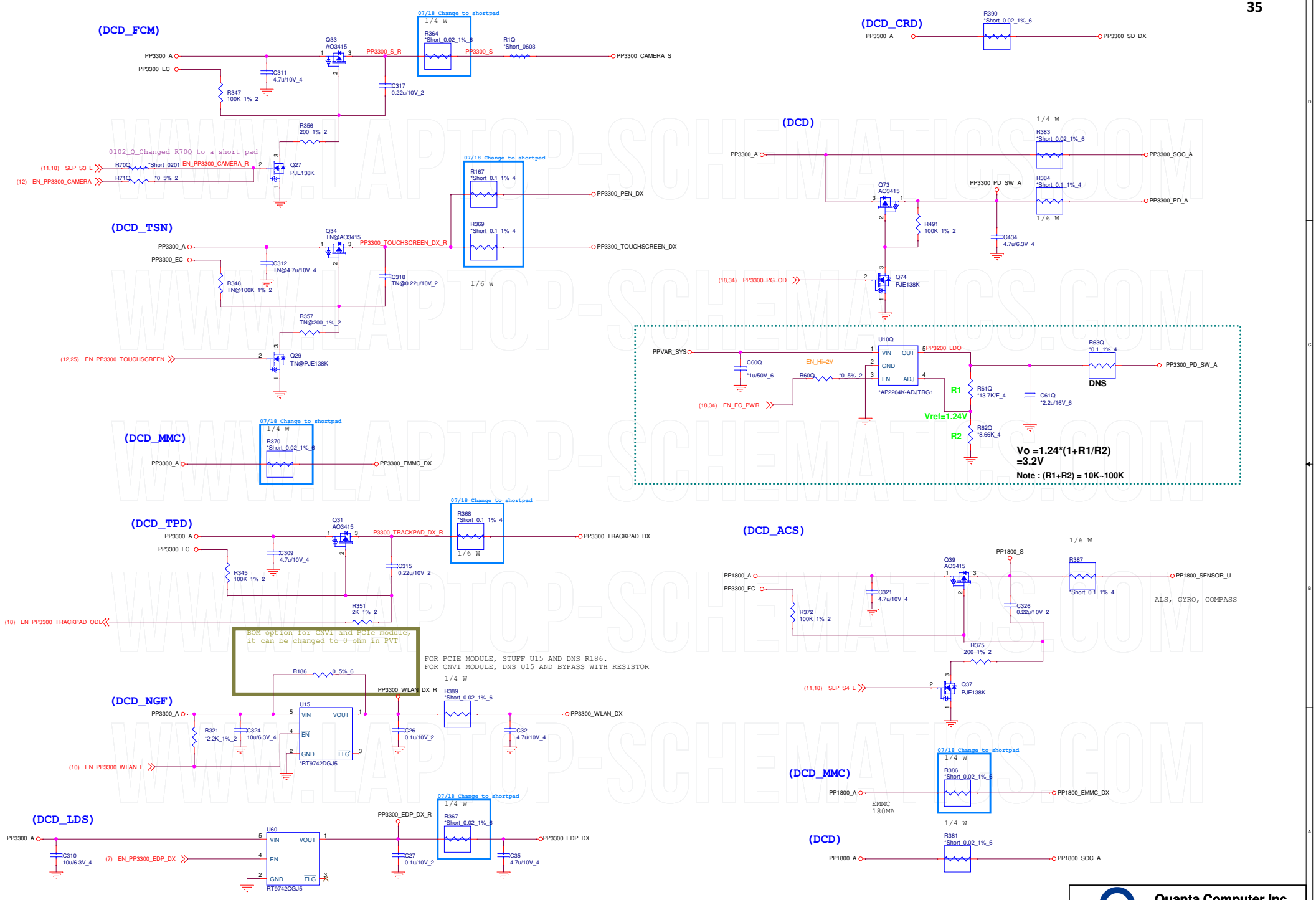



CHOICES FOR THE REGULATORS CAN BE SUBSTITUE AFTER CONFIRM THE FUNCTIONALITY.

Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | POWER: 1.8V(EC) 3.3V AND 5V | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 34 of 45 | |

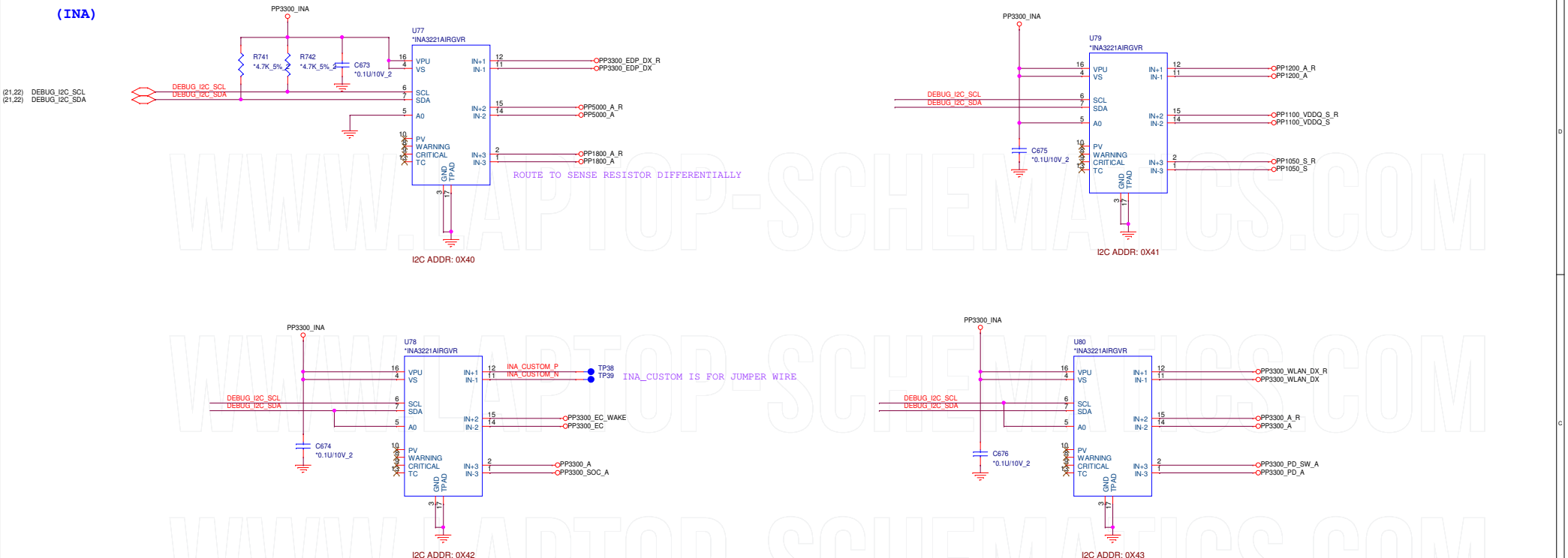


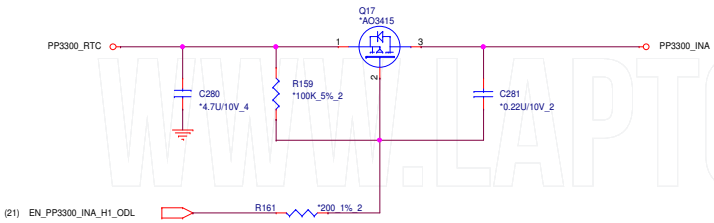

Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

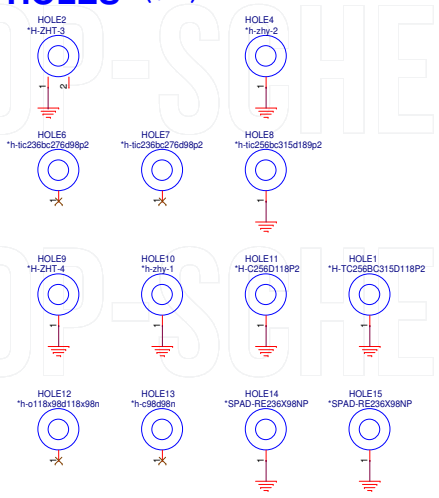
| Size | Document Number | Rev |
|---|---|---|
| | POWER - LOAD SWITCHES | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 35 of 45 | |

## (INA)

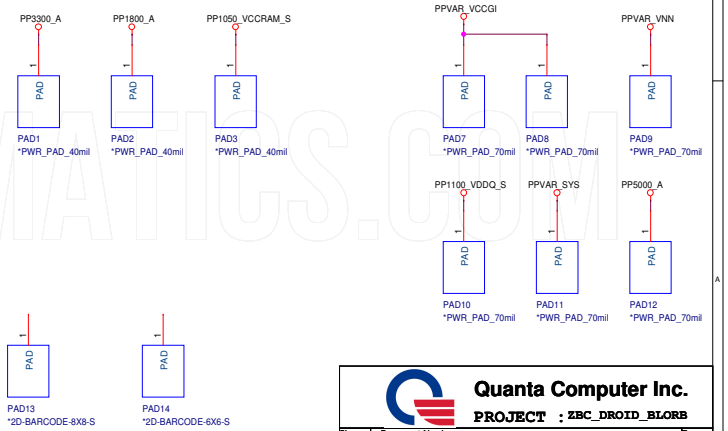



## HOLES (OTH)




## POWER TEST PAD (OTH)




Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | INAs | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 36 of 45 | |

(CRG)

# INTERSIL BUCK - BOOST CHARGER

INCREASE OR ADD POSCAPS IF AUDIBLE NOISE IS HEARD

PPVAR_VBUS_IN
C101Q *0.1u/50V_4
C100Q *0.1u/50V_4

RECOMMENDED VALUE FROME DATASHEET
R522 0.02_0.5%_0612
PPVAR_PWR_IN_BB
PPVAR_VBUS_IN
RC SNUBBER REQUIRED?
C538 *10u/50V_12 DNS
R505 1_5%_2
R526 1_5%_2
0515 Change QPN to CS-1001JE00
C536 4.7u/10V_4
BB_CSP
BB_CSN
C534 1u/50V_6
C537 1u/50V_6
C90Q 10u/35V_6
C91Q 10u/35V_6
C92Q 10u/35V_6
C93Q 10u/35V_6
C94Q 10u/35V_6
C95Q 10u/35V_6
C96Q 10u/35V_6
C97Q 10u/35V_6
C98Q 10u/35V_6
C99Q *10u/35V_6 DNS
C545 0.1u/50V_4

PPVAR_SYS
C550 0.1u/50V_4
C552 22u/25V_8
C554 22u/25V_8
C555 *22u/25V_8 DNS
C3563 *22u/25V_8 DNS
C560 22u/25V_8
RECOMMENDED VALUE FROME DATASHEET
R542 0.01_0.5%_0612
PPVAR_BAT_G
R541 1_5%_2
R543 1_5%_2
C557 1u/10V_4
0515 Change QPN to CS-1001JE00
BATTERY_SRP_BB
BATTERY_SRN_BB
C556 *1u/50V_6 DNS
C558 *1u/50V_6 DNS

Q12 CSD87330Q3D
Q23 CSD87330Q3D
L13 2.2uH_10x10x3
BB_SWITCH_1
BB_SWITCH_2
0529 Change R548/R549 to X5R
C548 0.22u/25V_4
C549 0.22u/25V_4
REQUIRE HIGHER OUTPUT CAPACITANCE
BUCK LEG
BOOST LEG
RATING HIGH ENOUGH?

PPVAR_VBUS_IN
DIODE OR
D11 BAT54CT-7-F
PPVAR_SYS
R506 1_1%_4
LDRIVE_1
LDRIVE_2
HDRIVE_1
HDRIVE_2
Q6 CSD25402Q3A
PPVAR_BAT_G
PPVAR_BAT
BATTERY_GATE_L
C141 *4700p/25V_4
0102_Q_removed R475,R479.R480,R481 used as 0 ohm in EVT/DVT builds for layout optimazation

U6 ISL9238HRTZ-T
DCIN VDDP VDD CSIN CSIP ACIN ASGATE ADP SDA SCL ACOK PROCHOT# PSYS AMON/BMON OTGEN/CMIN OTGPG/CMOUT COMP GND PROG
UGATE1 PHASE1 BOOT1 LGATE1 LGATE2 BOOT2 PHASE2 UGATE2
VSYS CSOP CSON VBAT BGATE BATGONE

R503 392K_1%_4
ADAPTER VOLTAGE VALID IF > 3.4V
PULL-UP FROM EC OR H1?
C533 0.1u/50V_4
R504 120K_1%_4
C535 1u/50V_6
R528 4.7_1%_4
C540 4.7u/10V_4
C544 4.7u/10V_4
PPVAR_BB_IN
VDD_BB_GATE_DRIVE
PP5000_BB_LDO_OUT
BB_CSN
BB_CSP
BB_ACIN
BB_ASGATE
PPVAR_VBUS_IN
TP109
(18) EC_I2C_CHARGER_3V3_SDA
(18) EC_I2C_CHARGER_3V3_SCL
(18,21) ACOK_OD
BB_CHARGER_PROCHOT_ODL
CHARGER_PMON
(11,18) PCH_PROCHOT_ODL
(18) CHARGER_PMON
R527 100_1%_2
(18) CHARGER_IADP
R530 *Short_0201
BB_CMIN
PP3300_EC
R521 *0_5%_2 DNS
R525 100K_1%_2
C541 0.01u/16V_4
TP110
BB_CMOUT
BB_COMP
R532 698_1%_4
C546 *470p/25V_2 DNS
C547 0.022u/25V_4
C541 GND PIN SHOULD GOES TO PIN E1 AVSS OF U45
R405 105K_1%_4
FOR 0.476A ADAPTER CURRENT LIMIT AND 733KHZ SWITCHING FREQUENCY:
2CELL : 93.1K
3CELL : 105K
I2C ADDR : 0X12

BB_PPVAR_SYS
BATTERY_SRP_BB
BATTERY_SRN_BB
BB_PPVAR_BAT
BATTERY_GATE_L
R539 *Short_0201
C551 1u/50V_6
R540 100_1%_2
C553 1u/50V_6
PPVAR_SYS
PPVAR_BAT
R538 *0_5%_2
CHARGER_BAT_PRES_L
R537 100K_1%_2
BATGONE LOW INDICATES BATTERY PRESENT

CV: 12.6V
3S1P Battery

R436 100K_1%_2
0102_Q_Changed R424 to a short pad
(21) H1_BATT_PRES_L
R424 *Short_0201
R426 100K_1%_2
(18) EC_BATT_PRES_L
(18) EC_I2C_BATTERY_3V3_SDA
(18) EC_I2C_BATTERY_3V3_SCL
BATT_TEMP
BATT_DISABLE_OD
J10
50458-00801-V02
PPVAR_BAT
PP3300_RTC
Q838 *2N7002K
R420 100K_1%_2
(21) BAT_DISABLE_ODL
Q55 2N7002K
C299 1u/6.3V_4

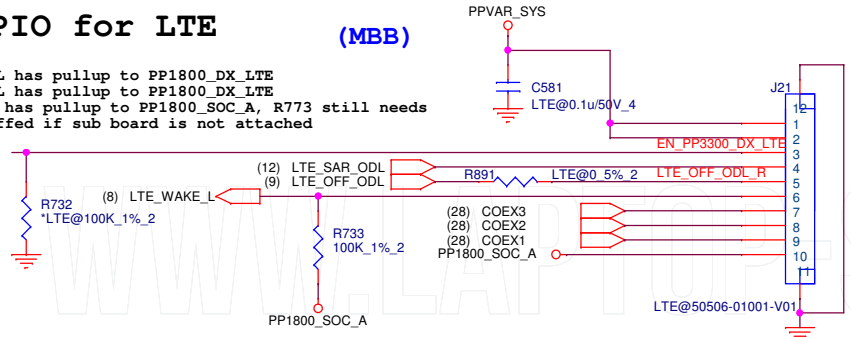
(DCD_THM)
PP3300_A
R702 13.7K_1%_2
TEMP_SENSOR_CHARGER (18)
R703 47K_NTC_4_1%
PLACE NEAR HOTSPOT OF THE CHARGER
CHARGER_PMON
C594 0.01u/50V_4
R174 6.04K_1%_2
SETS GAIN

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB
Size: Document Number: BATTERY CHARGER(OPTION 1) Rev: 1A
Date: Tuesday, November 05, 2019 Sheet 37 of 45

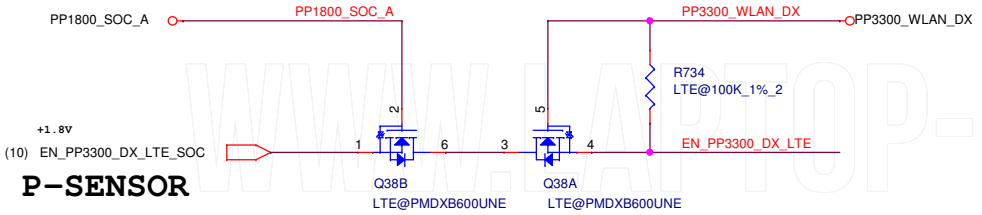
# GPIO for LTE

(MBB)

Coral sub board
-LTE_SAR_ODL has pullup to PP1800_DX_LTE
-LTE_OFF_OFL has pullup to PP1800_DX_LTE
-LTE_WAKE_L has pullup to PP1800_SOC_A, R773 still needs to be stuffed if sub board is not attached

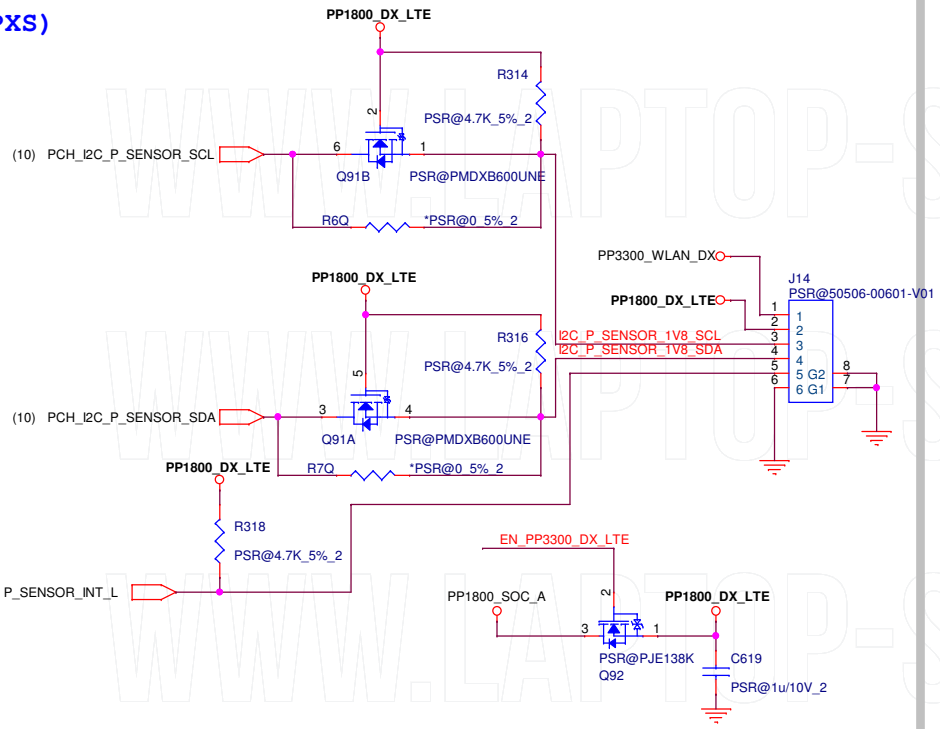



LEVERAGING CORAL BOARD!




## P-SENSOR

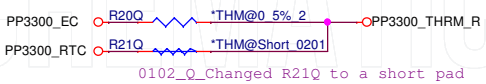
(PXS)




(SYS_THM)

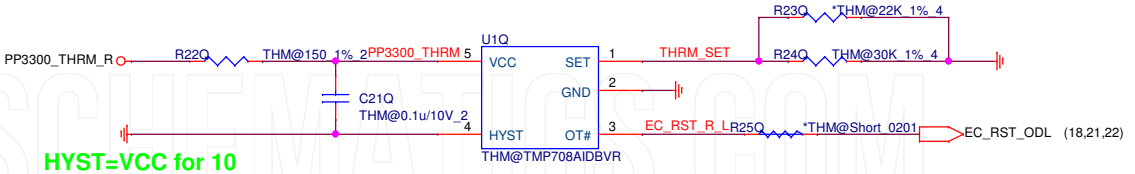
# Thermal Protector

Need fine tune
for thermal protect point
Note placement position
TEMP=76.3C




0102_Q_Changed R21Q to a short pad

Rset(Kohm)=0.0012T*T-0.9308T+96.147




HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | LTE,STEST | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 38 of 45 | |

(UTC2)

(18,22,26,27) LID_OPEN
(18) LED_3_L
R132 *Short_0201
R255 *0_5%_2
EC_GPIO_1
R197 *100K_5%_2

EC_GPIO1,2 CAN BE USED FOR CONNECTING THE GMR SENSOR ON THESUB-BOARD
OR IT CAN BE USED TO CONNECT AN SPARE EC GPIO PINS FOR ADDITIONAL CONTROL FROM EC

(18,27) TABLET_MODE_L
R322 *Short_0201
EC_GPIO_2

PPVAR_VBUS_IN
C87Q *10u/50V_12
C80Q *10u/35V_6
C62 10u/35V_6
C68 2AC@0.1u/50V_4
J6 2AC@51288-0060N-001

PULL-DOWN RESISTORS TO AVOID
FLOATING INPUT W/O SUB-BOARD

PP3300_RTC
C424 0.1u/16V_4
PP3300_PD_A
C425 2AC@0.1u/16V_4
R48 1.8K_1%_2
R49 1.8K_1%_2
R259 100K_5%_2

J17

(7) DDI1_AUX_P
(7) DDI1_AUX_N
DDI1_AUX_P
DDI1_AUX_N
EC_GPIO_1
USB_PD_C1_INT_ODL
EC_I2C_USB_C1_MUX_SCL
EC_I2C_USB_C1_MUX_SDA
EC_GPIO_2
USB_C1_HPD_3V3
USB_C1_PD_RST_ODL
EC_VOLUP_BTN_ODL
EC_VOLDN_BTN_ODL

(18) USB_PD_C1_INT_ODL
(18) EC_I2C_USB_C1_MUX_SCL
(18) EC_I2C_USB_C1_MUX_SDA
(18,29) USB_C1_PD_RST_ODL
C3562 *2AC@1u/6.3V_2

(18) EC_VOLUP_BTN_ODL
(18) EC_VOLDN_BTN_ODL
(30) USB_A0_STATUS_L

CC1, CC2 ARE FOR BIP INTERFACE

TP79
TP80
USB_C1_CC1
USB_C1_CC2
USB_C1_BC12_CHG_DET_L

(18) USB_C1_BC12_CHG_DET_L
(18) USB_C1_BC12_VBUS_ON
(18) USB_C1_MUX_INT_ODL
(18) USB_A1_CHARGE_EN_L
(18) EN_USB_A1_5V
(8) USB_A1_OC_ODL
(30) USB_A1_STATUS_L

PP3300_EC
R229 100K_5%_2
R185 100K_5%_2
R693 100K_5%_2
USB_C1_BC12_CHG_DET_L
EC_VOLUP_BTN_ODL
EC_VOLDN_BTN_ODL

PP5000_A
C426 2AC@0.1u/16V_4
(18) SUB_GPIO_ADC
R135 *2AC@Short_0201
0102_Q_Changed R135 to a short pad

FH34SRJ-40S-0.5SH(50)

(8) USB3_P4_C1_TX_P
(8) USB3_P4_C1_TX_N
(8) USB2_P3_A1_N
(8) USB2_P3_A1_P
(8) USB3_P4_C1_RX_P
(8) USB3_P4_C1_RX_N
(8) USB2_P4_C1_P
(8) USB2_P4_C1_N
(7) DDI1_TX3_N
(7) DDI1_TX3_P
(7) DDI1_TX2_N
(7) DDI1_TX2_P
(7) DDI1_TX1_N
(7) DDI1_TX1_P
(7) DDI1_TX0_N
(7) DDI1_TX0_P
(8) USB3_P3_A1_TX_N
(8) USB3_P3_A1_TX_P
(8) USB3_P3_A1_RX_N
(8) USB3_P3_A1_RX_P

J18
2AC@FH34SRJ-30S-0.5SH(50)

SELECT PER SEL SI TEAM

SUB_GPIO_ADC GOES TO AN ADC PIN OF EC WITH STUFFING OPTIONS
THE PIN CAN BE USED FOR VBUS DETECT OR FOR BOARD ID DETECT, OR USE AS A GENERAL GPIO FROM EC

SELECT PER SEL SI TEAM
CM TO ADJUST PINOUT/PIN COUNT

PP1800_SOC_A
R240 100K_5%_2
(7,18) USB_C1_HPD_1V8_ODL
USB_C1_HPD_1V8_ODL
Q19 2AC@PJE138K
USB_C1_HPD_3V3
R1401 2AC@499K_1%_2

MOTHER BOARD INTERFACE

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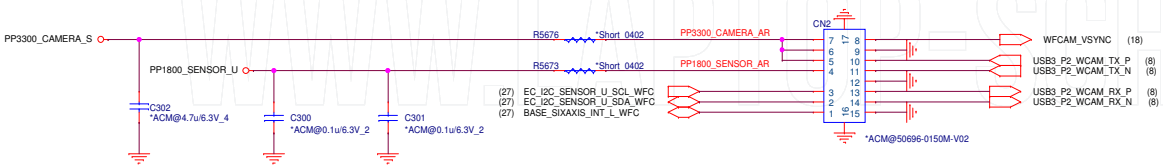
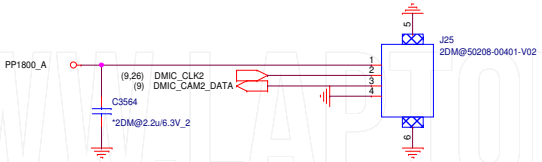
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | CONNECTORS TO SUB BOARD | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 39 of 45 | |

## AR CAMERA CONN
## (ACM)




## DMIC CONN
## (MIC2)




**PREFERRED DMIC CHANNEL CONFIG**
**INTERFACE 1: STRAP MIC TO LEFT=CHANNEL 0**
**INTERFACE 2: STRAP MIC TO RIGHT=CHANNEL 3**



Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | AR CONNECTORS | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 40 of 45 | |

Quanta Computer Inc.

PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

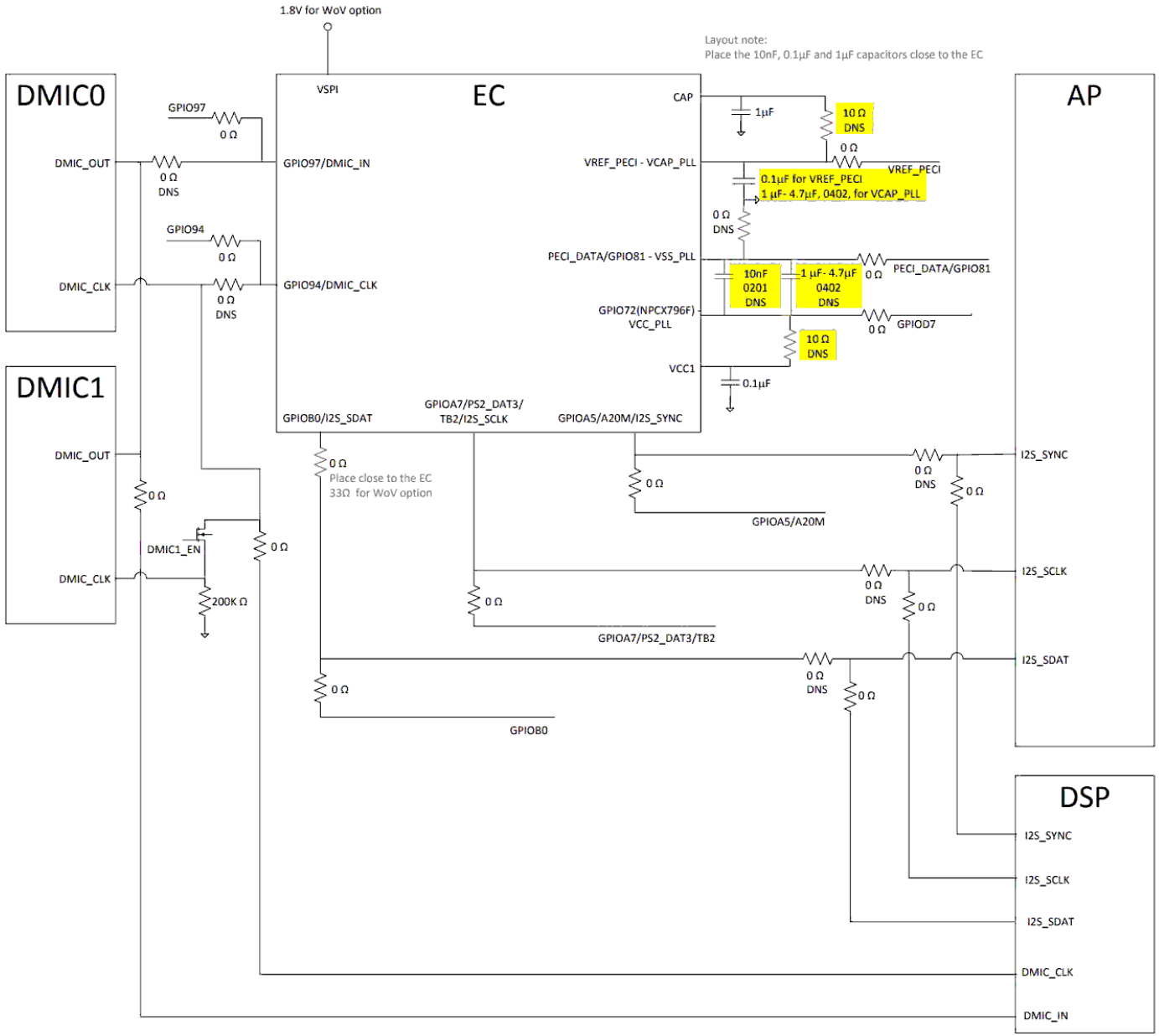
Date: Tuesday, November 05, 2019 Sheet 41 of 45

Quanta Computer Inc.

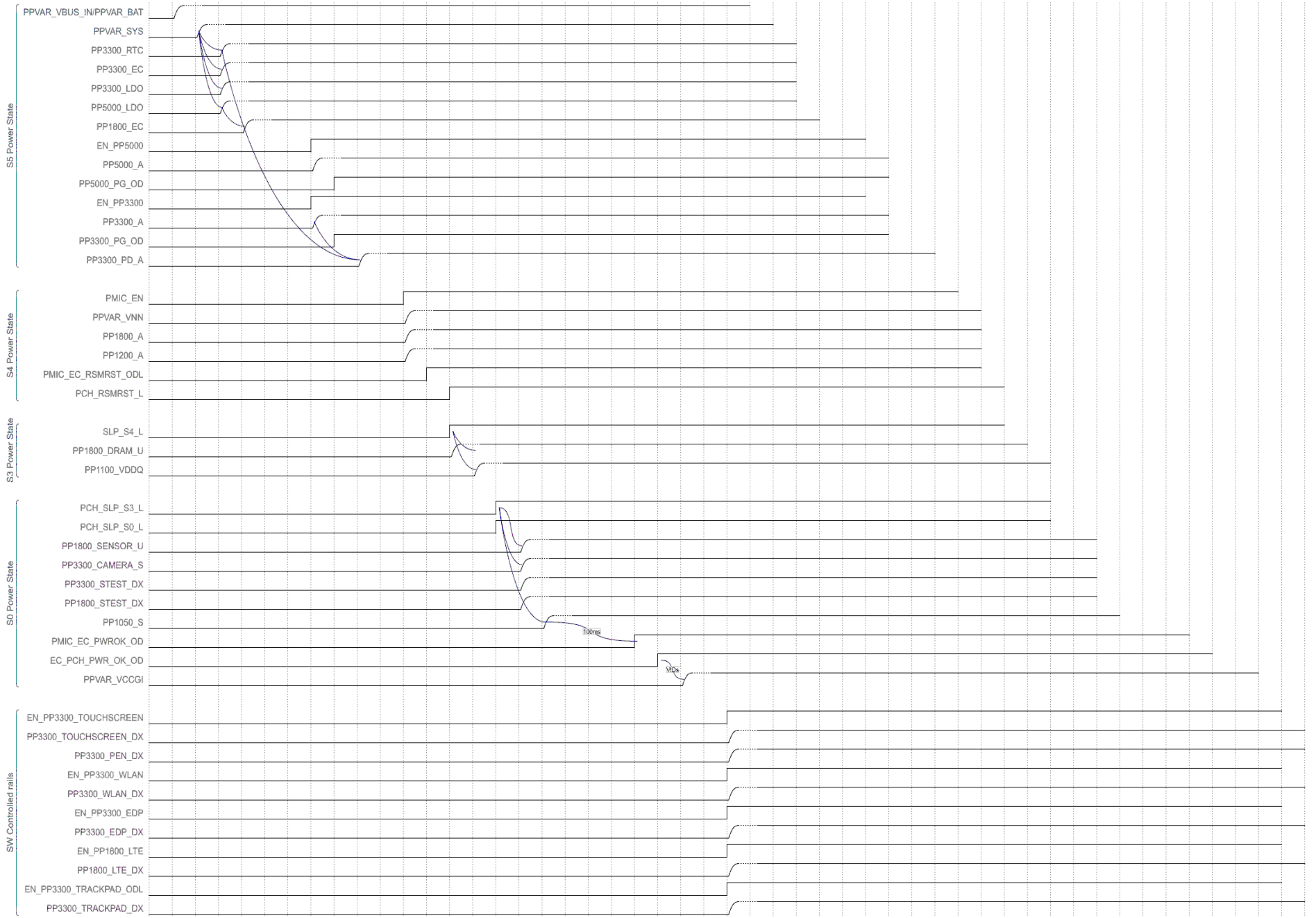
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | Blank | 1A |

Date: Tuesday, November 05, 2019 Sheet 42 of 45




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : ZBC_DROID_BLORB | | |
| Size | Document Number: WOV DIAGRAM | Rev 1A |
| Date: Tuesday, November 05, 2019 | Sheet 43 of 45 | |

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PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | POWER SEQUENCE | 1A |
| Date: Tuesday, November 05, 2019 | Sheet 44 of 45 | |

| GPIO # | Bump Name | Voltage | Bootstrap Termination | Default Termination | Bootstrap Purpose | Bootstrap Usage | Bootstrap | Octopus Signal Name |
|---|---|---|---|---|---|---|---|---|
| GPIO_27 | GPIO_27 | 1.8V | 20K PU | 20K PD | eMMC as boot Source<br>20K PU internal | 1 = enable (default)<br>0 = disable | eMMC Boot | DBG_PTI_DATA_16 |
| GPIO_28 | GPIO_28 | 1.8V | 20K PU | 20K PD | SPI as boot Source<br>20K PU internal | 1 = enable (default)<br>0 = disable | SPI Boot | DBG_PTI_DATA_17 |
| GPIO_42 | GP_INTD_DSI_TE1 | 1.8V | 20K PD | 20K PD | Flash Descriptor Override<br>for SPI security features | 1 = Override<br>0 = No Override (default) | Flash Descriptor | TP_WIFI_RST_N, TP135 |
| GPIO_43 | GP_INTD_DSI_TE2 | 1.8V | 20K PU | 20K PD | RSVD | 1 = Disable (default)<br>0 = Do Not Use | RSVD | GP_INTD_DSI_TE2 |
| GPIO_44 | USB_OC0_B | 1.8V | 20K PD | 20K PU | RVSD | 1 = Do Not Use<br>0 = disable (default) | RSVD | USB_A_OC_ODL |
| GPIO_45 | USB_OC1_B | 1.8V | 20K PD | 20K PU | Top Swap Override.<br>Have core look for BIOS code in SPI ROM | 1 = Enable<br>0 = disable (default) | Top Swap | USB_C_OC_ODL |
| GPIO_61 | LPSS_UART0_TXD | 1.8V | 20K PD | 20K PU | TXE to bypass ROM in SoC and go to patch space | 1 = enable bypass<br>0 = disable (default) | TXE ROM Bypass | PCHTX_MIPI60RX_UART |
| GPIO_62 | LPSS_UART0_RTS_ | 1.8V | 20K PD | 20K PU | RSVD | 1 = Do Not Use<br>0 = disable (default) | RSVD | stest_INT_L |
| GPIO_65 | LPSS_UART2_TXD | 1.8V | 20K PD | 20K PU | TXE to perform DnX for new FW Image over USB. | 1 = Force DnX<br>0 = Do Not Force (default) | DnX FW Load | PCHTX_UART2 |
| GPIO_66 | LPSS_UART2_RTS_ | 1.8V | 20K PD | 20K PU | LPC Boot BIOS strap | 1 = LPC Boot<br>0 = No LPC Boot (default) | LPC Boot | LTE_OFF_ODL |
| GPIO_79 | LPSS_SPI_0_CLK | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = Normal Operation | RSVD | H1_SLAVE_SPI_CLK_R |
| GPIO_80 | LPSS_SPI_0_FS0 | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = No halt (default) | RSVD | H1_SLAVE_SPI_CS_L_R |
| GPIO_81 | LPSS_SPI_0_FS1 | 1.8V | 20K PU | 20K PU | RSVD | 1 = Disable (default)<br>0 = Do Not Use | RSVD | GPIO_81_DEBUG (Boot halt) |
| GPIO_83 | LPSS_SPI_0_TXD | 1.8V | 20K PD | 20K PD | Sets the LPC buffer to 1.8V or 3.3V mode | 1 = 1.8V mode<br>0 = 3.3V mode (default) | LPC Voltage Select | H1_SLAVE_SPI_MOSI_R |
| GPIO_84 | LPSS_SPI_2_CLK | 1.8V | 20K PU | 20K PD | SPI Boot BIOS Strap | 1 = Don't SPI Boot (default)<br>0 = SPI Boot Debug if Secure boot fuse is set to 0 | SPI Boot Source | stest_SPI1_CLK_R |
| GPIO_85 | LPSS_SPI_2_FS0 | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = disable (default) | RSVD | stest_SPI_CS_L_R |
| GPIO_86 | LPSS_SPI_2_FS1 | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = enable (default) | RSVD | stest_CNTRL |
| GPIO_87 | LPSS_SPI_2_FS2 | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = Default | RSVD | TP_PCH_GPIO_87_PD |
| GPIO_89 | LPSS_SPI_2_TXD | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = Default | RSVD | stest_SPI1_MOSI_R |
| GPIO_159 | AVS_I2S0_SDI | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 =Default | RSVD | I2S0_PCH_RX |
| GPIO_163 | AVS_I2S1_WS_SYN | 1.8V | 20K PD | 20K PD | SMBus 3.3V/1.8V mode select | 1 = 1.8V mode<br>0 = 3.3V mode (default) | Buffers 1.8V/3.3V | I2S_SFRM_SPKR |
| GPIO_164 | AVS_I2S1_SDI | 1.8V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = Default | RSVD | WLAN_PE_RST |
| GPIO_168 | AVS_HDA_SDI | 1.8V | 20K PD | 20K PD | PMU 3.3V/1.8V mode select | 1 = 1.8V mode<br>0 = 3.3V mode (default) | PMU 1.8V/3.3V | I2S2_PCH_RX |
| GPIO_172 | AVS_M_CLK_B1 | 1.8V | 20K PD | 20K PD | SMBus No Reboot. Handled by PMC | 1 = Enable<br>0 = disable (default) | SMBus Reboot | DMIC_CLK2_R |
| GPIO_174 | AVS_M_CLK_AB2 | 1.8V | 20K PD | 20K PD | VDD2 Voltage Select | 1 = 1.24V<br>0 = 1.20V (default) | VDD2 Voltage | (Open, TP_GPIO_174) |
| GPIO_175 | AVS_M_DATA_2 | 1.8V | 20K PD | 20K PD | eSPI vs. LPC | 1 = eSPI mode<br>0 = LPC mode (default) | eSPI/LPC mode | DMIC_CAM2_DATA |
| GPIO_177 | SMB_CLK | 1.8V/3.3V | 20K PD | 20K PD | RSVD | 1 = Do Not Use<br>0 = Default | RSVD | (Open, TP160) |
| GPIO_191 | CNV_BRI_DT | 1.8V | 20K PD | None | eSPI Flash Sharing Mode. Set to 0 if GPIO_175 is set to 0 | 1 = Slave attached Share<br>0 = Master attached (default) | Flash Sharing | CNVI_BRI_DT_R |
| GPIO_192 | CNV_BRI_RSP | 1.8V | 20K PD | 20K PU | RSVD | 1 = Do Not Use<br>0 = Normal Operation | RSVD | CNVI_BRI_RSP |
| GPIO_193 | CNV_RGI_DT | 1.8V | 20K PU | None | RSVD | 1 = Normal Operation<br>0 = Do not use | RSVD | CNVI_RGI_DT_R |
| GPIO_194 | CNV_RGI_RSP | 1.8V | 20K PD | 20K PU | RSVD | 1 = Do Not Use<br>0 = Normal Operation | RSVD | CNVI_RGI_RSP |
| GPIO_195 | CNV_RF_RESET_B | 1.8V | 20K PD | None | RSVD | 1 = Do Not Use<br>0 = Normal Operation | RSVD | CNVI_RF_RESET_L |
| GPIO_196 | XTAL_CLKREQ | 1.8V | 20K PD | None | RSVD | 1 = Do Not Use<br>0 = Normal Operation | RSVD | (Not available) |

Quanta Computer Inc.
PROJECT : ZBC_DROID_BLORB

| Size | Document Number | Rev |
|---|---|---|
| | SOC-STRAPPING | 1A |

Date: Tuesday, November 05, 2019 Sheet 45 of 45