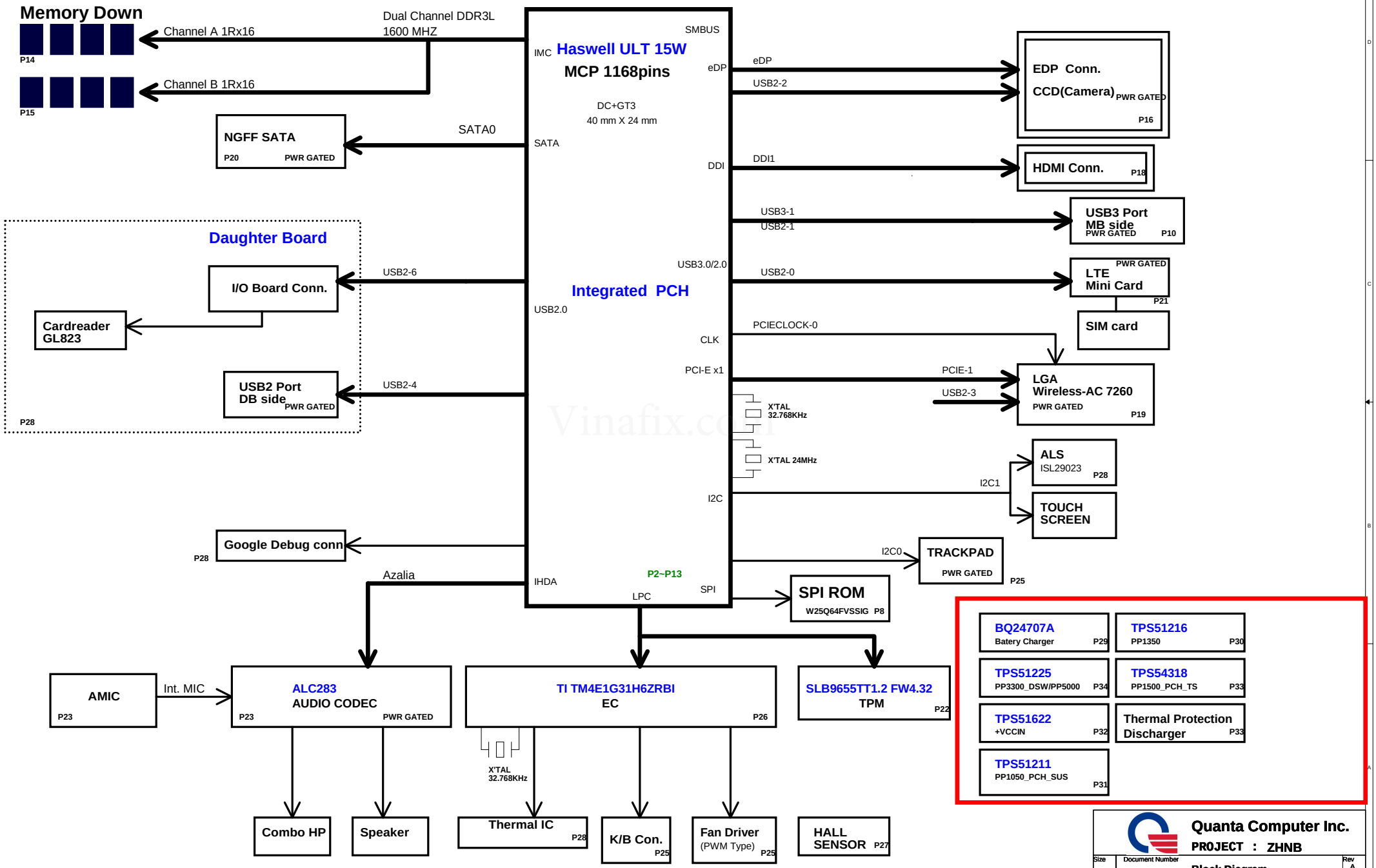
Benetton_EDU(ZHNB) SHB ULT SYSTEM BLOCK DIAGRAM

01



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	Block Diagram	A
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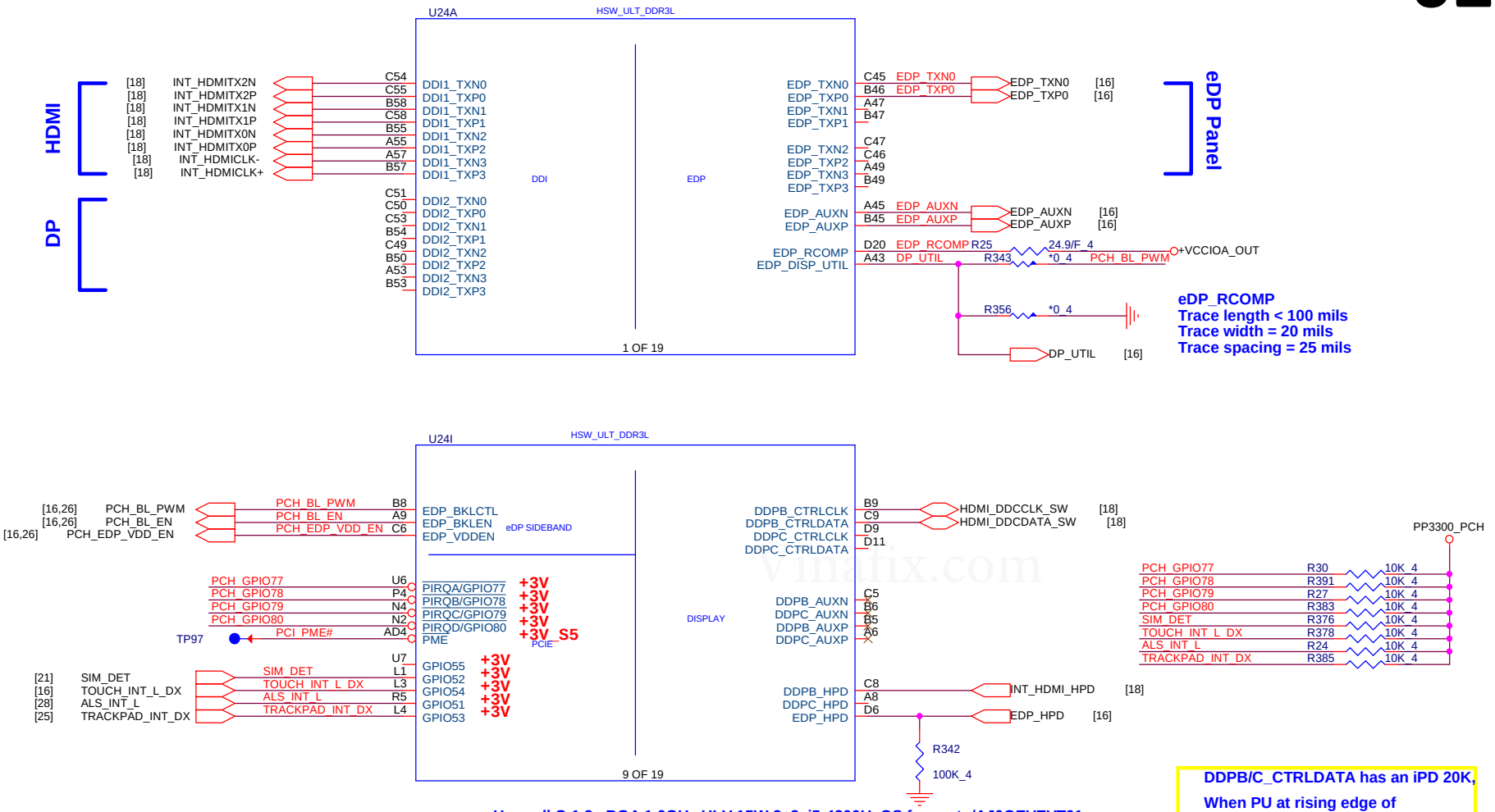
Haswell ULT (DISPLAY,eDP)

02



eDP_RCOMP
Trace length < 100 mils
Trace width = 20 mils
Trace spacing = 25 mils

Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01

DDPB/C_CTRLDATA has an iPD 20K,

When PU at rising edge of PCH_PWROK, the DDI port will be detected

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	Haswell 1/5 (DDI/eDP)	A
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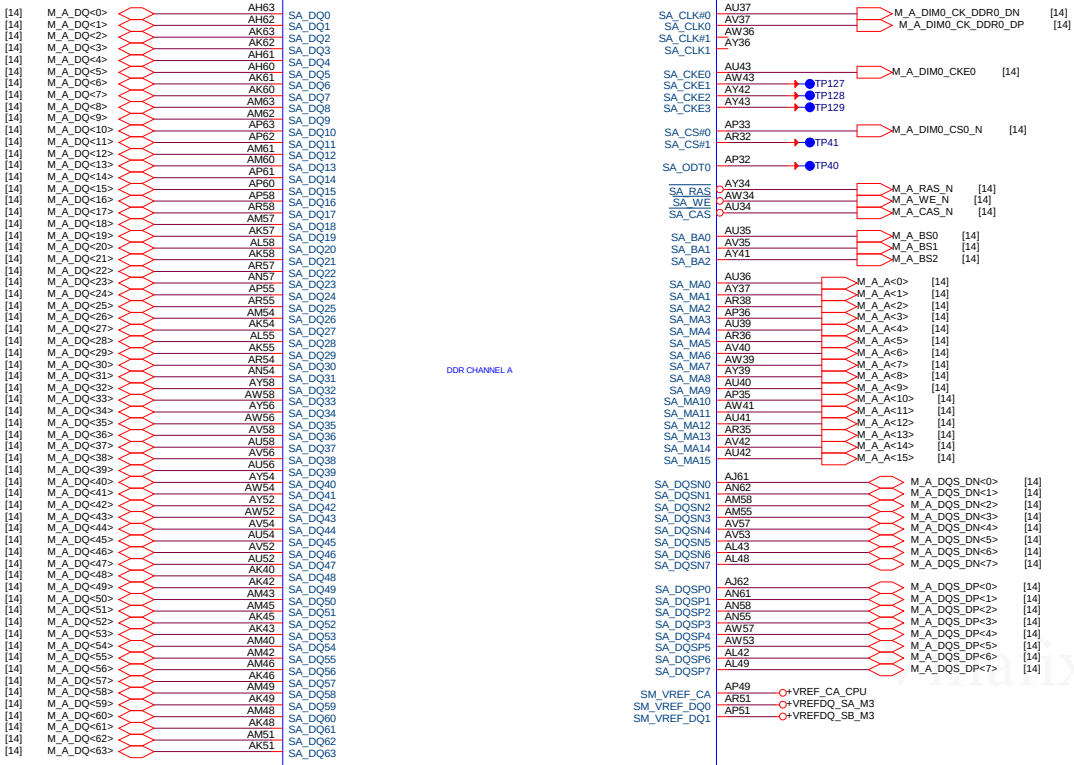
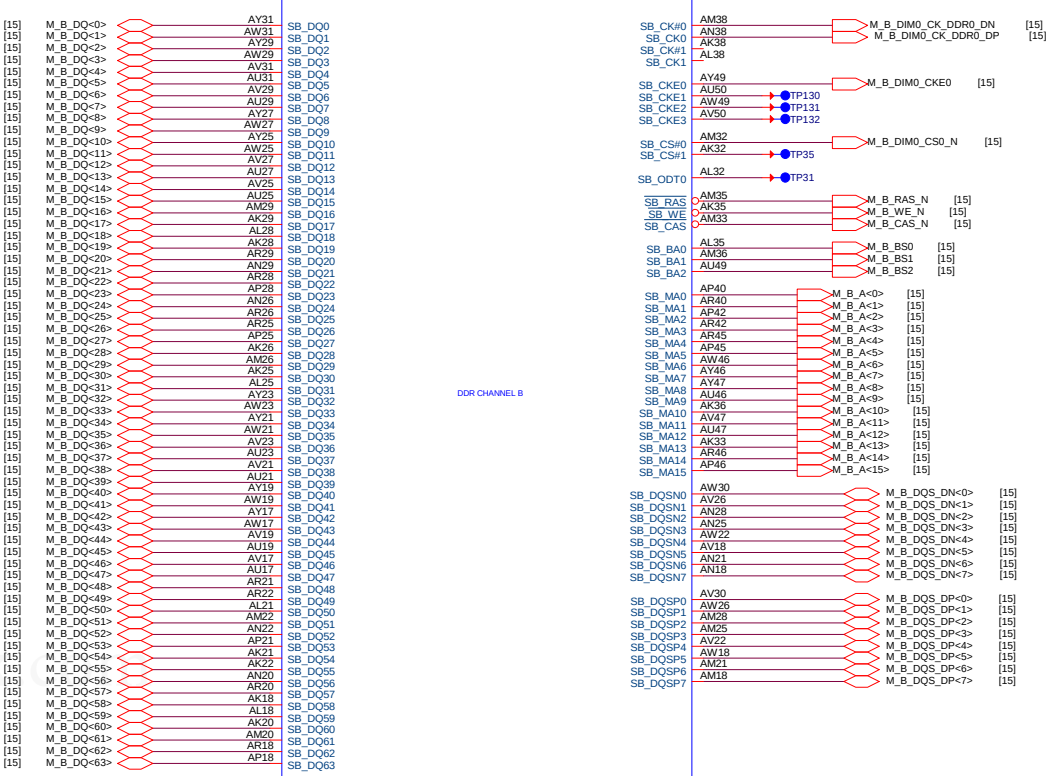
Haswell ULT (DDR3L)

U24C — HSW_ULT_DDR3L



Haswell Processor (DDR3L)

U24D — HSW_ULT_DDR3L



Size	Document Number	Rev
	Haswell 2/5 (DDR3 I/F)	A
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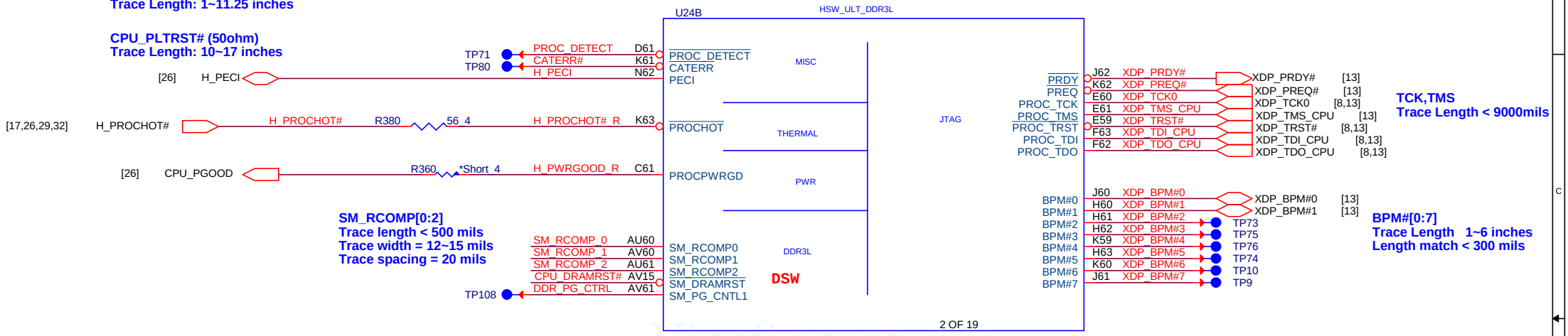
Haswell ULT (SIDEBAND)

H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

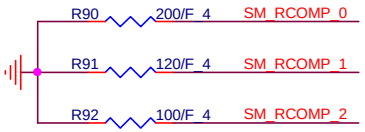


TCK,TMS
Trace Length < 9000mils

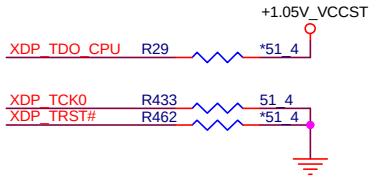
SM_RCOMP[0:2]
Trace length < 500 mils
Trace width = 12~15 mils
Trace spacing = 20 mils

BPM#[0:7]
Trace Length 1~6 inches
Length match < 300 mils

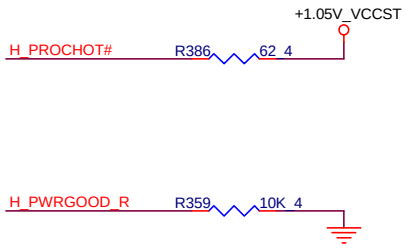
DRAM COMP



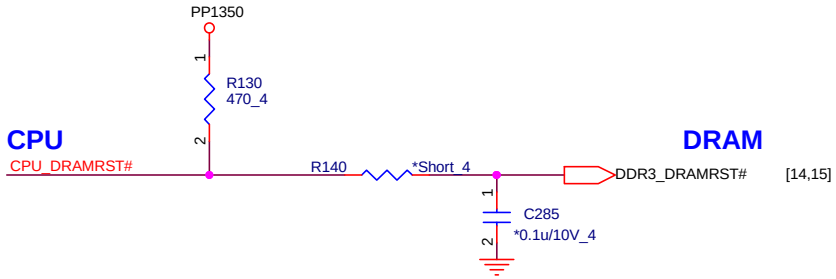
XDP PU/PD



PU/PD of CPU



DRAMRST



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	Haswell 3/5 (SideBand)	A
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Haswell ULT (POWER)

05

VDDQ Output Decoupling Recommendations		
330uFx2	7343	BOT socket side
22uFx11	0805	5 onTOP, 6 on BOT inside socket cavity
10uFx10	0805	5 onTOP, 5 on BOT inside socket cavity

VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

SVID

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to CPU

Place PU resistor close to CPU

VCCST PWRGD

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	Haswell 4/5 (POWER)	A

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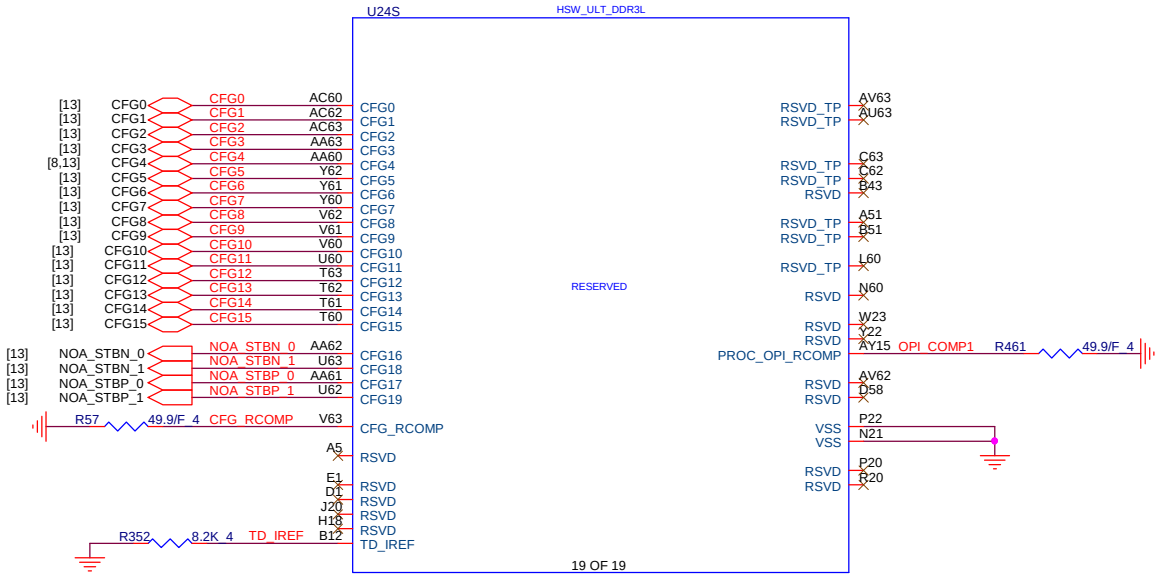
Haswell ULT (CFG,RSVD)

06



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	**(DEFAULT) NORMAL OPERATION; NO STALL**	STALL	CFG0 R417 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	**(DEFAULT) NORMAL OPERATION**	PCH-LESS MODE	CFG1 R423 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	**DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT**	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R409 *1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	**DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS**	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R403 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	**VRS SUPPORTING SVID PROTOCOL ARE PRESENT**	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R394 *1K_4
CFG10 SAFE MODE BOOT	**POWER FEATURES ACTIVATED DURING RESET**	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R56 *1K_4

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	Haswell 5/5 (CFG/GND)	A

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Haswell ULT PCH (PM)

07

U24H — HSW_ULT_DDR3L — SYSTEM POWER MANAGEMENT

[26] PCH_SUSACK_L — R428 *0_4 SUSACK#_R — SUSACK AK2
[13,17] SYS_RESET# — SYS_RESET# — SYS_RESET AC3
[5,13,26] SYS_PWROK — SYS_PWROK — C265 *1u/6.3V_4 — R421 *Short_4 — SYS_PWROK_R — SYS_PWROK AG2
PCH_PWROK — R482 *Short_4 — PCH_PWROK_R — PCH_PWROK AY7
APWROK_R — APWROK AB5
PCI_PLTRST# — PLTRST AG7 — +3V_S5

[26] PCH_RSMRST_L — R478 *Short_4 — PCH_RSMRST# — RSMRST AW6
[26] PCH_SUSWARN_L — R453 *0_4 — PCH_SUSPWRACK — SUSWARN/SUSPWRDNACK/GPIO30 AV4 — +3V_S5
[26] PCH_PWRBTN_L — R147 *Short_4 — PCH_PWRBTN# — PWRBTN AL7 — DSW
[29] ACPRESENT — R61 *Short_4 — PCH_ACPRESENT — ACPRESENT/GPIO31 AJ8 — DSW
PCH_BATLOW# — BATLOW/GPIO72 AN4 — DSW
[13,26] PCH_SLP_S0_L — R415 *Short_4 — PCH_SLP_S0#_R — SLP_S0 AF3 — +3V_S5
TP37 — SLP_WLAN/GPIO29 AM5 — DSW

PCH_SUSPWRACK — R427 0_4 — SUSACK#_R

8 OF 19

DSWVRMEN — AW7 DSWVREN — Deep Sx
DPWROK — AV5 DPWROK_R — R477 *Short_4 — DSWVREN [8]
WAKE — AJ5 PCIE_PCH_WAKE# — R74 *Short_4 — PCH_DPWROK [26]
PCH_WAKE_L [26]
DSW

+3V — +3V_S5 — +3V_S5 — DSW

CLKRUN/GPIO32 — V5 CLKRUN# R38 — *Short_4 — LPC_CLKRUN_L — LPC_CLKRUN_L [26]
SUS_STAT/GPIO61 — AG4 PCH_SUS_STAT — TP27
SUSCLK/GPIO62 — AE6 PCH_SUSCLK — PCH_SUSCLK [19]
SLP_S5/GPIO63 — AP5 PCH_SLP_S5_L — PCH_SLP_S5_L [13,26,30,35]

DSW — SLP_S4 — AJ6 PCH_SLP_S4_L — PCH_SLP_S4_L [13]
DSW — SLP_S3 — AT4 PCH_SLP_S3_L — PCH_SLP_S3_L [13,26,30,31,33,35]
DSW — SLP_A — AL5 PCH_SLP_A_L — PCH_SLP_A_L [13]
DSW — SLP_SUS — AP4 PCH_SLP_SUS_L — PCH_SLP_SUS_L [26,35]
DSW — SLP_LAN — AJ7 PCH_SLP_LAN# — TP38

4/22 modify, default skip EC control

PCH PM PU/PD

PP3300_PCH
CLKRUN# — R37 8.2K_4
SYS_RESET# — R406 10K_4

PCH_RSMRST# — R479 10K_4
SYS_PWROK — R80 *10K_4
DPWROK_R — R473 100K/F_4

PP3300_PCH_SUS
PCH_SUSPWRACK — R454 10K_4
SYS_PWROK — R426 *1K_4

PP3300_DSW
PCH_ACPRESENT — R62 10K_4
PCH_BATLOW# — R444 8.2K_4
PCIE_PCH_WAKE# — R75 10K_4
PCH_PWRBTN# — R151 *10K_4

PCH PWROK

[5,26] PCH_PWROK — PCH_PWROK — R483 *Short_4 — PCH_PWROK_R
R487 100K_4
PCH_RSMRST_L — R474 *0_4 — DPWROK_R
Non Deep Sx

PLTRST# Buffer

PCI_PLTRST# — R152 *Short_4 — PLTRST#

PP3300_PCH
C94 *0.1u/10V_4
U6 *TC7SH08FU
PCI_PLTRST# — 1
2
3
4
5
PLTRST# [13,19,21,22,26]
R155 100K_4

4/22 modify, default is bypass PLTRST#

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	PCH 1/6 (PM)	A
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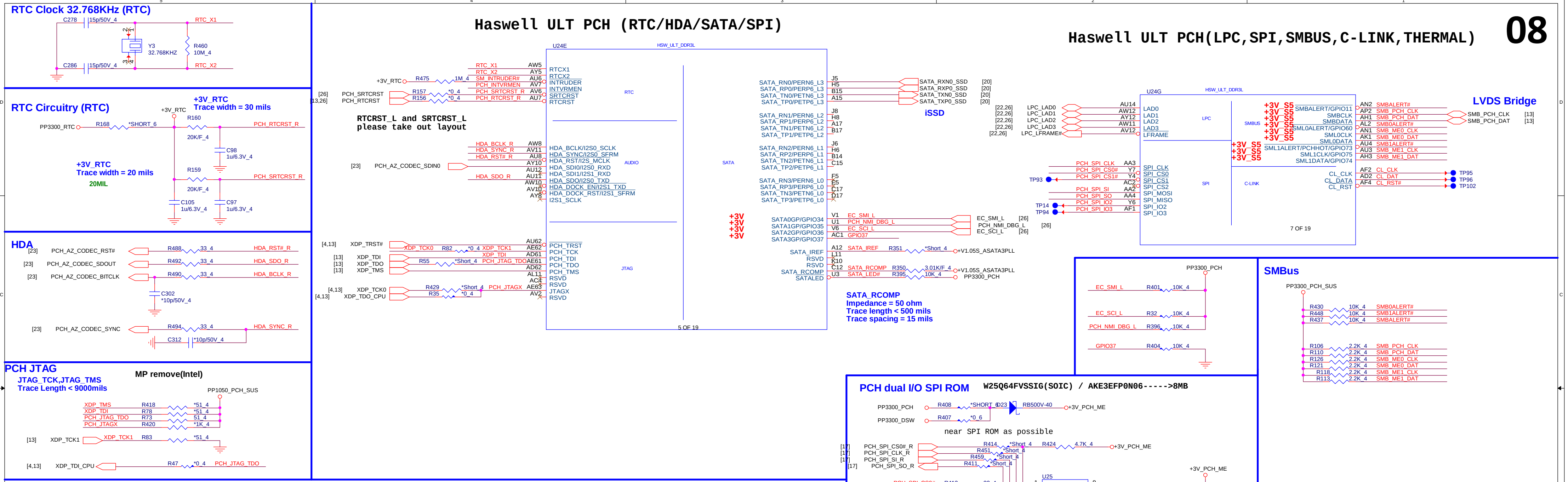
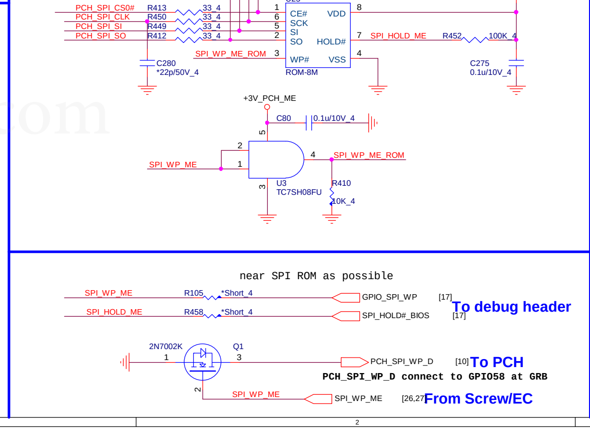
Haswell ULT PCH (RTC/HDA/SATA/SPI)



ULT Strapping Table

Note: R493 need stuff on MP.

Pin Name	Strap description	Sampled	Configuration	note
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	**0 = Default enable (iPD 20K)** 1 =Disable No-Reboot mode	PP3300_PCH R400 *1K_4 SPKR SPKR [10,23]
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	**0 = Default can program ME (iPD 20K)** 1 =can't program ME	HDA_SDO_R R493 *0_4 PCH_HDA_SDO [26]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**1=Should be always pull-up**	+3V_RTC R484 330K_4 PCH_INTVRMEN R485 *330K_4
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	[10] GPIO66 PP3300_PCH R330 *1K_4 GPIO66 R340 *1K_4
GPIO86	Boot BIOS Strap Bit		**0 = Default SPI (iPD 20K)** 1 =LPC	[10] GPIO86 PP3300_PCH R1 *1K_4 GPIO86 R7 *1K_4
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	[10] GPIO15 PP3300_PCH_SUS R50 *8.2K_4 x86 stuff GPIO15 R58 *1K_4
CFG4	DP presence strap		**0 = Enable an external display port is connected to the eDP** 1 =disable	[6,13] CFG4 CFG4 R64 1K_4
DSWVREN	Deep Sx well on die VR enable		**1=Should be always pull-up**	[7] DSWVREN +3V_RTC R476 330K_4 DSWVREN R472 *330K_4



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	PCH 2/6 (RTC/HDA/SATA/SPI)	A

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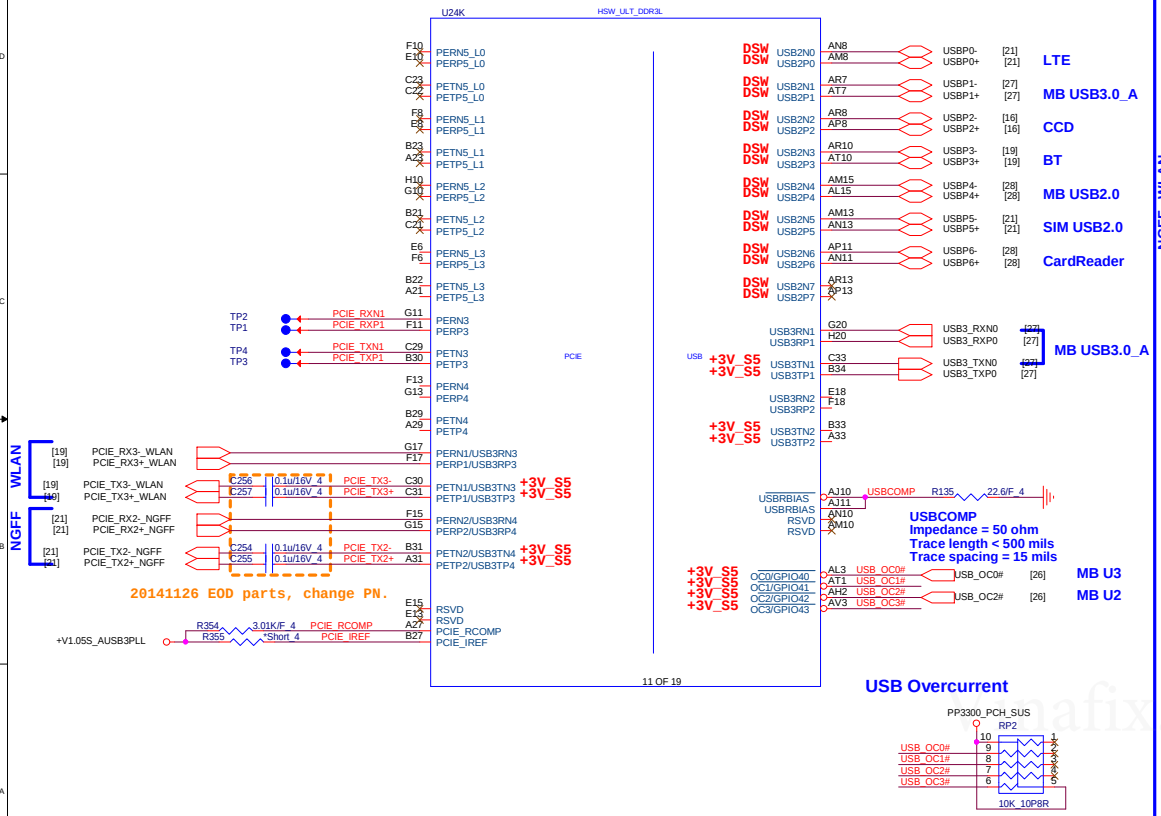
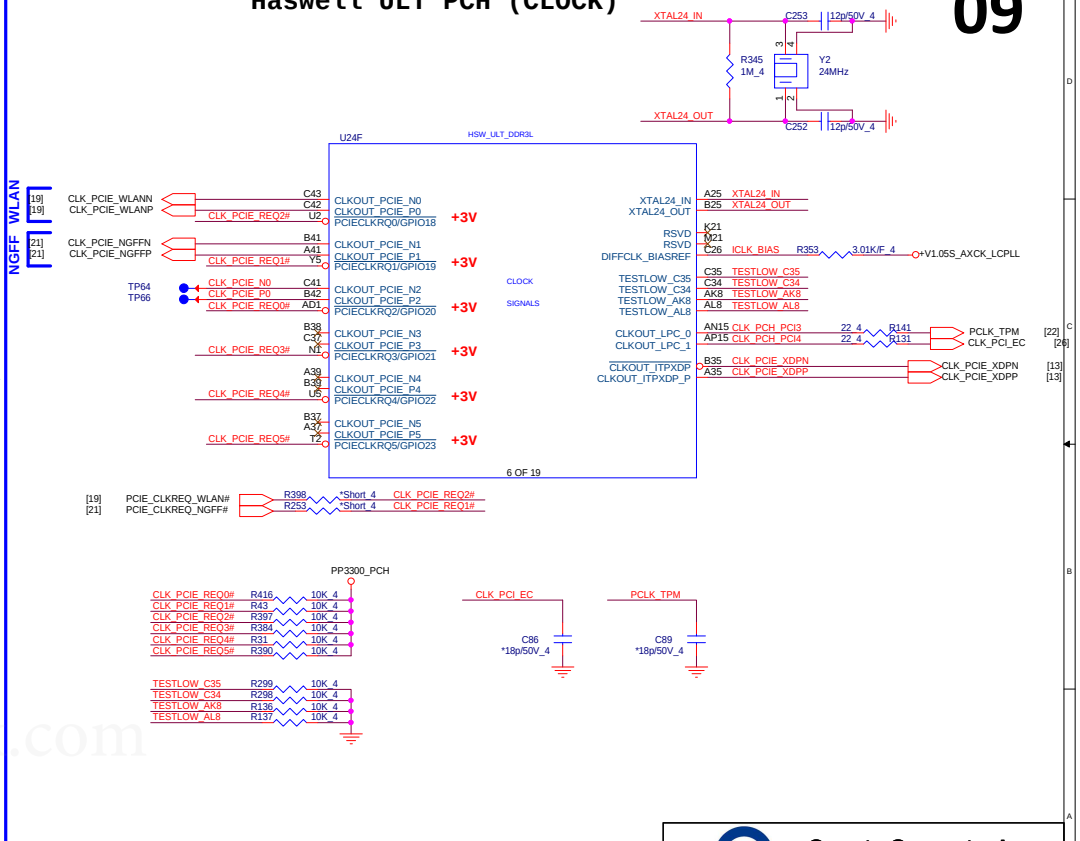
Haswell ULT PCH (PCIE,USB3.0,USB2.0)



Haswell ULT PCH (CLOCK)

09



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	PCH 3/6 (PCIE/USB/CLK)		A
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Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

U24J — HSW_ULT_DDR3L — 10 OF 19

LTE_DISABLE_L need PU to +3V_LTE

6/24 Connect DEVSLP0 to SSD.

4/23 modify, those 3 power enable pin are PD 100K already

4/23 modify, follow Intel suggestion to un-stuff for unused GPIO

strapping — GPIO86 [8]

strapping — GPIO66 [8]

TRACKPAD

TOUCHSCREEN / ALS

PCH GPIO PU/PD

useless GPIO: EC_RCIN_L R44 10K_4; IRQ_SERIRQ R36 10K_4; PCH_SSD_12_EN R399 *10K_4; PCH_SSD_18_EN R33 *10K_4; DEVSLP0 R382 10K_4; PCH_GPIO76 R393 10K_4; ODD_PRSNT# R440 10K_4; TPM_LP_EN_L R402 10K_4; PP3300_SSD_IO_EN R405 *10K_4; GPIO50 R392 10K_4; GPIO70 R348 10K_4; GPIO38 R375 10K_4; GPIO39 R6 10K_4

GSP: GPIO83 R28 *10K_4; GPIO84 R8 *10K_4; GPIO85 R5 *10K_4; GPIO87 R20 *10K_4; GPIO88 R2 *10K_4; GPIO89 R4 *10K_4; GPIO90 R377 *10K_4

UART: GPIO91 R364 *10K_4; GPIO92 R369 *10K_4; GPIO93 R365 *10K_4; GPIO94 R363 *10K_4; GPIO0 R3 *10K_4; GPIO1 R362 *10K_4; GPIO2 R366 *10K_4; GPIO3 R370 *10K_4

SDIO: GPIO64 R329 *10K_4; GPIO65 R349 *10K_4; GPIO67 R335 *10K_4; GPIO68 R341 *10K_4; GPIO69 R339 *10K_4

I2C: I2C0_SDA_GPIO4 R333 4.7K_4; I2C0_SCL_GPIO5 R334 4.7K_4; I2C1_SDA_GPIO6 R331 4.7K_4; I2C1_SCL_GPIO7 R332 4.7K_4

RAM ID

Vender	RAM_ID			Q PN	Mfr. PN	Freq.
	ID2	ID1	ID0			
Micron(4G)	0	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(4G)	0	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Hynix(4G)	0	1	0	AKD5PGSTW13	H5TC4G63AFR-PBA(25nm)	1600MHz
Micron(2G)	1	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHz
Hynix(2G)	1	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz
Hynix(2G)	1	1	0	AKD5PGSTW13	H5TC4G63AFR-PBA(25nm)	1600MHz

CPU thermal trip

Q11 FDV301N; Q12 MMBT3904-7-F; R313 1K_4; R314 1K_4; THRMTRIP# → SYS_SHDN# [26,33,34]

U23 74AUP1G07GW; C249 0.1u/10V_4; R344 10K_4; VCORE_PGOOD [5,32] → IMVP_PWRGD_3V [26]

Q23 2N7002DW; PP3300_WLAN_EN [19,26,35] → WLAN_WAKE_L [19]; PP3300_LTE_EN [21,26] → LTE_WAKE_L [21]

GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

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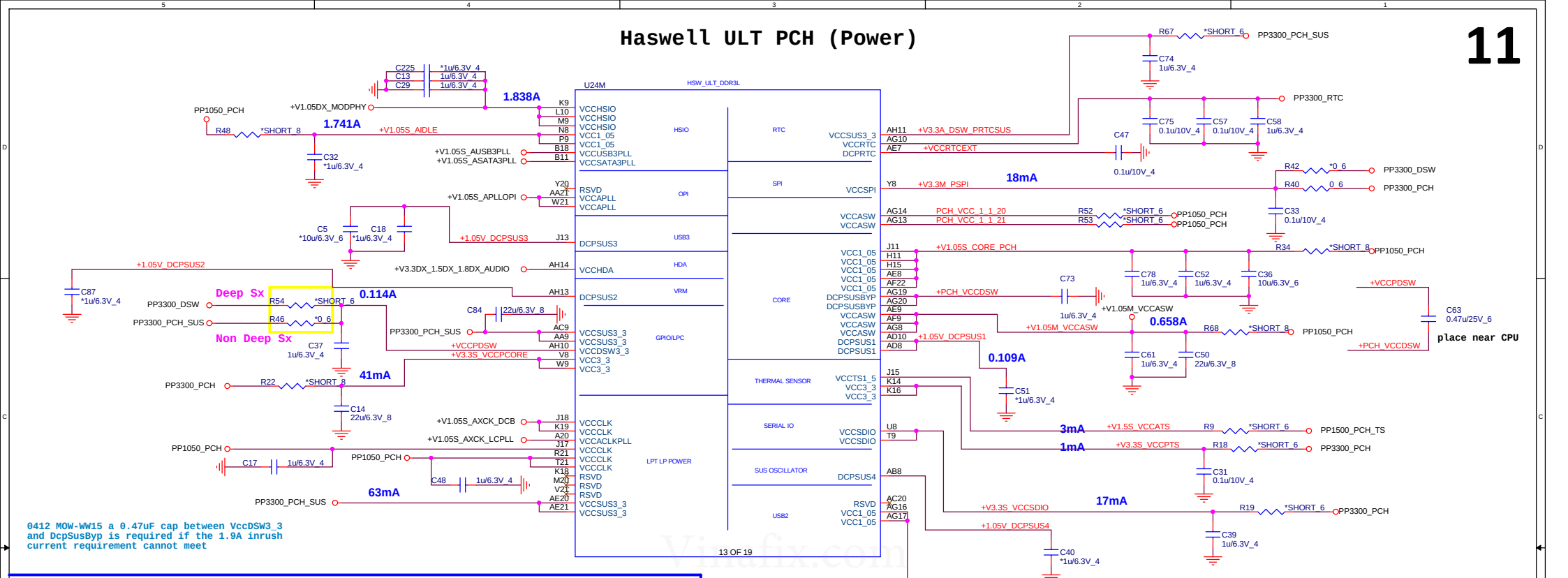
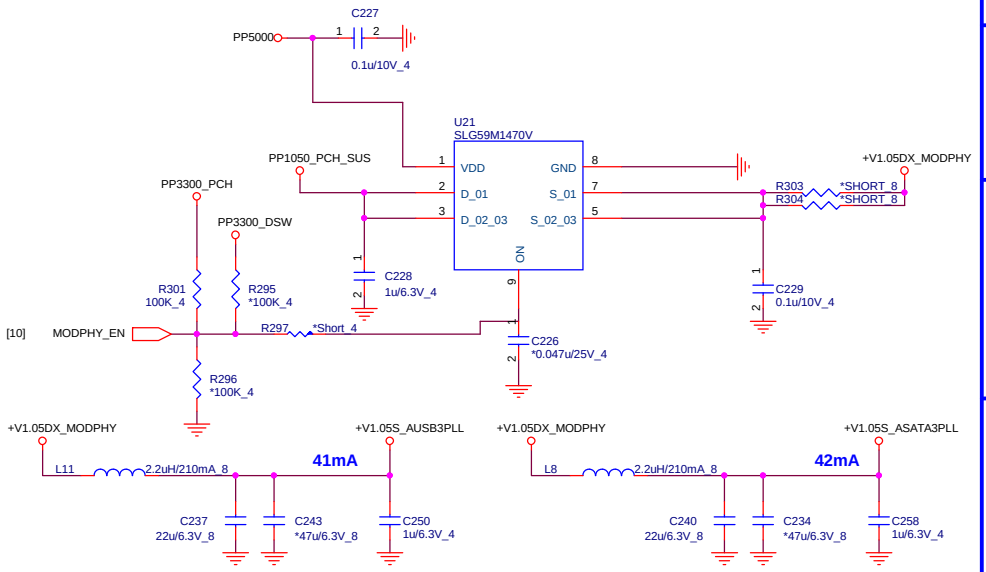
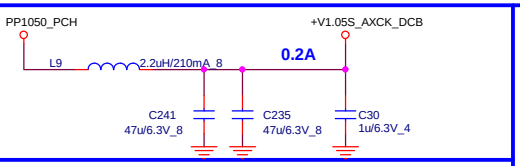
Haswell ULT PCH (Power)



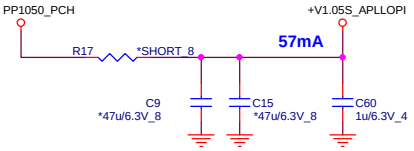
0412 MOW-WW15 a 0.47uF cap between VccDSW3_3 and DcpSusByp is required if the 1.9A inrush current requirement cannot meet

PCH VCCHSIO Power

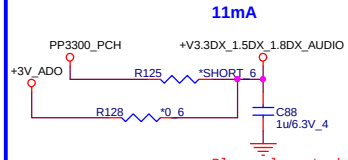


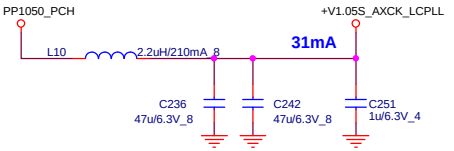


VCCAPLL power



PCH HDA Power





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	PCH 5/6 (POWER)	A

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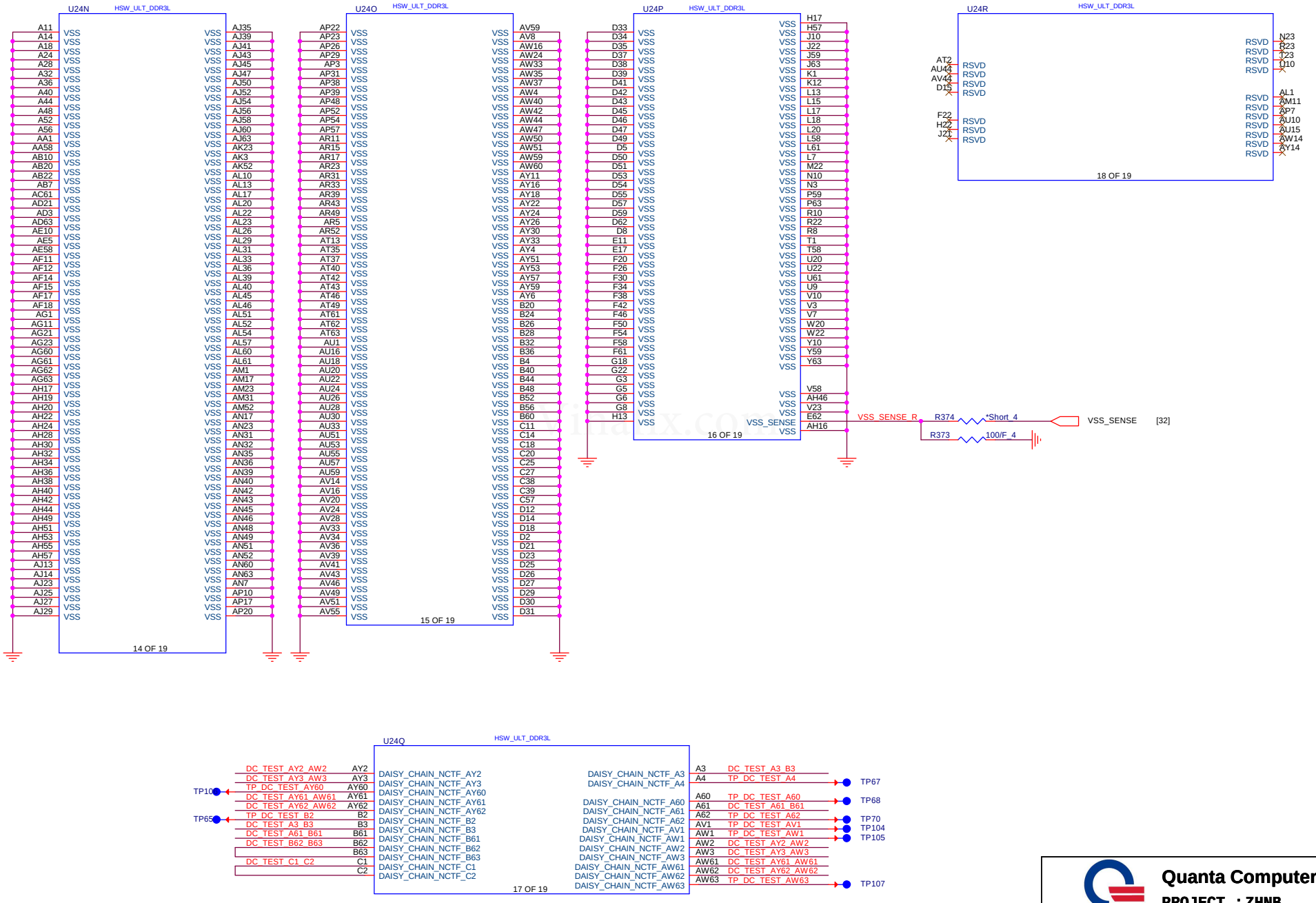
Haswell ULT (GND)



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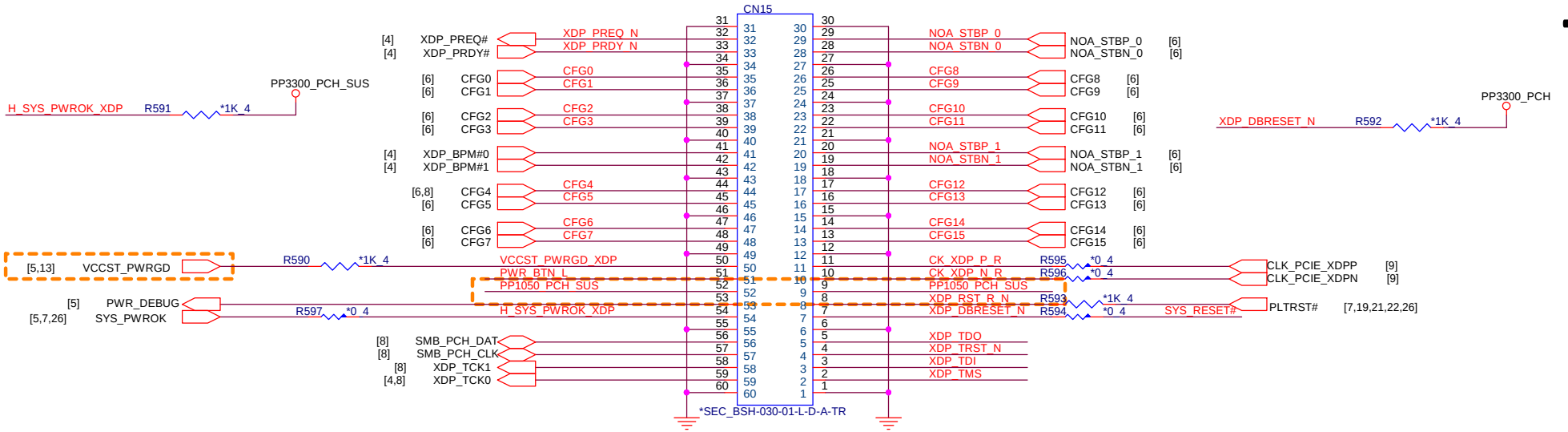
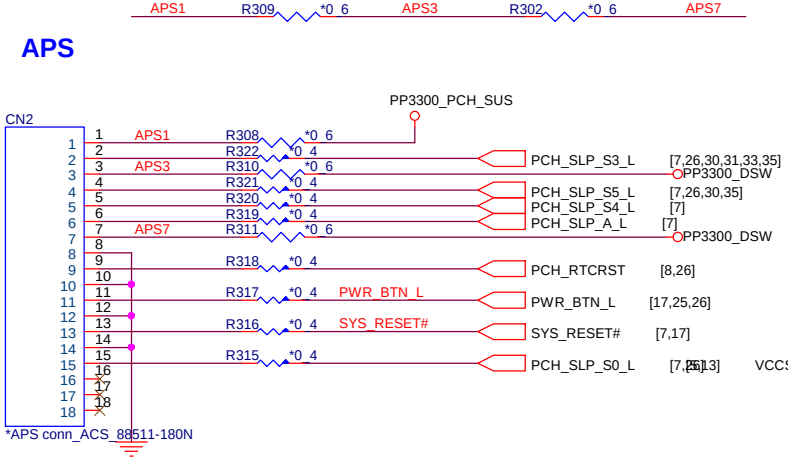
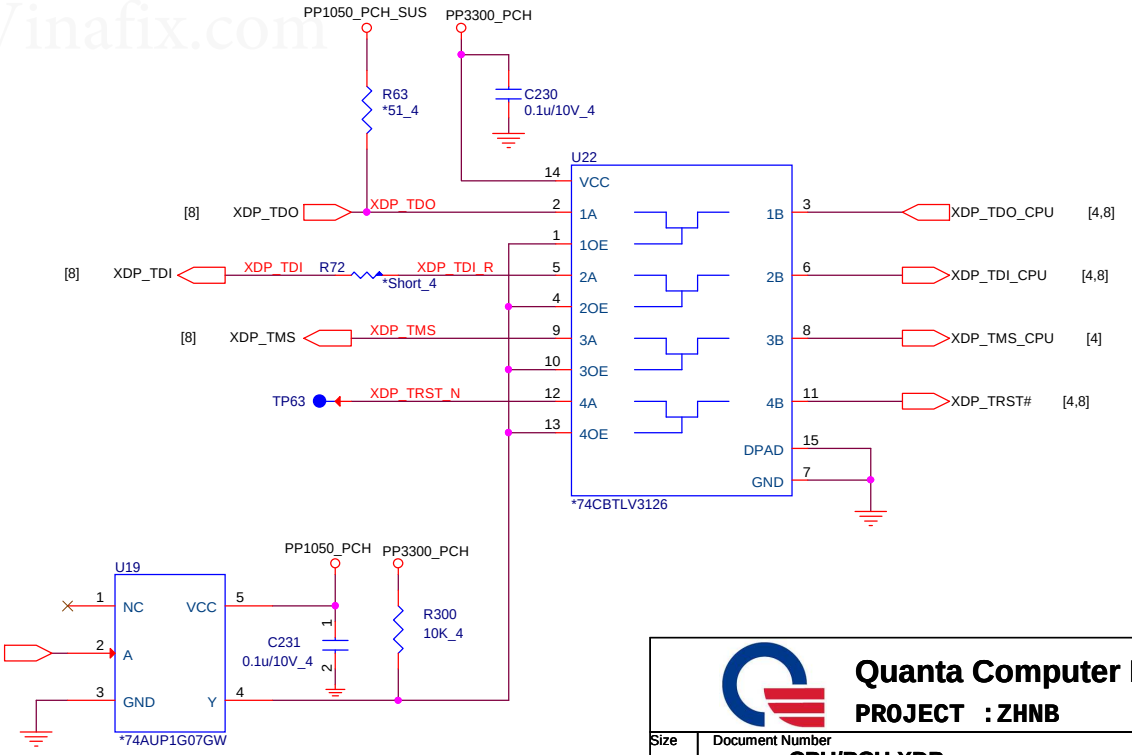


20141021 Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.

APS





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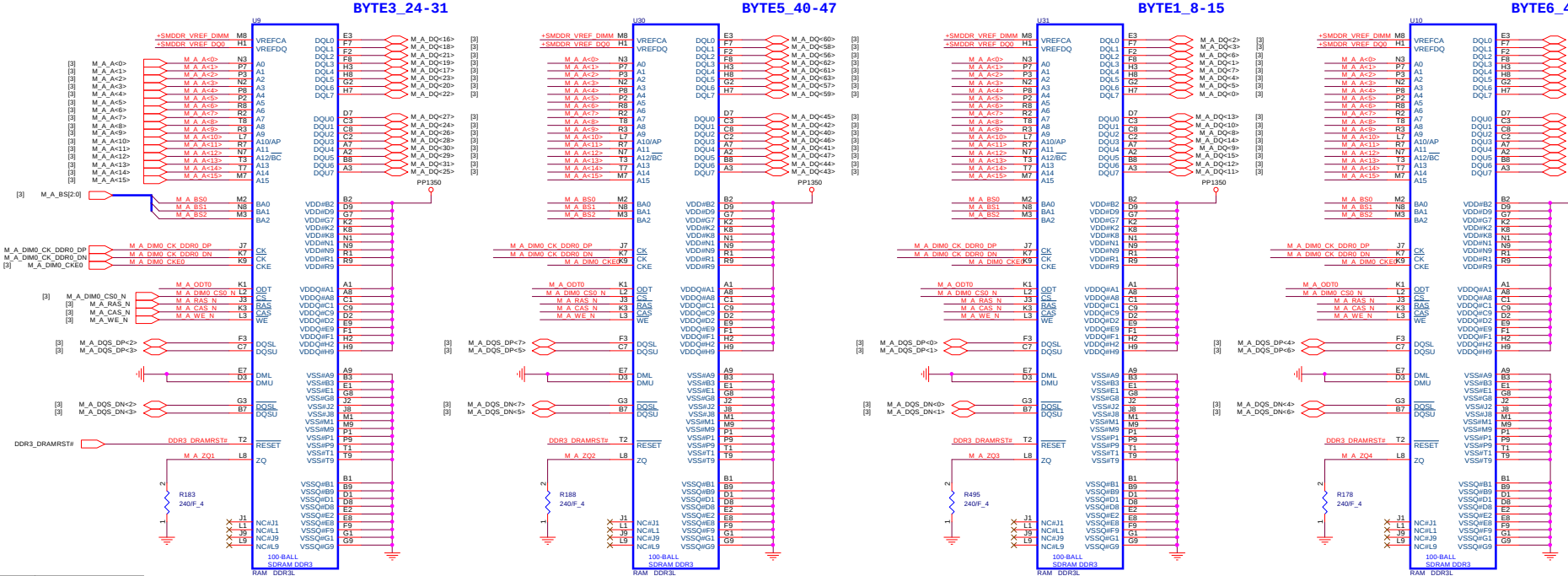
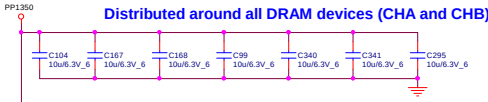
BYTE2_16-23
BYTE3_24-31
BYTE7_56-63
BYTE5_40-47
BYTE0_0-7
BYTE1_8-15
BYTE4_32-39
BYTE6_48-55



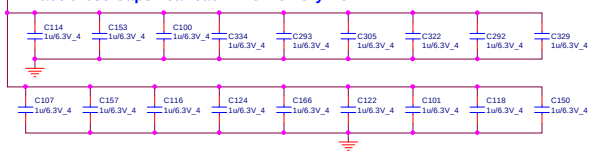
Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

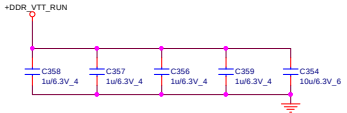
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

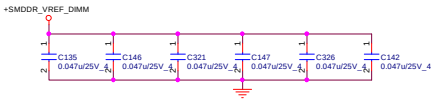
Distributed around all DRAM devices (CHA and CHB)



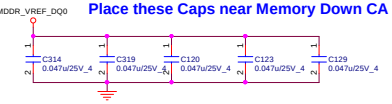
Place these Caps near each X16 Memory Down

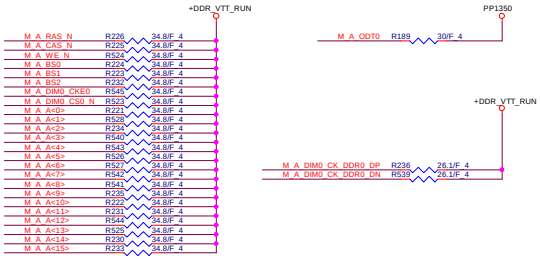




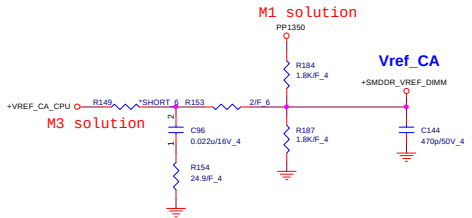


Place these Caps near Memory Down CA & DQ pin

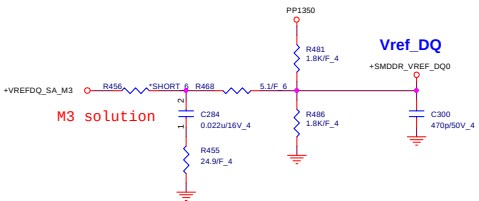


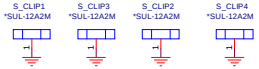


M1 solution



M1 solution





Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	DDR3L MEMORY DOWNx16 A	A

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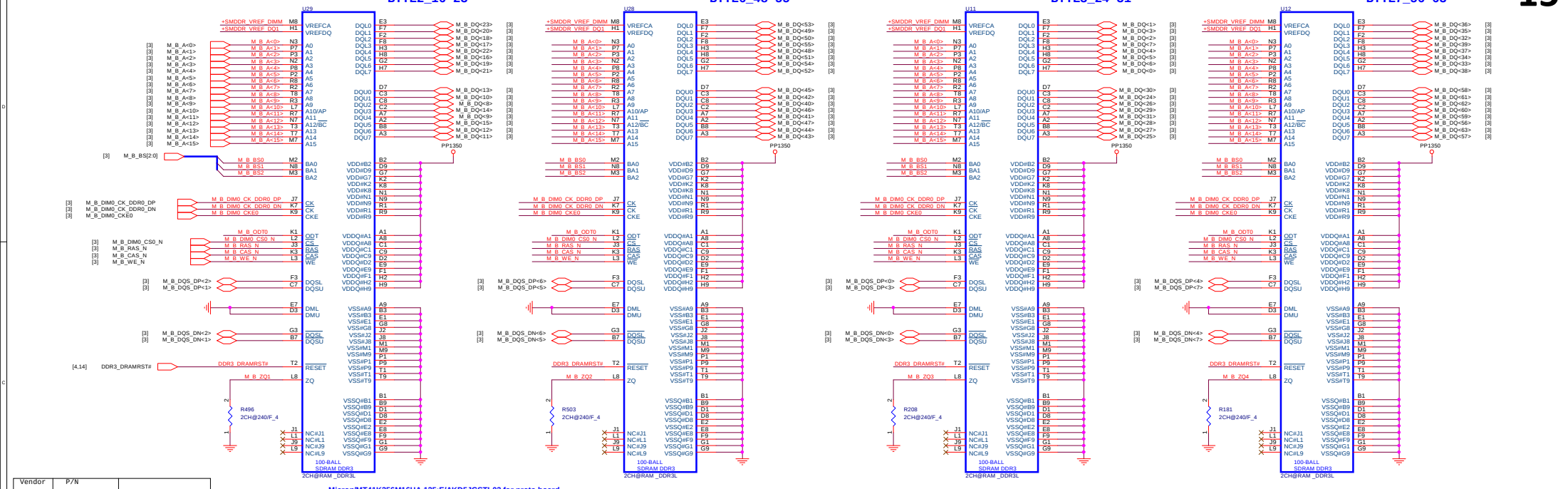
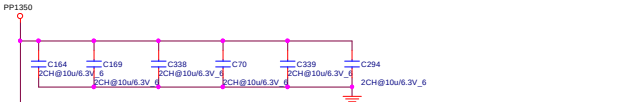
BYTE1_8-15
BYTE2_16-23
BYTE5_40-47
BYTE6_48-55
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE7_56-63

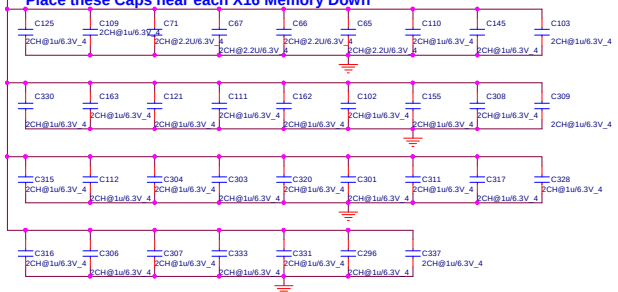


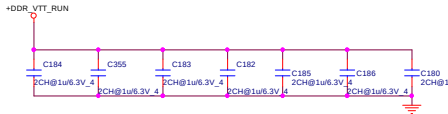
Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

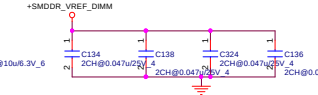
Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600Mhz 4Gb
Elpida	AKD5JGST407	DDR3L 1600Mhz 4Gb
Micron	AKD5JGSTL10	DDR3L 1600Mhz 4Gb



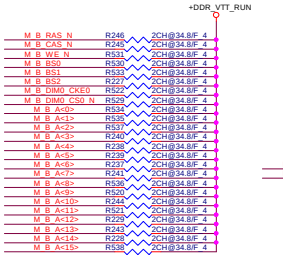
Place these Caps near each X16 Memory Down

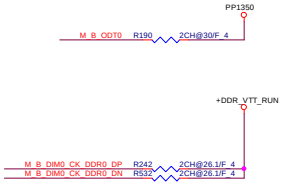




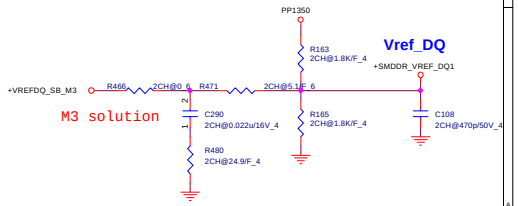


Place these Caps near Memory Down CA & DQ pin





M1 solution



Quanta Computer Inc. PROJECT : ZHNB			
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	DDR3L MEMORY DOWNx16 B		A
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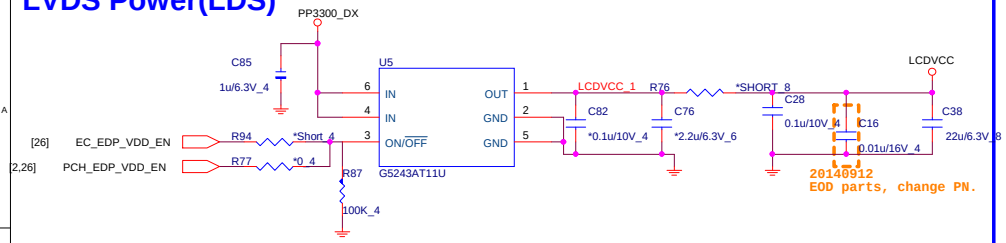
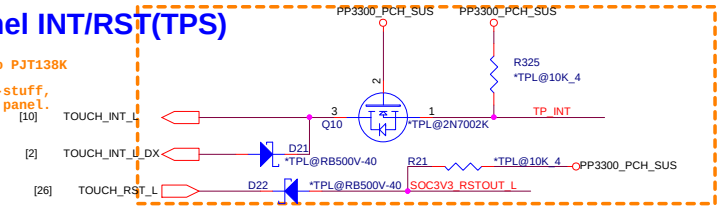
LVDS Power(LDS)



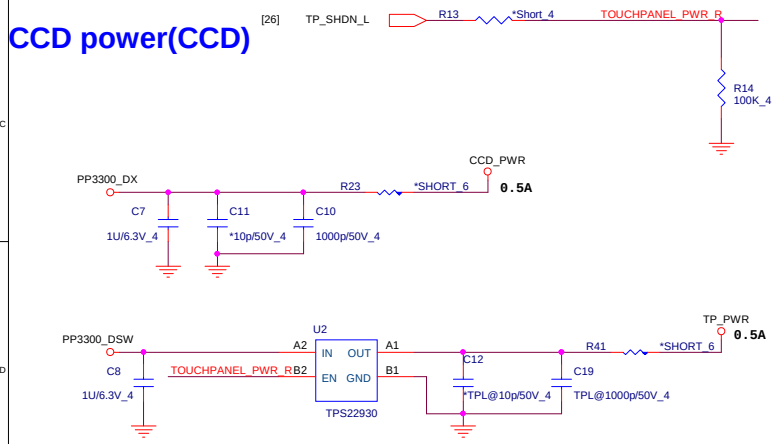
20140912
EOD parts, change PN.

Touch Panel INT/RST(TPS)

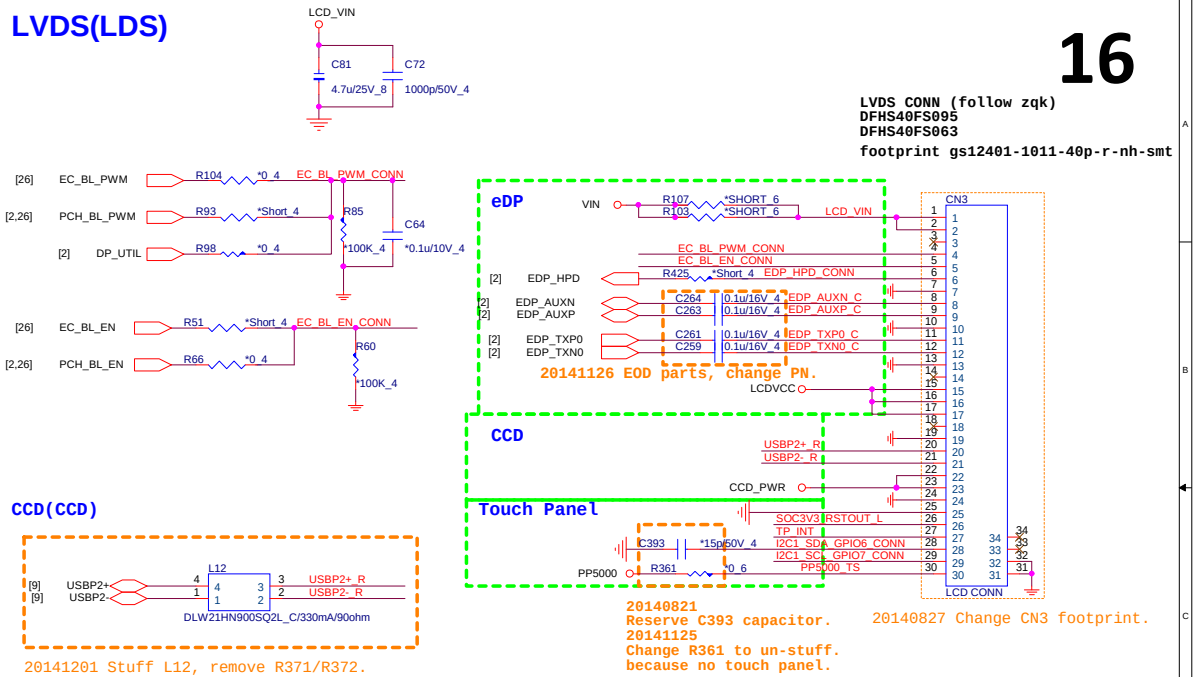
20140821
Q13 FET change to PJT138K
20141125
Change TPS to un-stuff,
because no touch panel.



CCD power(CCD)



LVDS(LDS)



20140827 Change CN3 footprint.

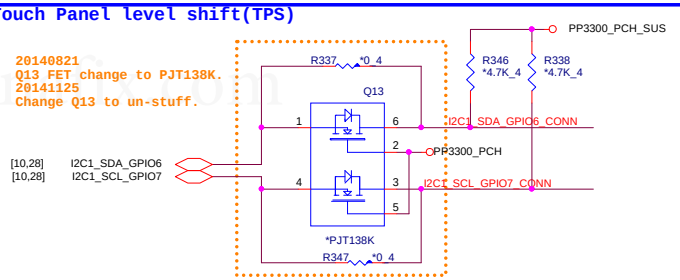
20140821
Reserve C393 capacitor.
20141125
Change R361 to un-stuff.
because no touch panel.

CCD(CCD)

20141201 Stuff L12, remove R371/R372.

Touch Panel level shift(TPS)

20140821
Q13 FET change to PJT138K.
20141125
Change Q13 to un-stuff.



16

LVDS CONN (follow zqk)
DFHS40FS095
DFHS40FS063
footprint gs12401-1011-40p-r-nh-smt

Quanta Computer Inc.
PROJECT : ZHNB

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	LVDS/CCD/DMIC/TS	A

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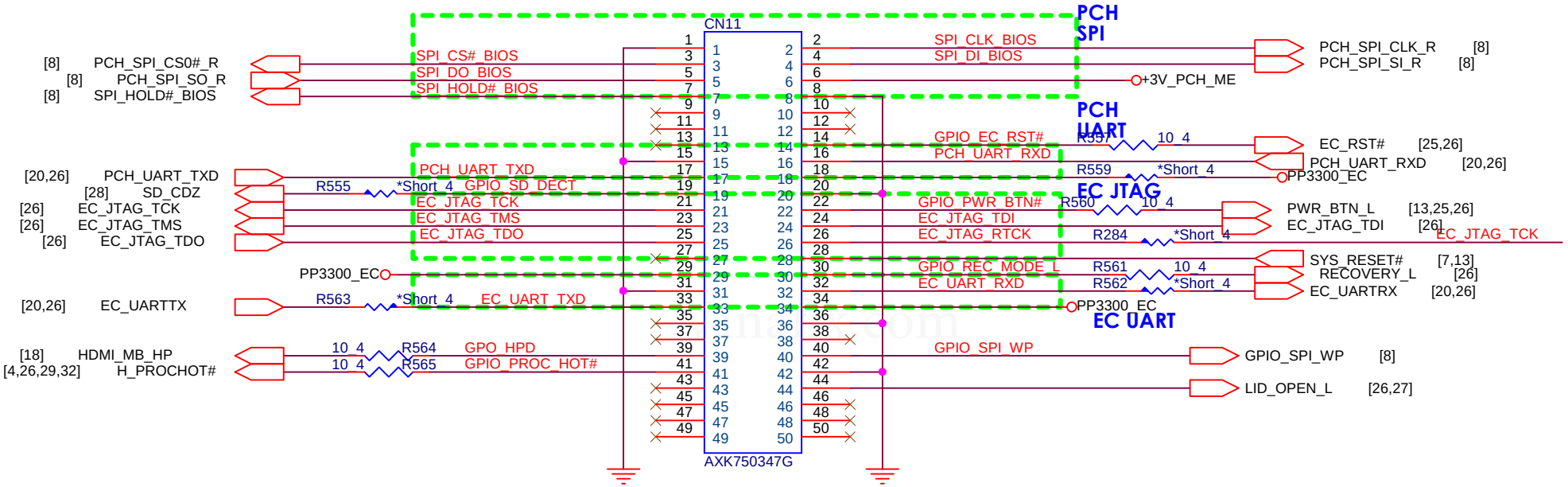
Debug Port(DBG)

```
PIN7 OD      PIN39 OD   PIN49 OD
PIN14 OD     PIN41 OD   PIN50 OD
PIN19 OD     PIN43 OD
PIN22 OD     PIN44 OD
PIN28 OD     PIN45 OD
PIN30 OD     PIN46 OD
PIN37 OD     PIN47 OD
PIN38 OD     PIN48 OD
```



Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: Google Debug	Rev: A
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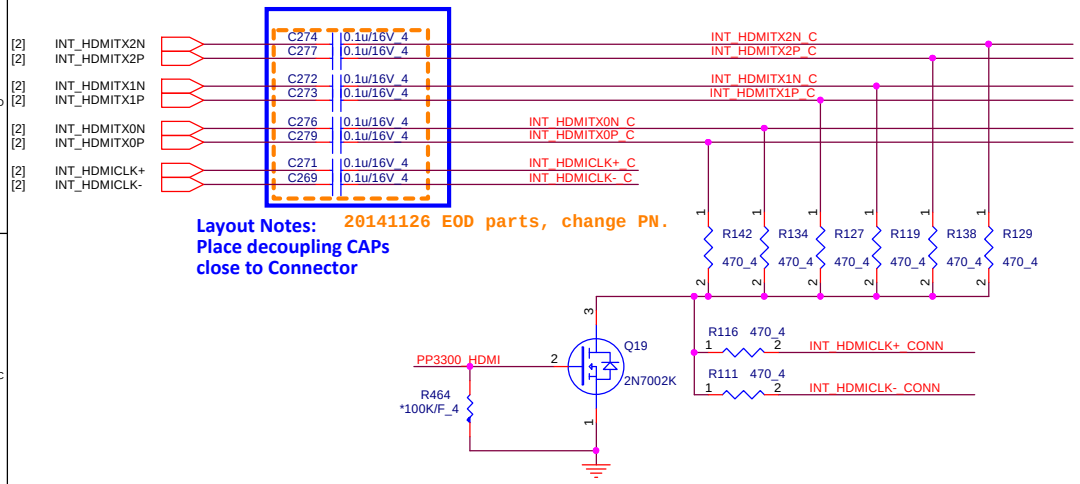
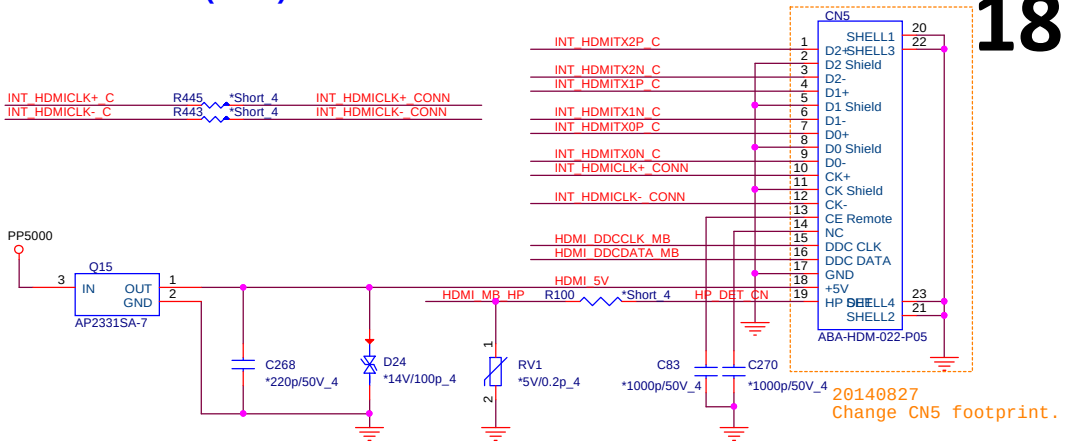
HDMI Cost Reduced level shift (HDM)



Layout Notes:
Place decoupling CAPs close to Connector

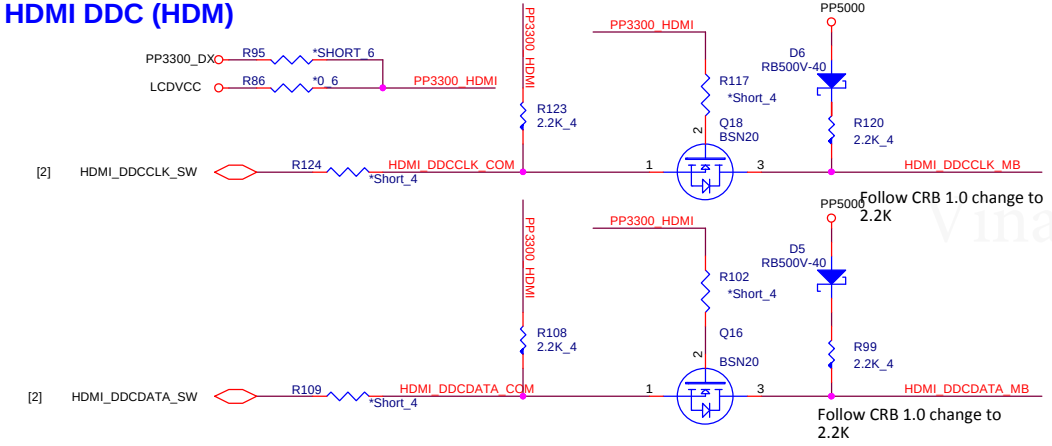
20141126 EOD parts, change PN.

HDMI connector (HDM)

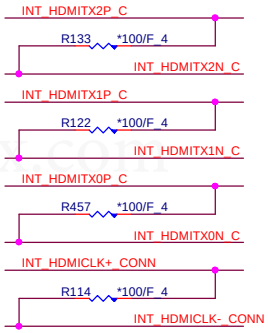


20140827
Change CN5 footprint.

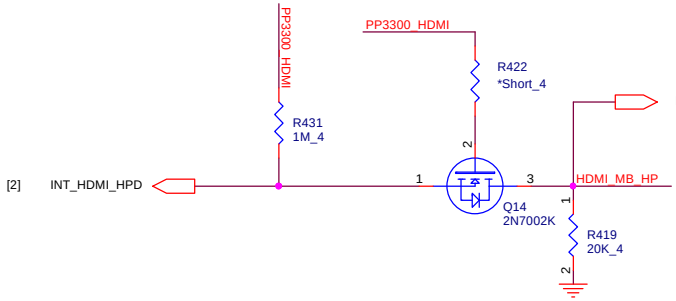
HDMI DDC (HDM)



EMI (EMC)



HDMI-detect (HDM)



Quanta Computer Inc.		
PROJECT : ZHNB		
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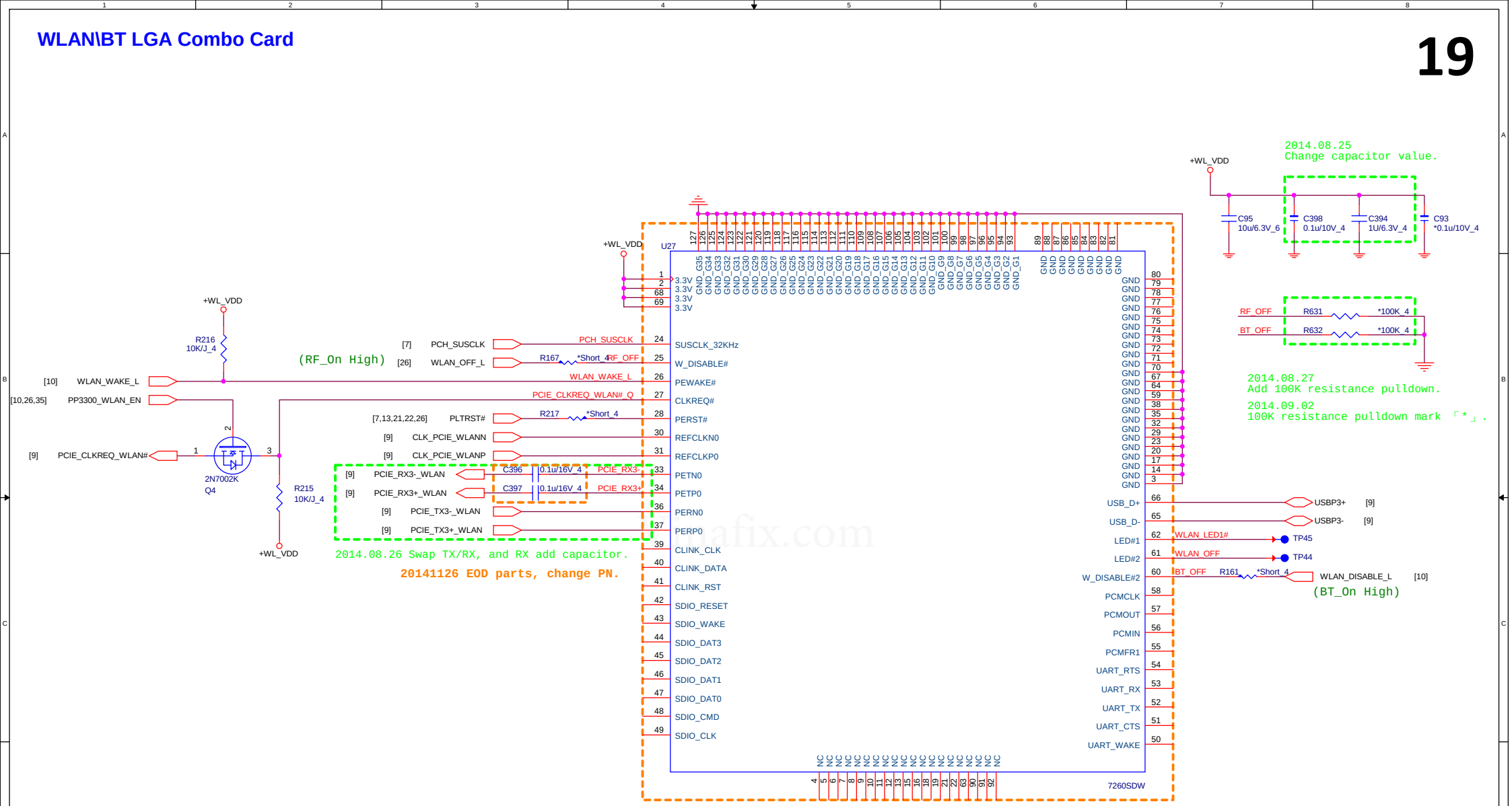
WLAN\BT LGA Combo Card



20140820 On board IC change to same as ZS8 connector
20140822 Return to another wifi onboard module 7260SDW
20140826 Change wifi onboard module 7260SDW footprint
20140909 Change wifi onboard module 7260SDW footprint
20141014 Change wifi onboard module 7260SDW PN.

Quanta Computer Inc.		
PROJECT : ZHNB		
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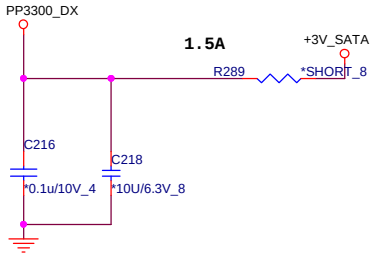
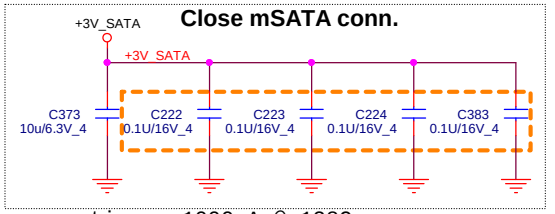
NGFF SSD connector.

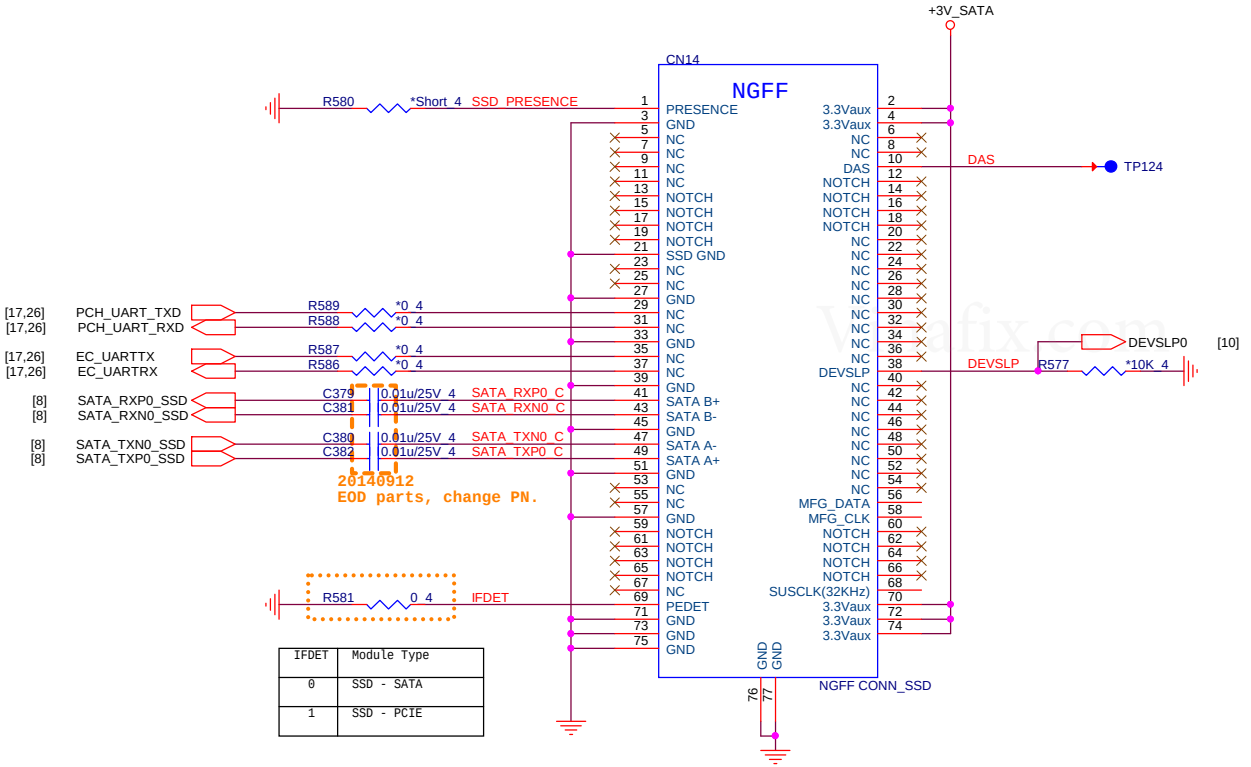
San Disk SSD Card.





20141126 EOD parts, change PN.

rating = 1000mA @ 128G



IFDET	Module Type
0	SSD - SATA
1	SSD - PCIE

Quanta Computer Inc.

PROJECT : ZHNB

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	NGFF SSD	A

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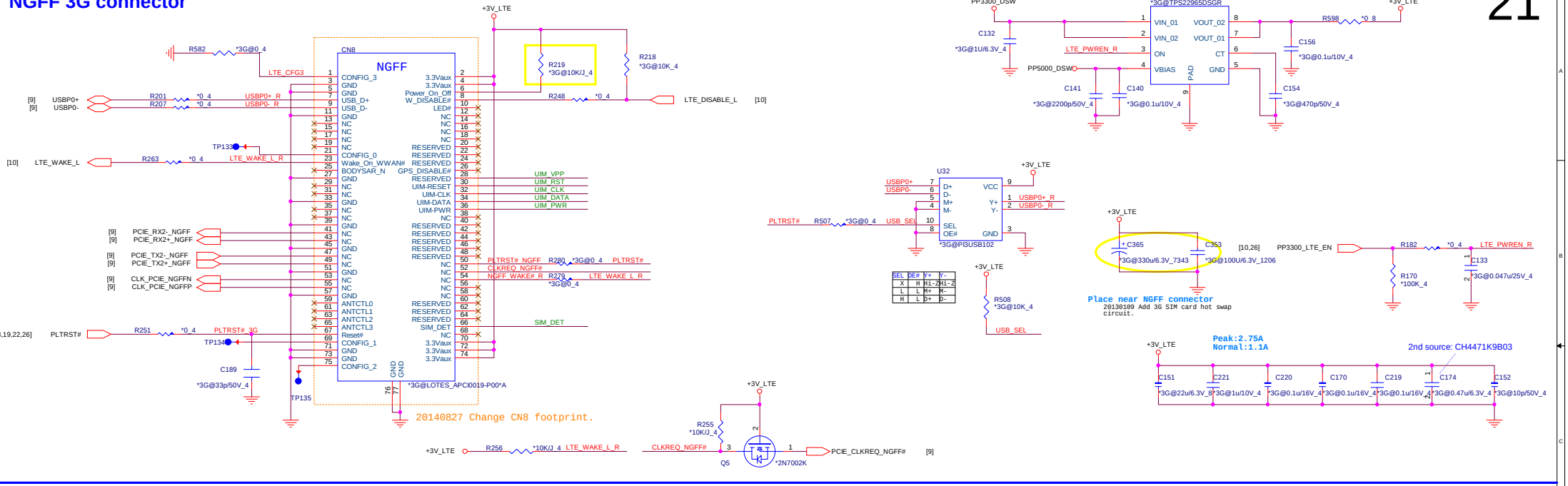
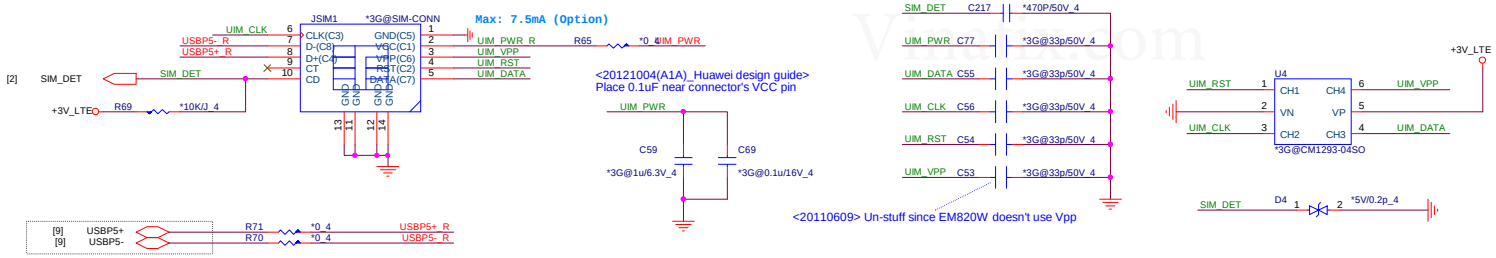
NGFF 3G connector



MultiMedia SIM (MNC)

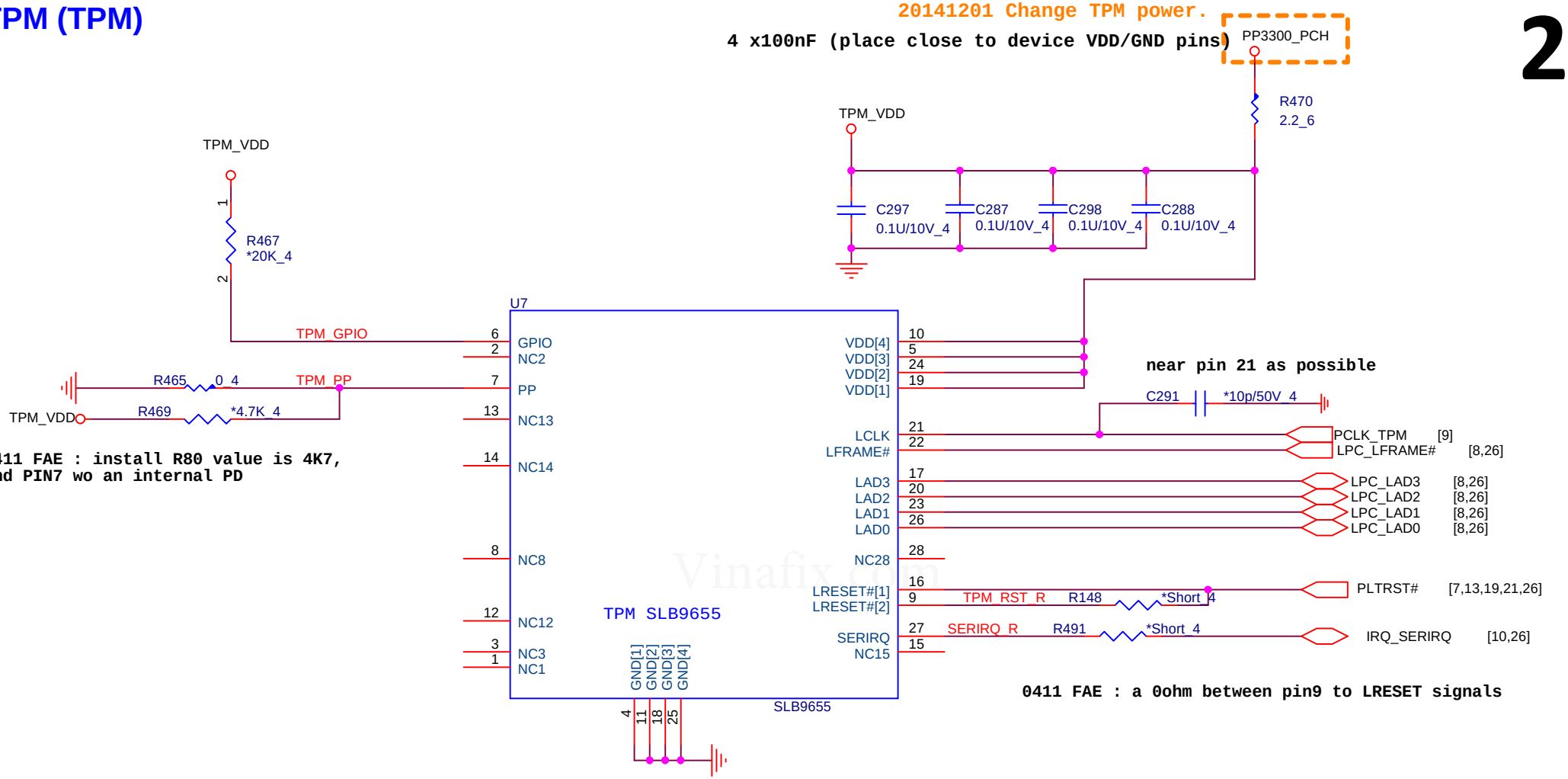
<Layout Notes> Keep USIM signals max length within 8000mils.



TPM (TPM)

20141201 Change TPM power.

4 x100nF (place close to device VDD/GND pins)



0411 FAE : install R80 value is 4K7, and PIN7 wo an internal PD

0411 FAE : a 0ohm between pin9 to LRESET signals

Quanta Computer Inc.

PROJECT : ZHNB

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	TPM SLB9655 / LED	A

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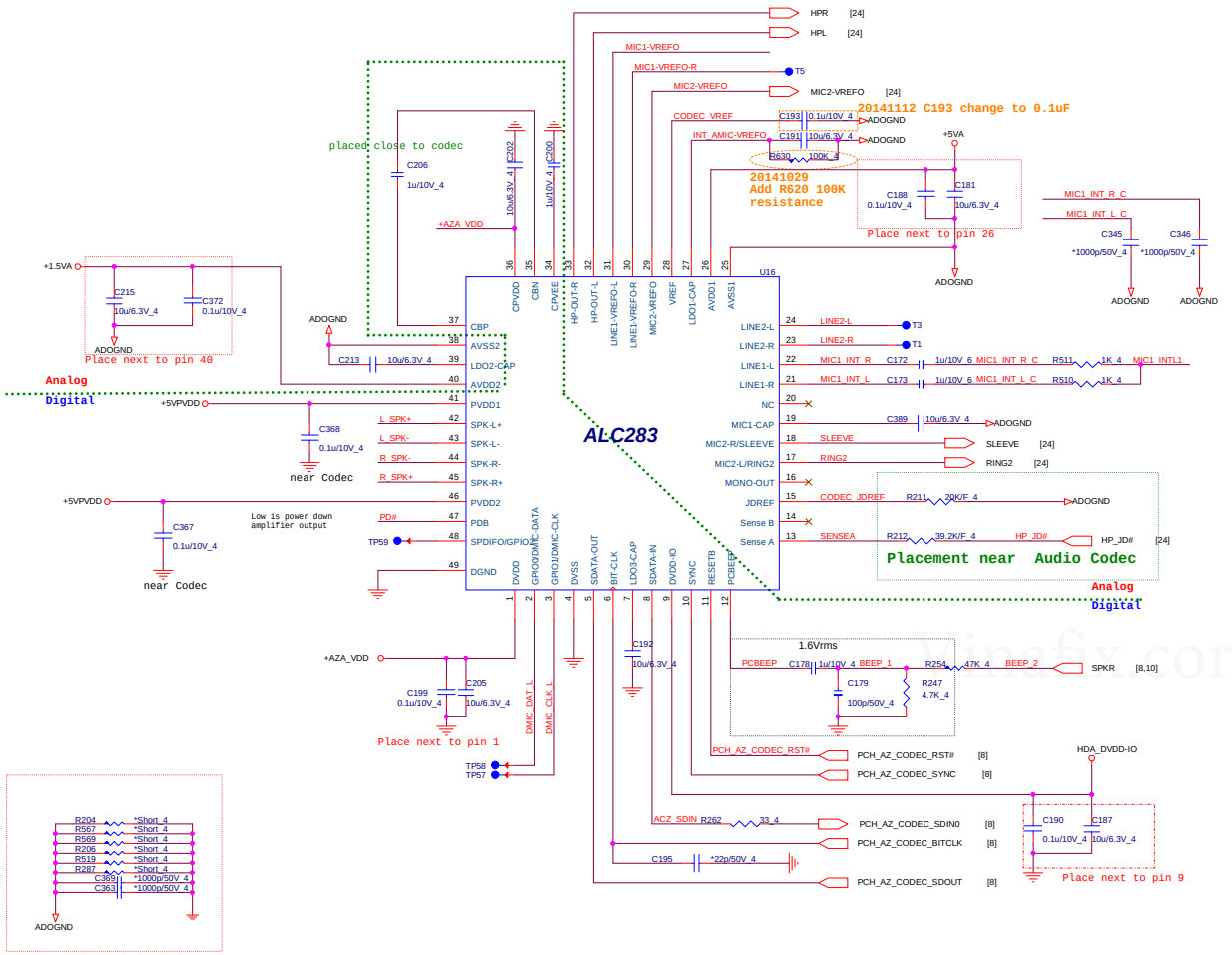
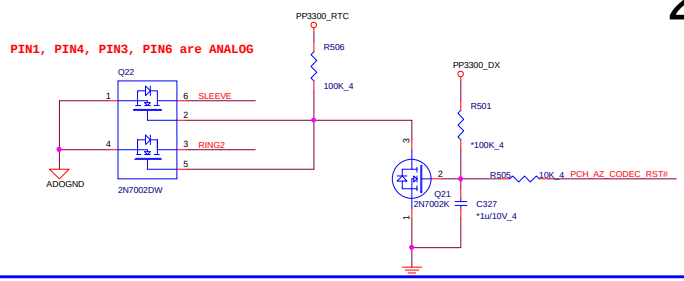
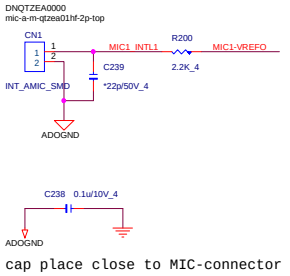
Codec(ADO)



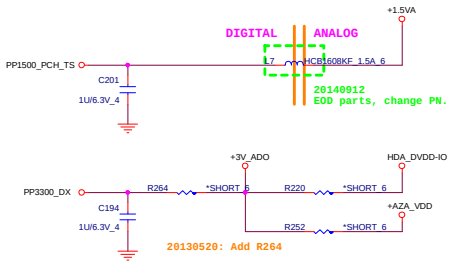
Grounding circuit(ADO)



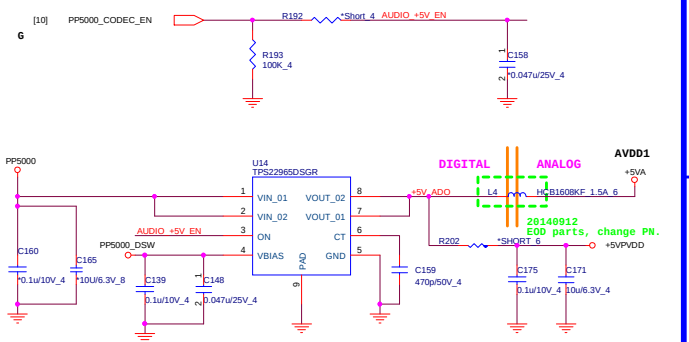
INT MIC array



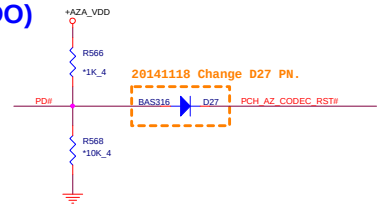
Codec PWR 3V/1.5V(ADO)



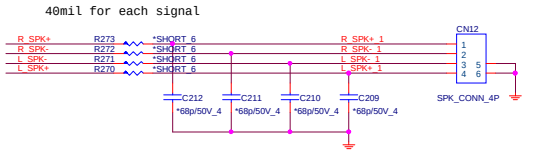
Codec PWR 5V(ADO)



Mute(ADO)



Internal Speaker



Quanta Computer Inc.	
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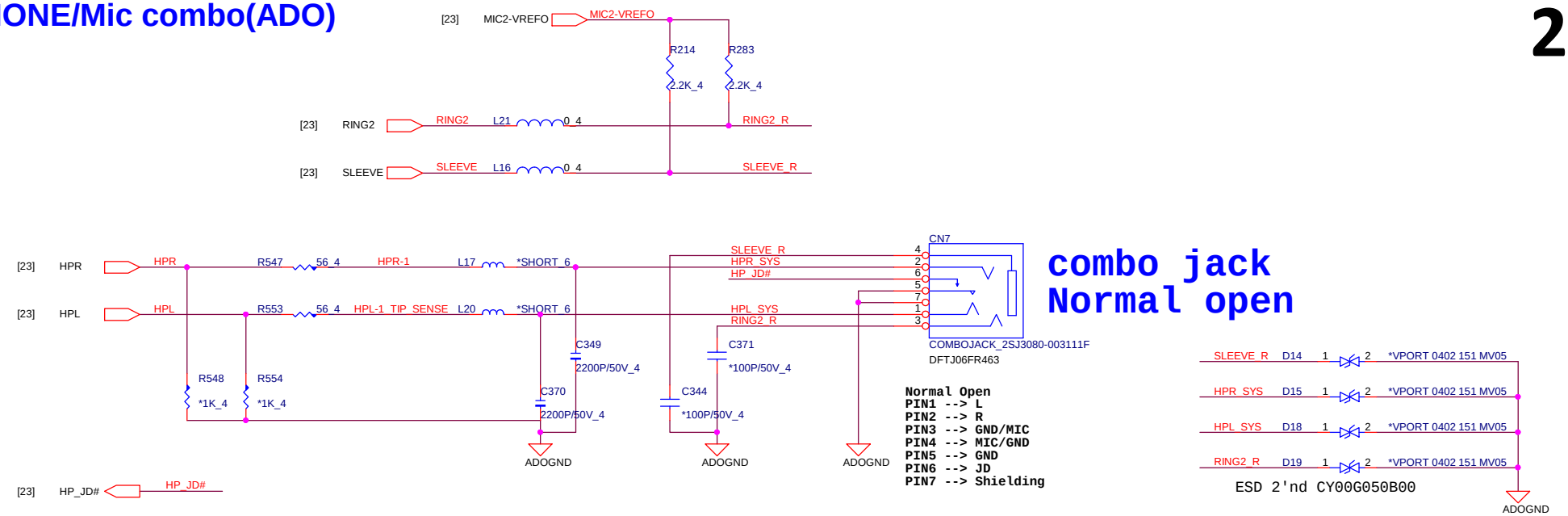
HEADPHONE/Mic combo(ADO)



combo jack Normal open

Normal Open
PIN1 --> L
PIN2 --> R
PIN3 --> GND/MIC
PIN4 --> MIC/GND
PIN5 --> GND
PIN6 --> JD
PIN7 --> Shielding

Quanta Computer Inc.
PROJECT : ZHNB

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	Audio Headset SW	A
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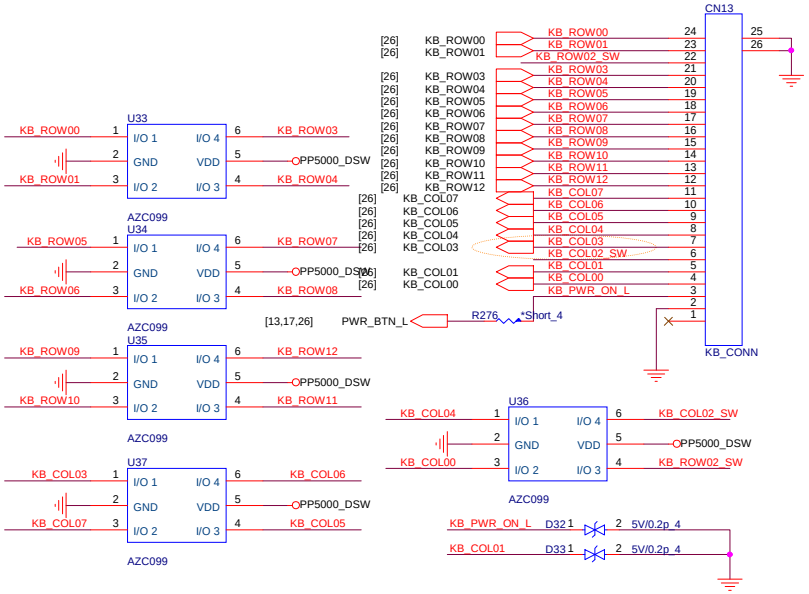
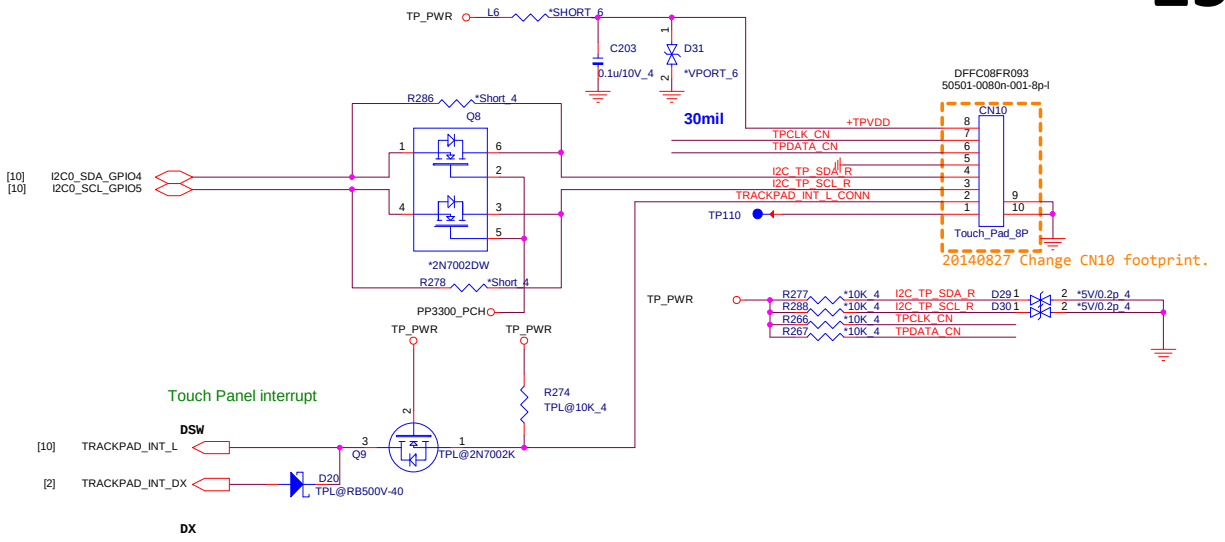
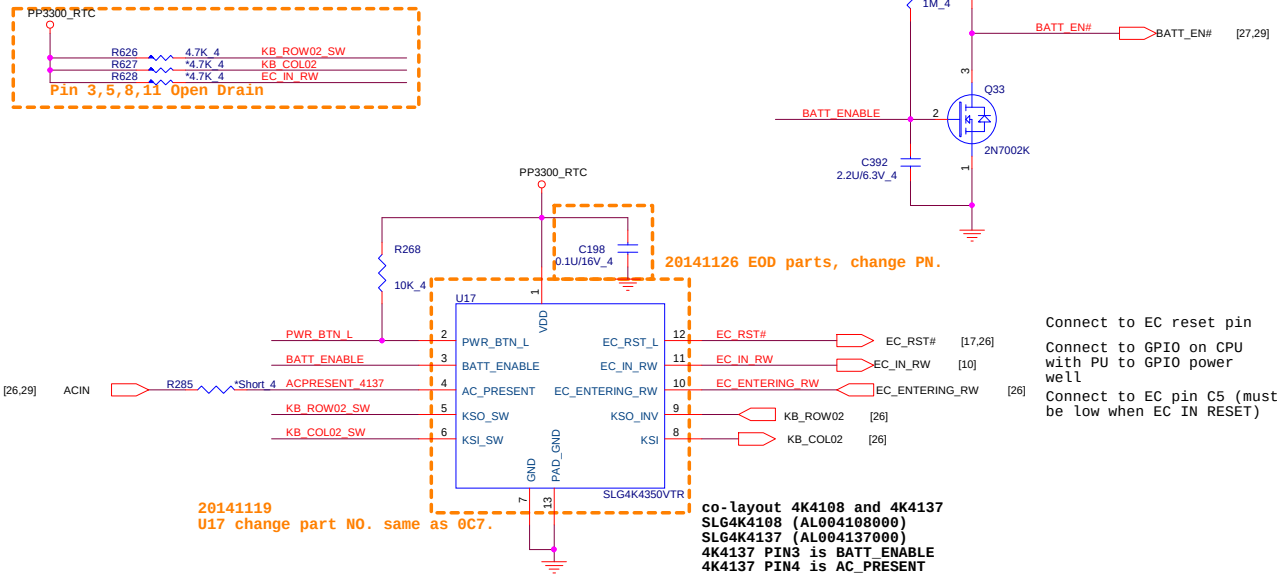
K/B (KBC)



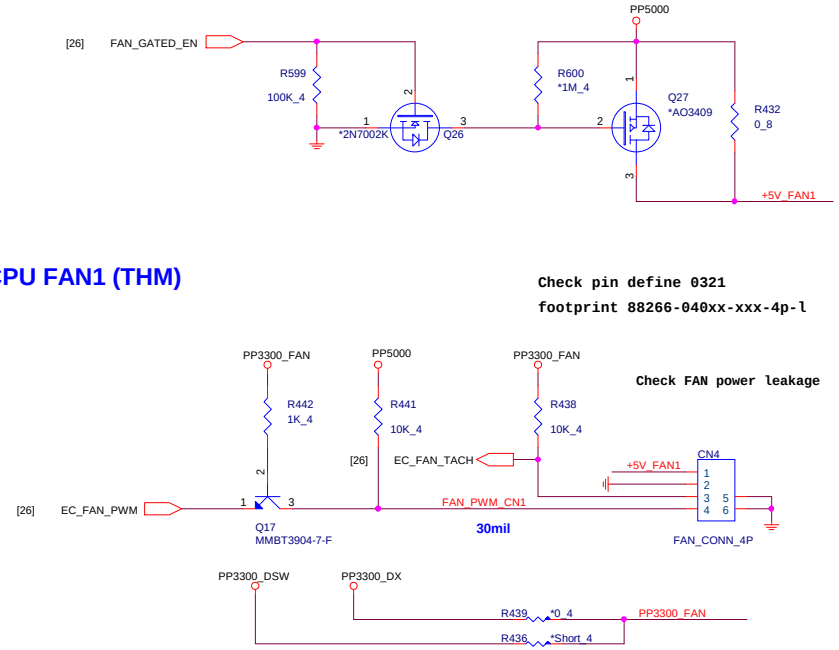
TOUCHPAD BOARD CONN (TPD)



HOLELESS RESET 2-CHIP(KBC)



CPU FAN1 (THM)



Quanta Computer Inc.
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Size	Document Number	Rev
	KB/TP/FAN/HW Reset	A
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EC(KBC)

20141107 Change U5 PN.
20141201 Change U5 new PN.

20140912 EOD parts, change PN.

20140912 EOD parts, change PN.

20140912 EOD parts, change PN.

20141120 Change EC_BRD_ID, ID2 change to High, ID3 change to Low, because EC change code.

20141118 Change D28 PN.

20140912 EOD parts, change PN.

SM BUS ARRANGEMENT TABLE

SM Bus 0	BATT and CHARGER
SM Bus 1	NA
SM Bus 2	THERMAL SENSOR

SM BUS/I2C PU(KBC)

BATT and CHARGER / LCD BL
EC_SMB0_CLK R185 4.7K_4
EC_SMB0_DATA R186 4.7K_4

Light BAR
EC_SMB1_CLK R209 4.7K_4
EC_SMB1_DATA R213 4.7K_4

THERMAL SENSOR
EC_SMB2_CLK R498 4.7K_4
EC_SMB2_DATA R499 4.7K_4

EC HIB WAKE SOURCES

For test only

J1 *SHORT_ PAD1

Quanta Computer Inc.	
PROJECT : ZHNB	
Size	Document Number: KBC TI TM4E1G31H6ZRBI
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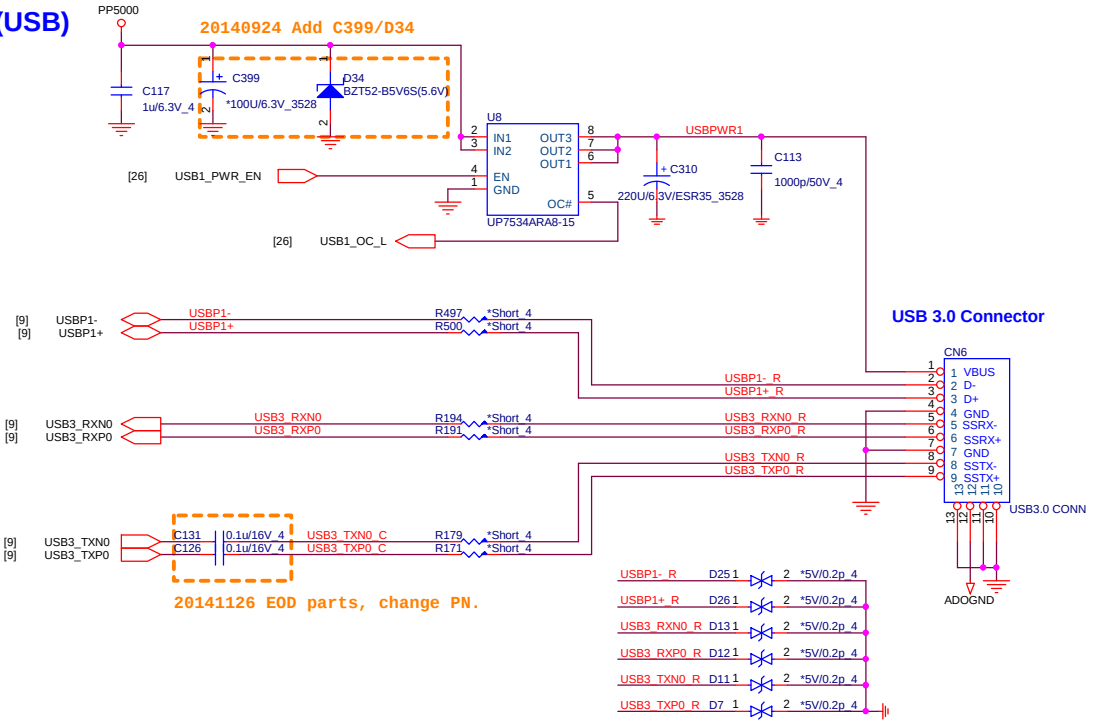
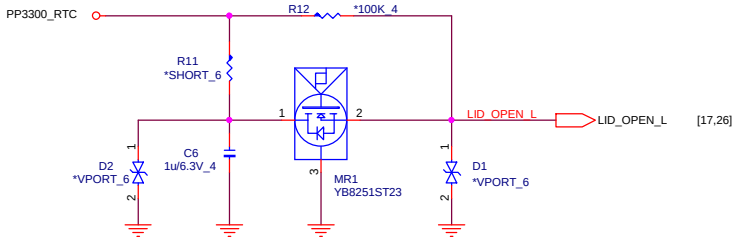
Date: Thursday, December 04, 2014	Sheet 26 of 39

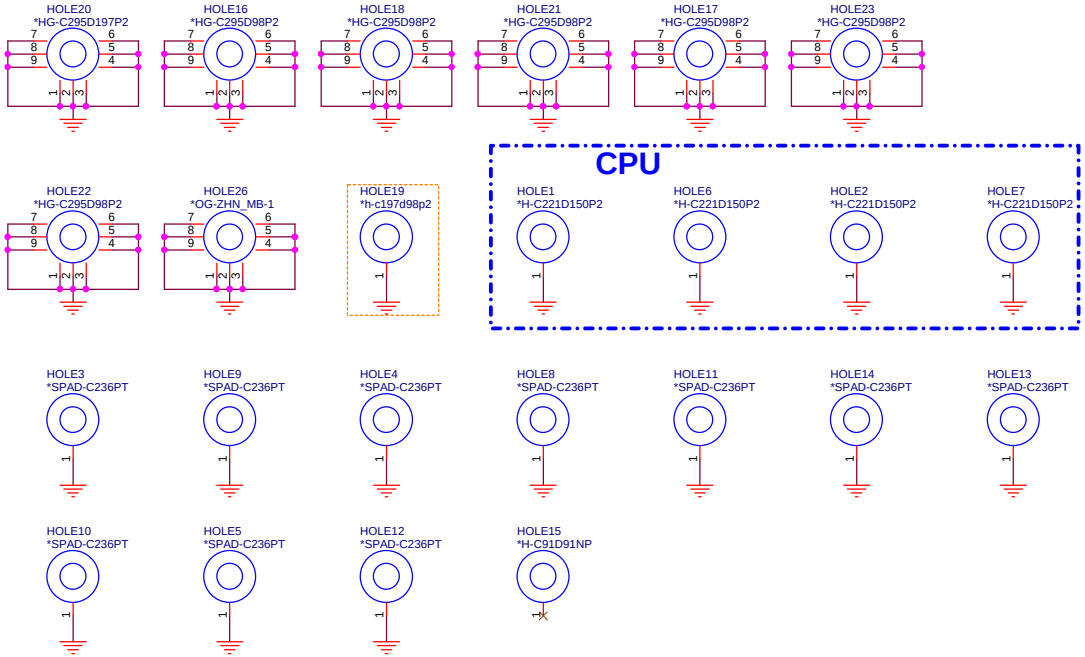
USB3.0(USB)



Lid Switch (HSR)

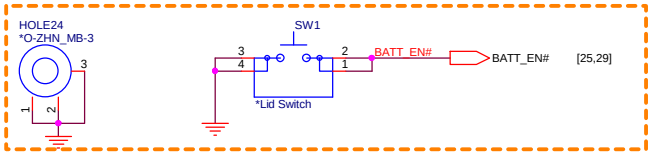


HOLE(OTH)



20140909 Change HOLE19 footprint.

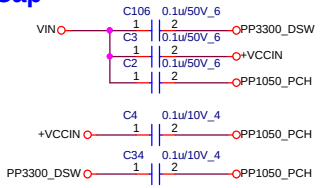
BATT Enable short pad



20141119 HOLE24 remove BATT_EN# pin3.
SW1 change to un-stuff,
because enable control by U17.

ROM WP#

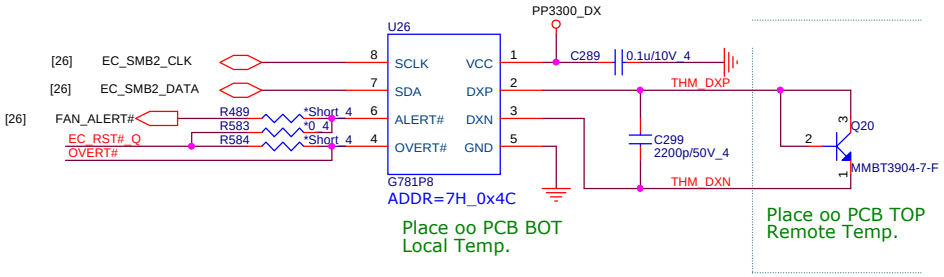
EMI Cap

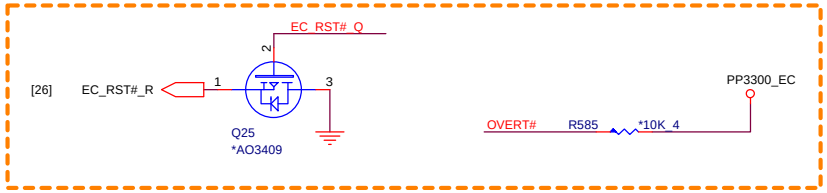


Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	USB3/Hole	A
Date: Thursday, December 04, 2014	Sheet 27 of 39	

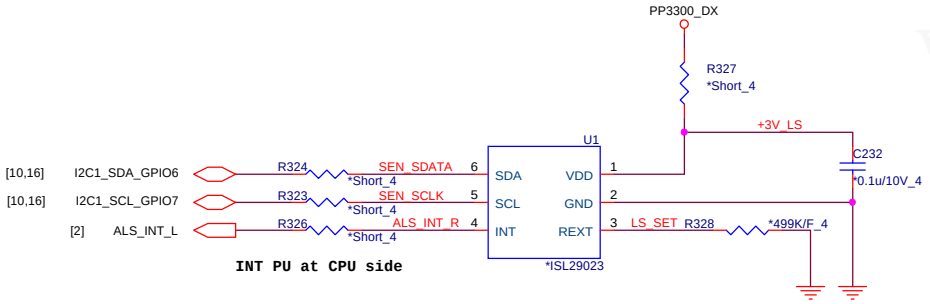
Thermal Sensor(THM)





20140925 Q25/R585 mark 「*」un-stuff.
OVERT# power PP3300_DX change to PP3300_EC.

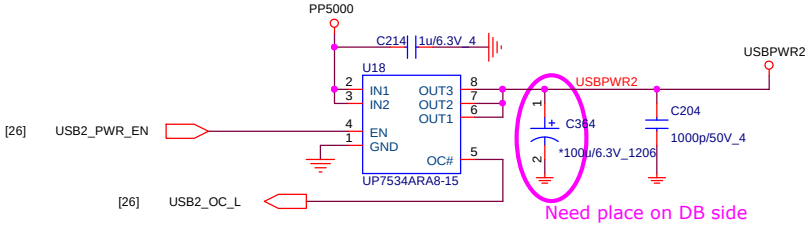
Light sensor & TP (SER)

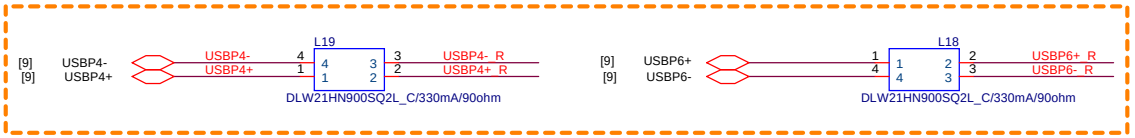


INT PU at CPU side

ADDR: 1000100

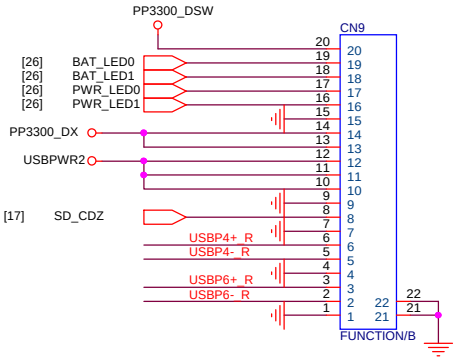
FUNCTION DB





20141201 stuff L18/L19, remove R549/R550/R551/R552.

footprint 88511-2001-20p-l
DFFC20FR043



HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2

Quanta Computer Inc.
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Size	Document Number	Rev
	DB/ALS/Thermal sensor	A
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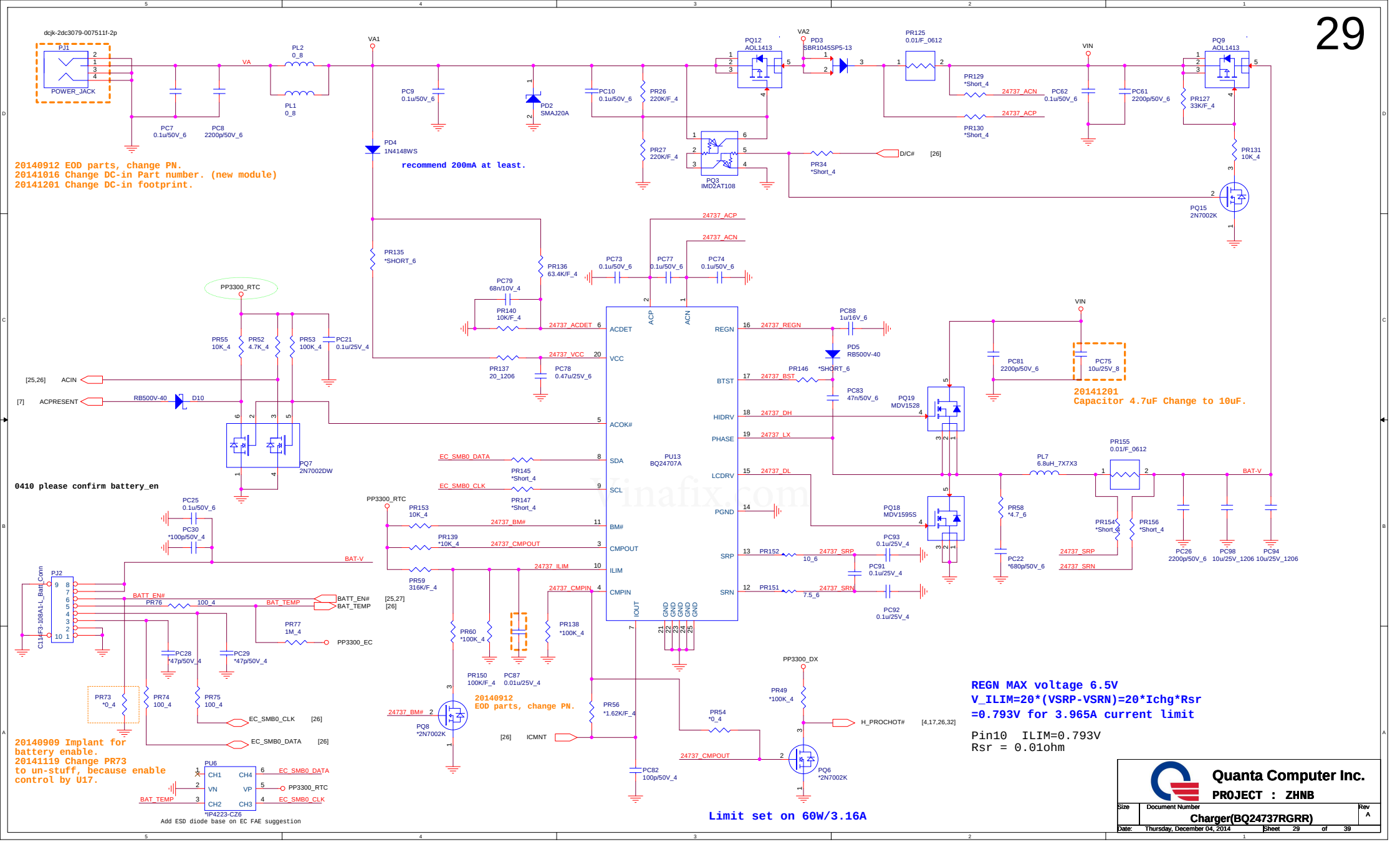
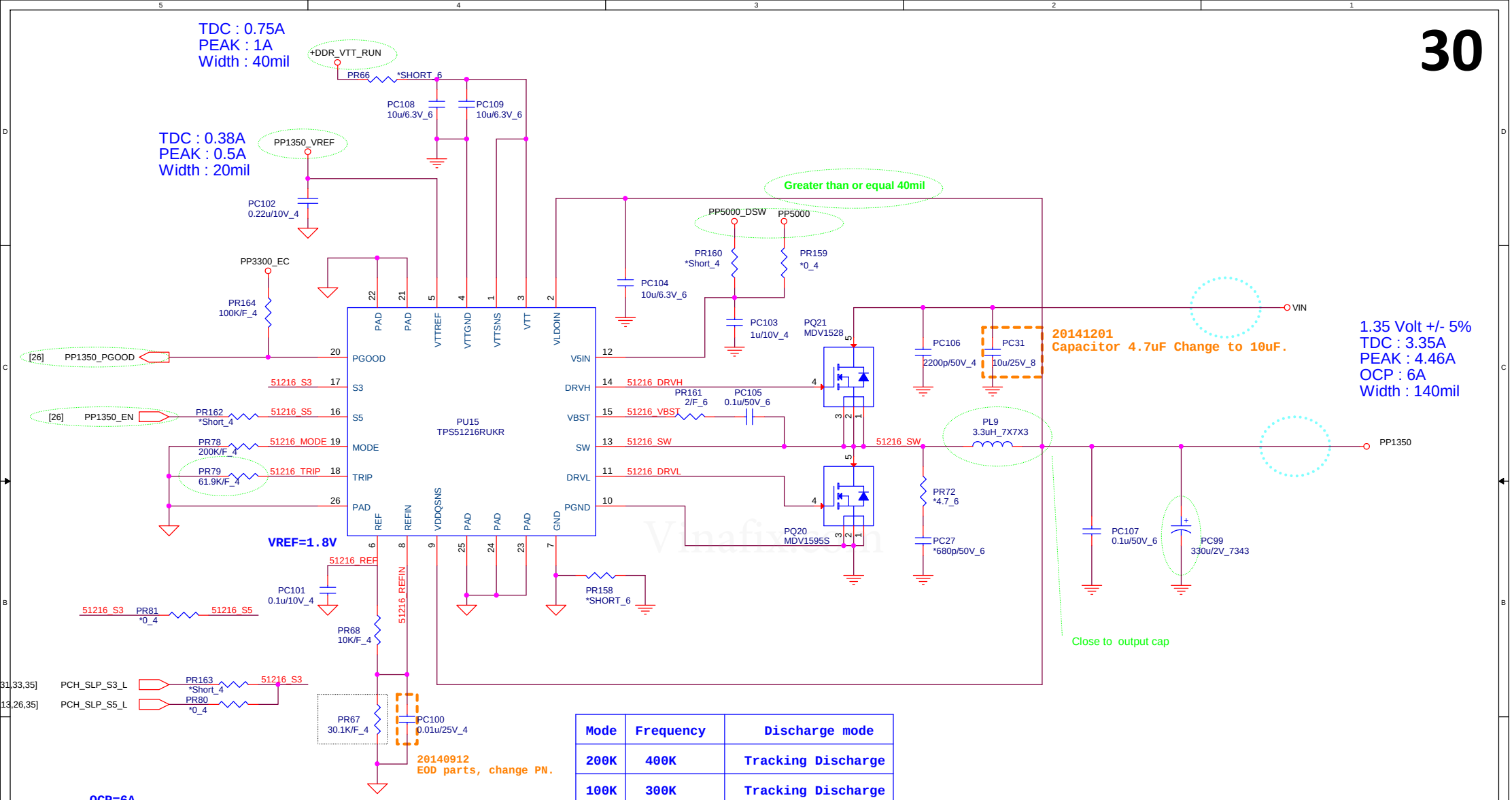


Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number	Rev
	Charger(BQ24737RGRR)	A
Date: Thursday, December 04, 2014	Sheet 29 of 39	



Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

OCP=6A
L ripple current
=(19-1.35)*1.35/(3.3u*400k*19)
=0.95A
Vtrip=[6-(0.95/2)]*14mohm
=0.07735V
Rlimit=0.07335/10uA*8=61.88Kohm

Quanta Computer Inc.
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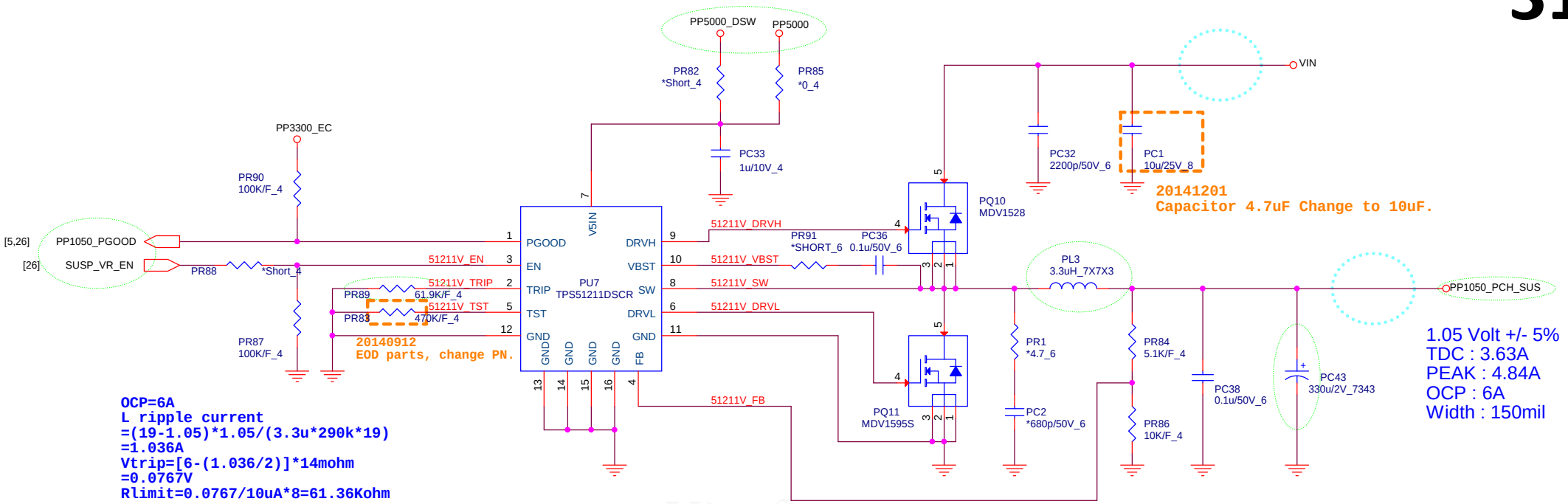
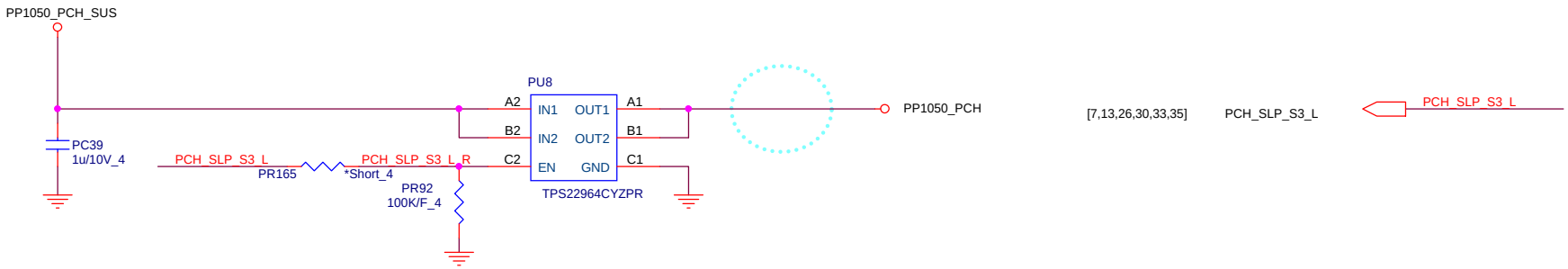
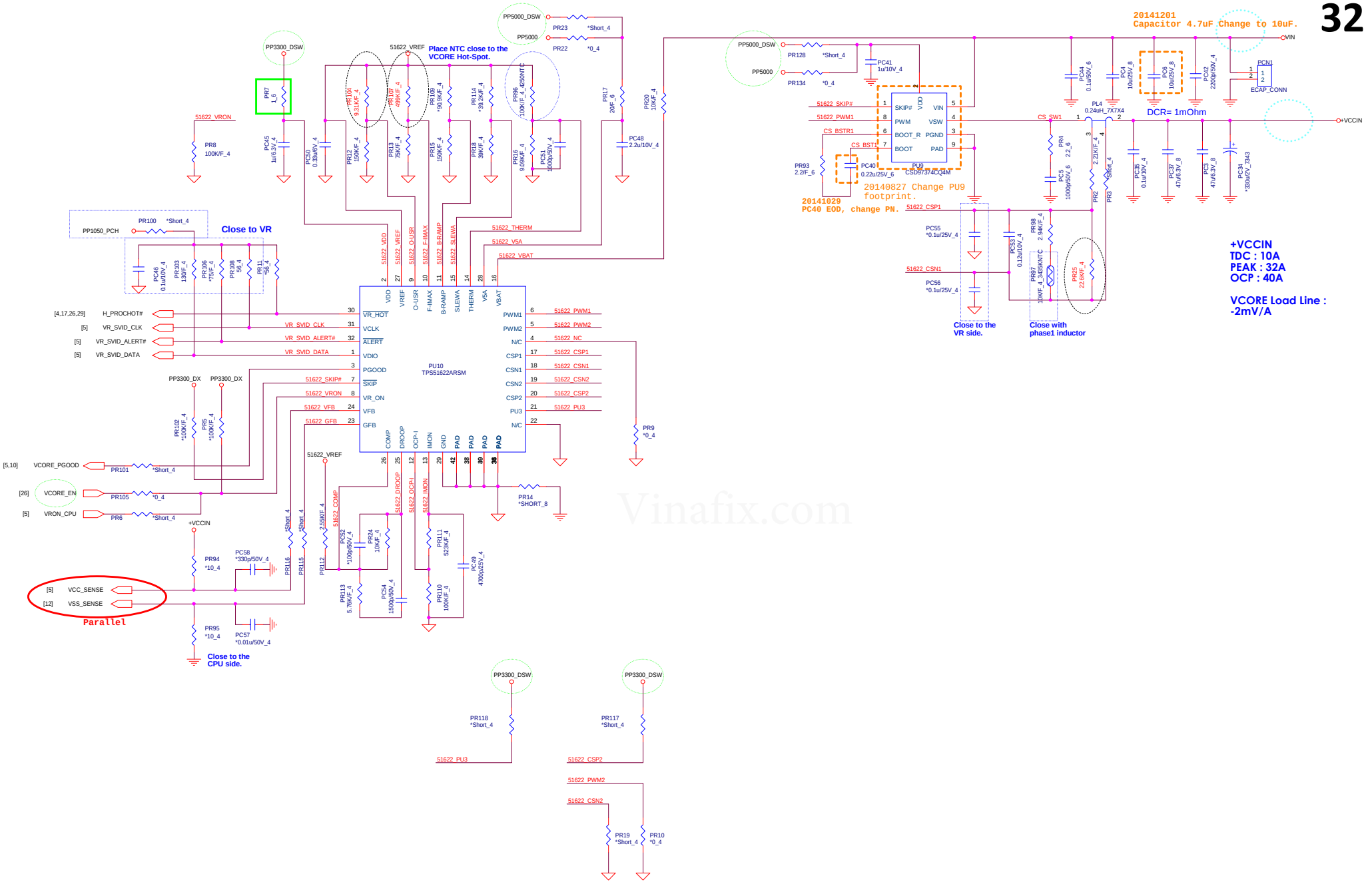
Size	Document Number	Rev
	DDR 1.35V(TPS51216)	A
Date: Thursday, December 04, 2014	Sheet 30 of 39	



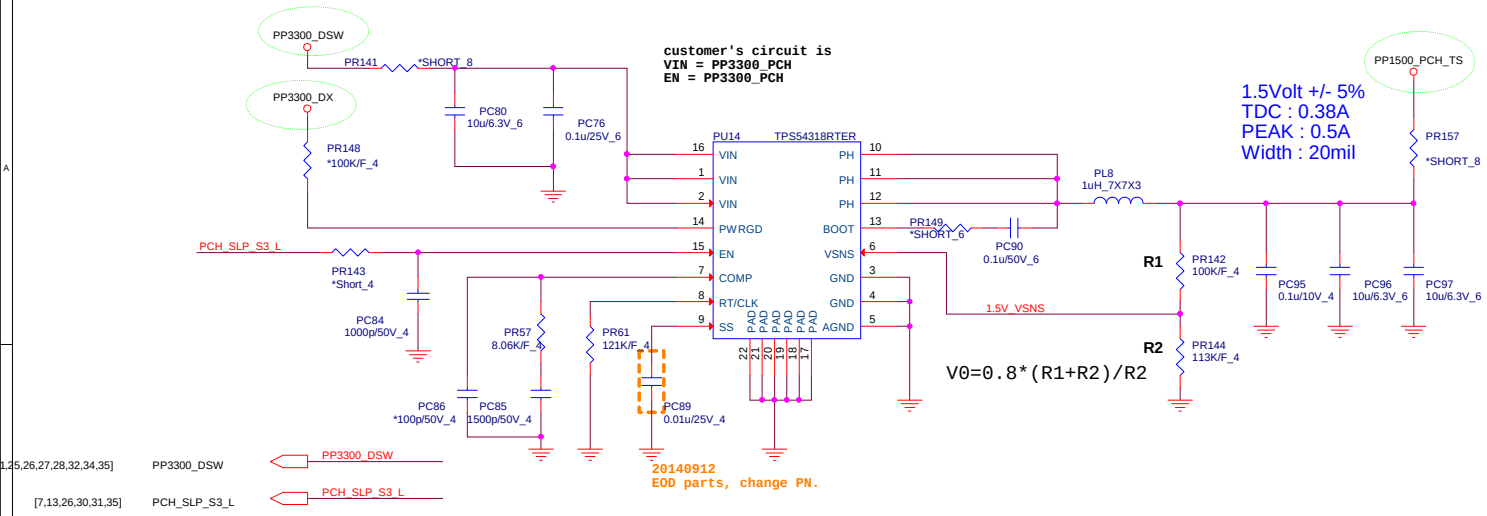
place at PQ37 area

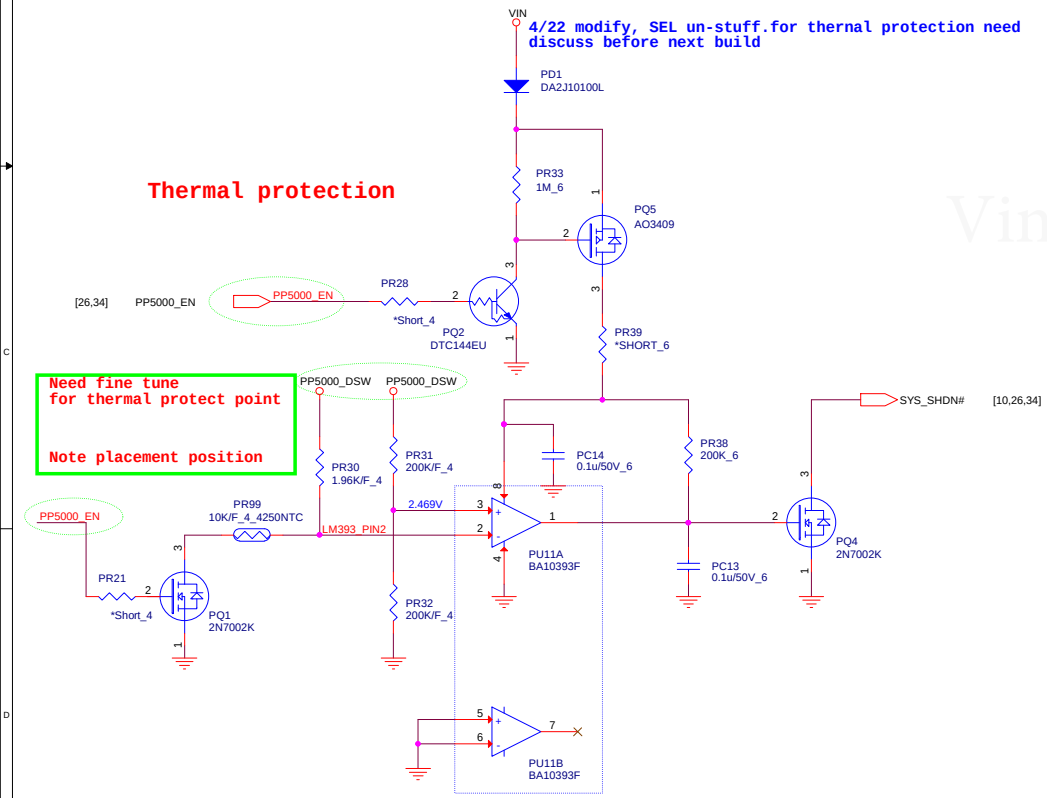


Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: +1.05V(TPS51211)	Rev: A
Date: Thursday, December 04, 2014	Sheet 31 of 39	



Quanta Computer Inc.	
PROJECT : ZHNB	
Size	Document Number: +VCCIN(TPS51622) — Rev A
Date: Thursday, December 04, 2014	Sheet 32 of 39





For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	+1.2V/+1.5V/+1.8V/Thermal protect	A
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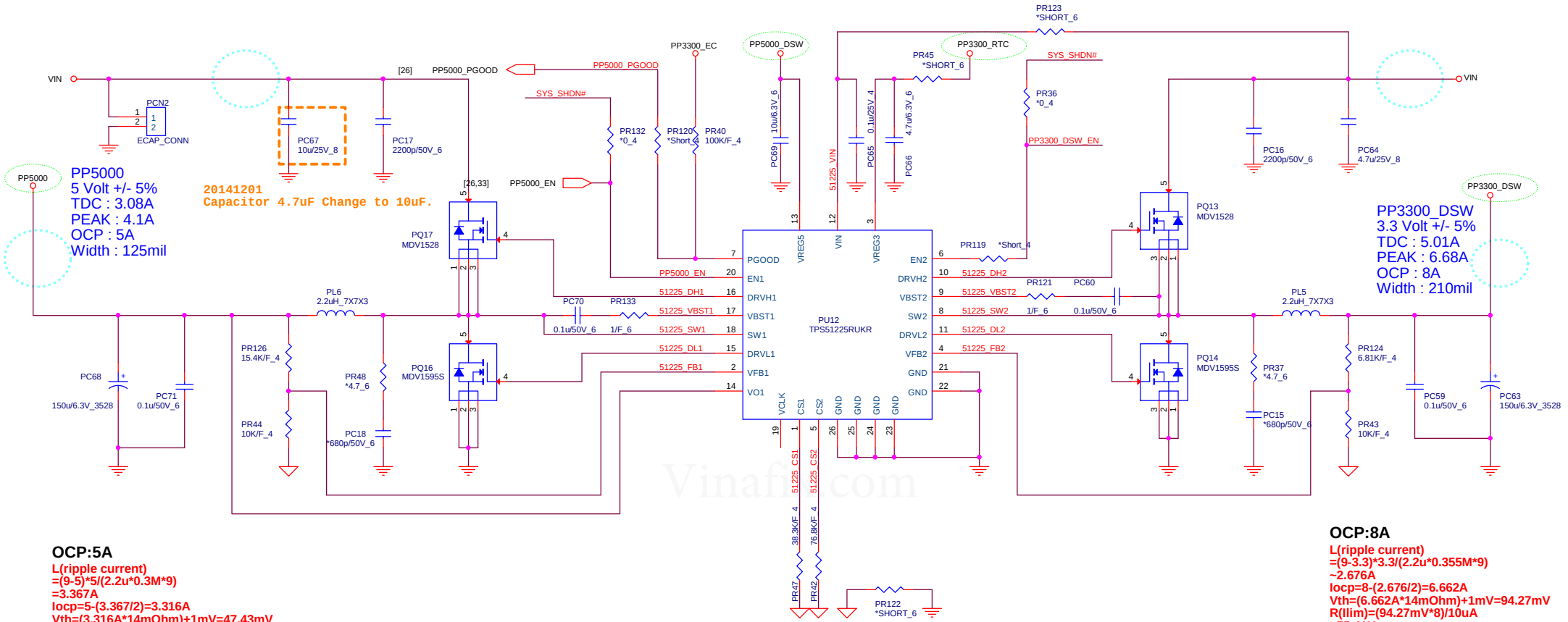
SYS_SHDN# → SYS_SHDN# [10,26,33]

PP3300_DSW_EN → PP3300_DSW_EN [26]

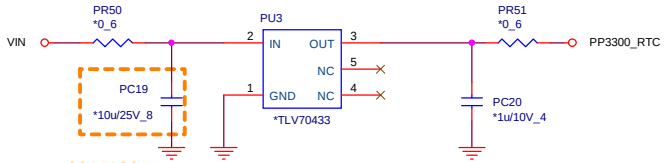


OCP:5A

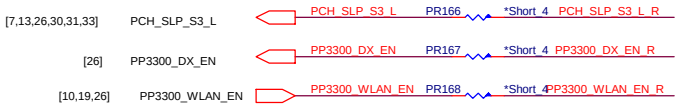
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=5-(3.367/2)=3.316A
Vth=(3.316A*14mOhm)+1mV=47.43mV
R(Ilim)=(47.43mV*8)/10uA
=37.94K

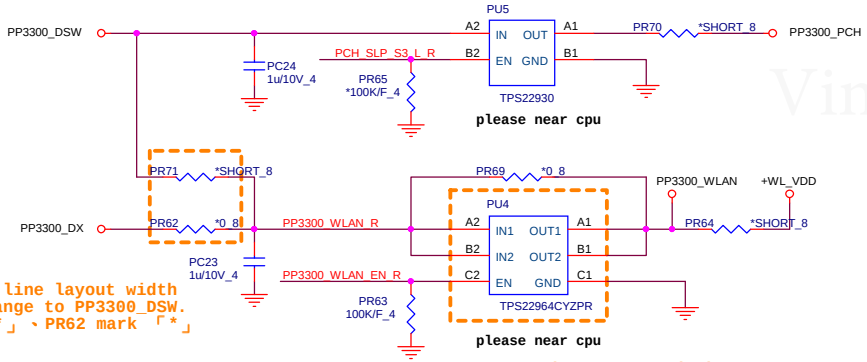
OCP:8A

L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=8-(2.676/2)=6.662A
Vth=(6.662A*14mOhm)+1mV=94.27mV
R(Ilim)=(94.27mV*8)/10uA
=75.41K



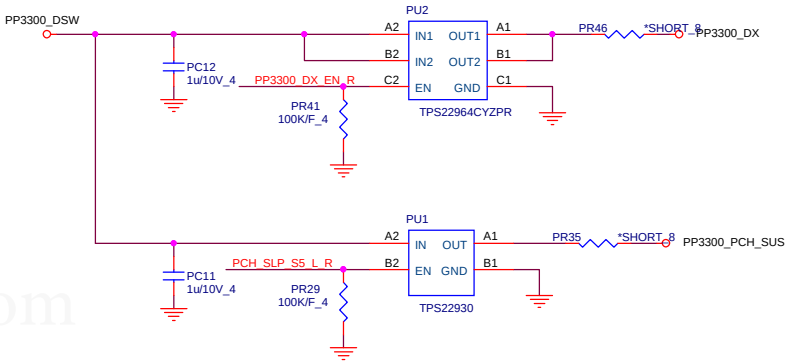
Quanta Computer Inc.		
PROJECT : ZHNB		
Size	Document Number: SYSTEM 5V/3V (TPS51225)	Rev: A
Date: Thursday, December 04, 2014	Sheet 34 of 39	



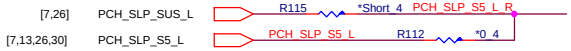


20140902 Power line layout width non-enough, change to PP3300_DSW.
PR71 cancel 「*」、PR62 mark 「*」

20140901 Change PU4 switch



4/24 modify



Quanta Computer Inc.
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Size	Document Number	Rev
	Load Switch	A
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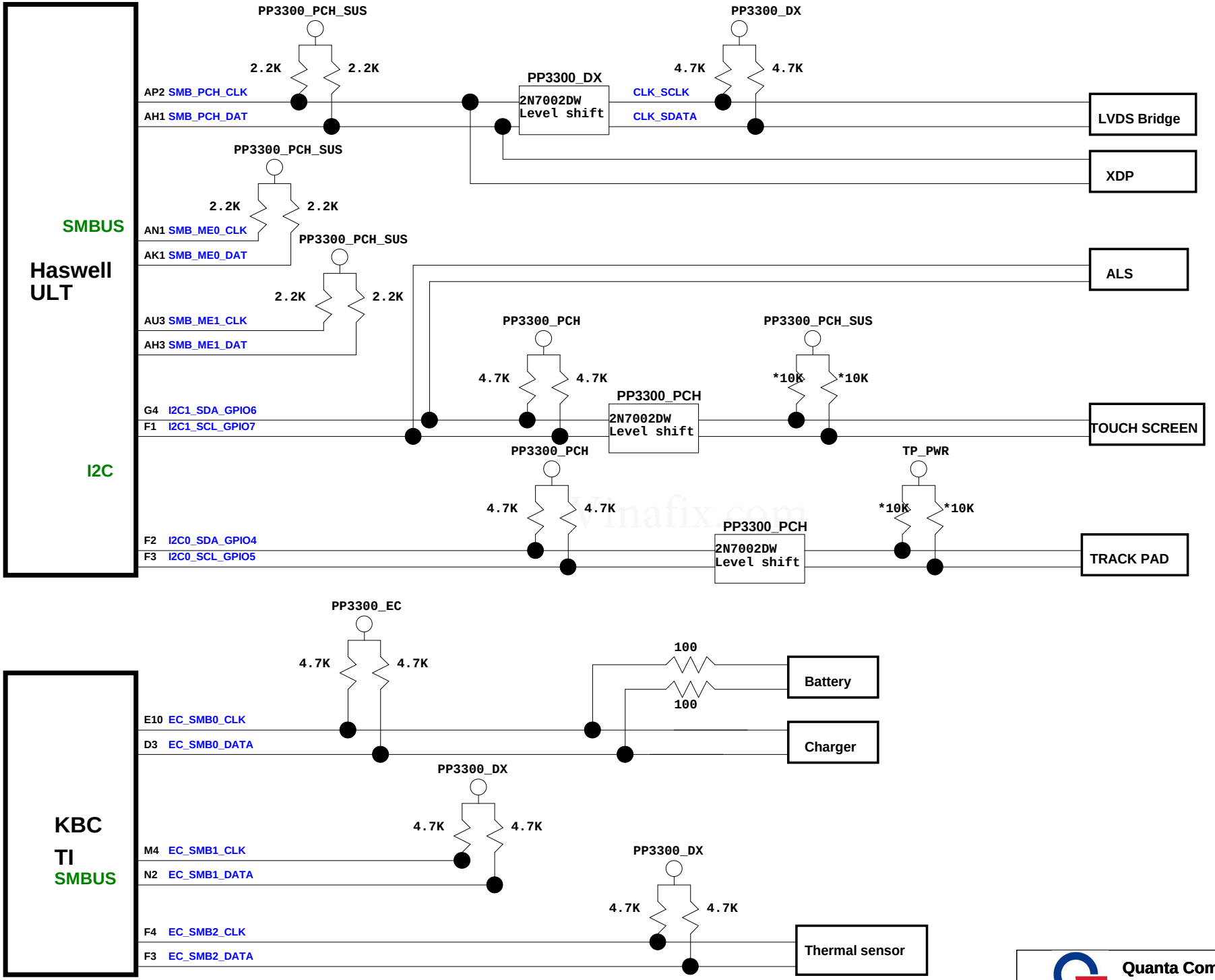
Battery Mode



Quanta Computer Inc.
PROJECT : ZHNB

Size	Document Number	Rev
	SMBUS_I2C	A

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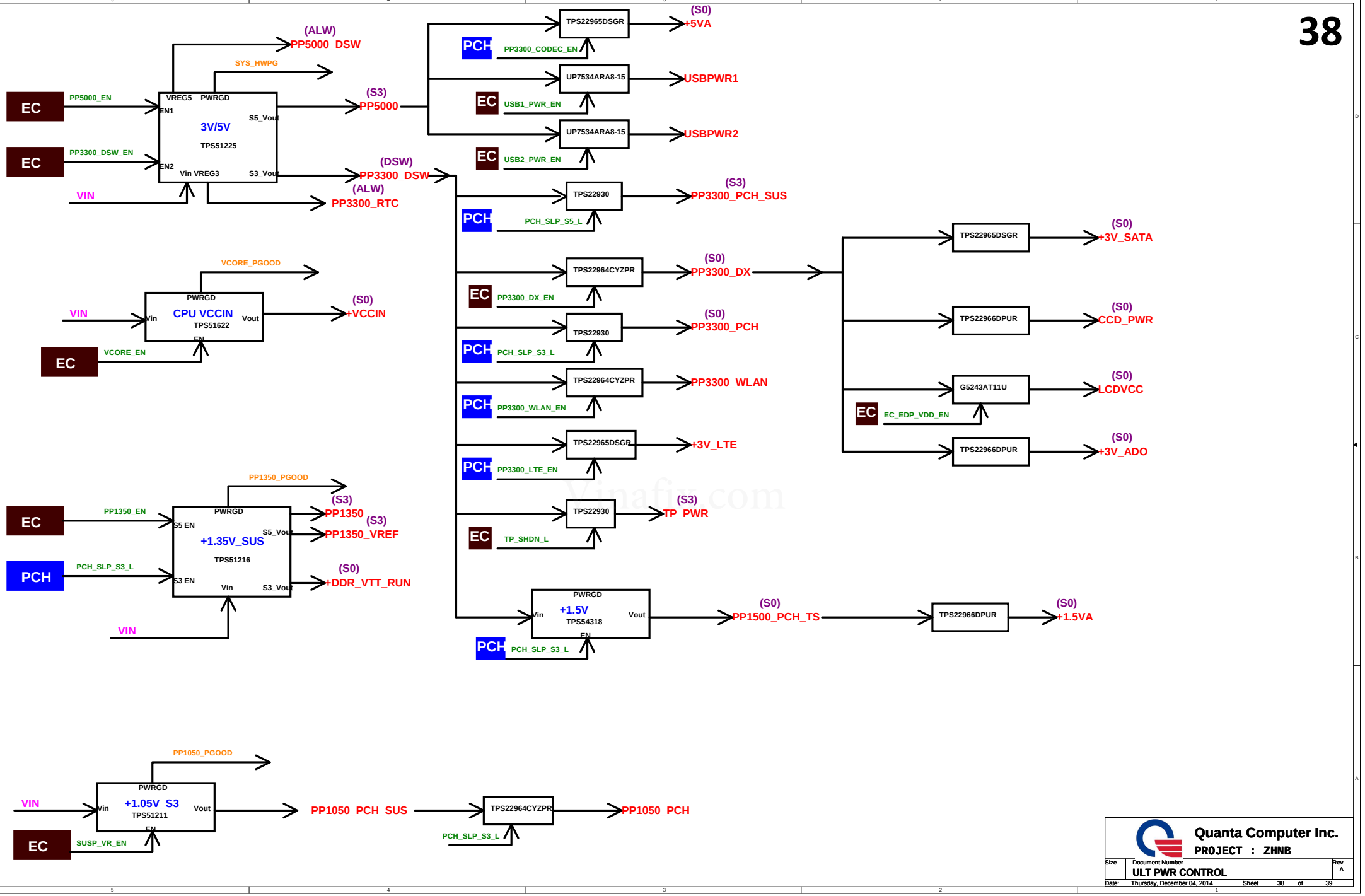

Quanta Computer Inc.
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Size	Document Number	Rev
	ULT PWR CONTROL	A

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Model	Version	CHANGE LIST
ZHNB	1A-1	2014/08/21 Page16: LCD conn. I2C1_SDA_GPIO6_CONN pin reserve a 15pF capacitor. 2014/08/21 Page16: Touch panel level shift Q13 FET change to PJT138K. 2014/08/22 Page19: Wifi U27 change to another onboard module 7260SDW. 2014/08/22 Page21: NGFF 3G / SIM mark 「*」.
	1A-2	2014/08/27 Page19: Change wifi onboard module 7260SDW footprint. 2014/08/27 Page19: Pin W_DISABLE# / W_DISABLE#2 add 100K resistance pulldown. 2014/08/27 Page16: Change LVDS conn. CN3 footprint. 2014/08/27 Page18: Change HDMI conn. CN5 footprint. 2014/08/27 Page21: Change NGFF 3G conn. CN8 footprint. 2014/08/27 Page25: Change touchpad board conn. CN10 footprint. 2014/08/27 Page32: Change VCORE PU9 footprint.
	1A-3	2014/09/1 Page34: Change LDO PU4 switch.
	1A-4	2014/09/2 Page35: LDO PR71 cancel 「*」、PR62 mark 「*」. 2014/09/2 Page19: Wifi 100K resistance R631/R632 mark 「*」
	1A-5	2014/09/9 Page29: Implant PR73 for battery enable. 2014/09/9 Page19: Change wifi onboard module 7260SDW footprint.
	1A-6	2014/09/12 Page16: C16 EOD, change PN. 2014/09/12 Page21: C379/C380/C381/C382 EOD, change PN. 2014/09/12 Page23: L4/L7 EOD, change PN. 2014/09/12 Page26: C208/C352/C360/L15 EOD, change PN. 2014/09/12 Page29: PC87/PJ1 EOD, change PN. 2014/09/12 Page30: PC100 EOD, change PN. 2014/09/12 Page31: PR83 EOD, change PN. 2014/09/12 Page33: PR89 EOD, change PN.
	1B-1	2014/09/24 Page26: USB3.0 U8 P1/P2 add C399/D34.
	1B-2	2014/09/25 Page28: Thermal MOSFET Q25/Resistance R585 mark 「*」un-stuff. OVERT# power PP3300_DX change to PP3300_EC.
	1B-3	2014/10/14 Page19: Change wifi onboard module 7260SDW PN.
	1B-4	2014/10/16 Page29: Change DC-in PN. (new module)
	1B-5	2014/10/21 Page13: Intel require modify ITP CN15 P9/P51 add PP1050_PCH_SUS, P50 PP1050_PGOOD change to VCCST_PWRGD.
	1C-1	2014/10/29 Page23: Codec pin27 add 100K resistance 2014/10/29 Page31: PC40 EOD, change PN.
	1C-2	2014/11/07 Page26: Change U5 EC PN.
	1C-3	2014/11/12 Page23: C193 change to 0.1uF. 2014/11/12 Page all: 0 ohm resistance change to short pad.
	1C-4	2014/11/18 Page23/Page26: change D27/D28 PN.
	1C-5	2014/11/19 Page25: U17 change part NO. same as 0C7, add MOSFET Q33. 2014/11/19 Page27: Remove HOLE24 BATT_EN# pin3, because enable control by U17. 2014/11/19 Page27: Lid SW change to un-stuff, because enable by U17. 2014/11/19 Page29: PR73 change to un-stuff, because enable control by U17.
	1C-6	2014/11/20 Page26 Change EC_BRD_ID, ID2 change to High, ID3 change to Low, because EC change code.
	1C-7	2014/11/25 Page16 Change TPS/R361/Q13 to un-stuff, because no touch panel.
	1C-8	2014/11/26 CH4102K1B03 EOS parts, change to CH4103K1B08
	1D-1	2014/12/01 Page22 Change TPM power. 2014/12/01 Page26 Change EC new PN. 2014/12/01 Page27 Stuff L12/L18/L19, remove R371/R372/R549/R550/R551/R552. 2014/12/01 Page29 Change DC-in footprint. 2014/12/01 PC1/PC19/PC31/PC6/P67/PC75 4.7uF change to 10uF.
	2A	
	3A	

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

Quanta Computer Inc.
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Size | Document Number: Change list | Rev A
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