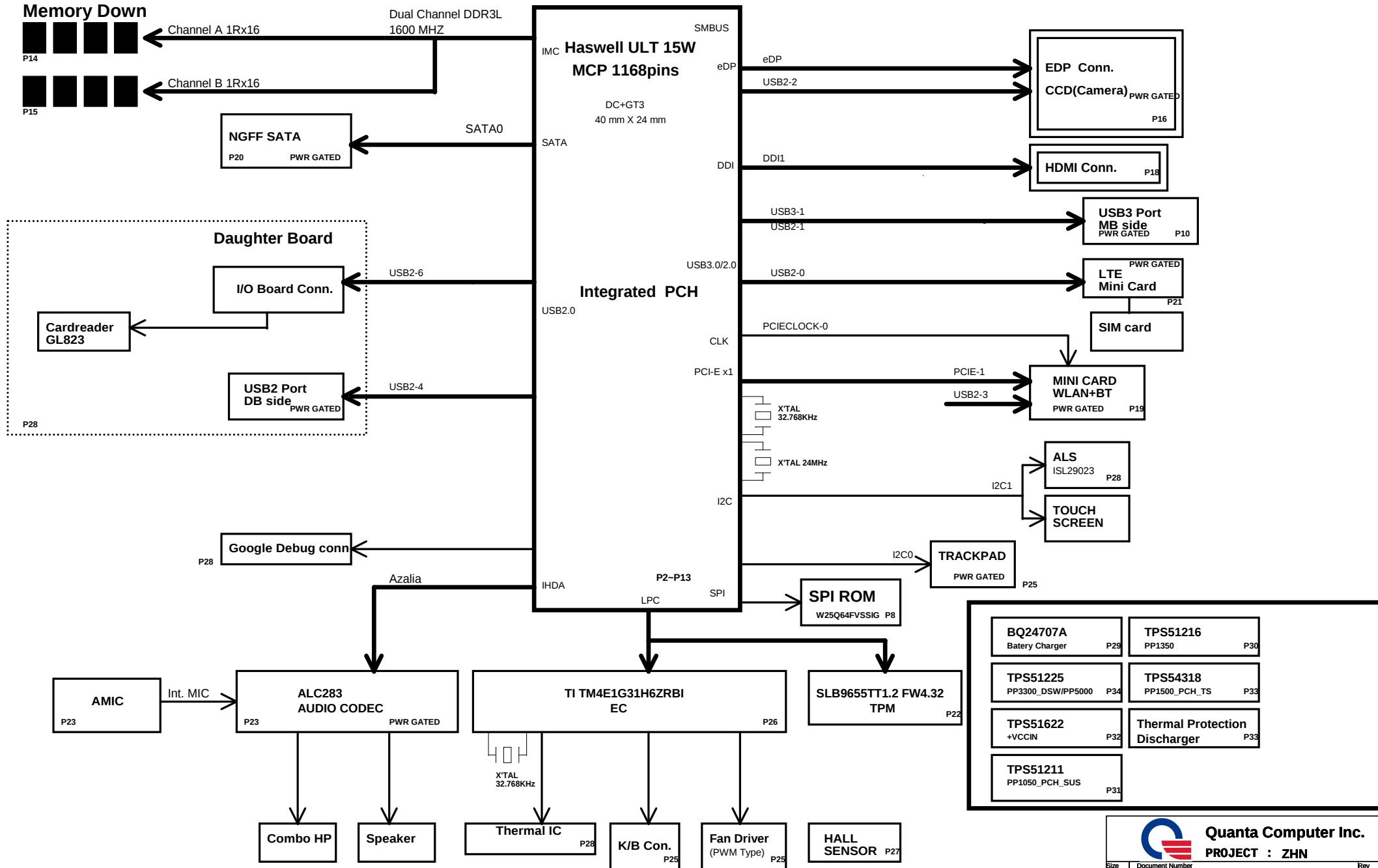
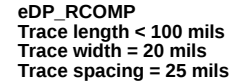


ZHN SHB ULT SYSTEM BLOCK DIAGRAM

01



02



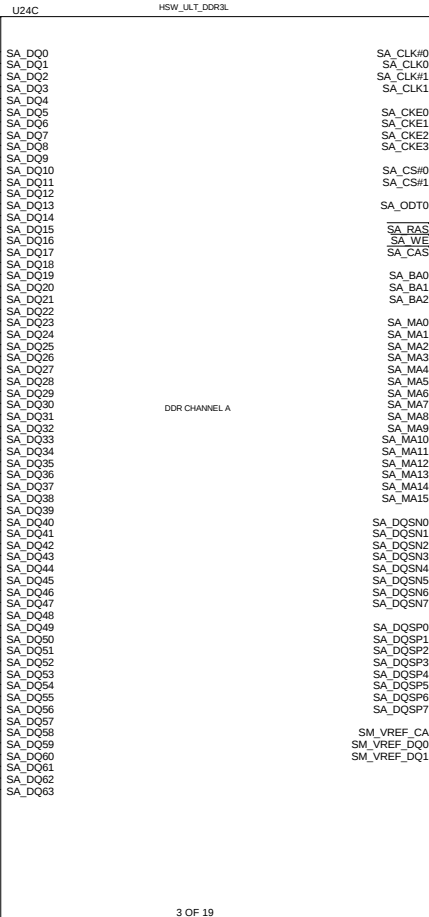
PROJECT : ZHN

Haswell 1/5 (DDI/eDP)

Sheet 2 of 39

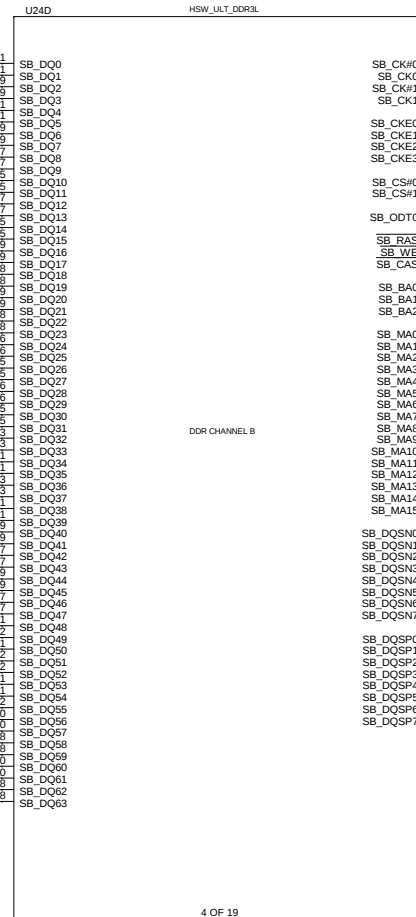
Rev	3B
-----	----

Haswell ULT (DDR3L)



3 OF 19

Haswell Processor (DDR3L)



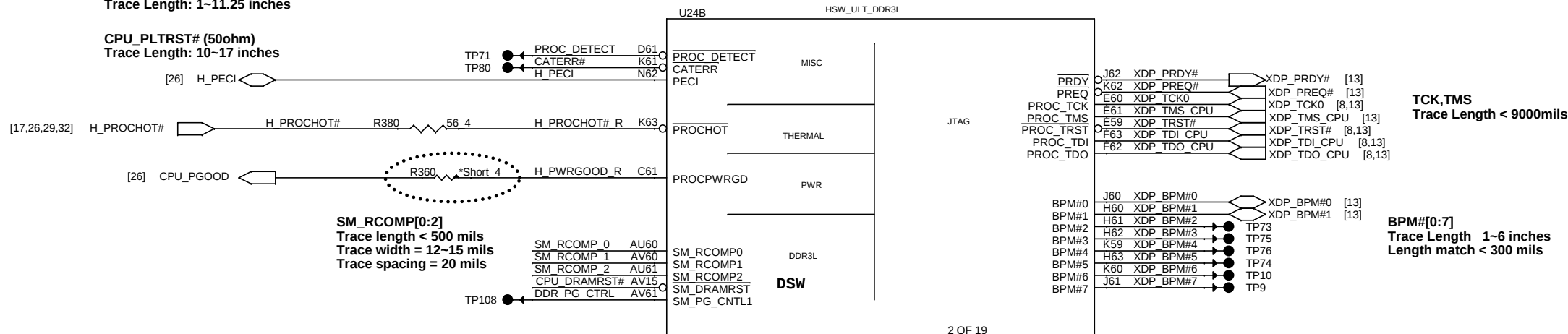
4 OF 19

Haswell ULT (SIDE BAND)

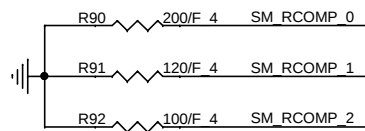
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 inches

H_PWRGOOD (50ohm)
Trace Length: 1~11.25 inches

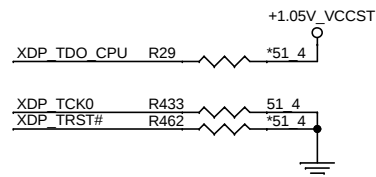
CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches



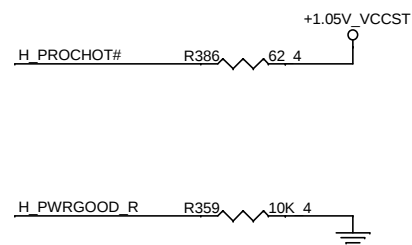
DRAM COMP



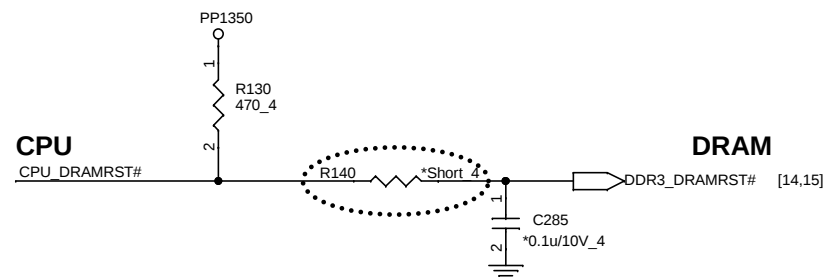
XDP PU/PD



PU/PD of CPU



DRAMRST



Quanta Computer Inc.

PROJECT : ZHN

Size	Document Number	Rev
	Haswell 3/5 (SideBand)	3B
Date:	Monday, August 26, 2013	Sheet 4 of 39

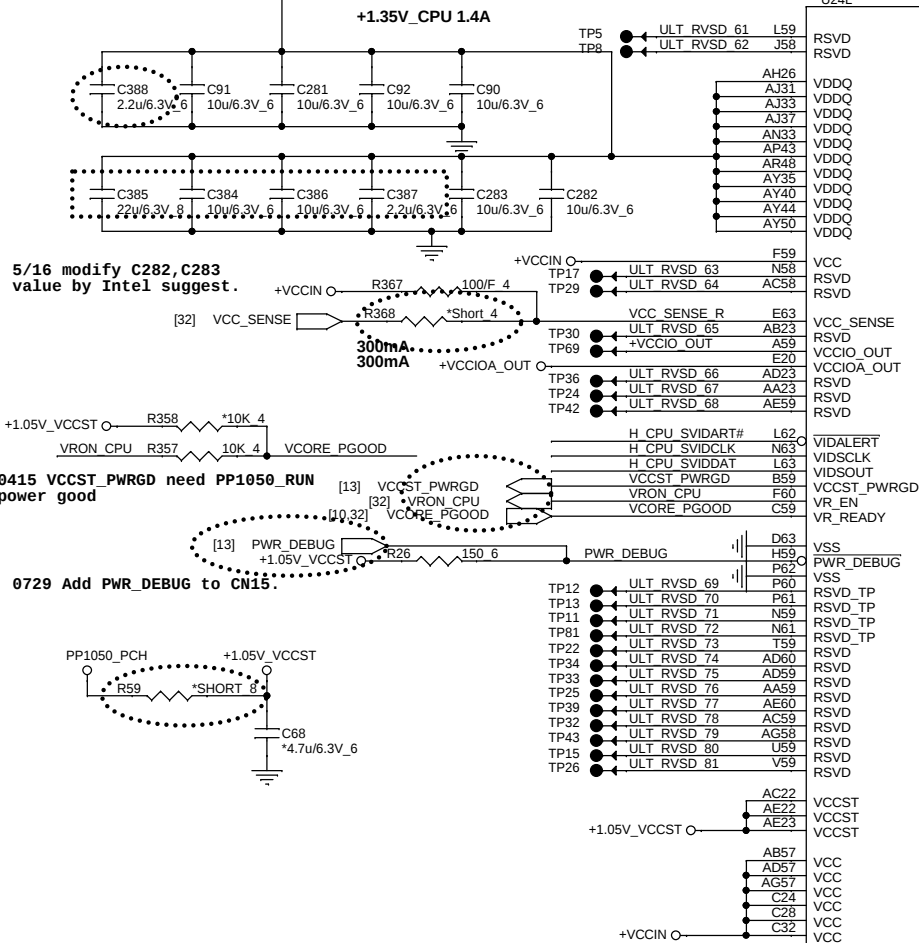
Date: Monday, August 26, 2013 Sheet 4 of 39

Haswell ULT (POWER)

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

6/21 Add C384-C388 by Intel DDR.



U24L HSW_ULT_DDR3L

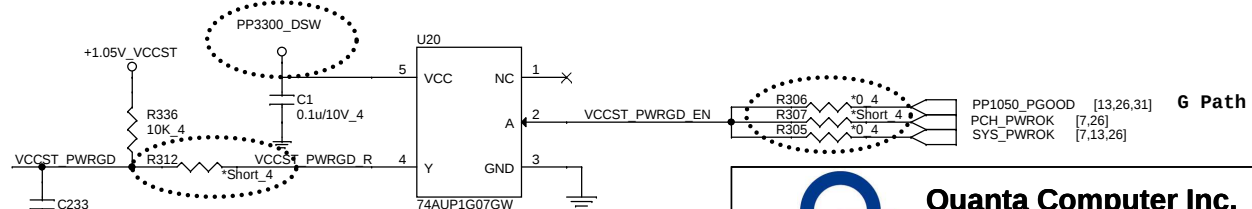
HSW ULT POWER

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VCC Output Decoupling Recommendations

470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

VCCST PWRGD

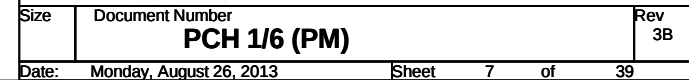




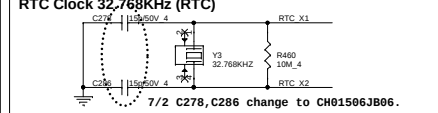
Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	Haswell 5/5 (CFG/GND)	3B
Date:	Monday, August 26, 2013	Sheet 6 of 39

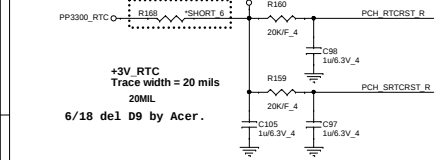
07



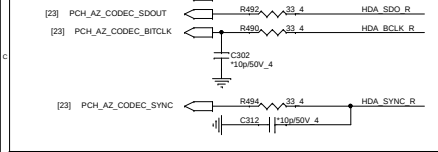
RTC Clock 32.768KHz (RTC)



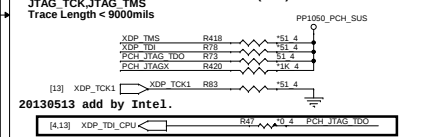
RTC Circuitry (RTC)



HDA



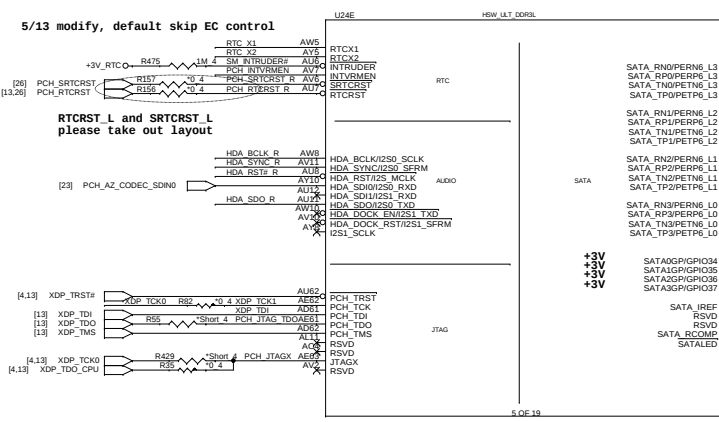
PCH JTAG



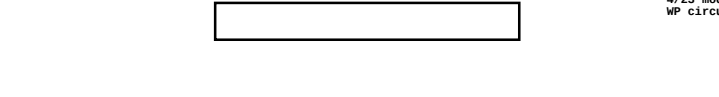
ULT Strapping Table

Pin Name	Strap description	Sampled	Configuration
GPIOB1(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (IPD 20K) 1 = can't program ME
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1 = Should be always pull-up
GPIO66	Top-Block Swap override		0 = Default disable (IPD 20K) 1 = Enable TBS function
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality (IPD 20K) 1 = Default enable with confidentiality
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable
DSWVREN	Deep Sx well on the VR enable		1 = Should be always pull-up

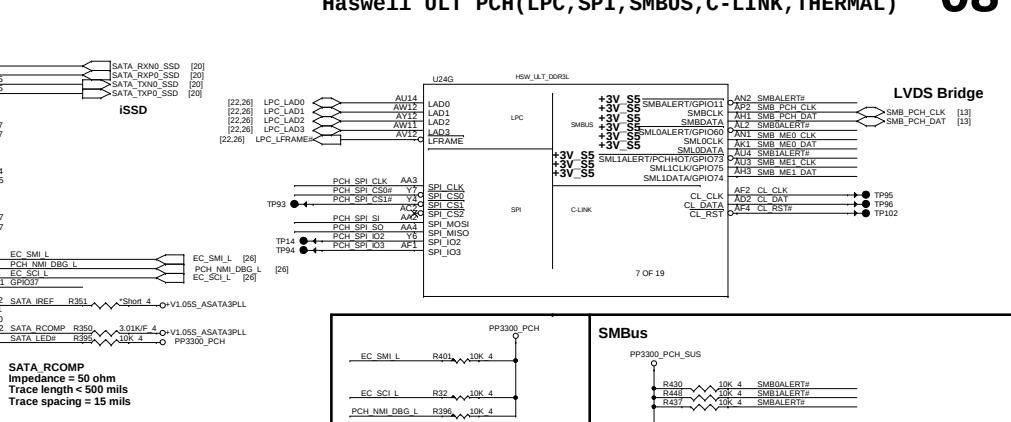
Haswell ULT PCH (RTC/HDA/SATA/SPI)



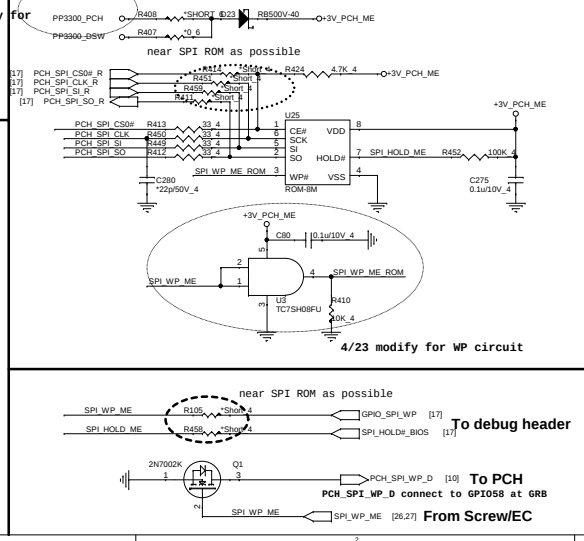
6/18 del RTC battery circuit by Acer.



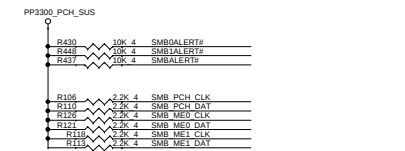
Haswell ULT PCH(LPC, SPI, SMBUS, C-LINK, THERMAL)



PCH dual I/O SPI ROM



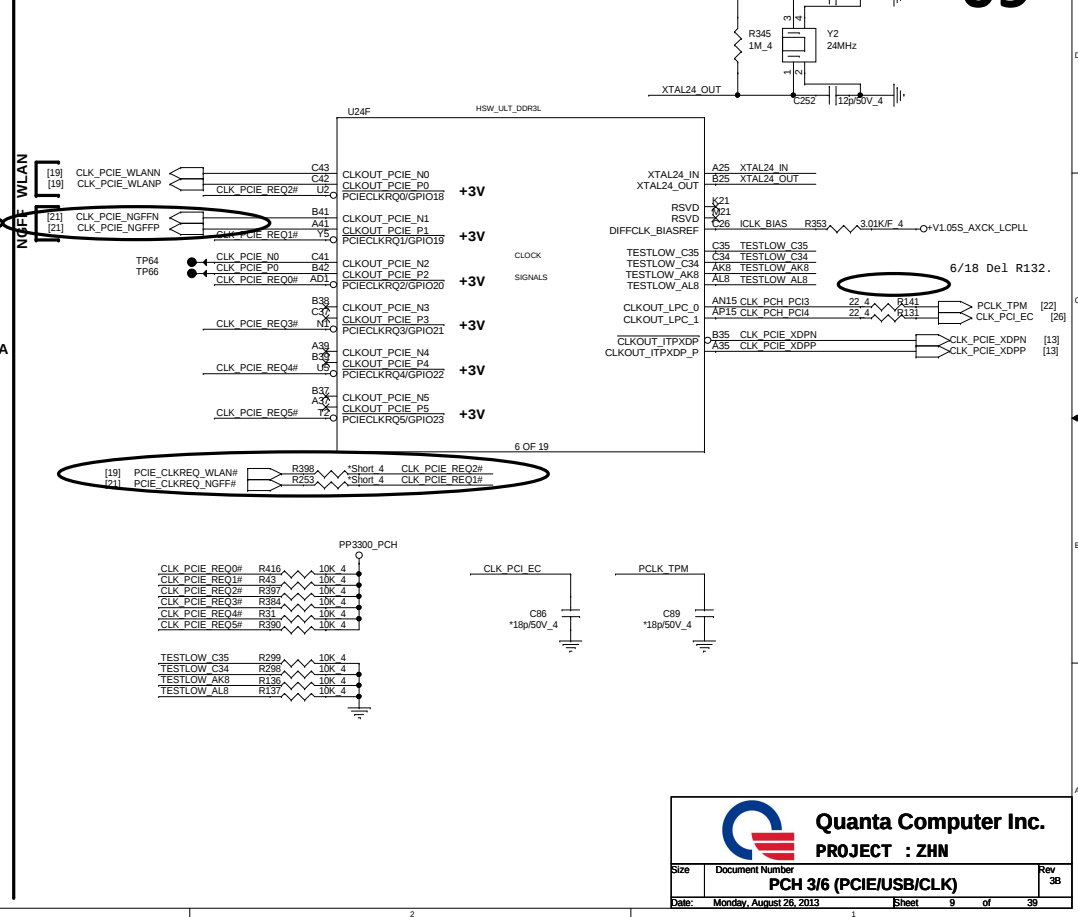
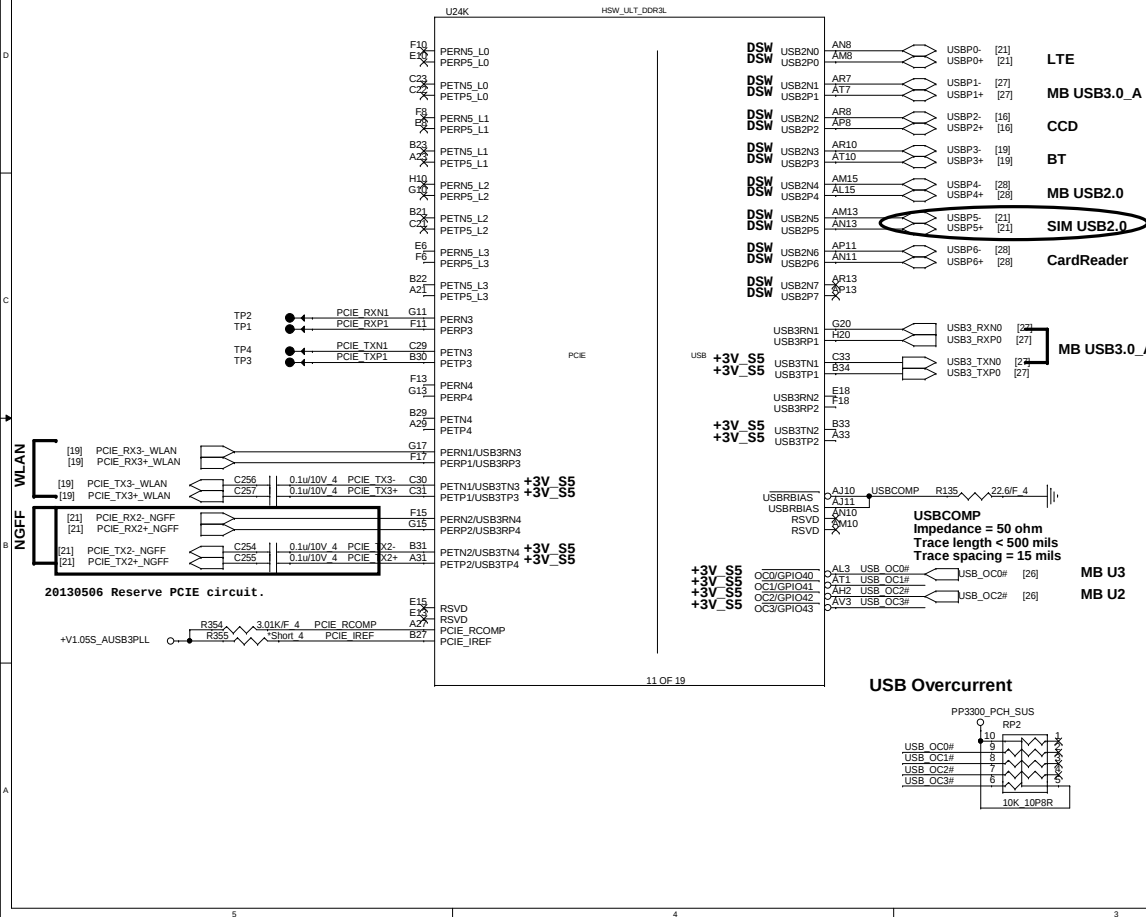
SMBus



Haswell ULT PCH (PCIE,USB3.0,USB2.0)

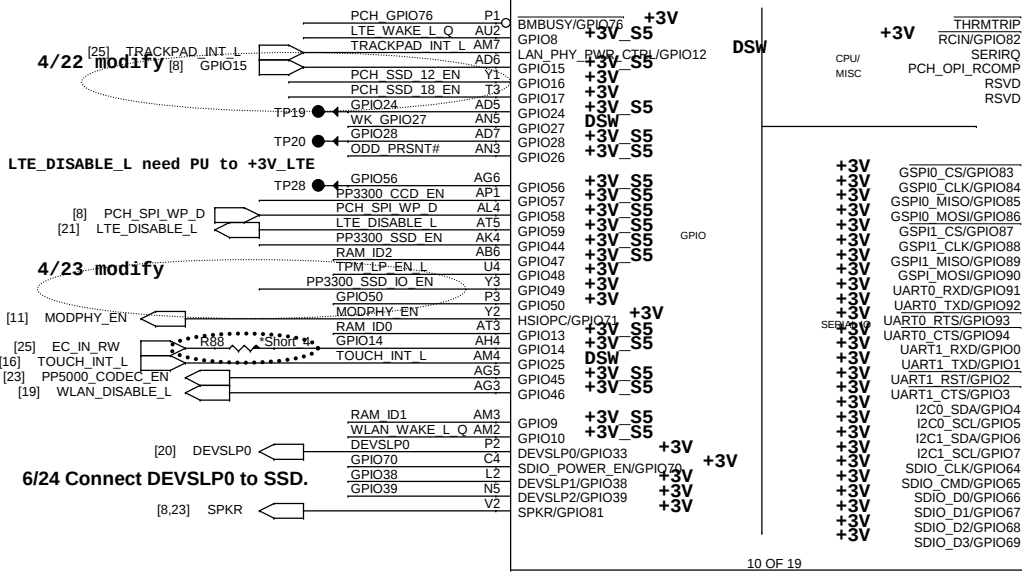
Haswell ULT PCH (CLOCK)

09



Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

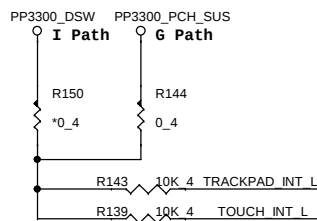
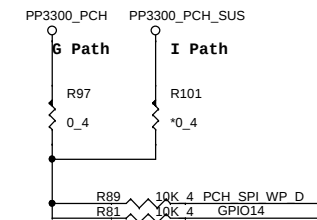
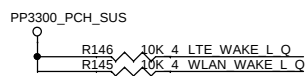
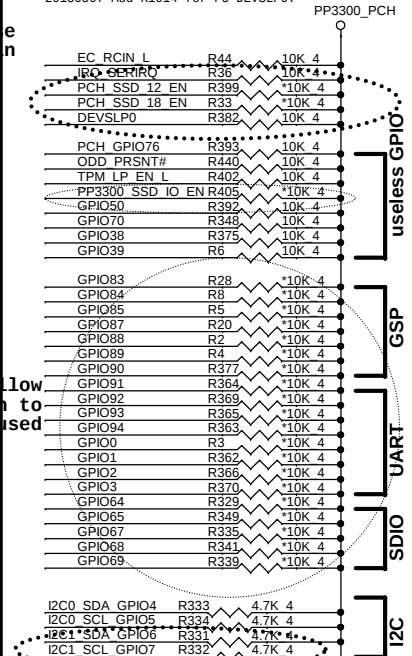
U24J HSW_ULT_DDR3L



PCH GPIO PU/PD

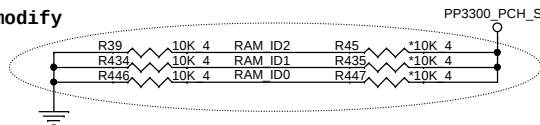
10

20130507 Add R1014 for PU DEVSLP0.

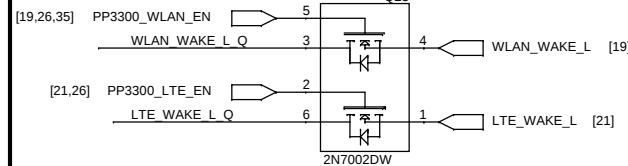


RAM ID

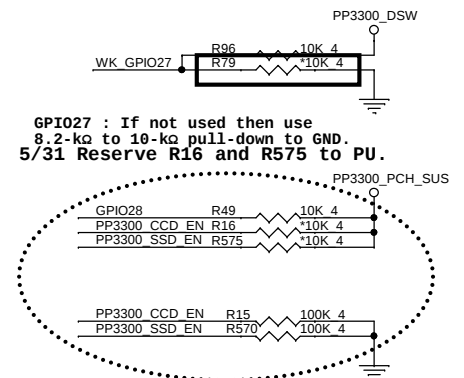
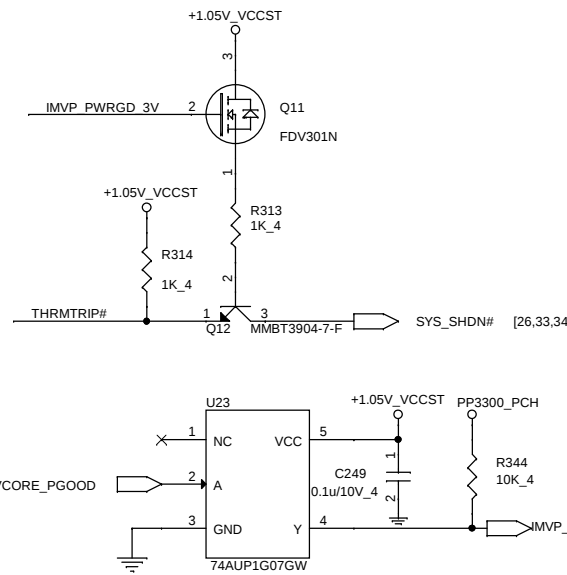
4/22 modify



Vender	RAM_ID			Q PN	Mfr. PN	Freq.
	ID2	ID1	ID0			
Micron(4G)	0	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHZ
Hynix(4G)	0	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHZ
Elpida(4G)	0	1	0	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHZ
Micron(2G)	1	0	0	AKD5JGSTL10	MT41K256M16HA-125:E	1600MHZ
Hynix(2G)	1	0	1	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHZ
Elpida(2G)	1	1	0	AKD5JGST407	EDJ4216EFBG-GNL-F	1600MHZ



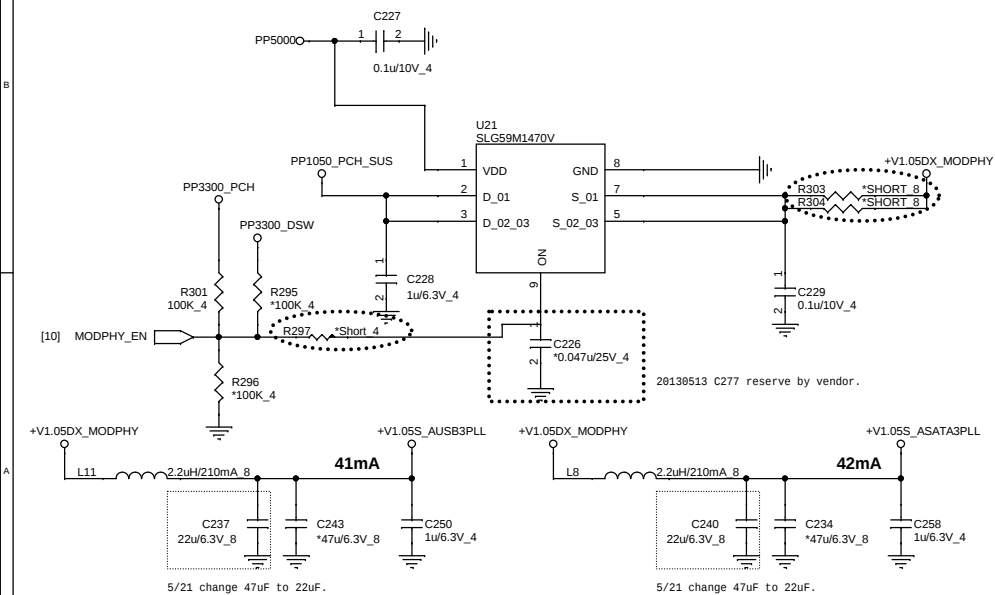
CPU thermal trip



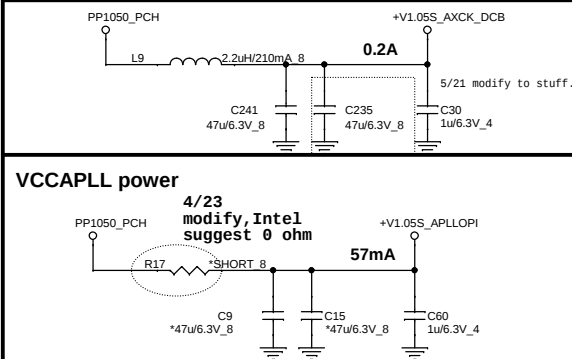
Haswell ULT PCH (Power)

0412 MOW-WW15 a 0.47uF cap between VccDSW3_3 and DcpSusByp is required if the 1.9A inrush current requirement cannot meet

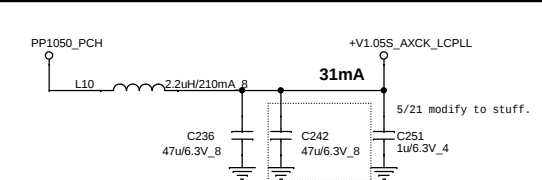
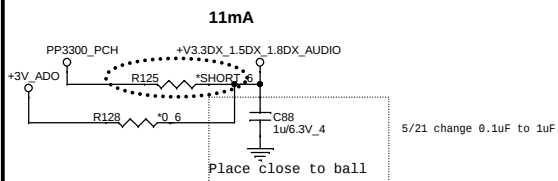
PCH VCCHSIO Power



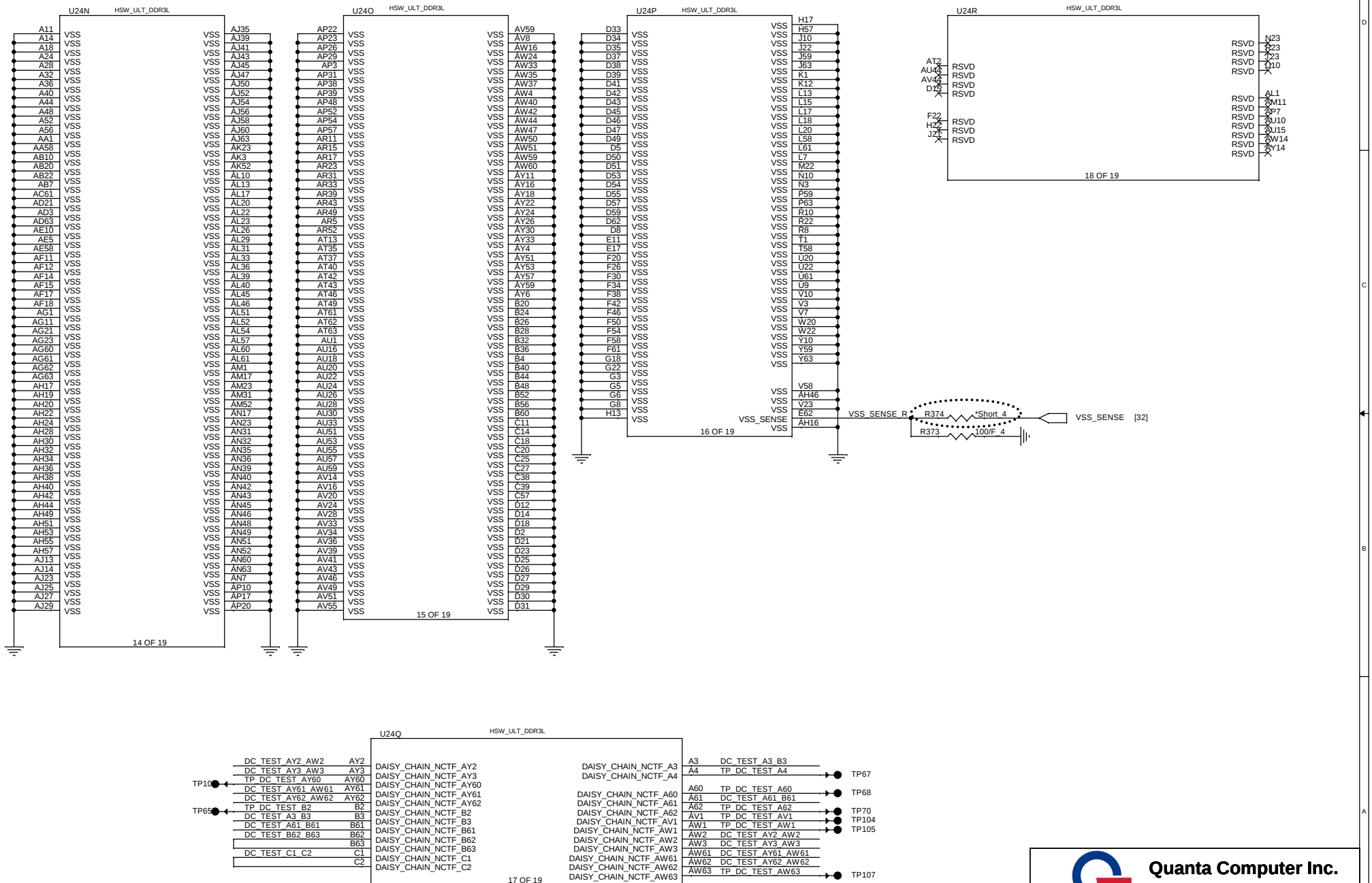
VCCAPLL power



PCH HDA Power	
0	0.000000
1	0.000000
2	0.000000
3	0.000000
4	0.000000
5	0.000000
6	0.000000
7	0.000000
8	0.000000
9	0.000000
10	0.000000
11	0.000000
12	0.000000
13	0.000000
14	0.000000
15	0.000000
16	0.000000
17	0.000000
18	0.000000
19	0.000000
20	0.000000
21	0.000000
22	0.000000
23	0.000000
24	0.000000
25	0.000000
26	0.000000
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30	0.000000
31	0.000000
32	0.000000
33	0.000000
34	0.000000
35	0.000000
36	0.000000
37	0.000000
38	0.000000
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85	0.000000
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87	0.000000
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95	0.000000
96	0.000000
97	0.000000
98	0.000000
99	0.000000

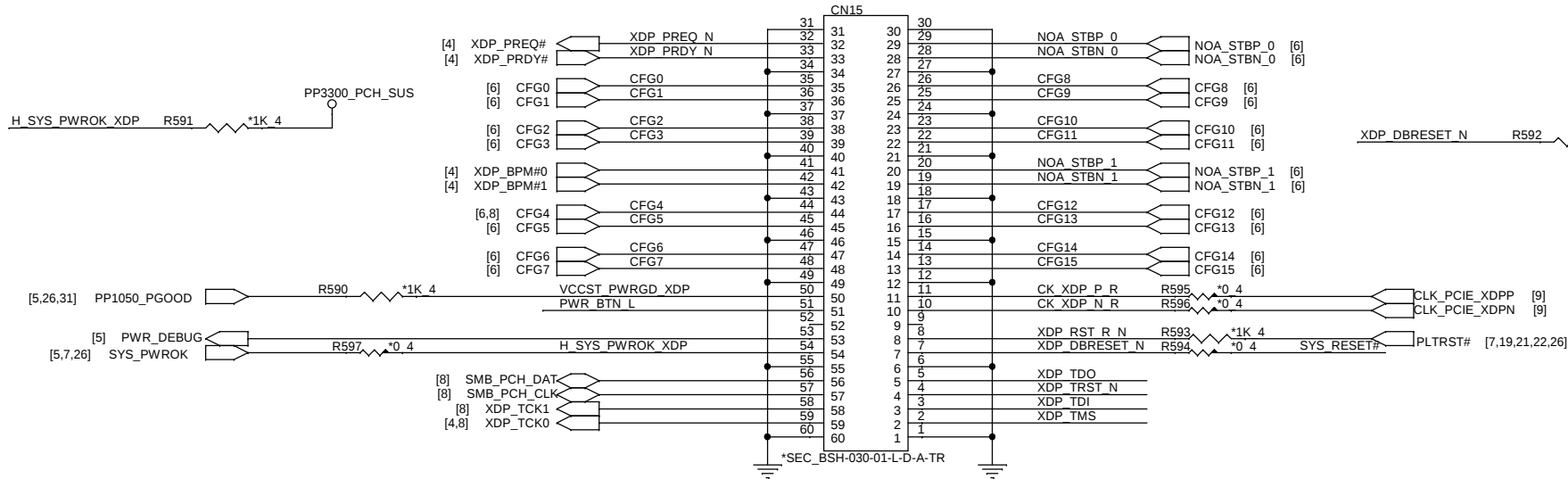


Haswell ULT (GND)

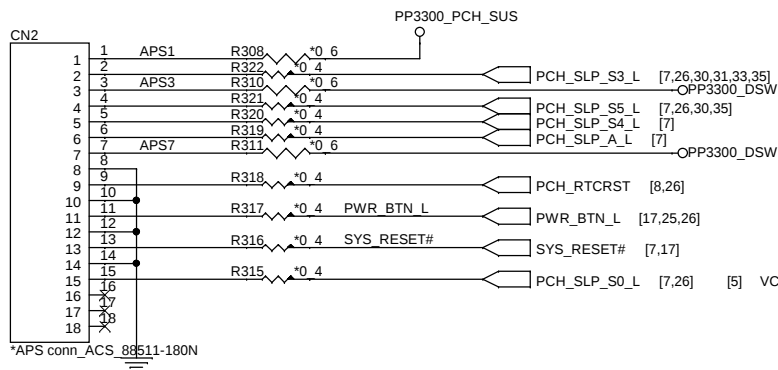


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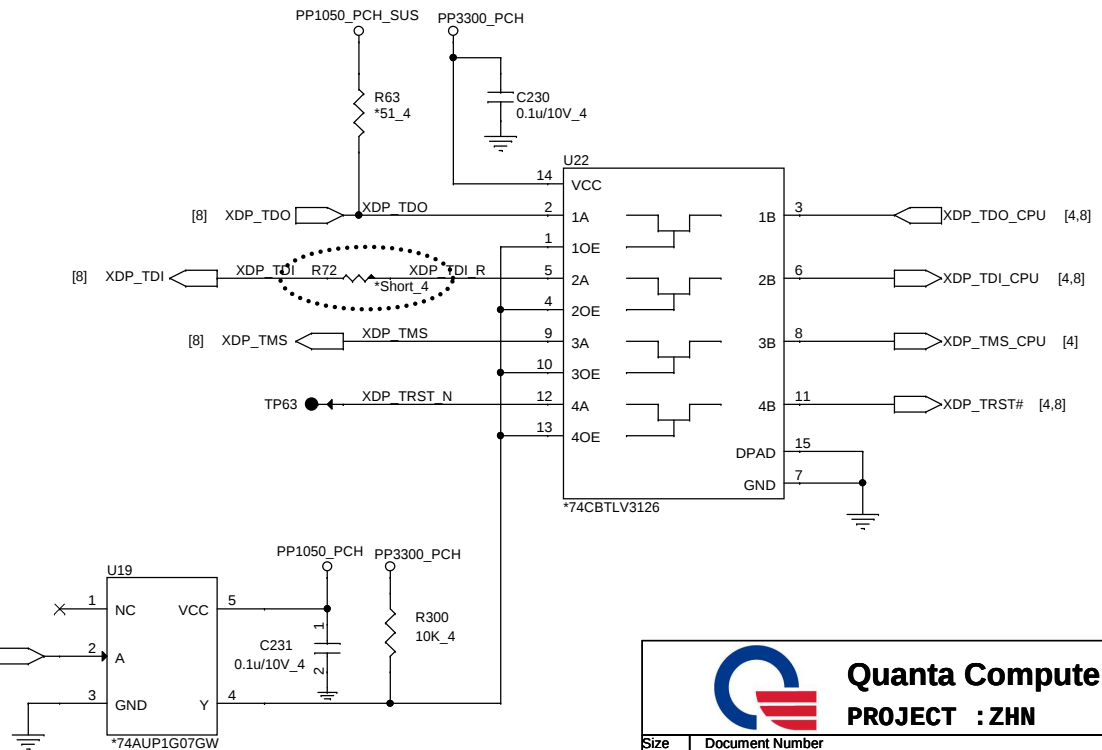
Size	Document Number	Rev
	PCH 6/6 (GND)	38
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APS



*APS conn_ACS 88511-180N



<DDR>

BYTE2_16-23

BYTE3_24-31

BYTE7_56-63

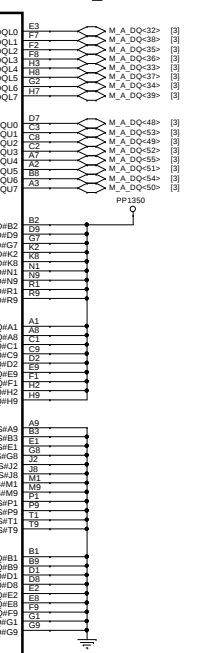
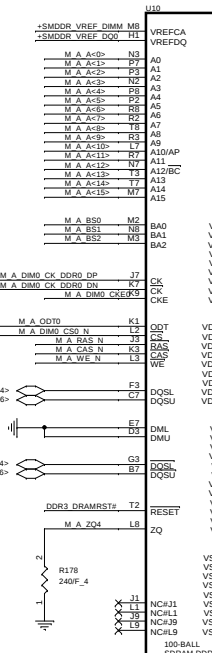
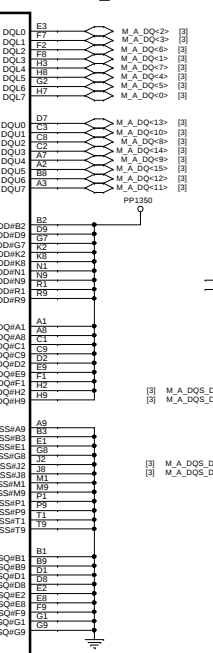
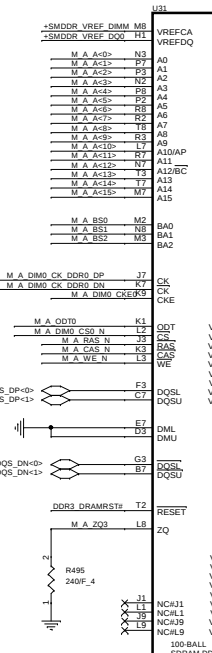
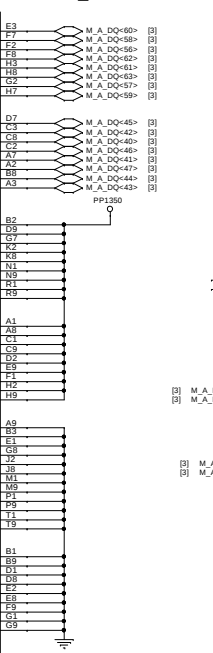
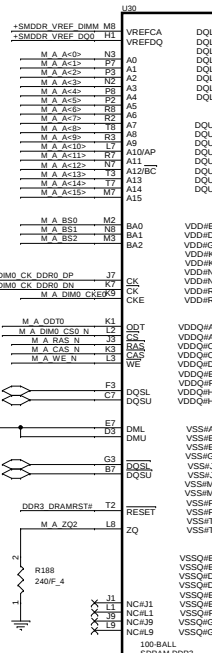
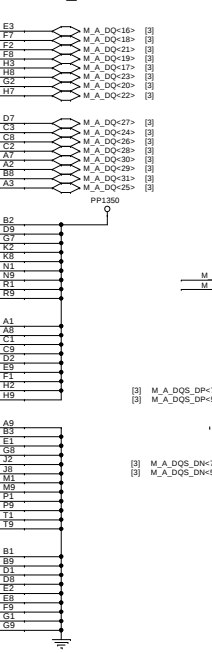
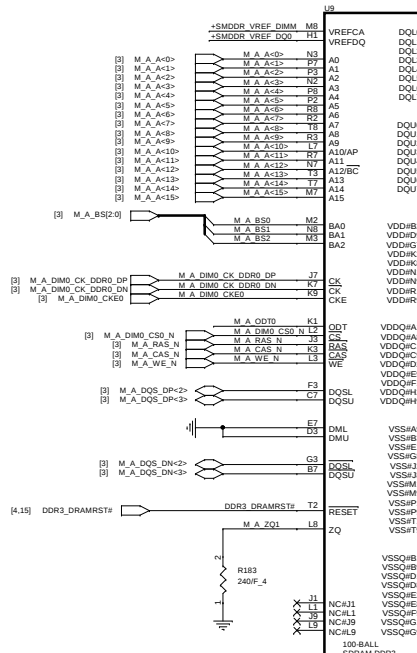
BYTE5_40-47

BYTE0_0-7

BYTE1_8-15

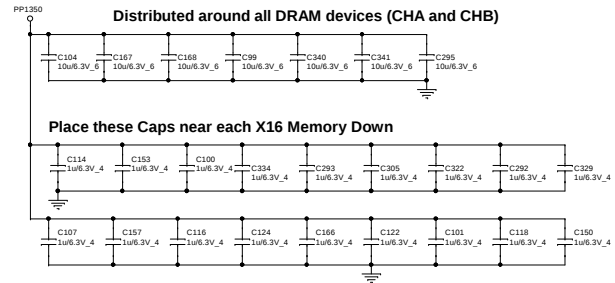
BYTE4_32-3

BYTE6_48-55



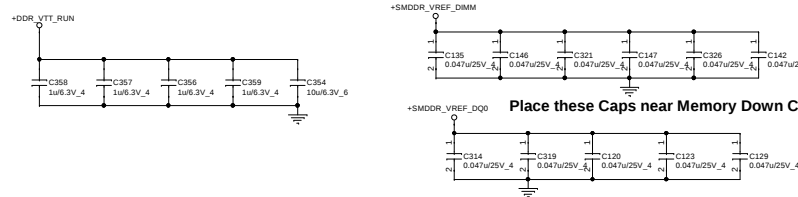
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

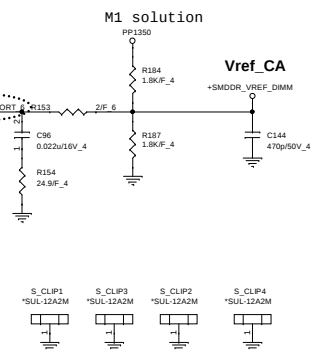


Distributed around all DRAM devices (CHA and CHB

Place these Caps near each X16 Memory Down



Place these Caps near Memory Down CA & DO pin



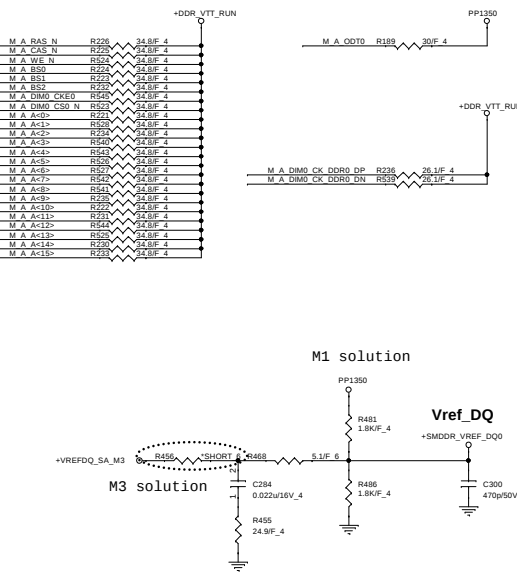
M1 solution

Vref CA

M3 solution

M1 solution

Vref_1



M3 solution

<DDR>

BYTE1_8-15

BYTE2_16-23

BYTE4_40-47

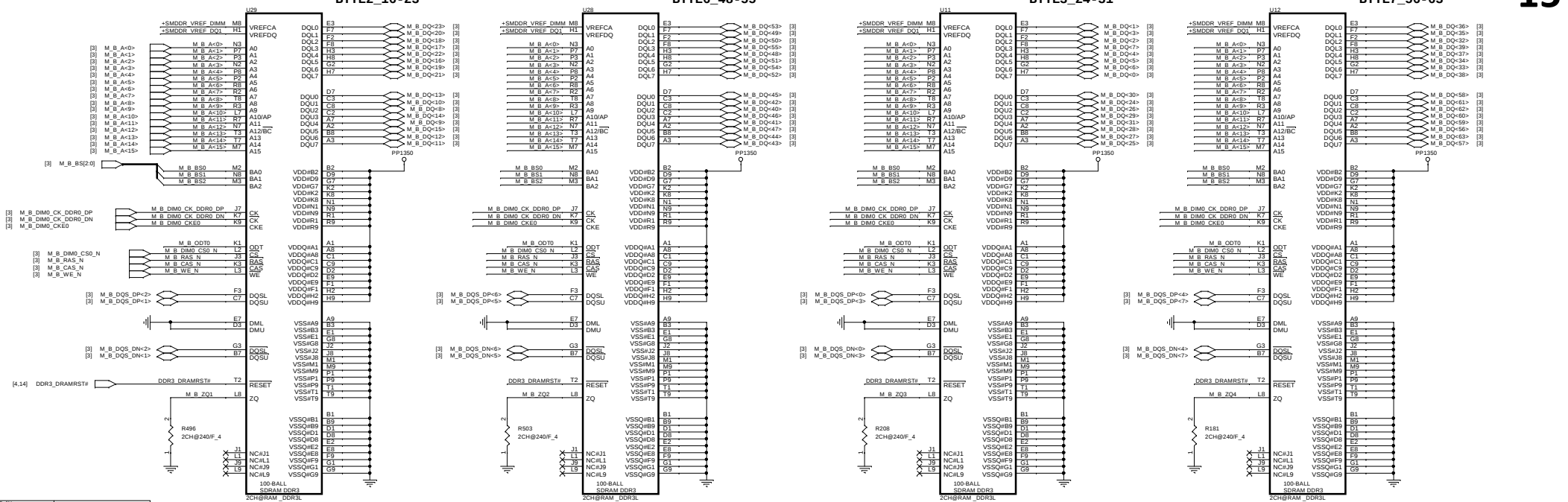
BYTE6_48-55

BYTE0_0-7

BYTE3_24-31

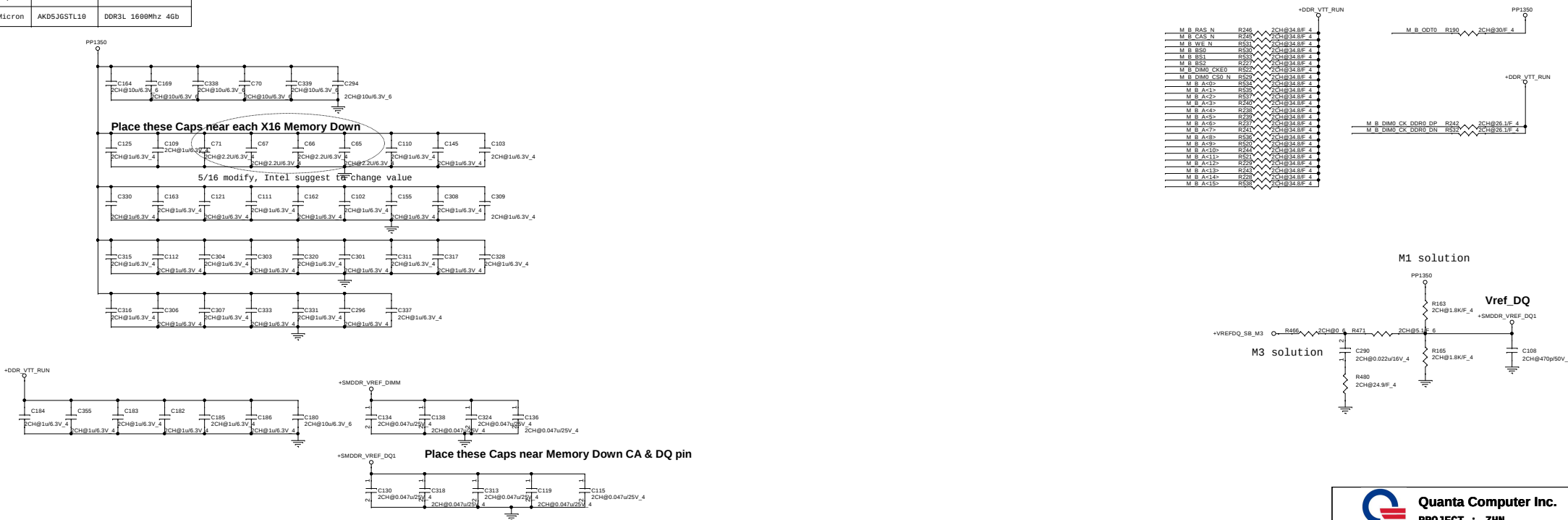
BYTE7_32-39

BYTE7_56-63



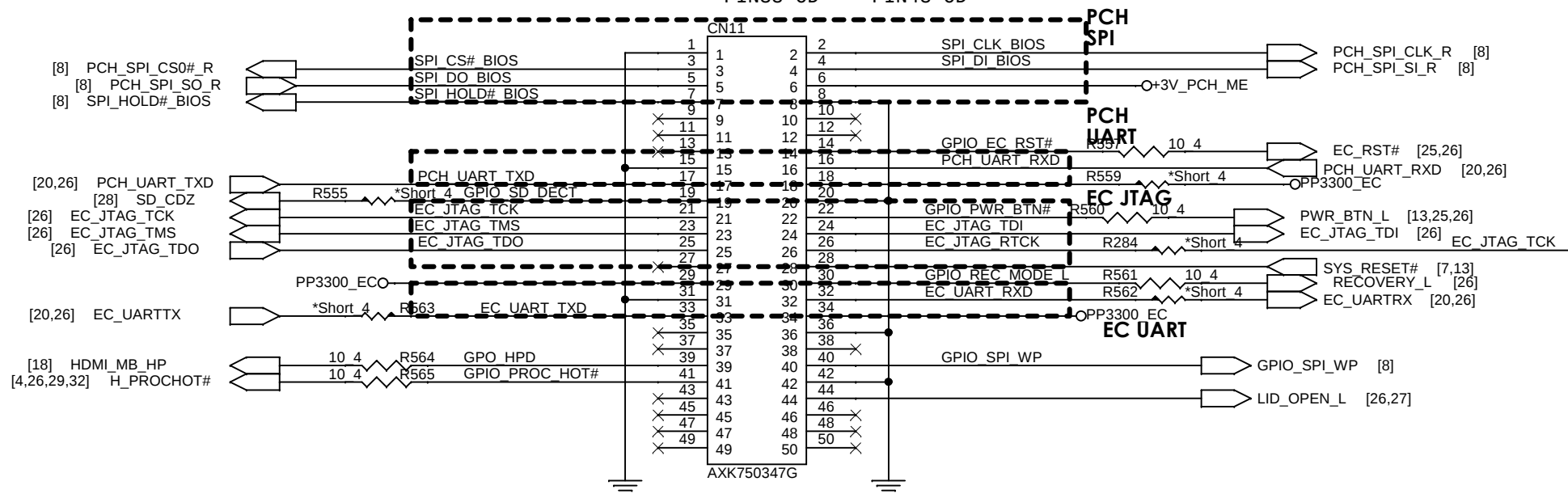
Vendor	P/N
Hynix	AKD5J6ETW04
Elipida	AKD5J6ST407
Micron	AKD5J6STL10

MicronMT1K1256M16HA-12S/E/AKD5JGSTL02 for proto board



Debug Port(DBG)

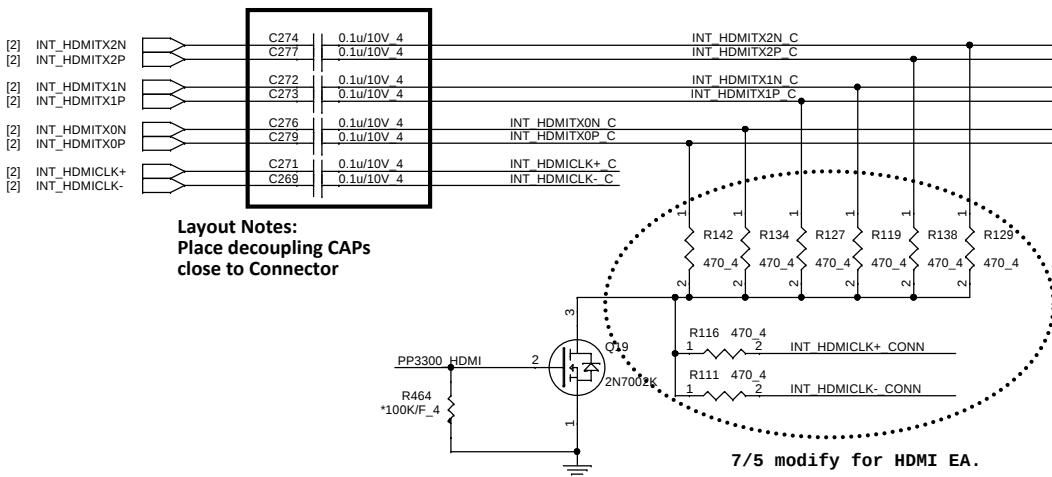
PIN7 OD PIN39 OD PIN49 OD
 PIN14 OD PIN41 OD PIN50 OD
 PIN19 OD PIN43 OD
 PIN22 OD PIN44 OD
 PIN28 OD PIN45 OD
 PIN30 OD PIN46 OD
 PIN37 OD PIN47 OD
 PIN38 OD PIN48 OD



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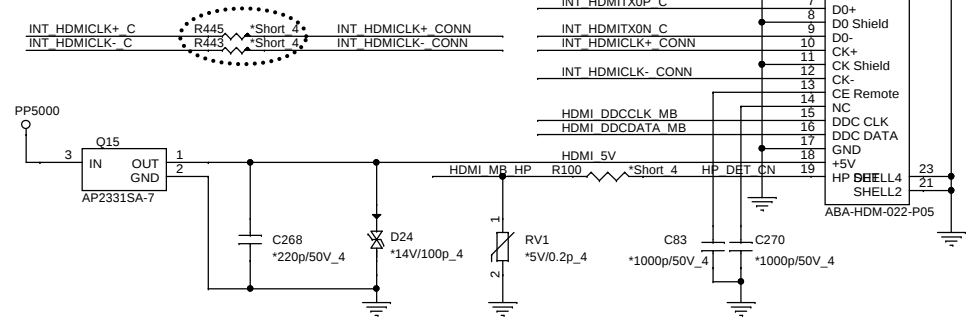
HDMI Cost Reduced level shift (HDM)



HDMI connector (HDM)

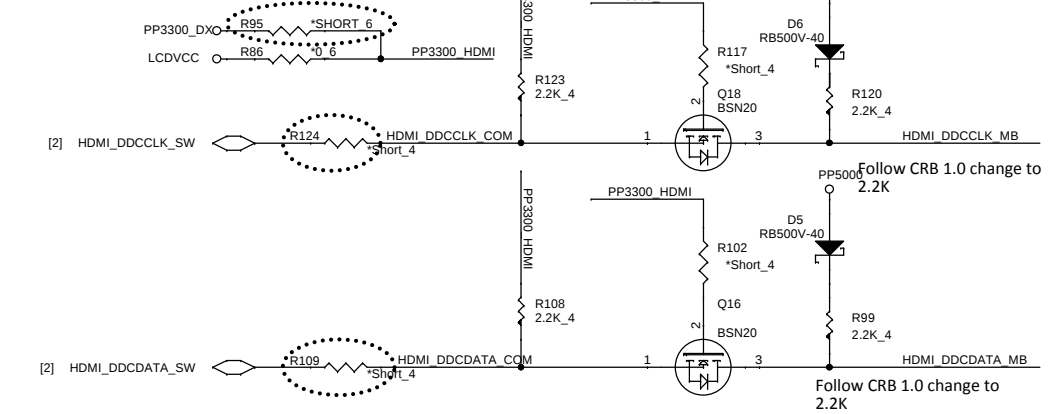
DFHS19FR079
new footprint not ready

8/21 Del L13 and R443, R445
change to shortpad.

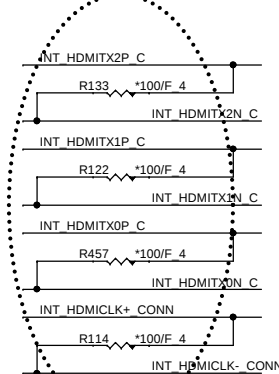


18

HDMI DDC (HDM)

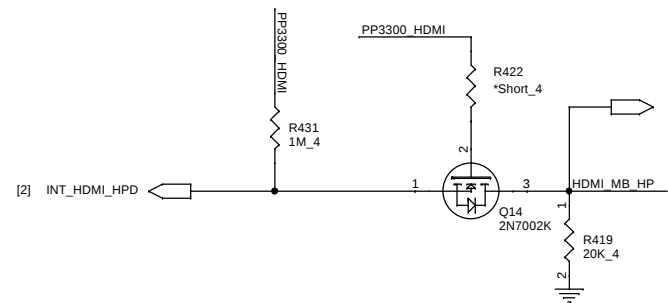


EMI (EMC)



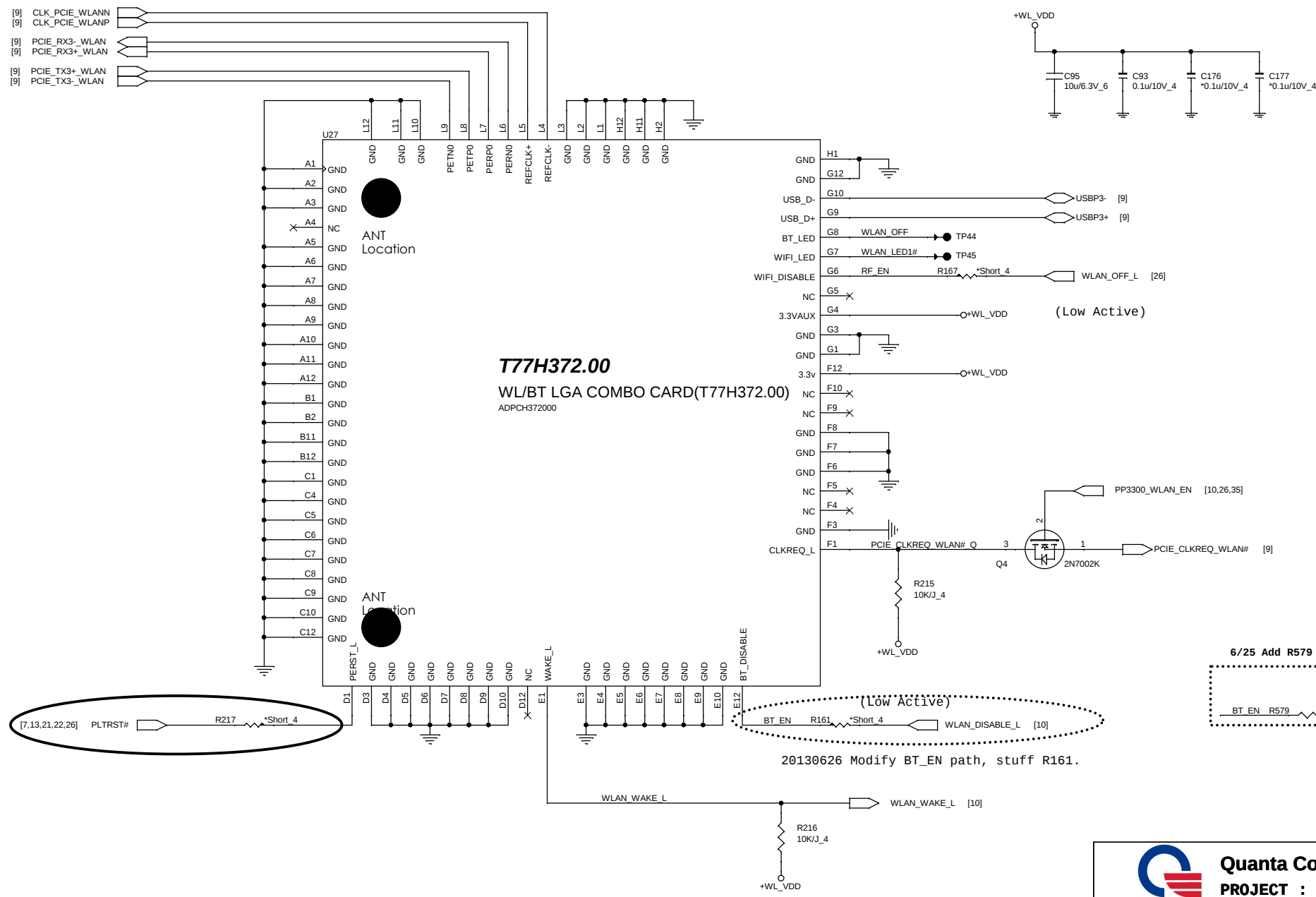
4/22 modify for layout
7/5 unstuff by HDMI EA.

HDMI-detect (HDM)

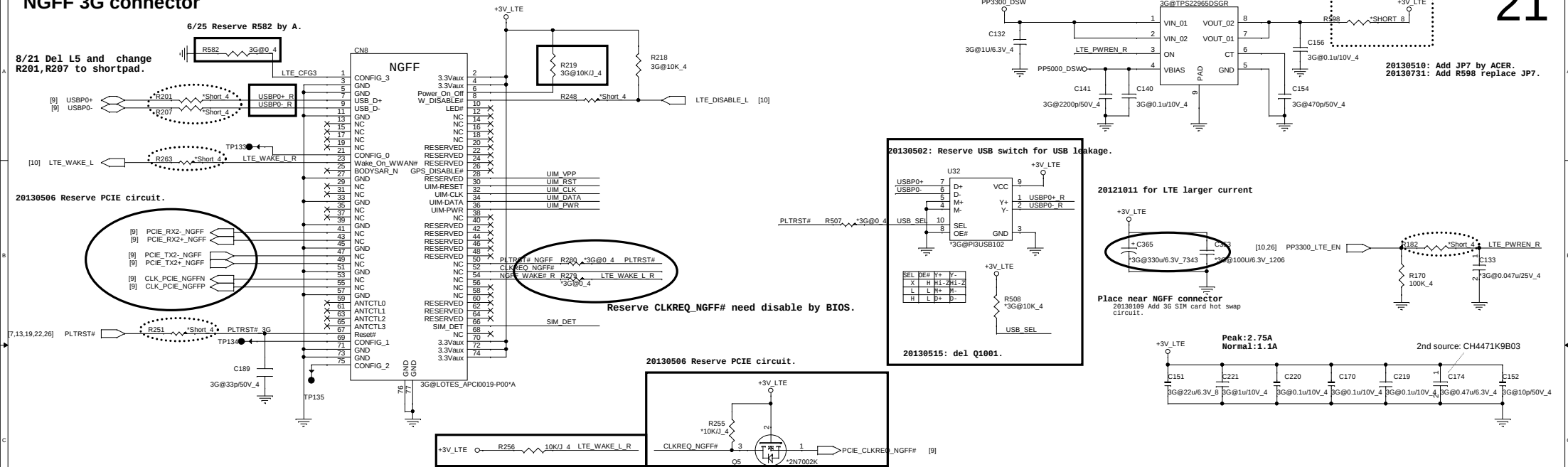


**Quanta Computer Inc.**
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HDMI

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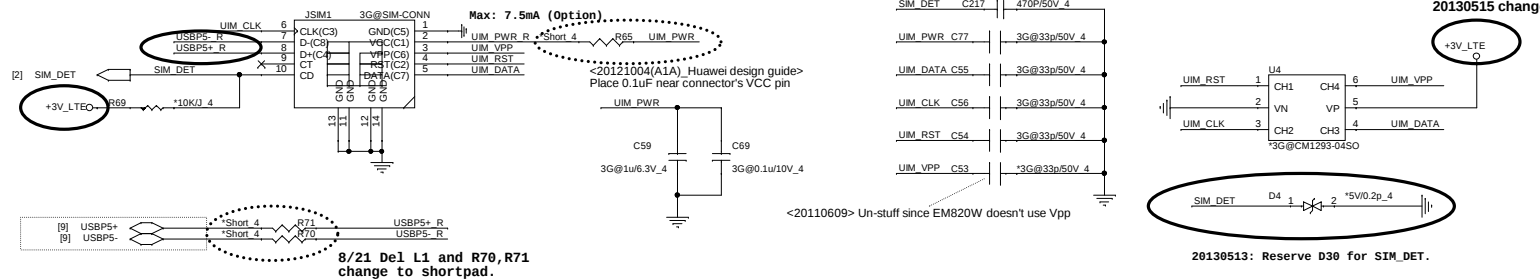
NGFF 3G connector



MultiMedia SIM (MNC)

<Layout Notes> Keep USIM signals max length within 8000mils.

5/14 Add R65



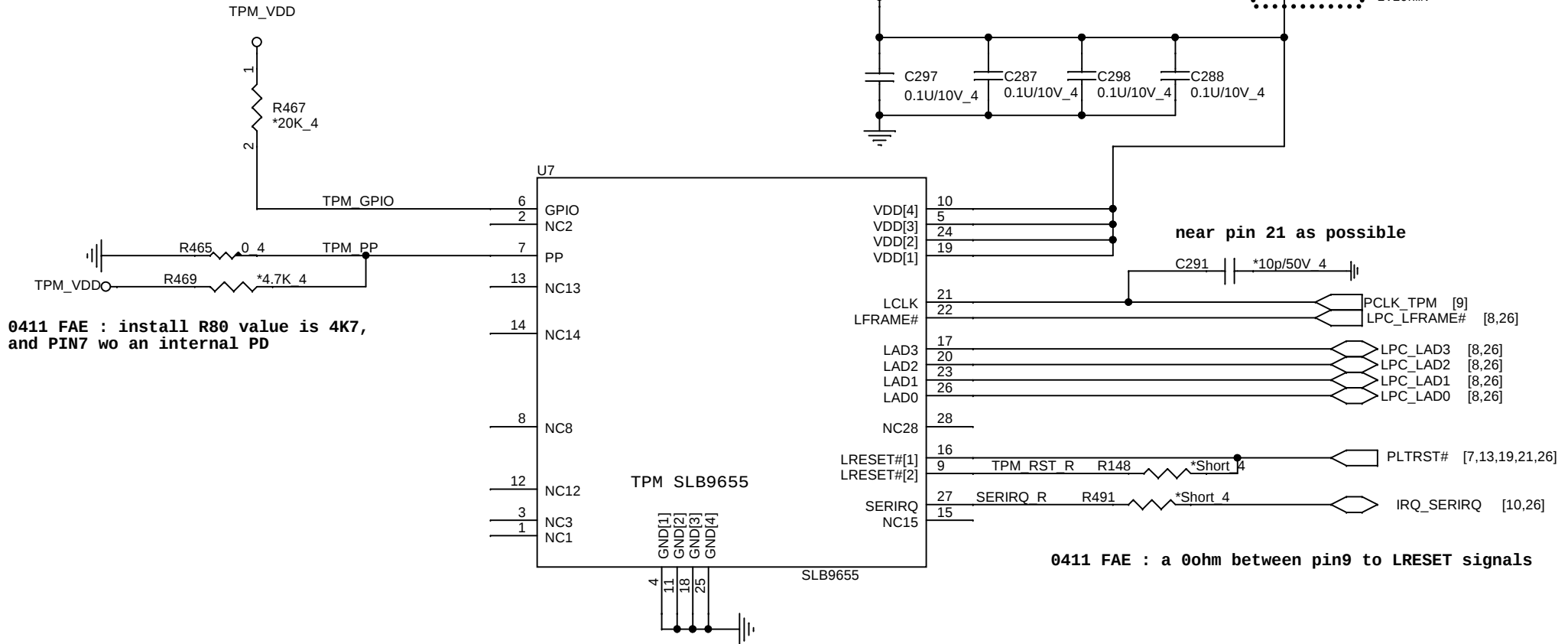
20130513: Reserve D30 for SIM_DET.

 Quanta Computer Inc. PROJECT : ZHN		Rev
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NGGF/ SIM conn		
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TPM (TPM)

22

4 x100nF (place close to device VDD/GND pins)



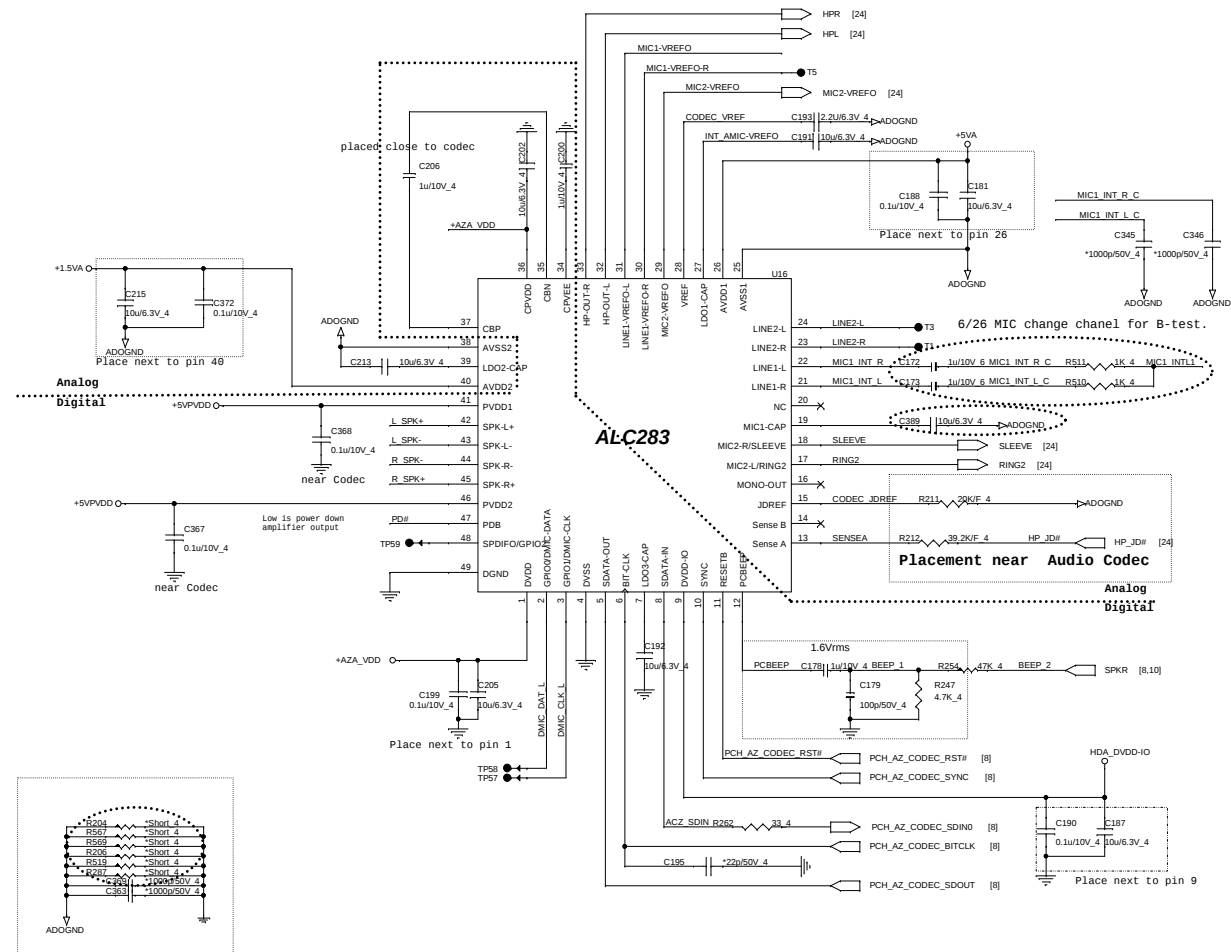
Quanta Computer Inc.

PROJECT : ZHN

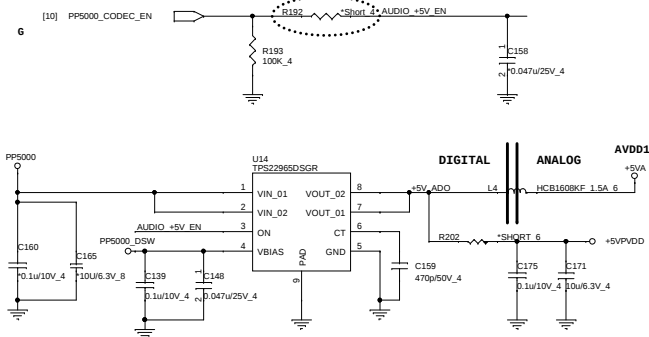
Size	Document Number	Rev
	TPM SLB9655 / LED	3B

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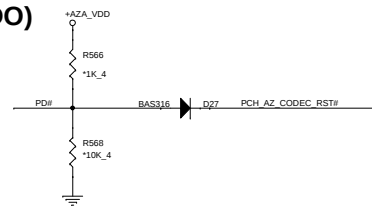
Codec(ADO)



Codec PWR 5V(ADO) 5/31 RevB Del R195, C161.

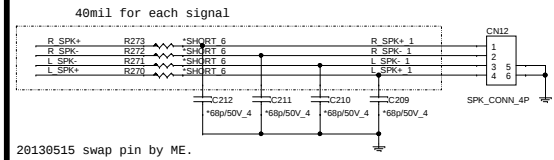


Mute(ADO)



Internal Speaker

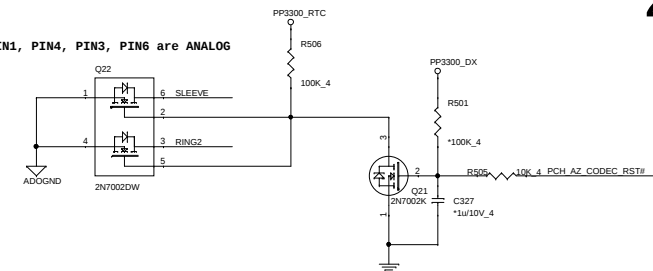
footprint 88266-040xx-xxx-4p-1



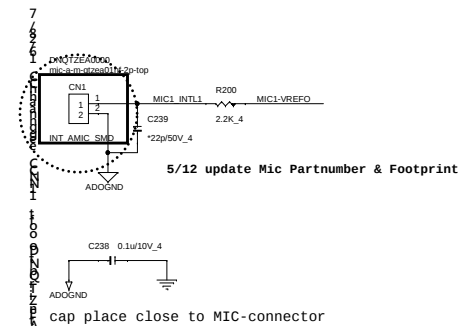
20130515 swap pin by ME.

Grounding circuit(ADO)

PIN1, PIN4, PIN3, PIN6 are ANALOG

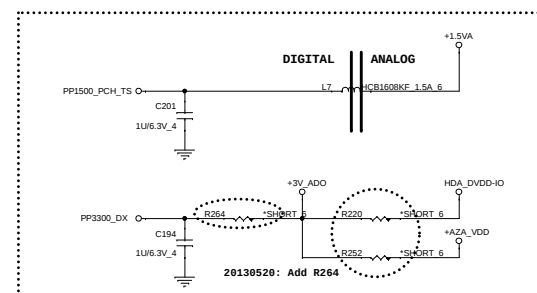


INT MIC array



Codec PWR 3V/1.5V(ADO)

20130517 U13 remove, power source pass through to output.



24

change L16,L21 from 00000 to 0ohm by SMT.

[23] MIC2-VREFO

[23] RING2

[23] SLEEVE

MIC2-VREFO

R214
2.2K_4

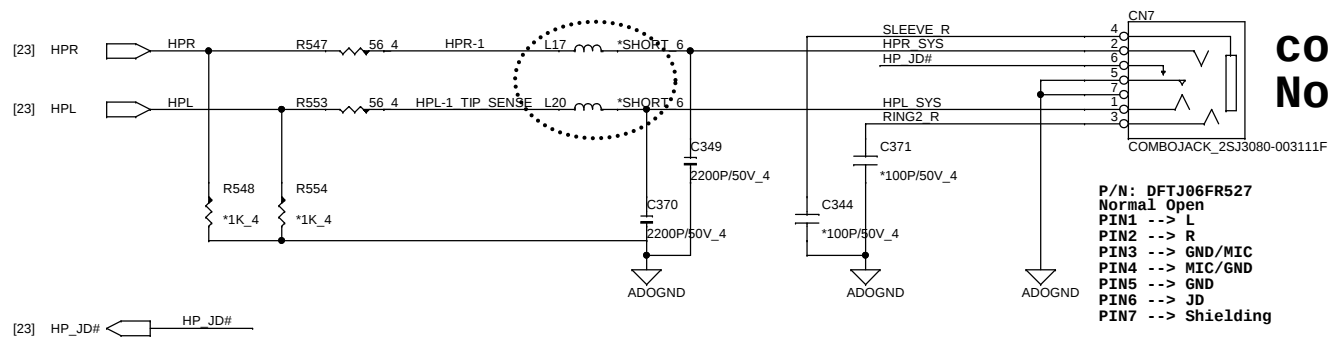
R283
2.2K_4

RING2_R

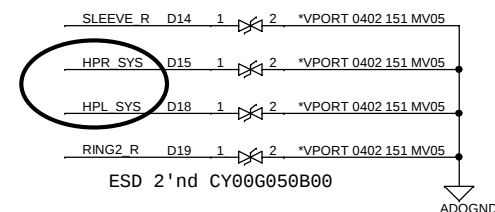
SLEEVE_R

L21
0.4

L16
0.4



combo jack
Normal open

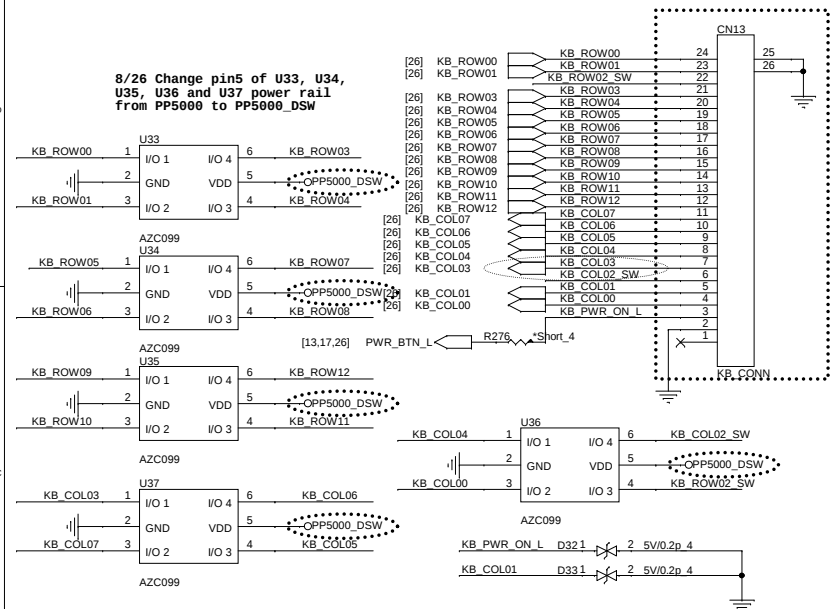


Quanta Computer Inc.
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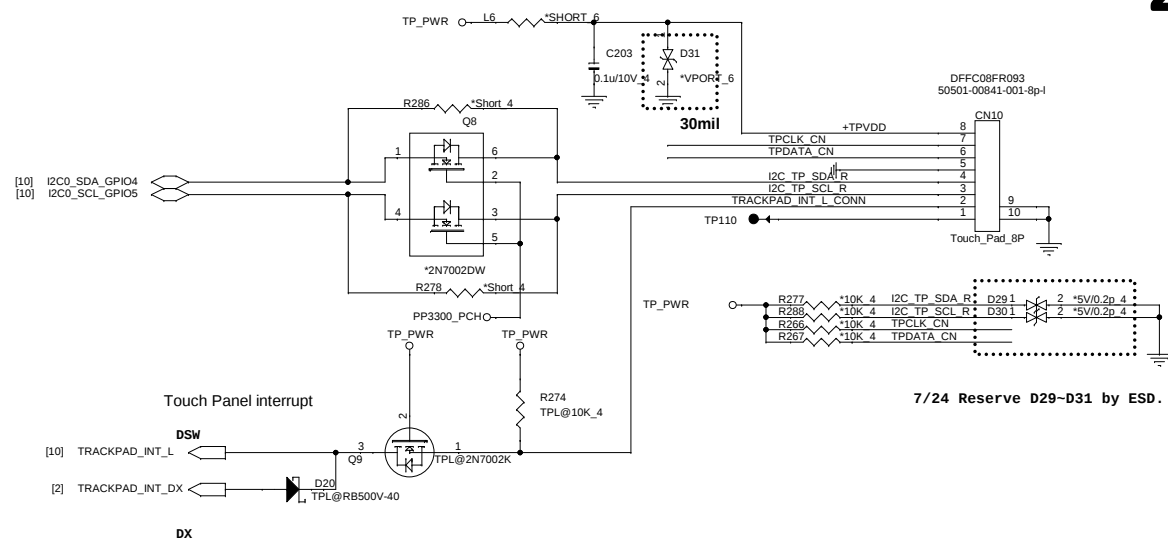
Size	Document Number	Rev
	Audio Headset SW	3B
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K/B (KBC)

8/22 DFFC24FR098
footprint 88502-2401-24P-L-SMT



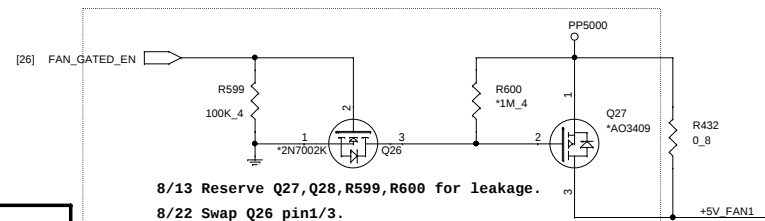
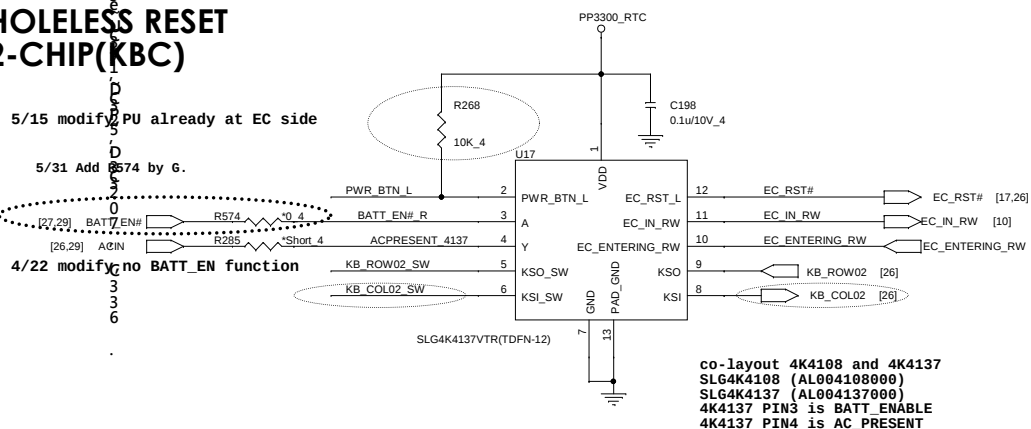
TOUCHPAD BOARD CONN (TPD)

HOLELESS RESET
2-CHIP(KBC)

5/15 modify CPU already at EC side

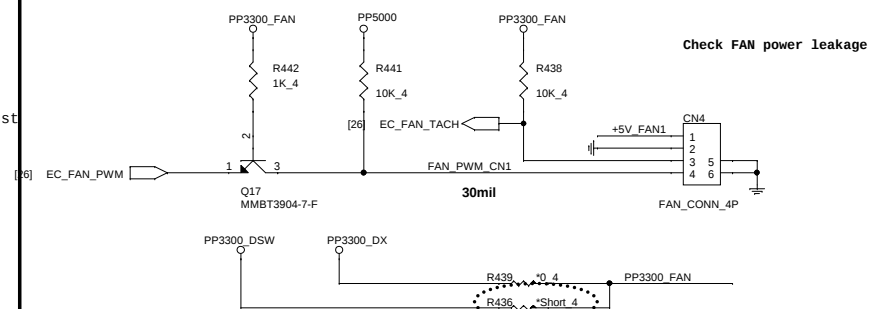
5/31 Add R574 by G.

4/22 modify no BATT_EN function



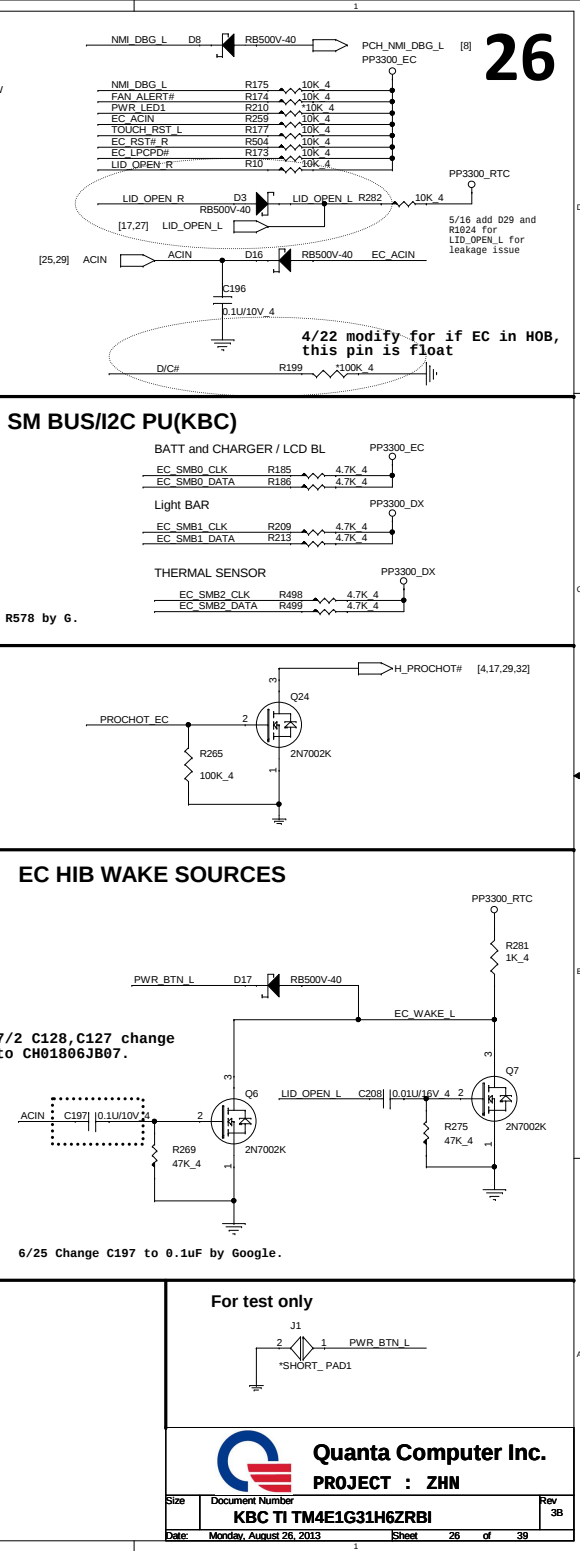
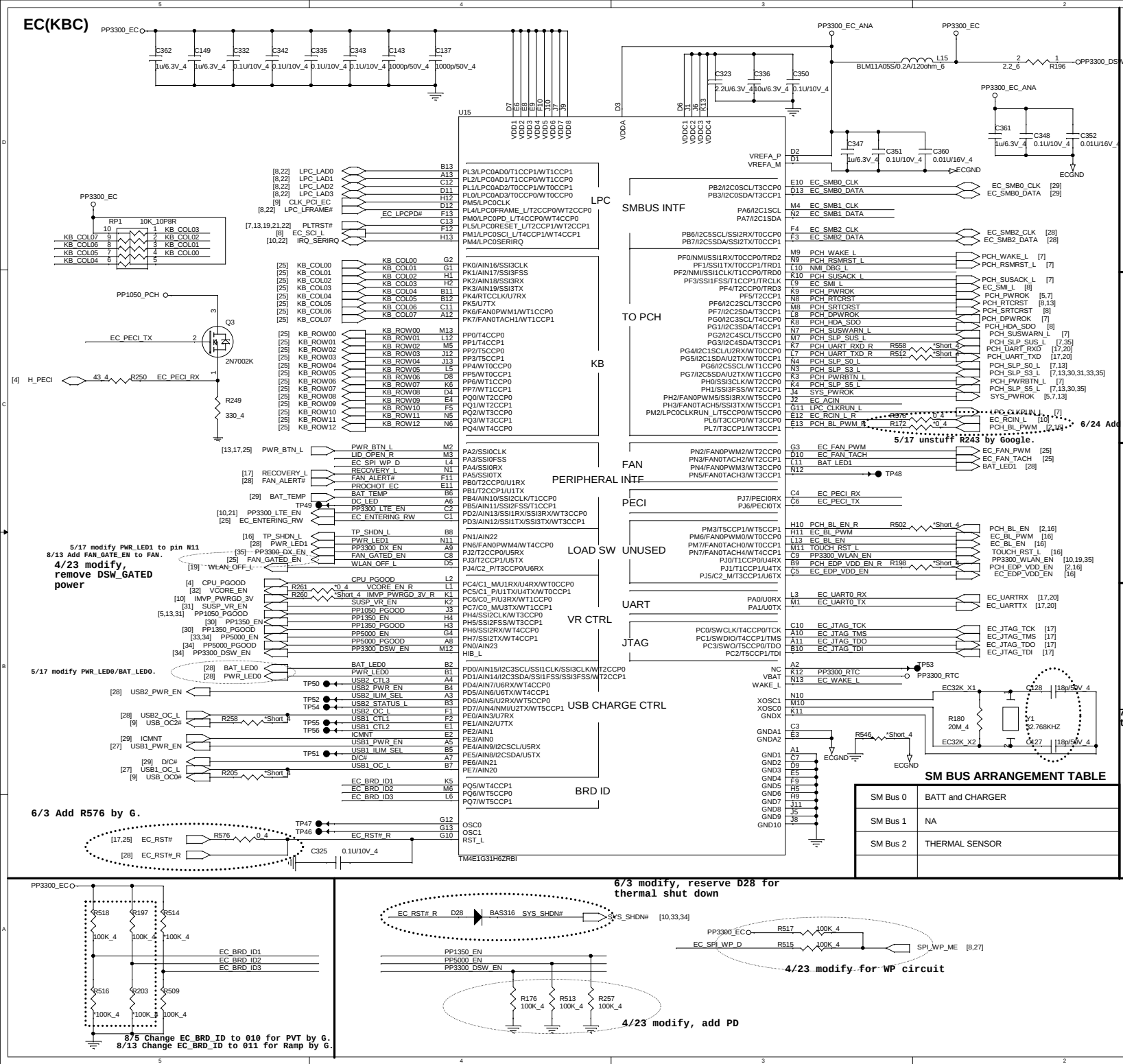
CPU FAN1 (THM)

Check pin define 0321
footprint 88266-040xx-xxx-4p-1

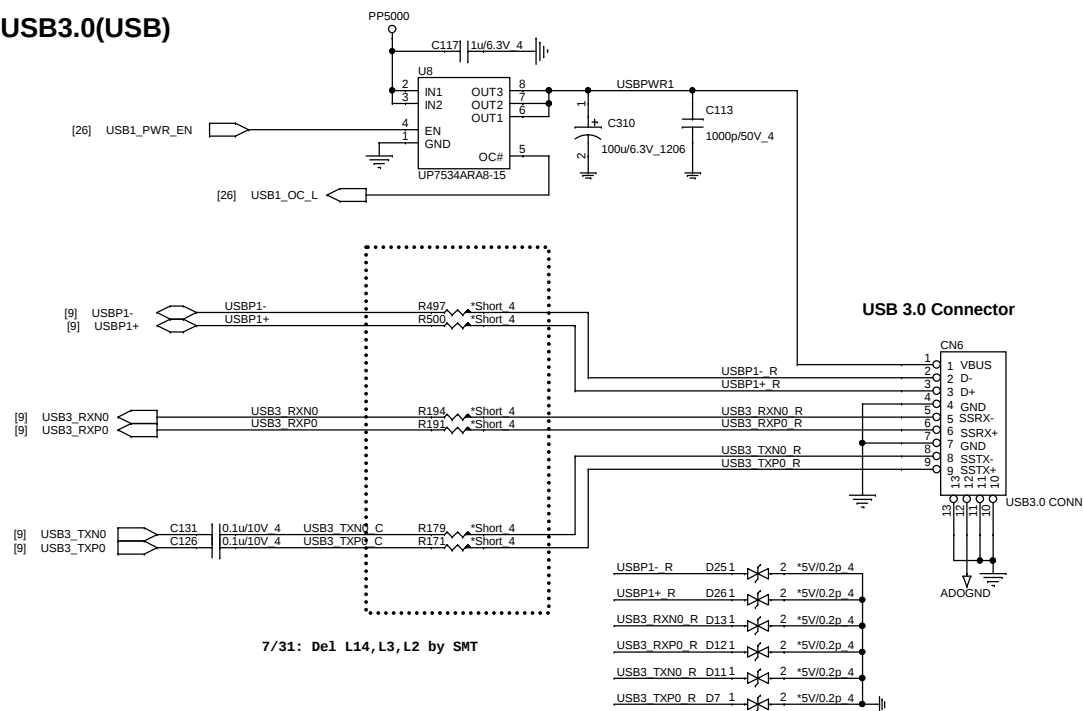


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PROJECT : ZHN

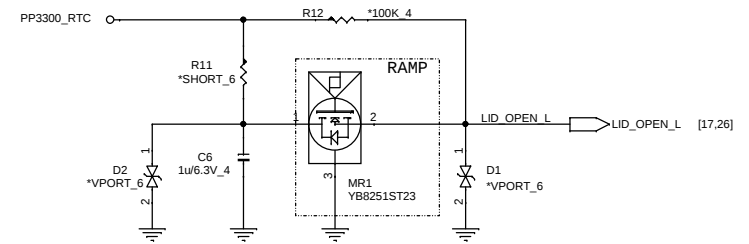
Size	Document Number	Rev
	KB/TP/FAN/HW Reset	38
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USB3.0(USB)

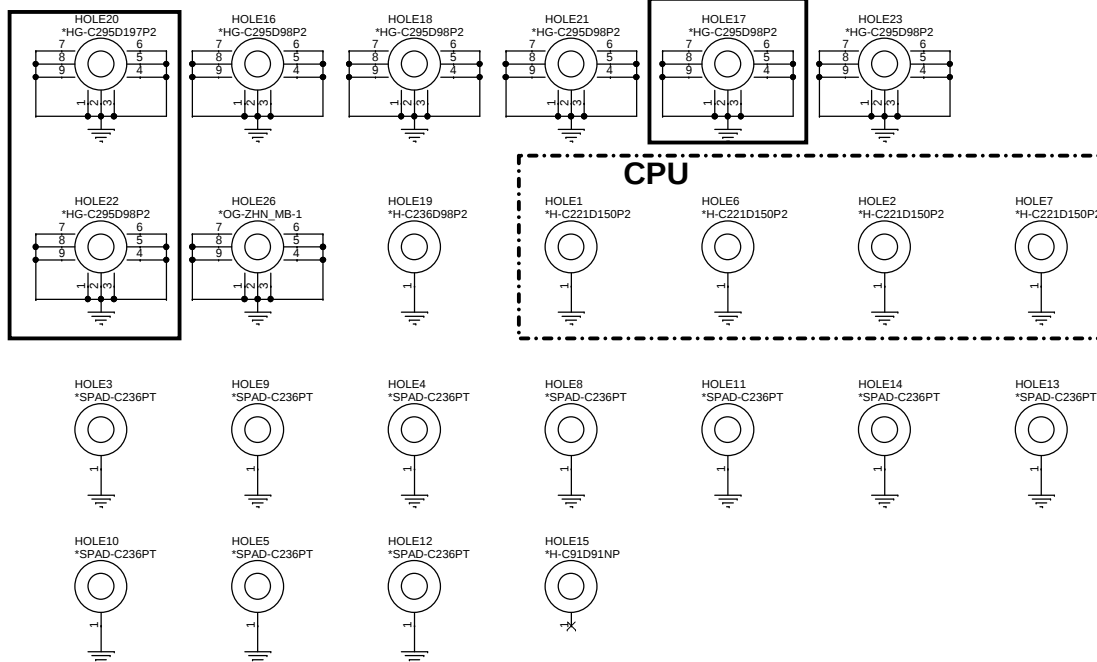


Lid Switch (HSR)

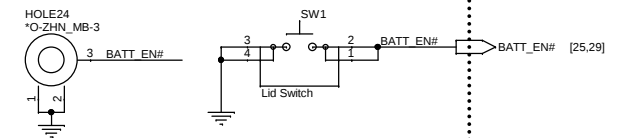


HOLE(OTH)

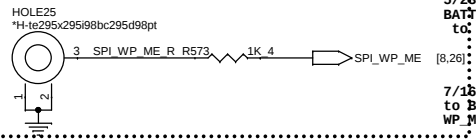
6/26 change footprint by ME.



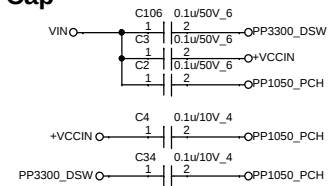
BATT Enable short pad



ROM WP#

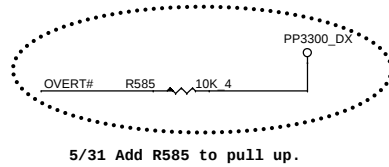
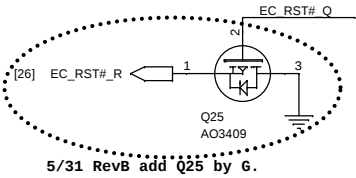
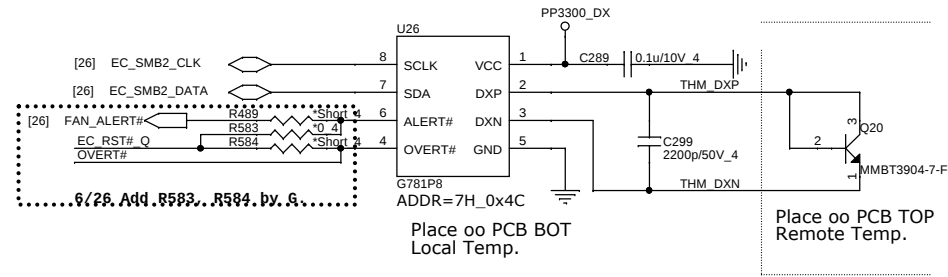


EMI Cap

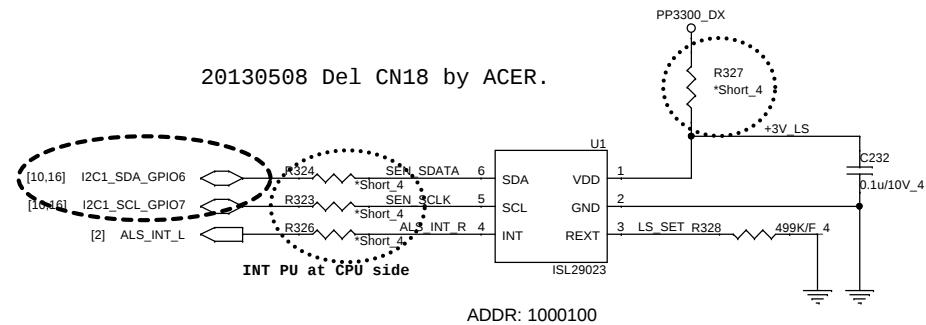


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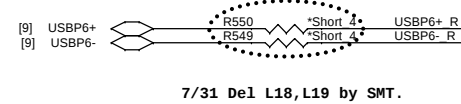
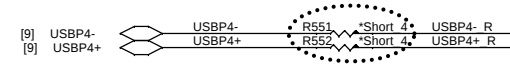
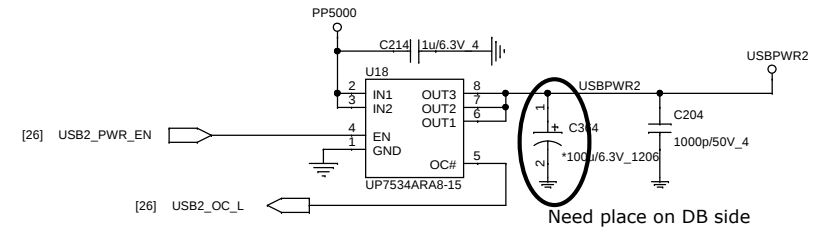
Thermal Sensor(THM)



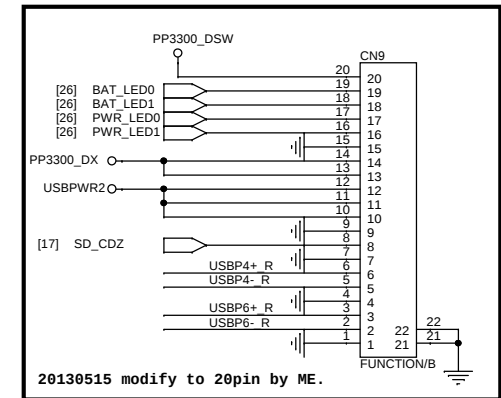
Light sensor & TP (SER)



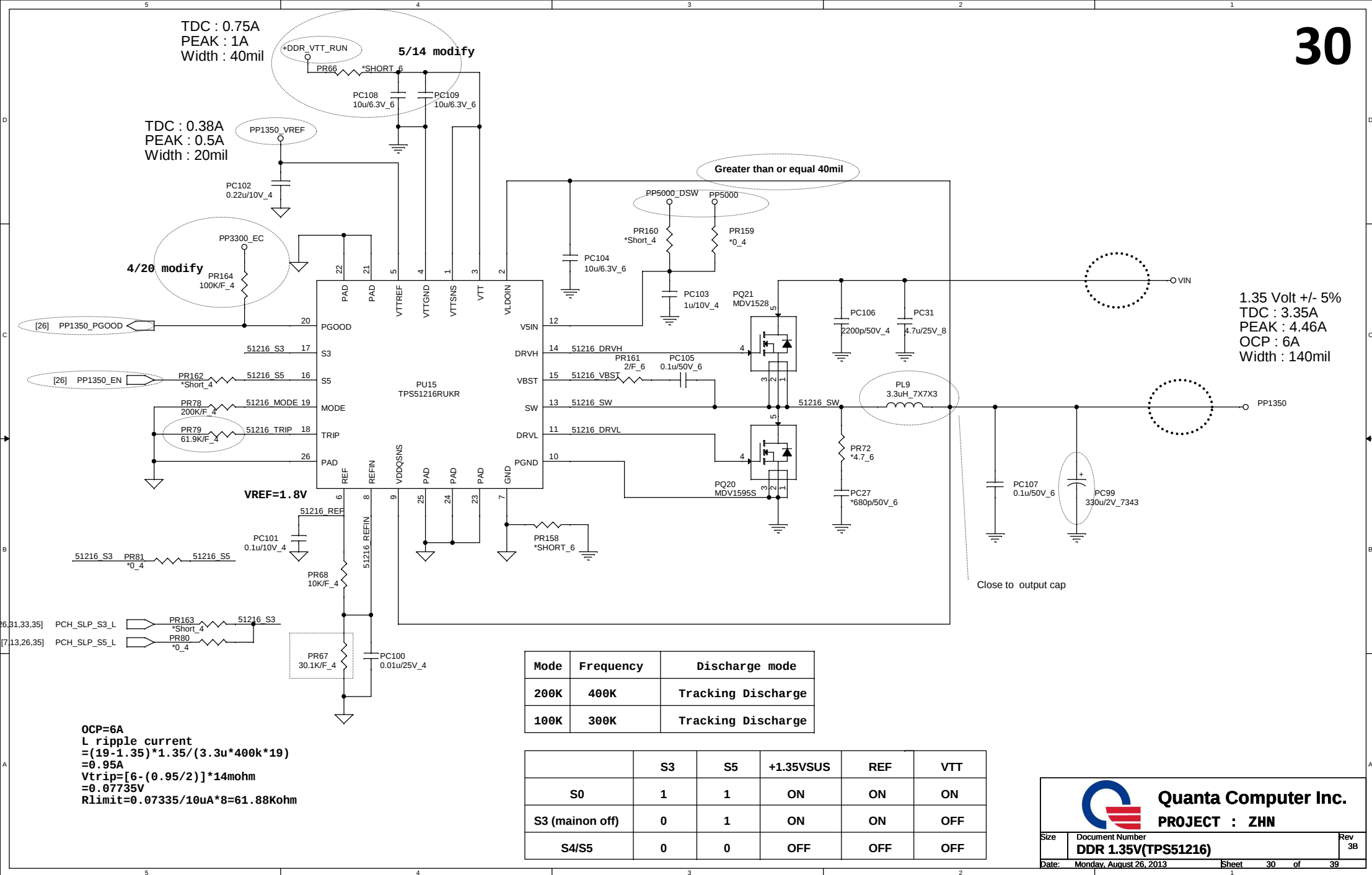
FUNCTION DB

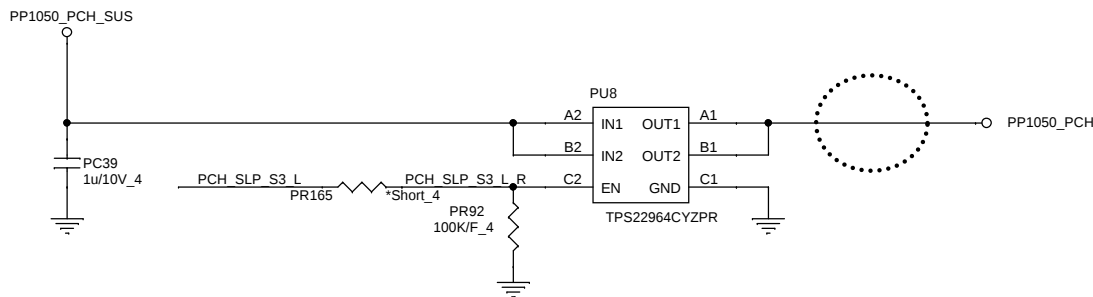
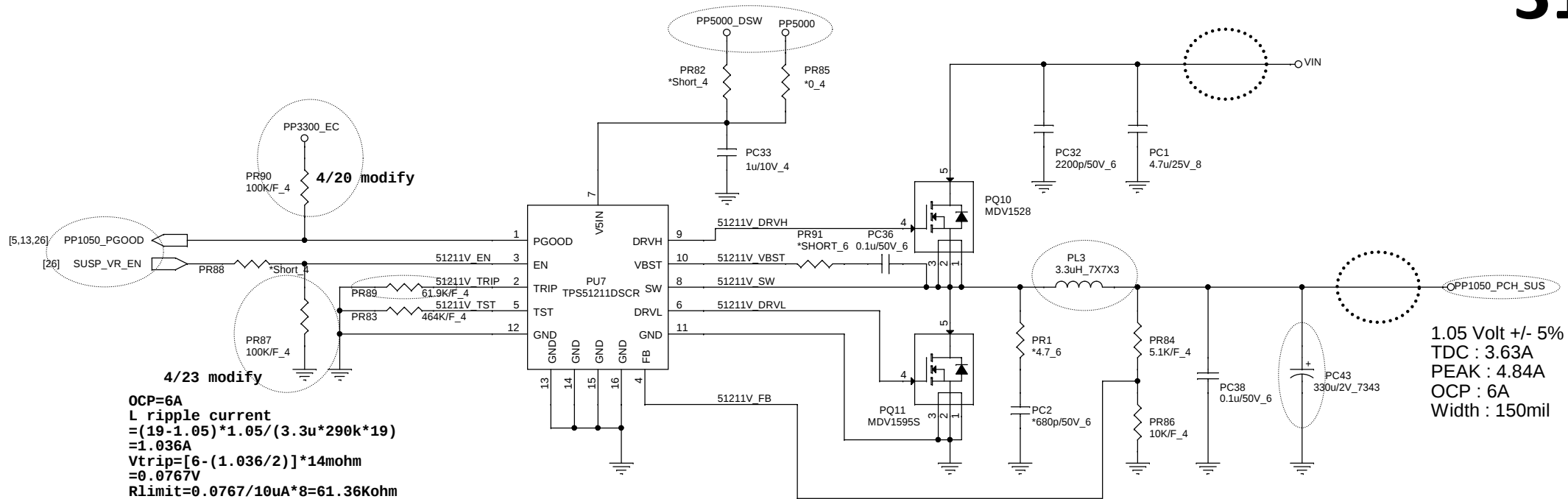


footprint 88511-2001-20p-1
DFFC20FR043



HSR	+3VPCU
	LID_OPEN_L
	GND
LED	+3VPCU
	LED x 4
	GND
USB	+3V x 2
	GND x 2
	USBP0+
	USBP0-
CR	CR_DET
	+3V x 2
	USBP6+
	USBP6-
	GND x 2

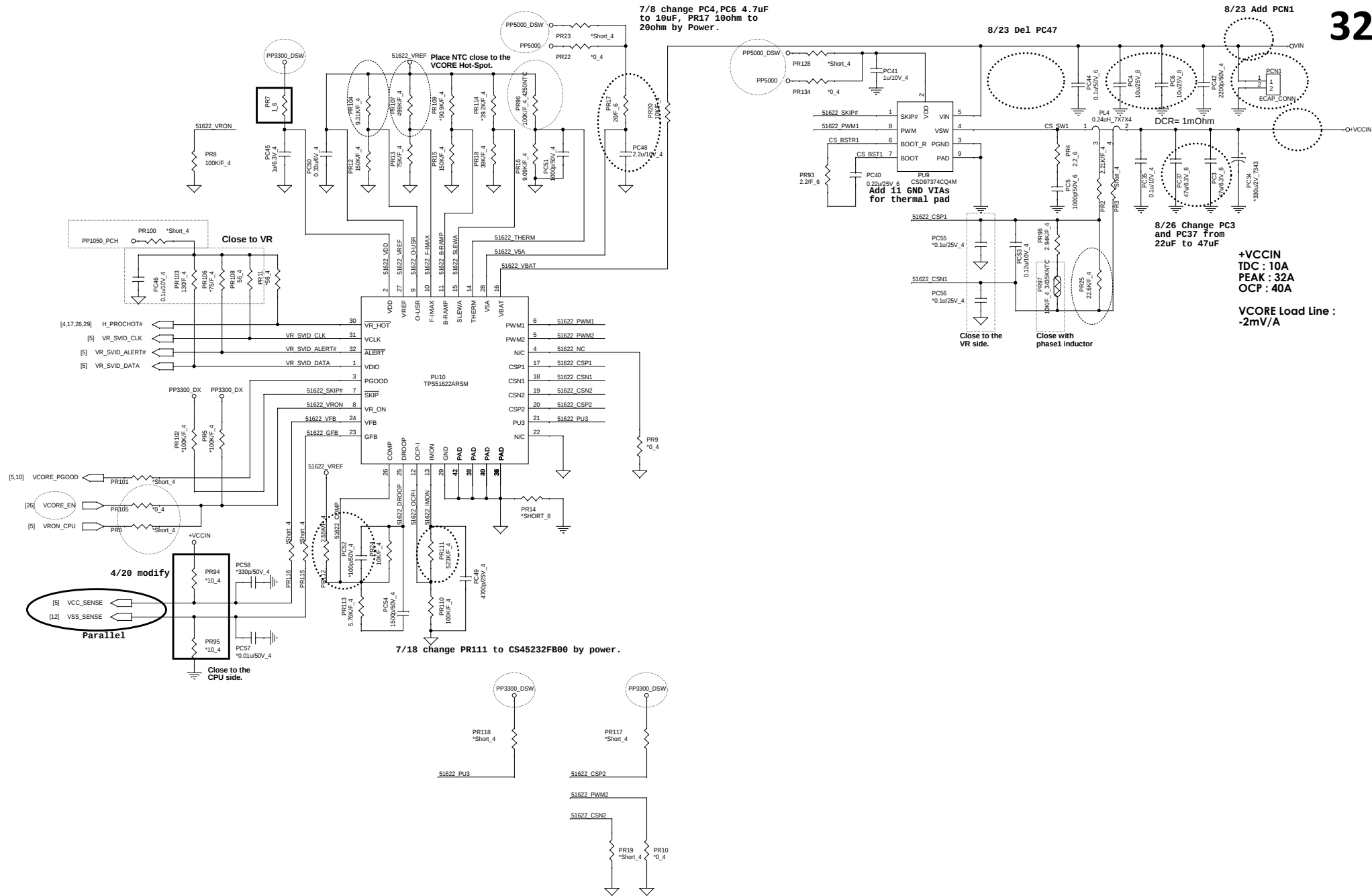


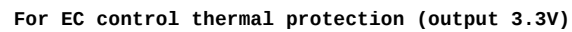
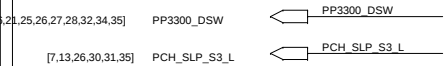


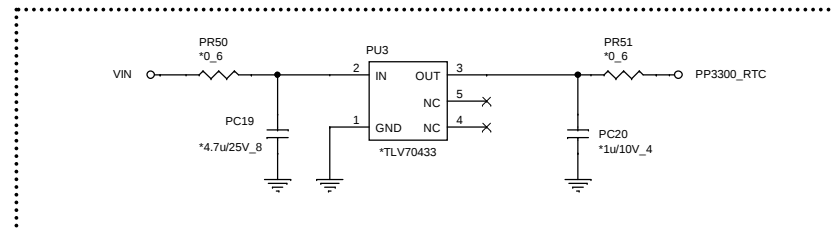
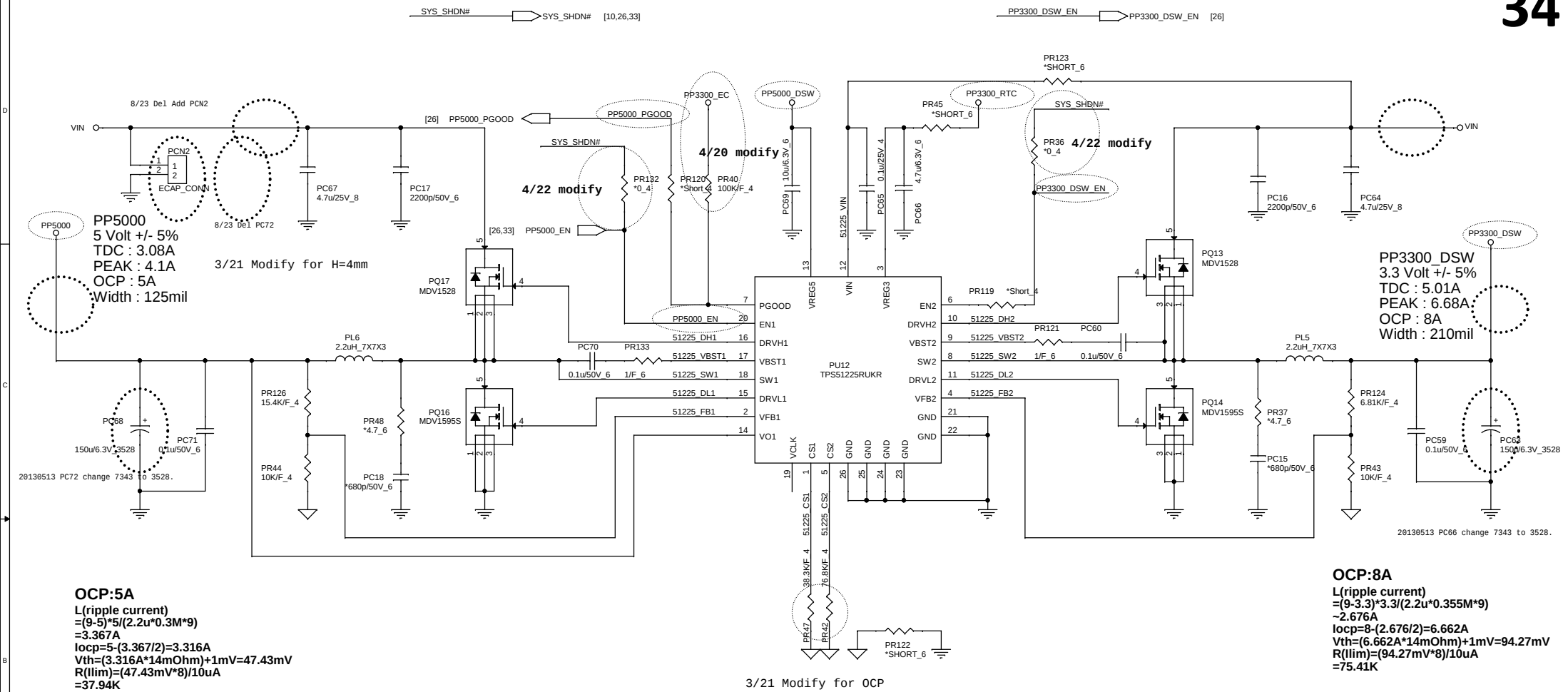
Quanta Computer Inc.
PROJECT : ZHN

Size	Document Number	Rev
	+1.05V(TPS51211)	3B

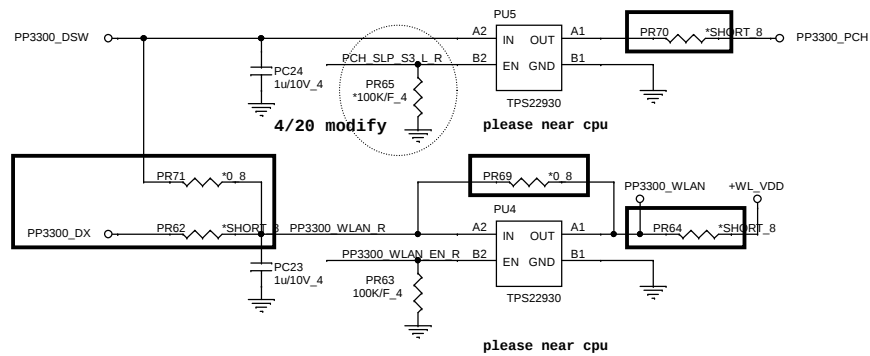
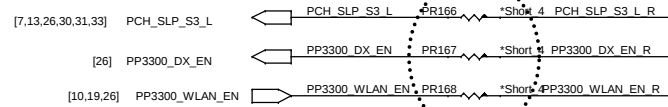
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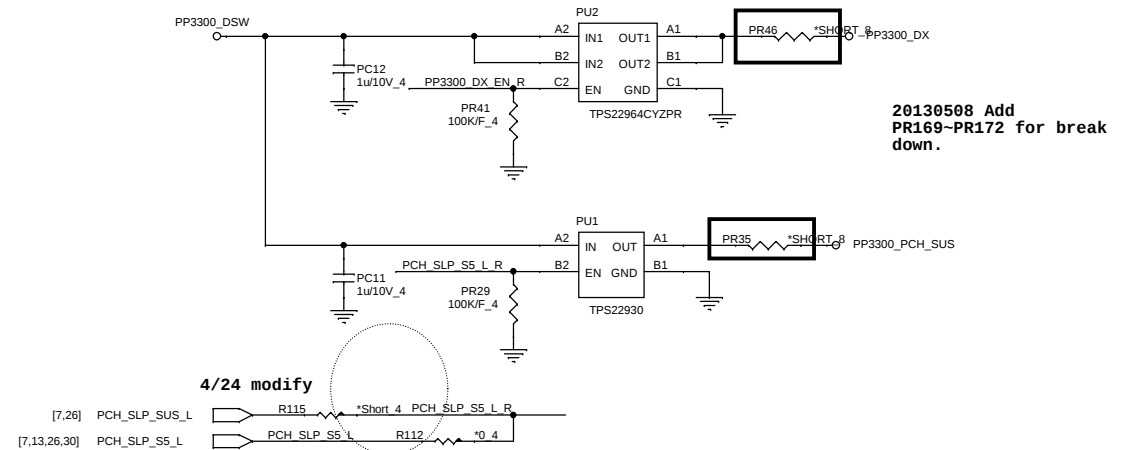


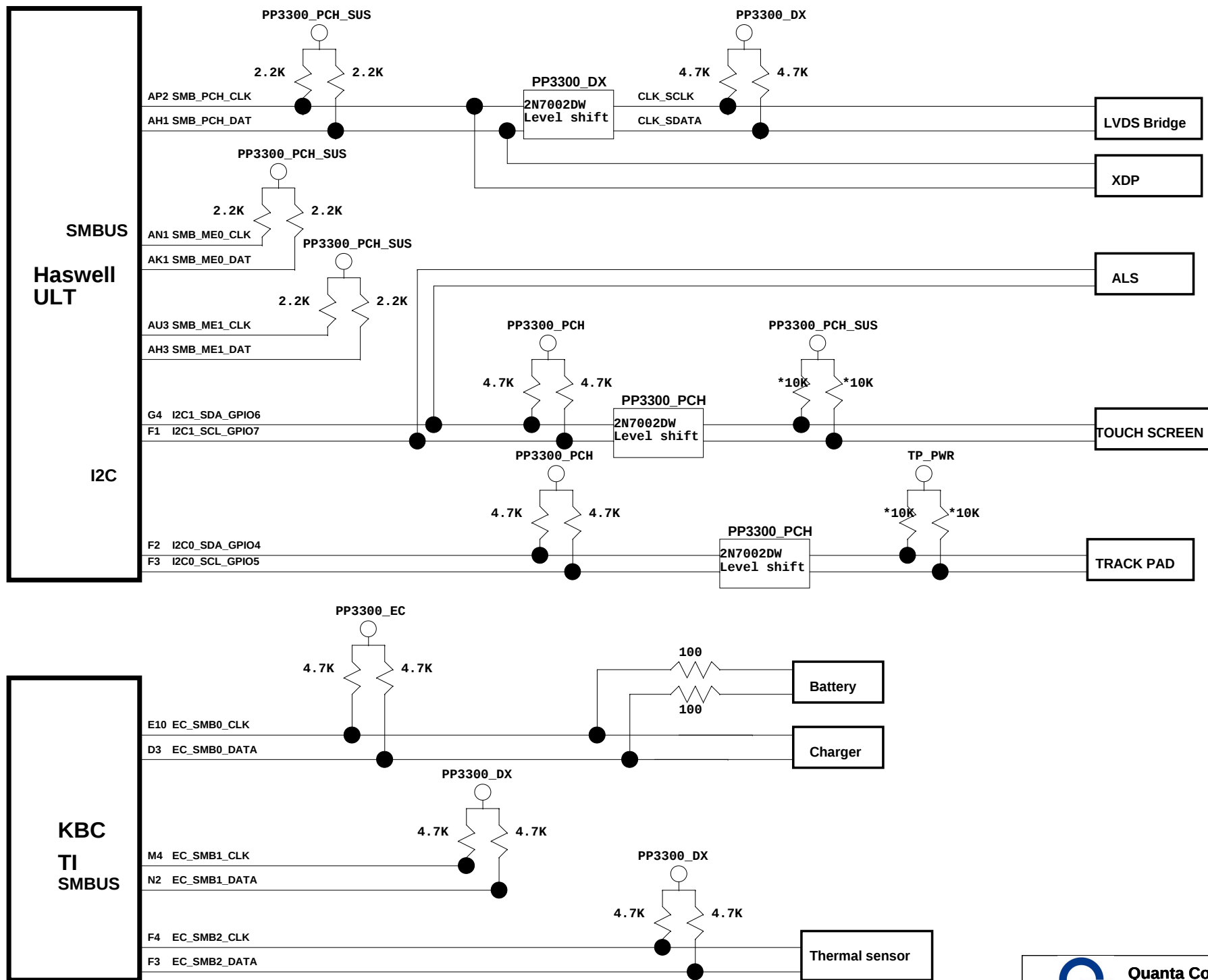


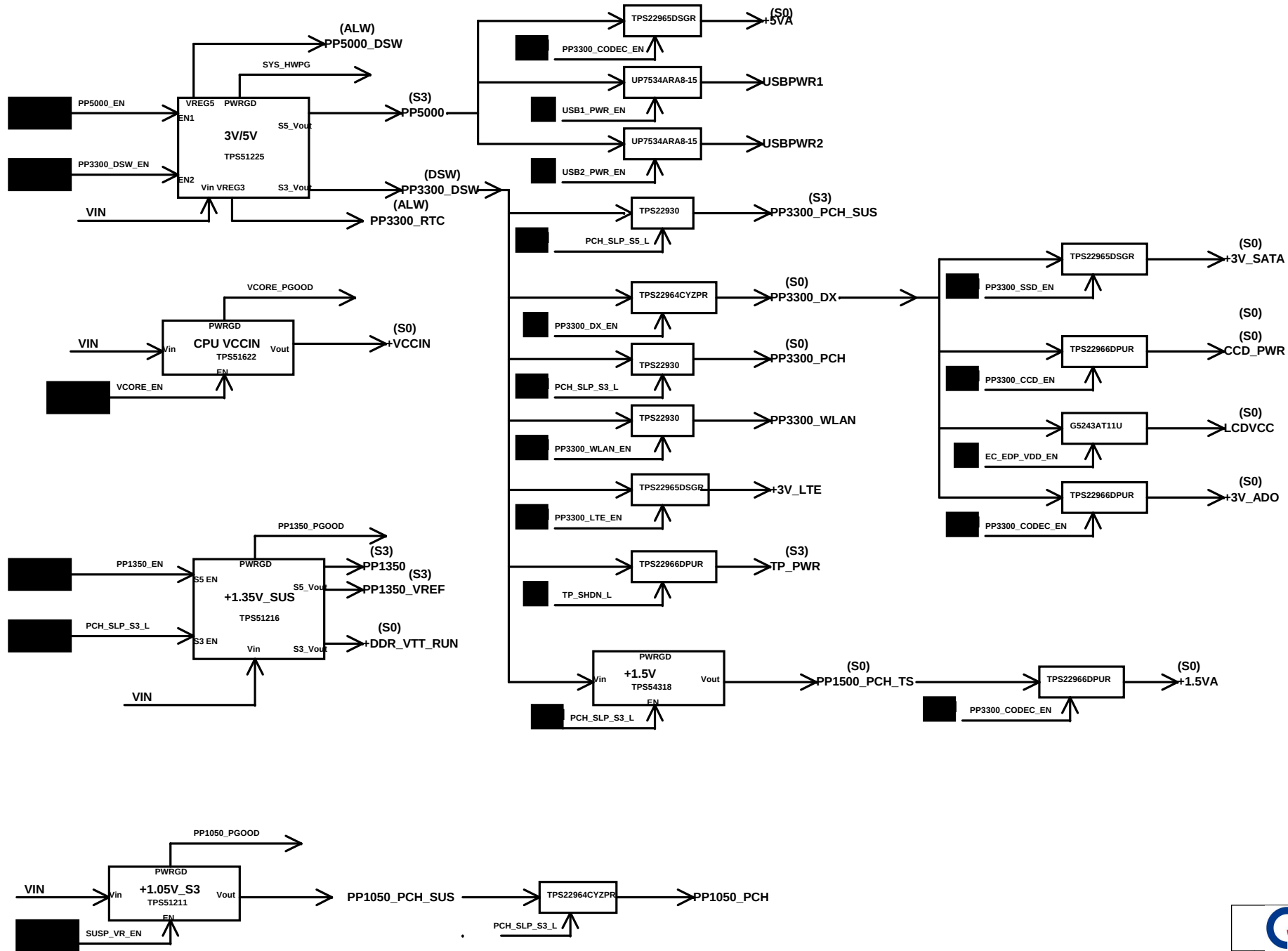
6/23 Add PR166~168 for debug.



20130517 Page35 Add PR174 & reserve PR175,PR176 to input pwr PU4 by ACER.







Model	Version	CHANGE LIST		
Benetton	1A	20130428 Page 21: Change net name USBP0_ R to USBP0_ R, USBP0_ R, USBP0_ R to USBP0_ R		
		20130502 Page21: Reserve USB switch USB0R, Q100,R1000 for USB leakage.		
		20130502 Page31 Del +LVB_SSD, +L2V_SSD power circuit.		
		20130502 Page11 Del CNI for XDP debug.		
		20130502 Page17 Del RVN3 Del EEPROM Mode strapng R163,R162,R176,R177.		
		20130501 Page16 Del DMIC circuit R421,R422,C315,C316.		
		20130501 Page2224 Del DMIC & Auto switch by Google.		
		20130501 Page20 Add Cap C6410-C6411.		
		20130501 Page29 Change P11 and P12 footprint.		
		20130501 Page9 Add CSMP and CLK_PCL LPC with R1004.		
20130506 Page23 Change AMIC(CN17) footprint to mic-kec22424612p.				
20130506 Page21 Reserve PCIe circuit & USB0 pin5 connect to GND & change JSIM1footprint to sim-c01x-3-14p-out by ME.				
20130506 Page9 Reserve PCIe circuit				
20130507 Page16 Add R1014 for PU DEVSLP0.				
20130507 Change connector footprint by ME.				
20130508 Page 29 Change connector P11 footprint by ME, add PLR,PL9 for EMI.				
20130508 Page21 Del CN18 by ACER.				
20130508 Page35 Add PR100-PR172 for power breakdown.				
20130509 Page19 Del R100,R102,R104, R105 by ACER.				
20130509 Page25: change R31-con CN13 to 24pin first by ACER.				
20130510 Page27 Add Hole and SWR for BATT_EN0.				
20130510 Page21: Add P911 by ACER.				
20130510 Page28: Add R1015.				
20130510 Page25:change R31-con CN13 to 24pin first by ACER.				
20130510 Page31: Add JP12.				
20130511 Page34: change PC64,PC72 from 7143 to 3528.				
20130513 Page21: Reserve D10 for SDR_DET.				
20130513 Page28: Change CN2 from 28 to 24 pins for LEDIR.				
20130513 Page22: Del RS,R7,LED1, move to LEDIR.				
20130513 Page21: Reserve NXP-onboard R1016-R1018.				
20130514 Page21 Add R1020.				
20130514 Page21 Add PR173.				
20130514 Page25: swap CN13 pin define.				
20130515 Page23: swap CN8 pin define by ME.				
20130515 Page27: Add HS41 IC by ME.				
20130515 Page28: change CN2 from 24 to 20pins.				
20130516 Page21: add diode D29 and R1024 for LID_OPEN_1 for leakage issue				
20130516 Page16 add R1023 by Atmel.				
20130517 Page25: swap CN12 pin define by ME.				
20130517 Page16: change L4 solution by ACER.				
20130517 Page28 USB remove , mSATA power connect to PP3300_DX.				
20130517 Page23 U13 remove, power source pins through to output.				
20130517 Page25: Add PR174 & reserve PR175,PR176 to input pair of P14 by ACER.				
20130517 Page28: net Bat_LED1-->(pin name) L116, PWRLD1-->N11; Battery LED0-->B, PWRLD0-->B1				
20130517 Page25: U13 pin L-->HW02; pin 6-->C0L3(113 key)				
20130517 Page16: stuff BS2,unstuff R100 & R243.				
20130520 Page21 Add R1025				
20130520 Page21 Remove +3V_ATC interseet				
20130520 Page14 RemoveRemove +SMD08_VREF_DQ0 interseet				
20130520 Page15 RemoveRemove +SMD08_VREF_DQ1 interseet				
20130520 Page11 Remove +V3_BDX, L5DX, L8DX_AUDIO interseet				
20130520 Page19 Remove +V1_BDS, MPL10P1 interseet				
20130520 Page27: Add C447,C449,C449,C449,C449,C449				
20130520 Page27 Add Add USBPWR2 at CN2.10				
20130521 Page21 Add R1026 for PU GPIO20.				
20130521 Page11: Change C143 from 0.1uF to 1uF; C78 1uF to 0.1uF; R103 shortpad to Behn; C208&C204 stuff; C274&C206 47uF to 22uF .				
20130522 Page28: Change CN13 footprint to mingsi-80902-001-52p.				
20130522 Page25: 12 Change U22 P10 to A100-HV-T01.				
20130522 Page28: Change CN15 P10 to DFHS12FR161.				
20130522 Page21: modify all component to ZCH0value & Hynix Ram P10 for BOM.				
20130522 Remove from 0222-2000.				
20130522 Page25: stuff R206,R205 by Google.				
20130522 Page16: change R103,R102 from 47K to 2.2K by TS suggestion & stuff Q23.				
20130523 Page27: change Change hole24 from BATT_EN0 to SPI_WP_ME, and add R573				
20130523 Page27: R74 on-stuff by L.				
20130523 Page13 R72, R300, C230, C231, U19, U22 stuff by L.				
20130523 Page4 R29 on-stuff.				
2A		20130531 Page28 Add Q25 to EC_RST0 by G.		
		20130531 Page23 Del R195, C181.		
		20130531 Page19 Reserve R100 and R575 to PU PP2300_PCH_SUS.		
		20130603 Page26 Add R576, reserve D20 for thermal shut down		
		20130603 Page13 Add TP111-TP122 by ICT		
		20130613 Page19: change R103,R102 to 47K for ALS abnormal.		
		20130613 Page16: stuff R425 for EDP.		
		20130616 Page28: change CN14 from mSATA to NGFF type and add C383.		
		20130617 Page18: change CN5 footprint from htsnd-B0103-1121-13p-fds to htsnd-B0103-1121-13p-fds-unt.		
		20130617 Page27: change CN6 footprint from sub-51065-00902-001-5p to sub-51065-00902-001-5p-unt.		
		20130618 Page21: Del RTC circuit (D9, R100,RTT1,Q2,R10,R102,R104,R100) by A.		
		20130618 Page28 Del R132.		
		20130620 Page21: Change R479 to 2.2ohm.		
		20130620 Page28 6/20 Add R577 by Kingston SSD; change CN14 to DFHS12FR003 by ME.		
		20130620 Del all Offpage of power signals in all page.		
		20130621 Add C384-C388 by Intel D0R layer.		
		20130621 Change CN1 to D9090024000 by ME.		
		20130624 Page 36 Add R578 for B-test by G.		
		20130624 Page 10 Modify RAM ID table & connect DEVSLP0 to NGFF SSD for B-test by G.		
		20130624 Page 35 Add PR106-108 for B-test debug.		
		20130624 Remove PP5000, ALN to PP5000, DEVN by G.		
		20130625 Page27 R74 stuff by G.		
		20130625 Page28 Change C197 to 0.1uF; Change EC_BRD_ID to 001 by G.		
		20130625 Page29 Change PMS2 to 47Kohm by G.		
		20130625 Page21 Add TP127-TP132 for XDP by Intel.		
		20130625 Page28 Add R580-R581 by Kingston SSD.		
		20130625 Page21 Reserve R582 by G.		
		20130625 Page21 Change MIC, channel from pin19/20 to pin21/22, and add cap C389 by vendor.		
		20130626 Page19 Modify RT_JFN path, stuff R161.		
		20130626 Page21: Add TP133-135 by A.		
		20130626 Page28 Add R583,R584 by G.		
		20130626 Page27: Change Hole2,22 footprint by ME.		
		20130626 Page21: Change C77&C206 to 15uF by crystal.		
		20130626 Page28: Change C127,C128 to 10pF by crystal.		
		20130626 Page21: Change P050N to C1310&S102 to C-test by Power.		
		20130705 Page18 Change R142,R134,R127,R119,R113,R129,R116,R111 from 680 to 470ohm; unstuff R114,R122,R133,R457 by HDMI EA unt.		
20130709 Page12: change PC4,PC6 from 47uF to 10uF, PR17 from 10ohm to 20ohm by Power.				
3A		20130711 Page11 R408 connection change to PP3300_PCH1 by leakage.		
		20130711 Page25: unstuff R574 by G.		
		20130716 Page14: unstuff PCLP,CN,PC20 by power.		
		20130716 Page27: modify Hole17 to GND; Hole24 to BATT_EN0; Hole25 to SPI_WP_ME by G.		
		20130718 Page13: Change R1011 to C45&C39 800 by power.		
		20130718 Page11: unstuff U19,U22 by ICT.		
		20130722 Page12: modify PU10,PCLP,C17,PC4,PC4,PC4,PR10,PR11,PR112, unstuff PC32 by power.		
		20130722 Page21: Change SWC2 to H1 by ME.unt.		
		20130723 Page28: Change EC_BRD_ID from 001 to 010(unst R197,R516; unstuff R201,R518).		
		20130724 Page22: Reserve D20-D31 by ESD.		
		20130724 Page29-35 Del JP and change Behn to shortpad.		
		20130724 Page16 Del colayout L12 by SMT.		
		20130729 Page28: Add R585 for OVERTE pull high by G.		
		20130729 Page28: Reserve R586-R589 for UART debug.		
		20130729 Page13: Reserve CN15, R590-R597 for XDP debug by Intel.		
		20130731 Page21: Add R590 replace JPT.		
		20130731 Page28 Del L18,L19 by SMT.		
		20130731 Page27 Del L14,L15,3 by SMT.		
		20130731 Page23: Change CN1 to D9Q1ZE/A0000 (SMD type: mic-als-t342-22u4-2p) by SMT.		
		20130801 Page22: Change CN1 to footprint to mic-a-m-quad1612p-unt		
		20130801 Page25: Reserve CPU_C207,C130		
		20130801 Page25: Add U13-U17,U12,U12,U13 for ESD		
		20130801 Page19: stuff R302 by G.		
		20130801 Page20 Un-Stuff R577 by G		
		20130802 Page5: Add C390-C396		
		20130802 Page5: Remove C396-C396		
		20130802 Change C31, C206, C244, C82, C248, C49, C262, C260, C41, C46, C42, C246, C21, C267, C23, C28, C25, C44, C27, C28, C24, C43, C45, C22, C247, C245,C14, C38, C50, C84, C151, C237, C240, C85, PC3, PC37 from CH1221M900 to CH1221M902.		
		20130805 Page28: Change EC_BRD_ID to 010 for PVT by G.		
		20130806 Page12: Change PR112 value to 2.50K by power.		
		20130806 Change C15, C206, C244, C82, C248, C49, C262, C260, C41, C46, C42, C246, C21, C267, C23, C28, C25, C44, C27, C28, C24, C43, C45, C22, C247, C245,C14, C38, C50, C84, C151, C237, C240, C85, PC3, PC37 from CH1221M902 to CH1221M903.		
		20130806 Unstuff C12,C15,C26,C42,C49 for acoustic noise by Pwr.		
		20130813 Page25: Reserve Q27,Q28,R590,R600 for IAN leakage.		
		20130813 Change R55,R12,R54,R400,R152,R507,R152,R51,R53,R54 from 0 to shortpad.		
		20130817 Page21: Change R576,R1,R577,R578 from 0 to shortpad & del L1,L15 co lay by SMT.		
		20130821 Page18: Change R443,R445 from 0 to shortpad & del L1,L15 co lay by SMT.		
		20130821 Page13: Change L16,L21 from CXP200000 to Behn by SMT.		
		20130822 Page25: Change CN13 footprint from R5502-2401-24P-R-SMT to R5502-2401-24P-L-SMT and swap CN13, Q28 pin define.		
		20130823 Page12 Del PC47 and Add PCN1		
		20130823 Page13 Del PC73 and Add PCN2		
		20130823 Page4: Change TP73, TP74, TP75 and TP76 footprint from TP2050 to TP2050		
		20130823 Page5: Change TP81 footprint from TP2050 to TP2050		
		20130823 Page21: Change TP91 footprint from TP2050 to TP2050		
		20130825 Change pins of U13, U34, U35, U36 and U37 power rail from PP5000 to PP5000_DSW		
		20130826 Page12: Change PC1 and PC37 from 22uF to 5uF. Unstuff others Vcc1n capacitors.		
20130826 Page2: Change C245, C244, C22, C24, C22, C24, C21, C21, C26 and G48 from 22uF to 5uF. Unstuff others Vcc1n capacitors.				
DOC NO.	PROJECT MODEL	Chrome	APPROVED BY:	DATE:
	PART NUMBER:		DRAWING BY:	REVISOR:
Quanta Computer Inc. F&B SECT - ZSW Change list Rev: 001				