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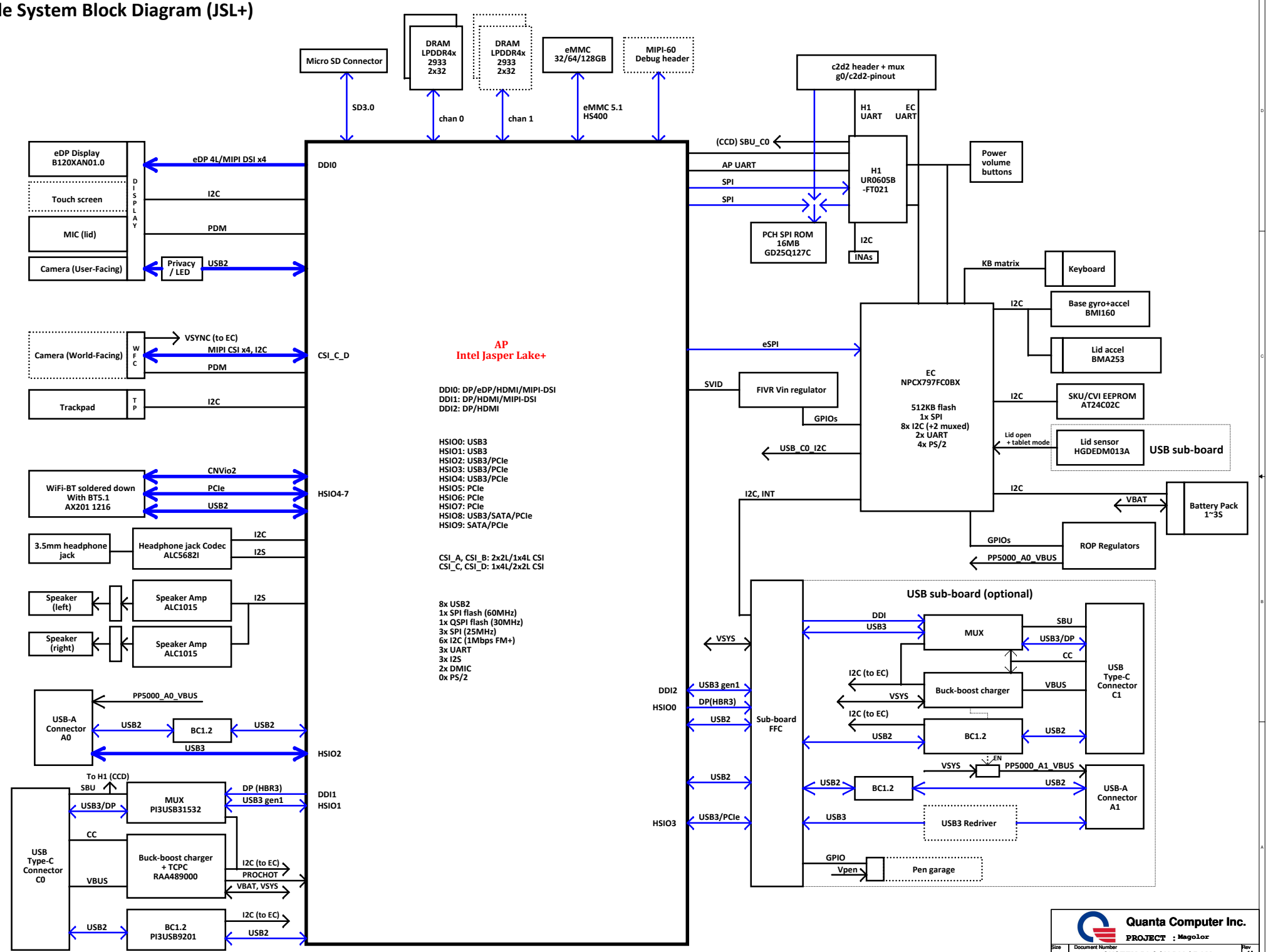
Dedede System Block Diagram (JSL+)



Quanta Computer Inc.

PROJECT : Magolor

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	SYSTEM BLOCK DIAGRAM	1A

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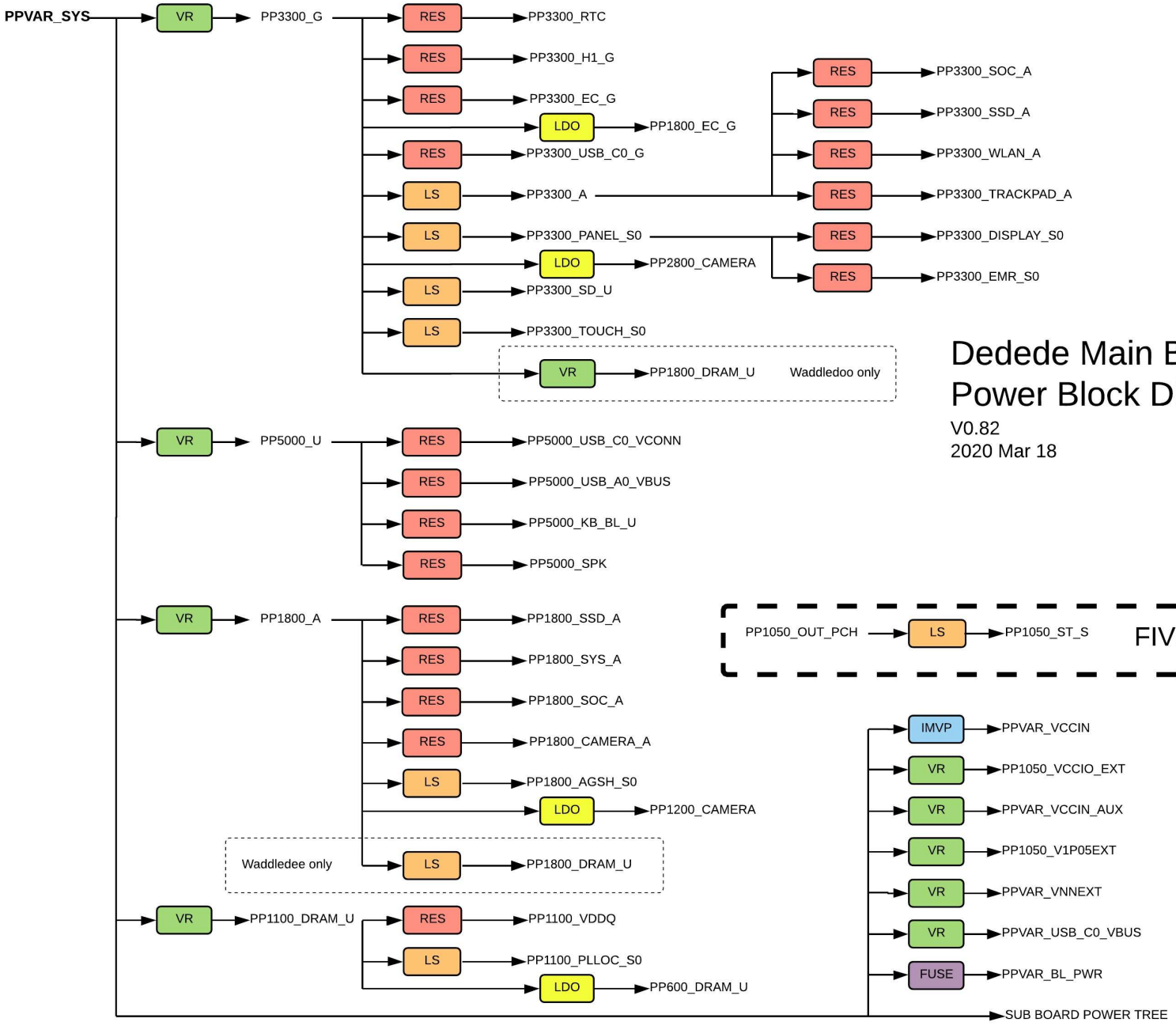
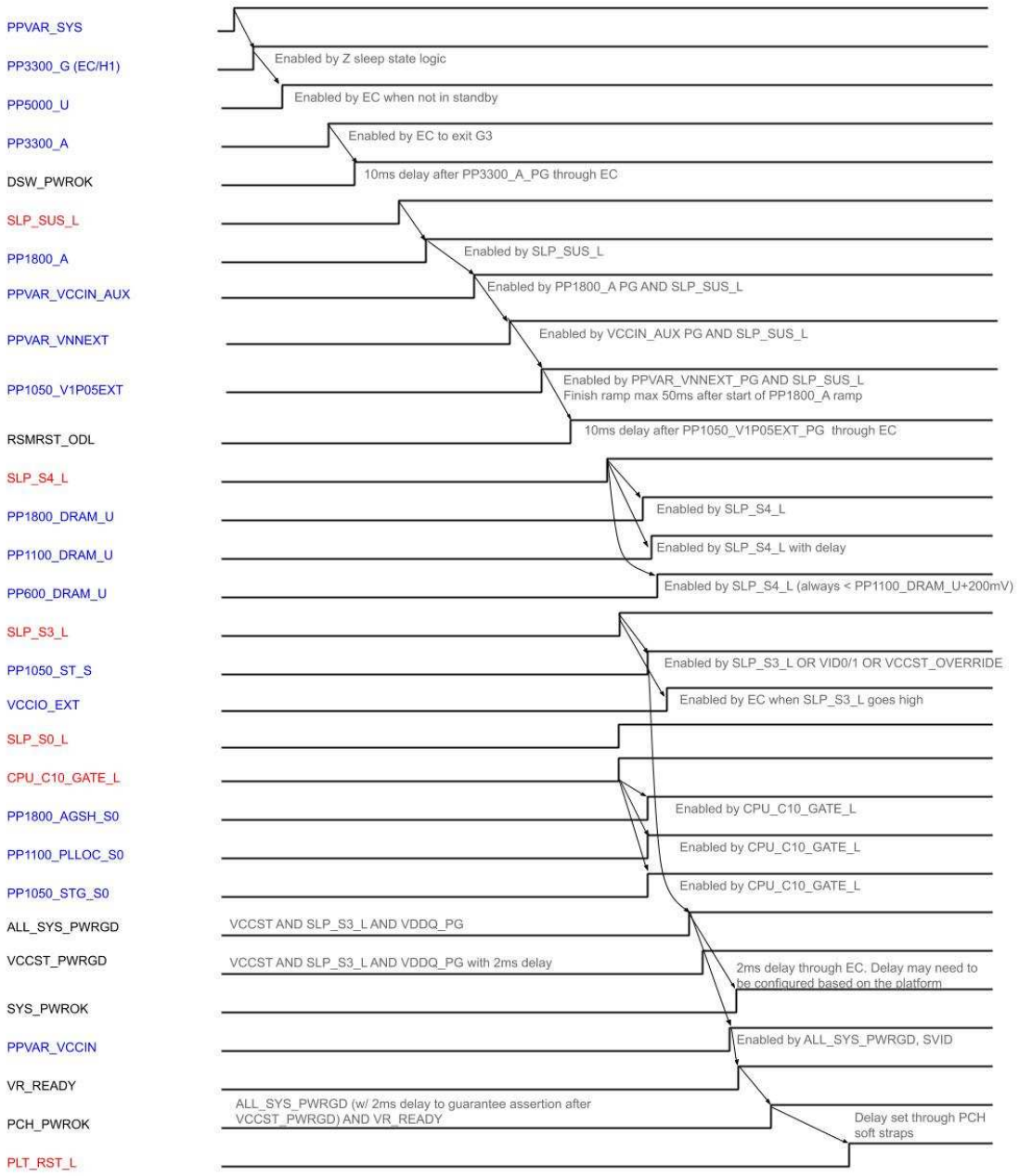


Dedede Main Board
Power Block Diagram

V0.82
2020 Mar 18

Quanta Computer Inc.
PROJECT : Hagolor
POWER TREE



Dedede Power Sequencing

Updated: 2/06/2020

Quanta Computer Inc.		
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Master	Port	Voltage Domain	Bus name	Bus Speed	Slave Device	7-bit Addr(s)	Int Priority	Note
AP(JSL+)	0	PP1800_A	AP_I2C_TP	400KHz	Trackpad	Project-specific	0	Trackpad
	1	PP3300_EMR_S0	AP_I2C_EMR	400KHz	SUBE-xxxxxMI	0x09	0	EMR pen
					HPDxxxx-920	?	0	EMR pen
	2	PP3300_TOUCH_S0	AP_I2C_TS	400KHz	Touchscreen	Project-specific	0	Touchsreen
					Panel	Project-specific	-	MIPI Panel
	3	PP1800_A	AP_I2C_CAMERA	400KHz	UFC	Project-specific	-	MIPI UFC
					WFC	Project-specific	-	MIPI WFC
	4	PP1800_A	AP_I2C_AUDIO	400KHz	ALC1015	0x28(left),0x29(right)	-	Speakers
					ALC5682I	0x1A	0	Headphone
					DA7219	0x1A	0	Headphone
	5	TBD	AP_I2C_SUB	400KHz	TBD	-	-	Expansion

Master	Port	Voltage Domain	Bus name	Bus Speed	Slave Device	7-bit Addr(s)	Int Priority	Note
EC	IT8320: 0 NPCX796: 7	PP3300_G	EC_I2C_EEPROM	1MHz	AT24C02D, GT34C02B, N24C02	0x30(PSWP),0x50(memory)	-	CBI EEPROM
					IT8320	0x35,0x5A,0x79	-	EC flash
					INA3221	0x40 ~ 0x43	-	INA
					INA231	0x44 ~ 0x4F	-	INA
	IT8320: 1 NPCX796: 5	PP3300_G	EC_I2C_BATTERY	100KHz	Smart battery	Pack-specific	-	Fuel gauge
	IT8320: 2 NPCX796: 0	PP1800_A	EC_I2C_SENSOR	400KHz	BMI160	0x68	-	Gyro/accel
					LSM6DS3TR	0x6A	-	Gyro/accel
					BMA253	0x18	-	Lid accel
					LIS2DE12	0x18	-	Lid accel
					KB backlight	Project-specific	-	KB backlight
					IMVP9	Project-specific	-	IMVP9
	IT8320: 5 NPCX796: 1	PP3300_G	EC_I2C_USB_C0	1MHz	SM5803	0x30,0x31,0x32	1	Charger
					SM5804	TBD	0	Charger+TCPC
					RAA489000	0x09(+0x0C SMBus ARA)	1	Charger
					RAA489000	0x22	0	TCPC
					ANX3447	0x2C,0x3F,0x3D,0x42,0x39,0x38	0	TCPC+MUX
					IT5205	0x48	-	MUX
					PI3USB31532	0x54	-	MUX
					PI3USB9201	0x5F	2	BC1.2
	IT8320: 4 NPCX796: 2	PP3300_G	EC_I2C_SUB_USB_C1	1MHz	SM5803	0x30,0x31,0x32	1	Charger
					SM5804	TBD	0	Charger+TCPC
					RAA489000	0x90(+0x0C SMBus ARA)	1	Charger
					RAA489000	0x22	0	TCPC
					ANX3447	0x2C,0x3F,0x3D,0x42,0x39,0x38	0	TCPC+MUX
					IT5205	0x48	-	MUX
					PI3USB31532	0x54	-	MUX
					PI3USB9201	0x5F	2	BC1.2
					TUSB544	0x44	-	Redriver
					NB7VPQ904M	0x19	-	Redriver
					PS8743	0x11	-	MUX+Redriver

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PCH GLITCH MITIGATION

U1JSLA

CPU_JSL_1338P

R22 100K_1%_2 — EN_PP3300_PANEL_S0 [8,38]

R23 100K_1%_2 — AP_EDP_BKLTEN [8,27]

R146 100K_1%_2 — EDP_AUX_P [8,27]

R147 100K_1%_2 — EDP_AUX_N [8,27]

R49 100K_1%_2 — EC_AP_USB_C0_HPD [29]

R6F1 150_1%_2 — DP_RCOMP

TP34 — DSI_TE — USED FOR MIPI PANELS

<STRAP. DDI2_HPD IS ON SPI PAGE :(

R148 *0_5%_2 — HDMI_DDC_SCL [8]

R149 *0_5%_2 — HDMI_DDC_SDA [8,13]

HDMI_SEL_L [29]

VTH<2V

Q9 DMG1012T-7

Q10 DMG1012T-7

CAPS/PULLS ARE ON SUB-BOARD

USB_C1_AUX_P [8] — USB_C1_AUX_P_HDMI_DDC_SCL [39]

USB_C1_AUX_N [8] — USB_C1_AUX_N_HDMI_DDC_SDA [39]

U1JSLF

CPU_JSL_1338P

PP3300_A

PP3300_TOUCH_S0

PP1800_A

R2 *2.2K_5%_2 — R11 *2.2K_5%_2 — R103 2.2K_5%_2 — R144 2.2K_5%_2 — R325 2.2K_5%_2 — R326 2.2K_5%_2 — R316 2.2K_5%_2 — R324 2.2K_5%_2 — R327 2.2K_5%_2 — R328 2.2K_5%_2 — R329 2.2K_5%_2 — R330 2.2K_5%_2 — R1029 *2.2K_5%_2 — R1030 *2.2K_5%_2

AP_I2C_AUDIO_SCL [24] / AP_I2C_AUDIO_SDA [24]

AP_I2C_CAM_SCL [26] / AP_I2C_CAM_SDA [26]

AP_I2C_TS_SCL [27] / AP_I2C_TS_SDA [27]

AP_I2C_EMR_SCL / AP_I2C_EMR_SDA — TP119 / TP118

AP_I2C_TRACKPAD_SCL_3V3 [25] / AP_I2C_TRACKPAD_SDA_3V3 [25]

AP_I2C_SUB_SCL [39] / AP_I2C_SUB_SDA [39]

EMR_INT_ODL — TP120

EN_PP3300_TOUCH_S0 [38]

TOUCH_RESET_L [27]

TOUCH_INT_ODL [27]

AP_I2C_SUB_INT_ODL [39]

GPPC_D_9_GSPI2_CLK_UART0A_TXD [13]

GPPC_D_8_GSPI2_CS0B_UART0A_RXD [13,17]

GPPC_D_11_GSPI2_MOSI_UART0A_CTSB [13]

GPPC_D_10_GSPI2_MISO_UART0A_RTSB [13]

EN_PP2800_CAMERA [38]

WCAM_RST_L [26] — UCAM_RST_L — TP113

EN_PP1200_CAMERA [38]

GP_C13_UART1_TXD [13] — AP_PEN_DET_ODL — AP_PEN_DET_ODL [10]

PEN_DET_ODL [29,39]

D32 SDM03U40-7

R117 100K_1%_2 — PP3300_A

EC_IN_RW_OD [21]

EC_AP_MKBP_INT_L [29]

GPPC_C_9_UART0_TXD [13]

GPPC_C_8_UART0_RXD [13]

AP_WP_OD [20]

GPPC_C_10_UART0_RTSB [13,17]

EMR_RESET_L — TP121

R46 100_1%_2 — CSI_RCOMP

MIPI_WCAM_D0P [26] / MIPI_WCAM_D0N [26] / MIPI_WCAM_D1P [26] / MIPI_WCAM_D1N [26]

MIPI_WCAM_CLKP [26] / MIPI_WCAM_CLKN [26]

MIPI_WCAM_D2P [26] / MIPI_WCAM_D2N [26] / MIPI_WCAM_D3P [26] / MIPI_WCAM_D3N [26]

Quanta Computer Inc.			
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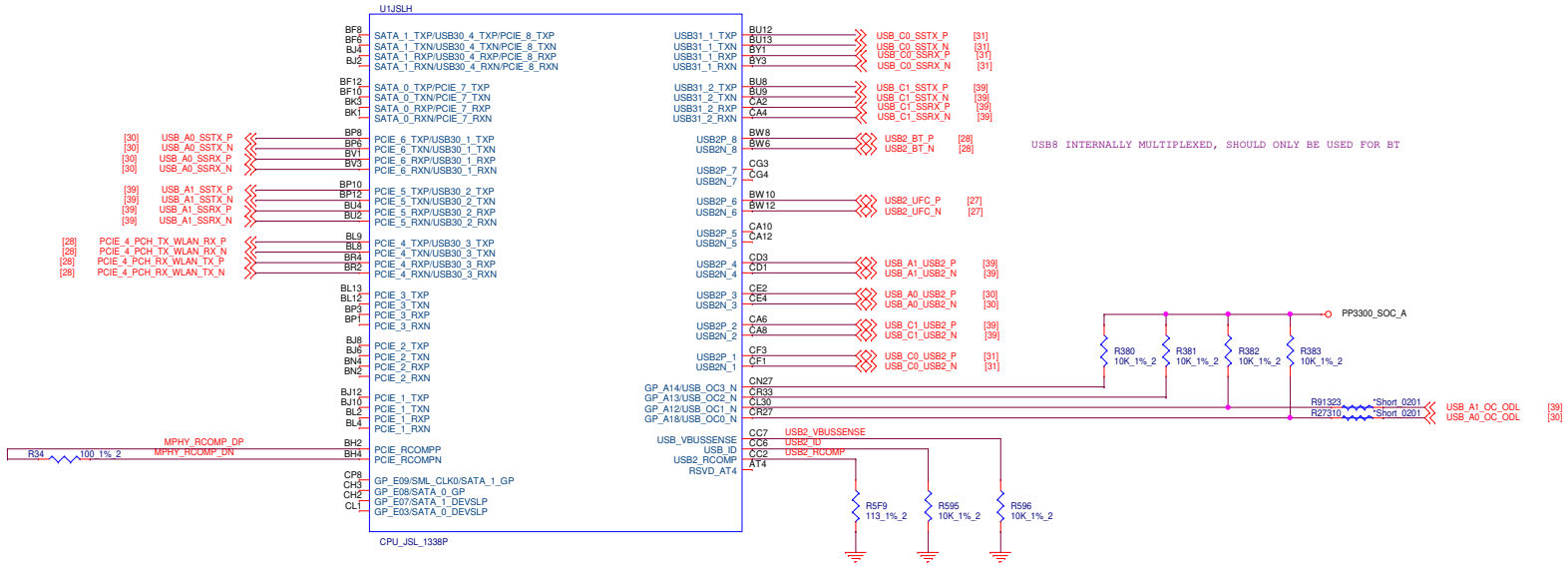

Quanta Computer Inc.		
PROJECT : Magolor		
Size	Document Number: JSL+: USB, PCIE, CNVI	Rev: 1A
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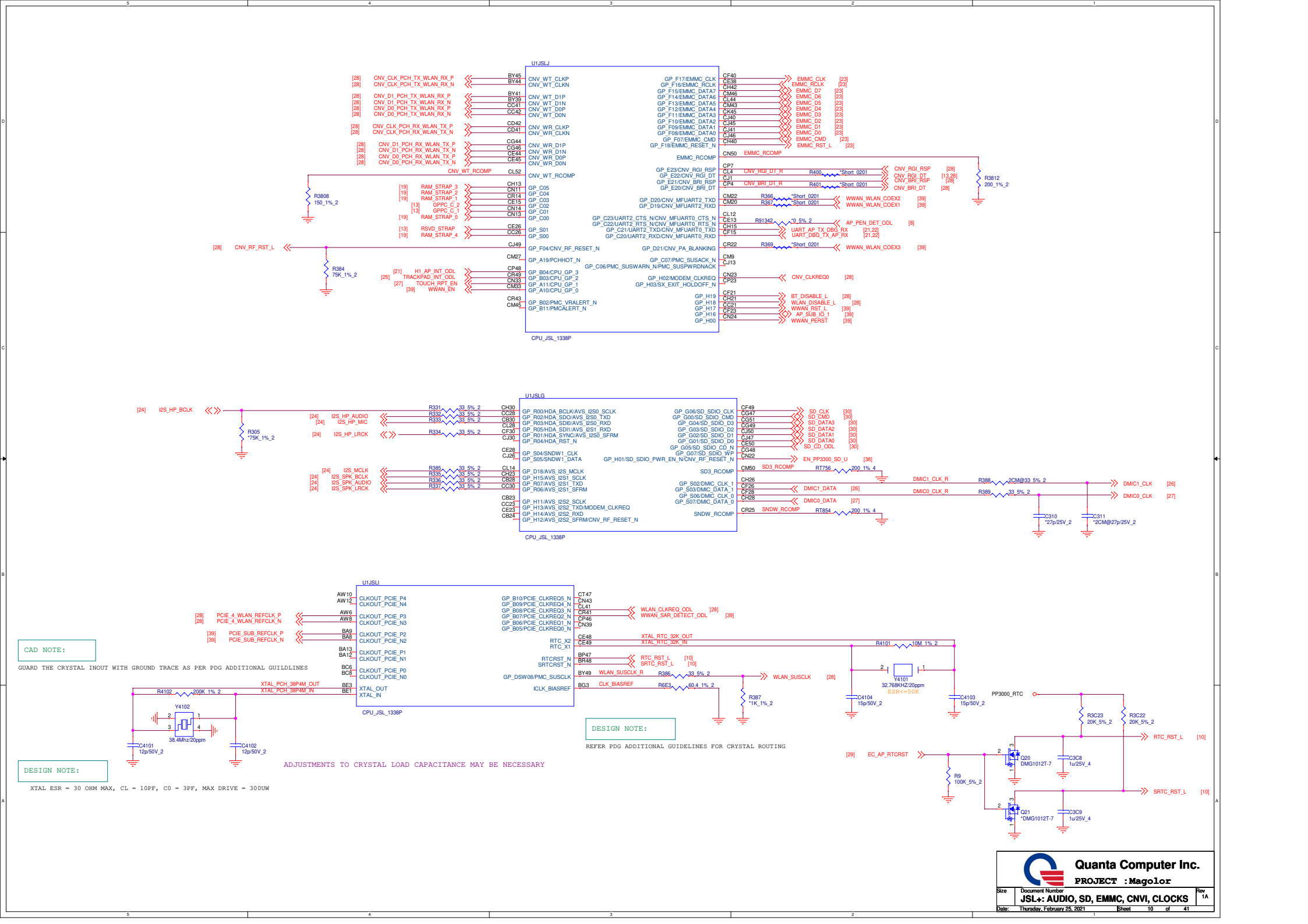
U1JSLJ
CPU_JSL_1338P
U1JSLG
CPU_JSL_1338P
U1JSLI
CPU_JSL_1338P
CAD NOTE:
GUARD THE CRYSTAL INOUT WITH GROUND TRACE AS PER PDG ADDITIONAL GUILDLINES
DESIGN NOTE:
XTAL ESR = 30 OHM MAX, CL = 10PF, C0 = 3PF, MAX DRIVE = 300UW
ADJUSTMENTS TO CRYSTAL LOAD CAPACITANCE MAY BE NECESSARY
DESIGN NOTE:
REFER PDG ADDITIONAL GUIDELINES FOR CRYSTAL ROUTING
Quanta Computer Inc.
PROJECT : Magolor
JSL+: AUDIO, SD, EMMC, CNVI, CLOCKS
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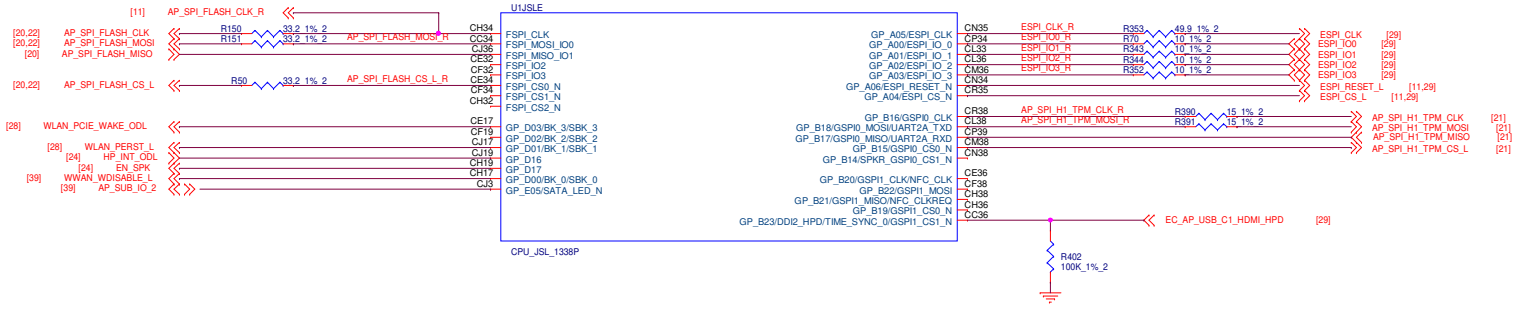
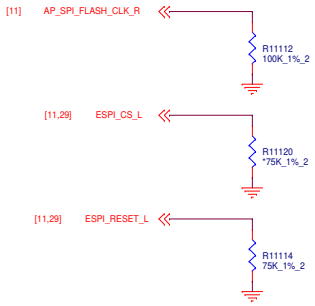


PCH GLITCH MITIGATION



Quanta Computer Inc.

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Size	Document Number	Rev
	JSL+: ESPI, SPI	1A

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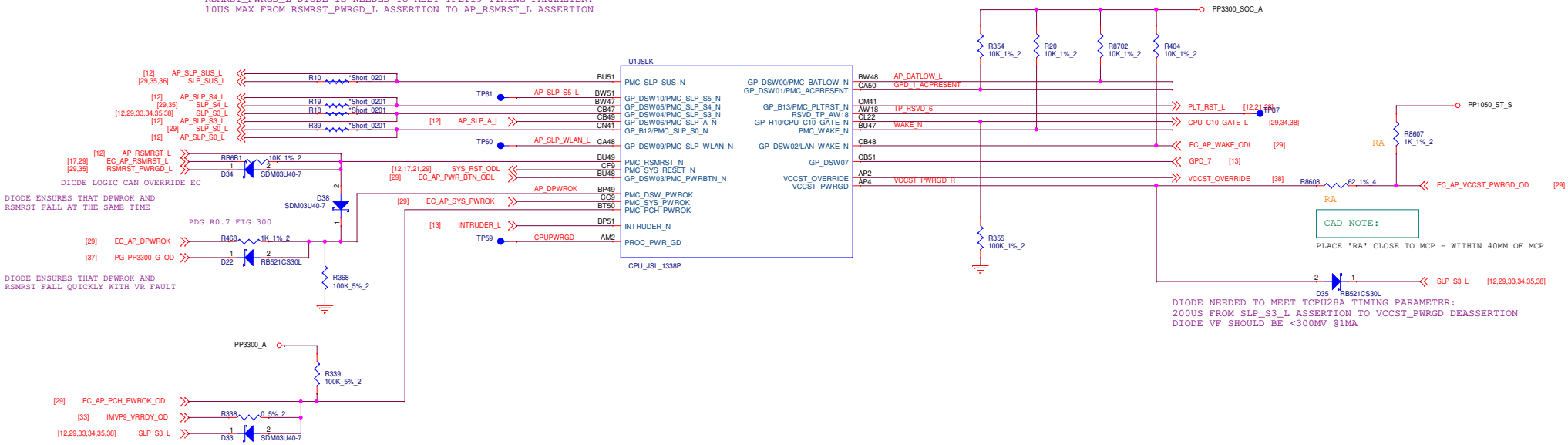
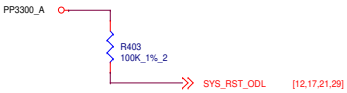
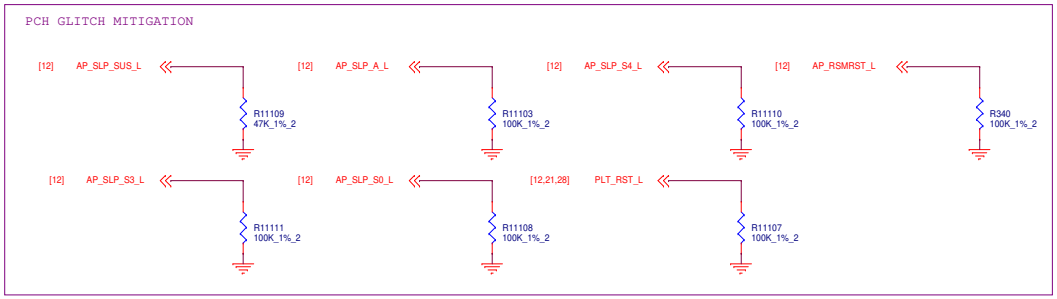
RSMRST_PWRGD_L DIODE IS NEEDED TO MEET TPLT19 TIMING PARAMETER:
10US MAX FROM RSMRST_PWRGD_L ASSERTION TO AP_RSMRST_L ASSERTION



DIODE NEEDED TO MEET TCPU28A TIMING PARAMETER:
200US FROM SLP_S3_L ASSERTION TO VCCST_PWRGD DEASSERTION
DIODE VF SHOULD BE <300MV @1MA

SEE FIGURE 280 OF PDG FOR PCH_PWROK LOGIC





Quanta Computer Inc.		
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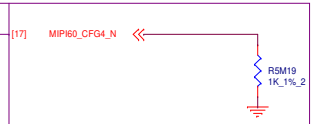
DISPLAY PORT PRESENCE STRAP

CFG4

0: ENABLED
AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

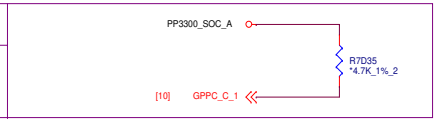
1: DISABLED; (DEFAULT)
NO PHYSICAL DISPLAY PORT ATTACHED TO THE EMBEDDED DISPLAY PORT



TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED

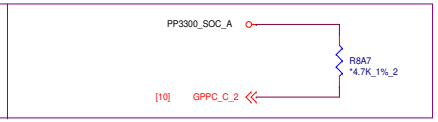
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED

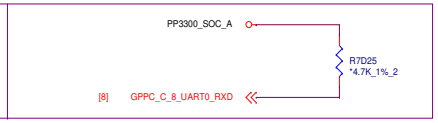
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



TLS CONFIDENTIALITY

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

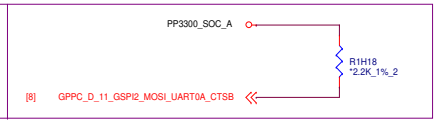
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB



MAF/SAF STRAP

LOW-> MAF ENABLE
HIGH-> SAF ENABLE

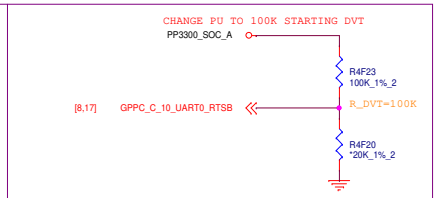
WEAK INTERNAL PD 20K



BOOT HALT

HIGH - DISABLED
LOW- ENABLED

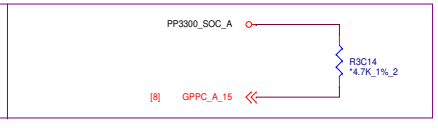
NO INTERNAL PU/PD
SAMPLING - RSMRSTB



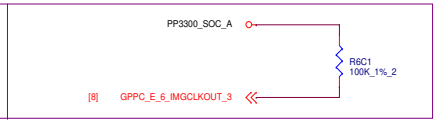
FLASH DESCRIPTOR SECURITY OVERRIDE

HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



???

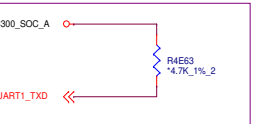


CPUNSSC CLOCK FREQ

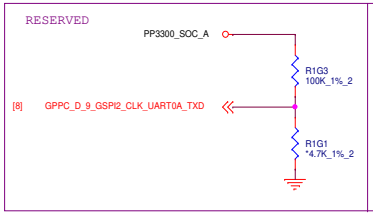
HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

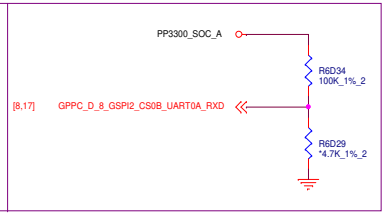
LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

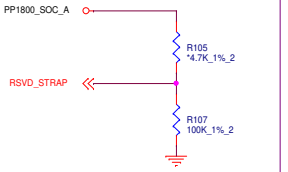


RESERVED





RESERVED FOR CHROMEOS

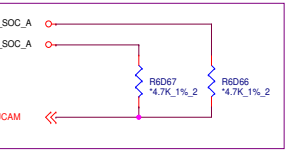


XTAL SEL1

LOW: 38.4/19.2MHZ (DEFAULT)
HIGH = 24MHZ

(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

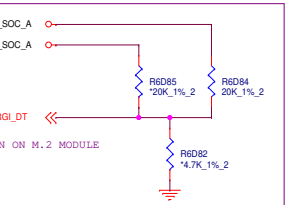
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB



M.2 CNVI MODES

LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE

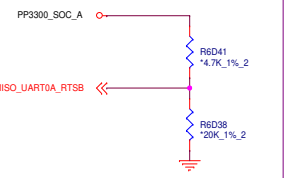
NO INTERNAL PU/PD
SAMPLING - RSMRSTB



RESERVED

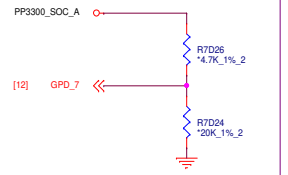
THIS STRAP HAS A 20K INTERNAL PULL-DOWN

DO NOT PULL THIS PIN HIGH ON BOARD



RESERVED

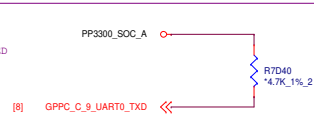
THIS STRAP HAS A 20K INTERNAL PULL-DOWN



ESPI OR EC LESS

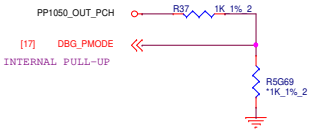
HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED

WEAK INTERNAL PD 20K



RESERVED

THIS STRAP HAS A 20K INTERNAL PULL-UP



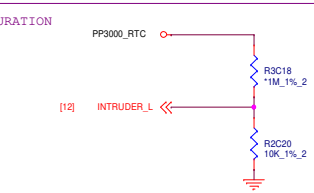
SPI VCCSIO CONFIGURATION

LOW: 3.3V

HIGH: 1.8V

NO INTERNAL PU/PD

SAMPLING - DSW_PWROK



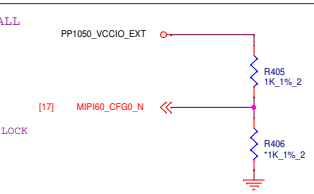
RESET SEQUENCE STALL

LOW: STALL

HIGH: NO STALL

INTERNAL PU(?)

STALLS AFTER PCU PLL LOCK UNTIL DEASSERTED

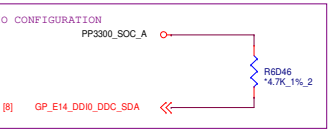


BSSB LSX #0 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

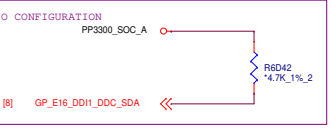


BSSB LSX #1 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

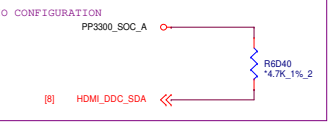


BSSB LSX #2 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

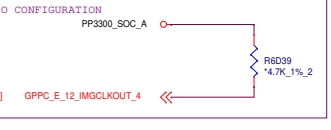


BSSB LSX #3 PINS VCCIO CONFIGURATION

HIGH: 3.3V

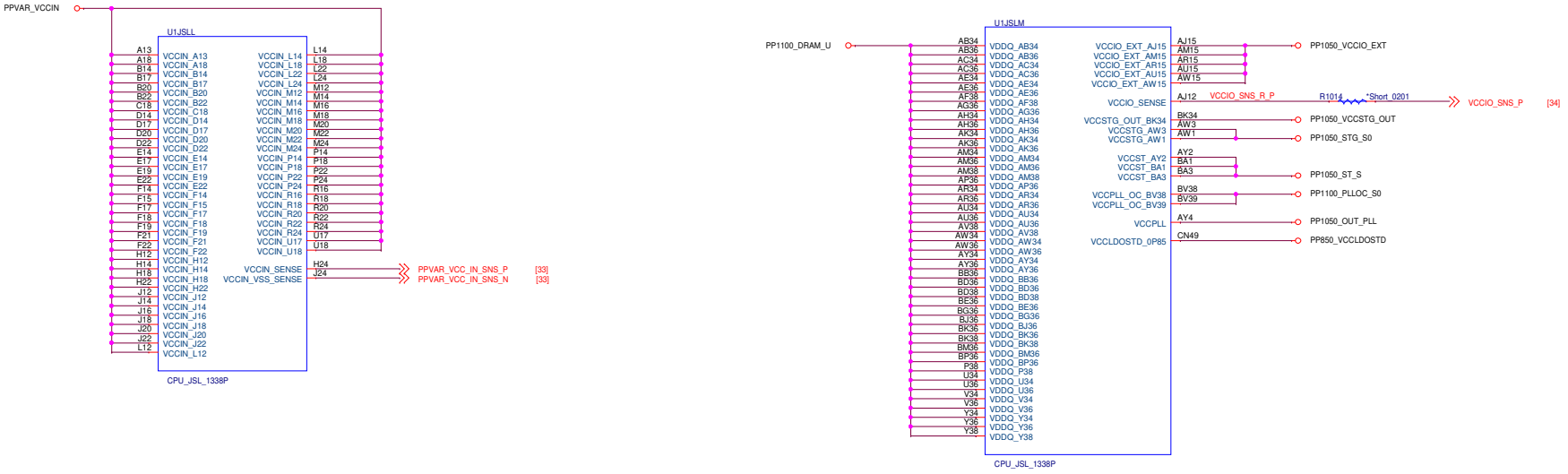
LOW: 1.8V

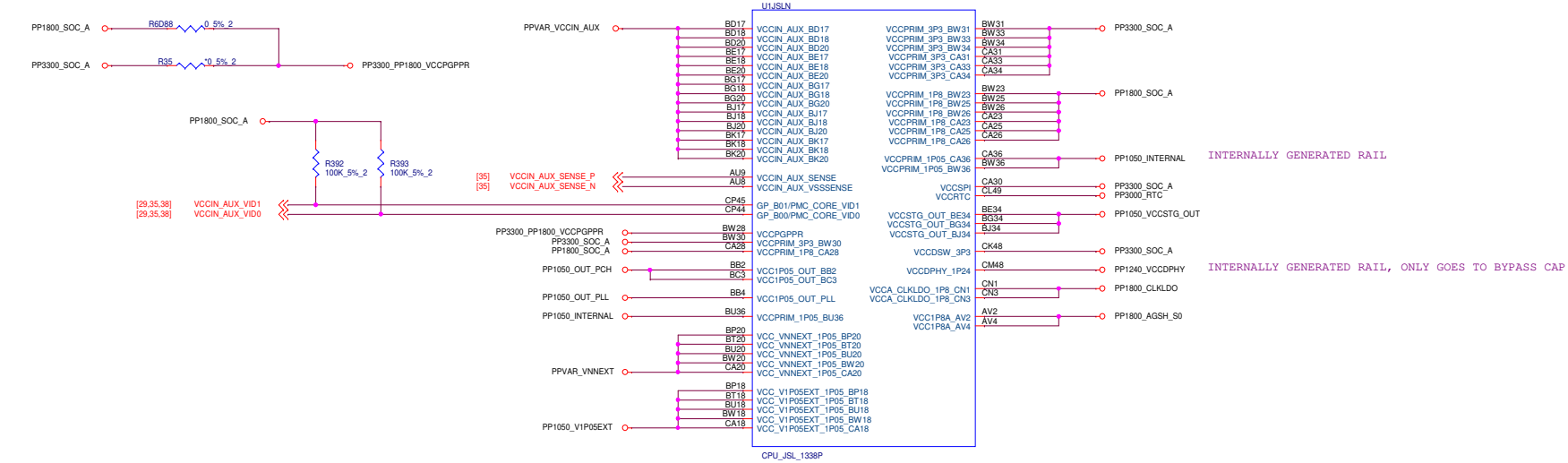
INTERNAL PD



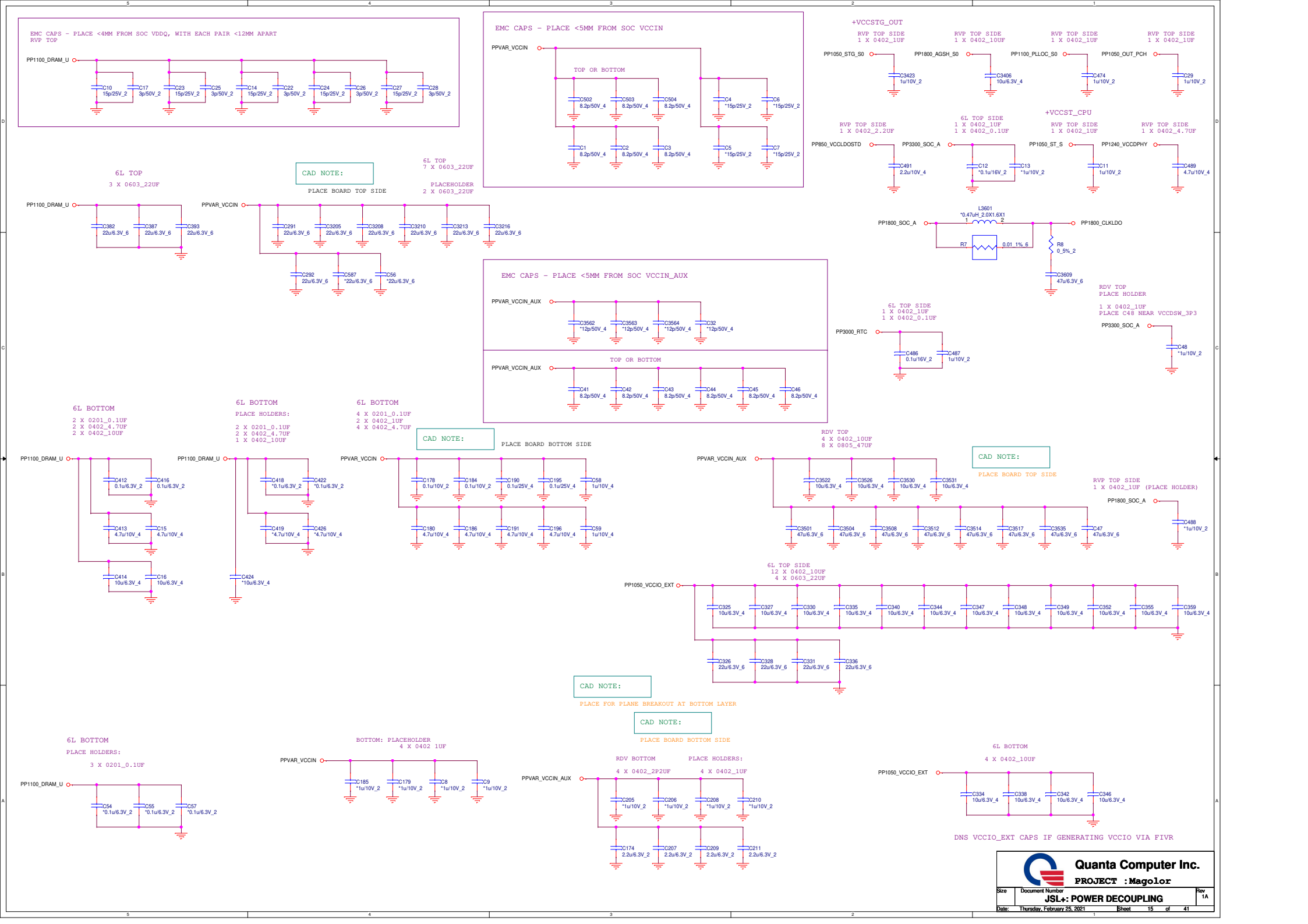
Quanta Computer Inc.
PROJECT : Magolor

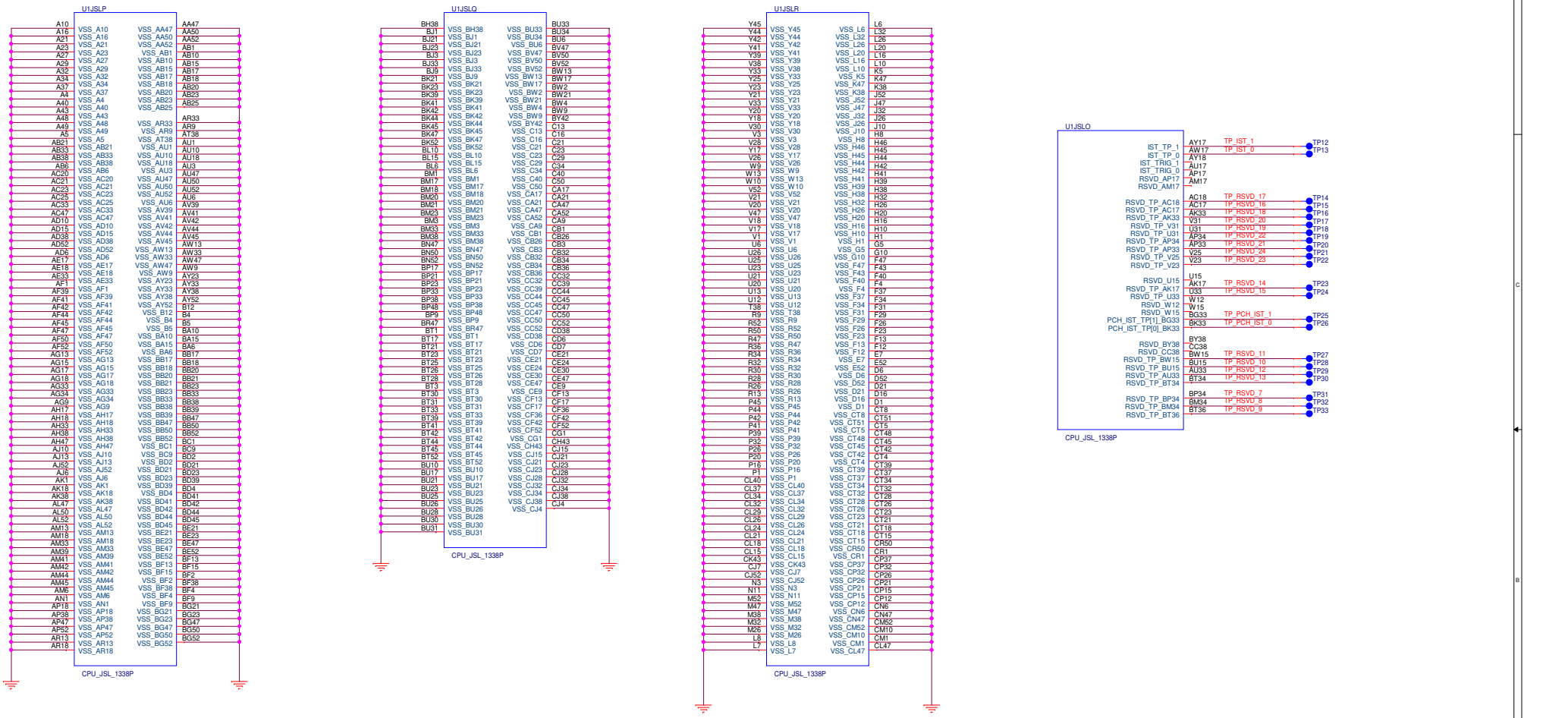
Size	Document Number	Rev
	JSL+: STRAPS	1A
Date: Thursday, February 25, 2021	Sheet 13 of 41	



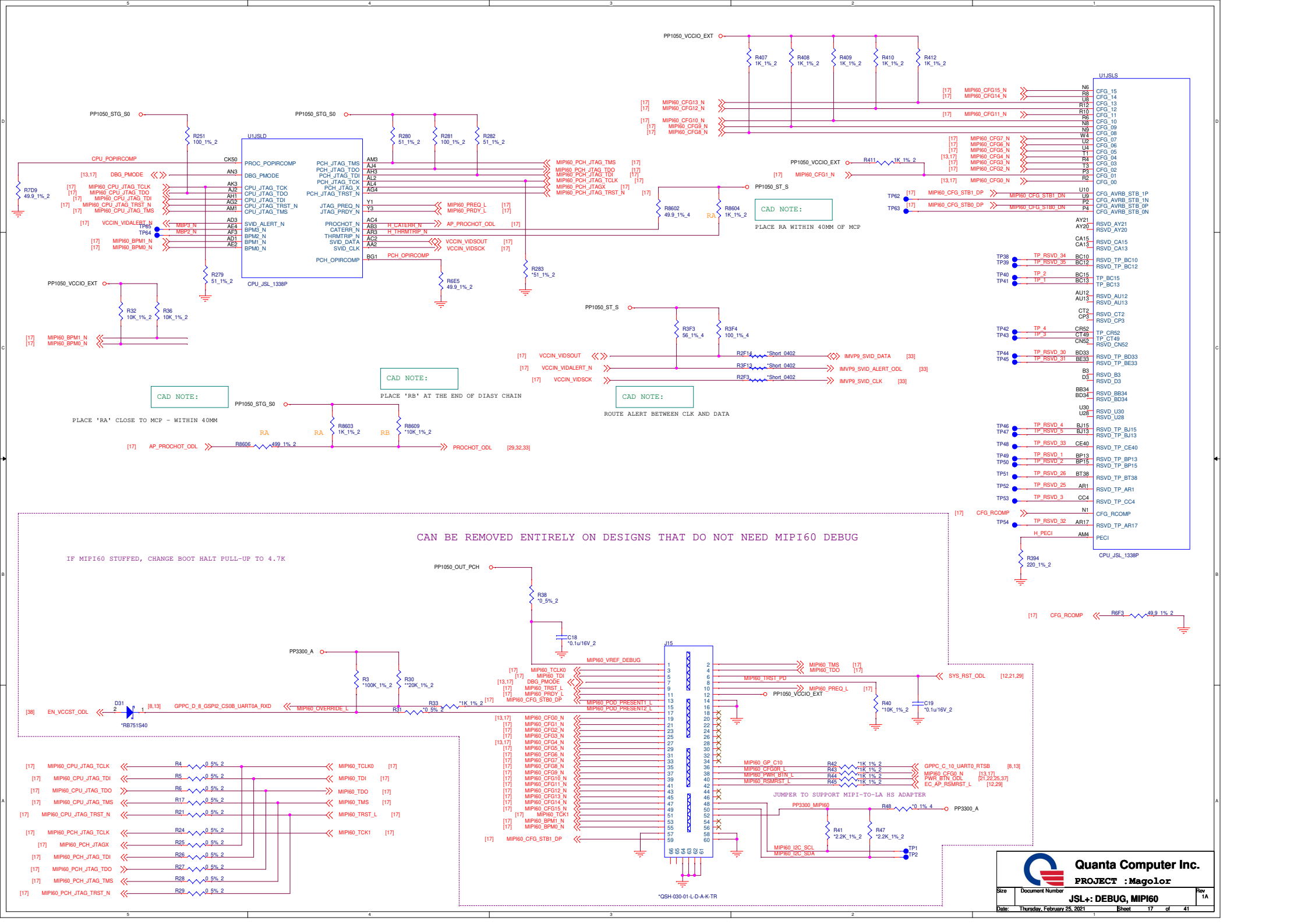


Quanta Computer Inc.		
PROJECT : Magolor		
Size	Document Number: JSL+: CPU AND PCH POWER	Rev: 1A
Date: Thursday, February 25, 2021	Sheet 14 of 41	


EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART
RVP TOP
PP1100_DRAM_U
C10 15p/25V_2
C17 3p/50V_2
C23 15p/25V_2
C25 3p/50V_2
C14 15p/25V_2
C22 3p/50V_2
C24 15p/25V_2
C26 3p/50V_2
C27 15p/25V_2
C28 3p/50V_2
EMC CAPS - PLACE <5MM FROM SOC VCCIN
PPVAR_VCCIN
TOP OR BOTTOM
C502 8.2p/50V_4
C503 8.2p/50V_4
C504 8.2p/50V_4
C4 *15p/25V_2
C6 *15p/25V_2
C1 8.2p/50V_4
C2 8.2p/50V_4
C3 8.2p/50V_4
C5 *15p/25V_2
C7 *15p/25V_2
+VCCSTG_OUT
RVP TOP SIDE
1 X 0402_1UF
RVP TOP SIDE
1 X 0402_10UF
RVP TOP SIDE
1 X 0402_1UF
RVP TOP SIDE
1 X 0402_1UF
PP1050_STG_S0
PP1800_AGSH_S0
PP1100_PLLOC_S0
PP1050_OUT_PCH
C3423 1u/10V_2
C3406 10u/6.3V_4
C474 1u/10V_2
C29 1u/10V_2
+VCCST_CPU
RVP TOP SIDE
1 X 0402_2.2UF
6L TOP SIDE
1 X 0402_1UF
1 X 0402_0.1UF
RVP TOP SIDE
1 X 0402_1UF
RVP TOP SIDE
1 X 0402_4.7UF
PP850_VCCLDOSTD
PP3300_SOC_A
PP1050_ST_S
PP1240_VCCDPHY
C491 2.2u/10V_4
C12 *0.1u/16V_2
C13 *1u/10V_2
C11 1u/10V_2
C489 4.7u/10V_4
6L TOP
3 X 0603_22UF
CAD NOTE:
PLACE BOARD TOP SIDE
6L TOP
7 X 0603_22UF
PLACEHOLDER
2 X 0603_22UF
PP1100_DRAM_U
PPVAR_VCCIN
C382 22u/6.3V_6
C387 22u/6.3V_6
C393 22u/6.3V_6
C291 22u/6.3V_6
C3205 22u/6.3V_6
C3208 22u/6.3V_6
C3210 22u/6.3V_6
C3213 22u/6.3V_6
C3216 22u/6.3V_6
C292 22u/6.3V_6
C587 *22u/6.3V_6
C56 *22u/6.3V_6
L3601
*0.47uH_2.0X1.6X1
PP1800_SOC_A
PP1800_CLKLDO
R7
0.01_1%_6
R8
0_5%_2
C3609
47u/6.3V_6
EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX
PPVAR_VCCIN_AUX
C3562 *12p/50V_4
C3563 *12p/50V_4
C3564 *12p/50V_4
C32 *12p/50V_4
TOP OR BOTTOM
C41 8.2p/50V_4
C42 8.2p/50V_4
C43 8.2p/50V_4
C44 8.2p/50V_4
C45 8.2p/50V_4
C46 8.2p/50V_4
6L TOP SIDE
1 X 0402_1UF
1 X 0402_0.1UF
PP3000_RTC
C486 0.1u/16V_2
C487 1u/10V_2
RDV TOP
PLACE HOLDER
1 X 0402_1UF
PLACE C48 NEAR VCCDSW_3P3
PP3300_SOC_A
C48 *1u/10V_2
6L BOTTOM
2 X 0201_0.1UF
2 X 0402_4.7UF
2 X 0402_10UF
6L BOTTOM
PLACE HOLDERS:
2 X 0201_0.1UF
2 X 0402_4.7UF
1 X 0402_10UF
6L BOTTOM
4 X 0201_0.1UF
2 X 0402_1UF
4 X 0402_4.7UF
CAD NOTE:
PLACE BOARD BOTTOM SIDE
RDV TOP
4 X 0402_10UF
8 X 0805_47UF
CAD NOTE:
PLACE BOARD TOP SIDE
RVP TOP SIDE
1 X 0402_1UF (PLACE HOLDER)
PP1100_DRAM_U
PPVAR_VCCIN
PPVAR_VCCIN_AUX
PP1800_SOC_A
C412 0.1u/6.3V_2
C416 0.1u/6.3V_2
C413 4.7u/10V_4
C15 4.7u/10V_4
C414 10u/6.3V_4
C16 10u/6.3V_4
C418 *0.1u/6.3V_2
C422 *0.1u/6.3V_2
C419 *4.7u/10V_4
C426 *4.7u/10V_4
C424 *10u/6.3V_4
C178 0.1u/10V_2
C184 0.1u/10V_2
C190 0.1u/25V_4
C195 0.1u/25V_4
C58 1u/10V_4
C180 4.7u/10V_4
C186 4.7u/10V_4
C191 4.7u/10V_4
C196 4.7u/10V_4
C59 1u/10V_4
C3522 10u/6.3V_4
C3526 10u/6.3V_4
C3530 10u/6.3V_4
C3531 10u/6.3V_4
C3501 47u/6.3V_6
C3504 47u/6.3V_6
C3508 47u/6.3V_6
C3512 47u/6.3V_6
C3514 47u/6.3V_6
C3517 47u/6.3V_6
C3535 47u/6.3V_6
C47 47u/6.3V_6
C488 *1u/10V_2
6L TOP SIDE
12 X 0402_10UF
4 X 0603_22UF
PP1050_VCCIO_EXT
C325 10u/6.3V_4
C327 10u/6.3V_4
C330 10u/6.3V_4
C335 10u/6.3V_4
C340 10u/6.3V_4
C344 10u/6.3V_4
C347 10u/6.3V_4
C348 10u/6.3V_4
C349 10u/6.3V_4
C352 10u/6.3V_4
C355 10u/6.3V_4
C359 10u/6.3V_4
C326 22u/6.3V_6
C328 22u/6.3V_6
C331 22u/6.3V_6
C336 22u/6.3V_6
CAD NOTE:
PLACE FOR PLANE BREAKOUT AT BOTTOM LAYER
CAD NOTE:
PLACE BOARD BOTTOM SIDE
6L BOTTOM
PLACE HOLDERS:
3 X 0201_0.1UF
PP1100_DRAM_U
C54 *0.1u/6.3V_2
C55 *0.1u/6.3V_2
C57 *0.1u/6.3V_2
BOTTOM: PLACEHOLDER
4 X 0402 1UF
PPVAR_VCCIN
C185 *1u/10V_2
C179 *1u/10V_2
C8 *1u/10V_2
C9 *1u/10V_2
RDV BOTTOM
4 X 0402_2P2UF
PLACE HOLDERS:
4 X 0402_1UF
PPVAR_VCCIN_AUX
C205 *1u/10V_2
C206 *1u/10V_2
C208 *1u/10V_2
C210 *1u/10V_2
C174 2.2u/6.3V_2
C207 2.2u/6.3V_2
C209 2.2u/6.3V_2
C211 2.2u/6.3V_2
6L BOTTOM
4 X 0402_10UF
PP1050_VCCIO_EXT
C334 10u/6.3V_4
C338 10u/6.3V_4
C342 10u/6.3V_4
C346 10u/6.3V_4
DNS VCCIO_EXT CAPS IF GENERATING VCCIO VIA FIVR
Quanta Computer Inc.
PROJECT : Magolor
Size
Document Number
JSL+: POWER DECOUPLING
Rev 1A
Date: Thursday, February 25, 2021
Sheet 15 of 41



Quanta Computer Inc.		
PROJECT : Magolor		
Size	Document Number: JSL+: GROUND, RESERVED	Rev: 1A
Date: Thursday, February 25, 2021	Sheet 16 of 41	


PP1050_VCCIO_EXT
R407 1K_1%_2
R408 1K_1%_2
R409 1K_1%_2
R410 1K_1%_2
R412 1K_1%_2
U1JSLS
CFG_15
CFG_14
CFG_13
CFG_12
CFG_11
CFG_10
CFG_09
CFG_08
CFG_07
CFG_06
CFG_05
CFG_04
CFG_03
CFG_02
CFG_01
CFG_00
CFG_AVRB_STB_1P
CFG_AVRB_STB_1N
CFG_AVRB_STB_0P
CFG_AVRB_STB_0N
CPU_JSL_1338P
PP1050_STG_S0
R251 100_1%_2
R280 51_1%_2
R281 100_1%_2
R282 51_1%_2
CPU_POPIRCOMP
DBG_PMODE
R7D9 49.9_1%_2
R279 51_1%_2
R283 *51_1%_2
R6E5 49.9_1%_2
PP1050_ST_S
R8602 49.9_1%_4
R8604 1K_1%_2
R411 1K_1%_2
PP1050_VCCIO_EXT
MIPI60_CFG1_N
CAD NOTE:
PLACE RA WITHIN 40MM OF MCP
TP62
TP63
MIPI60_CFG_STB1_DP
MIPI60_CFG_STB0_DP
MIPI60_CFG_STB1_DN
MIPI60_CFG_STB0_DN
R32 10K_1%_2
R36 10K_1%_2
R3F3 56_1%_4
R3F4 100_1%_4
VCCIN_VIDSOUT
VCCIN_VIDALERT_N
VCCIN_VIDSCK
*Short_0402
IMVP9_SVID_DATA
IMVP9_SVID_ALERT_ODL
IMVP9_SVID_CLK
CAD NOTE:
ROUTE ALERT BETWEEN CLK AND DATA
CAD NOTE:
PLACE 'RB' AT THE END OF DIASY CHAIN
CAD NOTE:
PLACE 'RA' CLOSE TO MCP - WITHIN 40MM
R8603 1K_1%_2
R8609 *10K_1%_2
R8606 499_1%_2
AP_PROCHOT_ODL
PROCHOT_ODL
CAN BE REMOVED ENTIRELY ON DESIGNS THAT DO NOT NEED MIPI60 DEBUG
IF MIPI60 STUFFED, CHANGE BOOT HALT PULL-UP TO 4.7K
PP1050_OUT_PCH
R38 *0_5%_2
C18 *0.1u/16V_2
PP3300_A
R3 *100K_1%_2
R30 **20K_1%_2
R33 *1K_1%_2
R31 *0_5%_2
D31
*RB751S40
EN_VCCST_ODL
GPPC_D_8_GSPI2_CS0B_UART0A_RXD
MIPI60_OVERRIDE_L
J15
MIPI60_VREF_DEBUG
MIPI60_TCLK0
MIPI60_TDI
DBG_PMODE
MIPI60_TRST_L
MIPI60_PRDY_L
MIPI60_CFG_STB0_DP
MIPI60_POD_PRESENT1_L
MIPI60_POD_PRESENT2_L
MIPI60_TMS
MIPI60_TDO
MIPI60_TRST_PD
MIPI60_PREQ_L
SYS_RST_ODL
R40 *10K_1%_2
C19 *0.1u/16V_2
MIPI60_GP_C10
MIPI60_CFG0R_L
MIPI60_PWR_BTN_L
MIPI60_RSMRST_L
GPPC_C_10_UART0_RTSB
PWR_BTN_ODL
EC_AP_RSMRST_L
JUMPER TO SUPPORT MIPI-TO-LA HS ADAPTER
PP3300_MIPI60
R48 *0_1%_4
PP3300_A
R41 *2.2K_1%_2
R47 *2.2K_1%_2
MIPI60_I2C_SCL
MIPI60_I2C_SDA
TP1
TP2
*QSH-030-01-L-D-A-K-TR
R4 0_5%_2
R5 0_5%_2
R6 0_5%_2
R17 0_5%_2
R21 0_5%_2
R24 0_5%_2
R25 0_5%_2
R26 0_5%_2
R27 0_5%_2
R28 0_5%_2
R29 0_5%_2
MIPI60_CPU_JTAG_TCLK
MIPI60_CPU_JTAG_TDI
MIPI60_CPU_JTAG_TDO
MIPI60_CPU_JTAG_TMS
MIPI60_CPU_JTAG_TRST_N
MIPI60_PCH_JTAG_TCLK
MIPI60_PCH_JTAGX
MIPI60_PCH_JTAG_TDI
MIPI60_PCH_JTAG_TDO
MIPI60_PCH_JTAG_TMS
MIPI60_PCH_JTAG_TRST_N
MIPI60_TCLK0
MIPI60_TDI
MIPI60_TDO
MIPI60_TMS
MIPI60_TRST_L
MIPI60_TCK1
R394 220_1%_2
CFG_RCOMP
R6F3 49.9_1%_2
Quanta Computer Inc.
PROJECT : Magolor
JSL+: DEBUG, MIPI60
Size
Document Number
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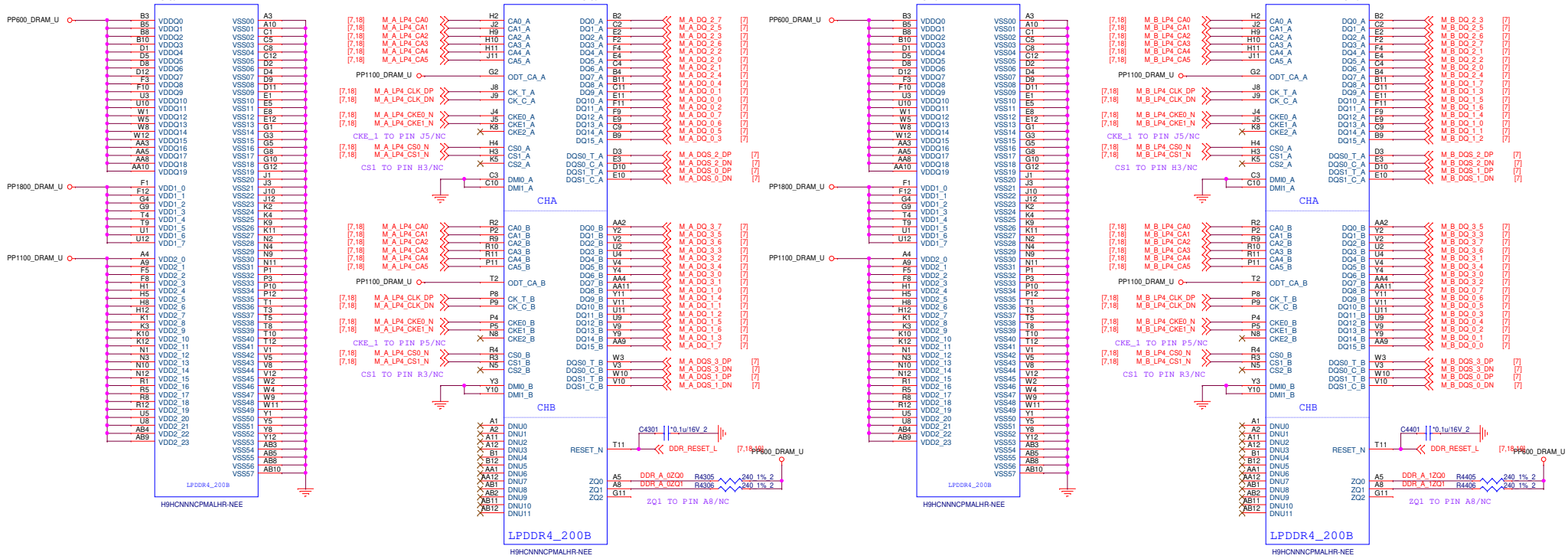
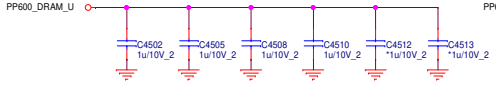
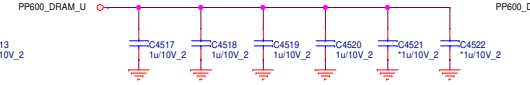
LPDDR4X 2933, 2GIB/PART

BIT SWAPPING IS ALLOWED WITHIN EACH BYTE

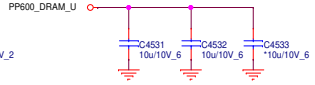


CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM

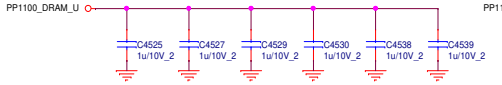


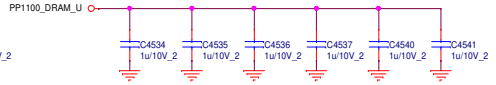


CAD NOTE: DISTRIBUTE EVENLY, 1 FOR EACH DRAM

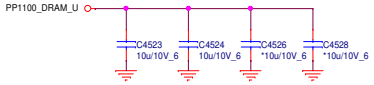


CAD NOTE: DISTRIBUTE EVENLY, 6 FOR EACH DRAM

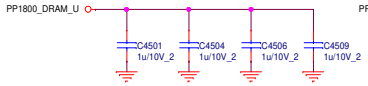




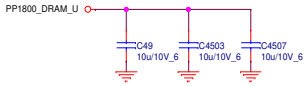
CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM

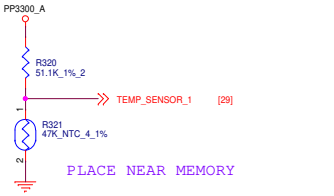


CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM

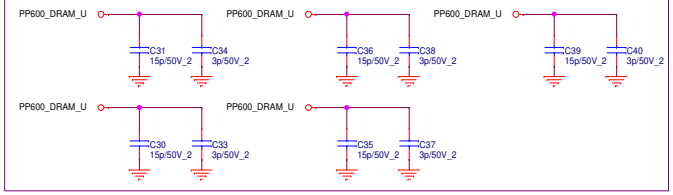


CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM





EMC CAPS - PLACE <4MM FROM MEMORY VDDQ, WITH EACH PAIR <12MM APART



Quanta Computer Inc.

PROJECT : Magolor

Size	Document Number	Rev
	LPDDR4X: CH A+B	1A

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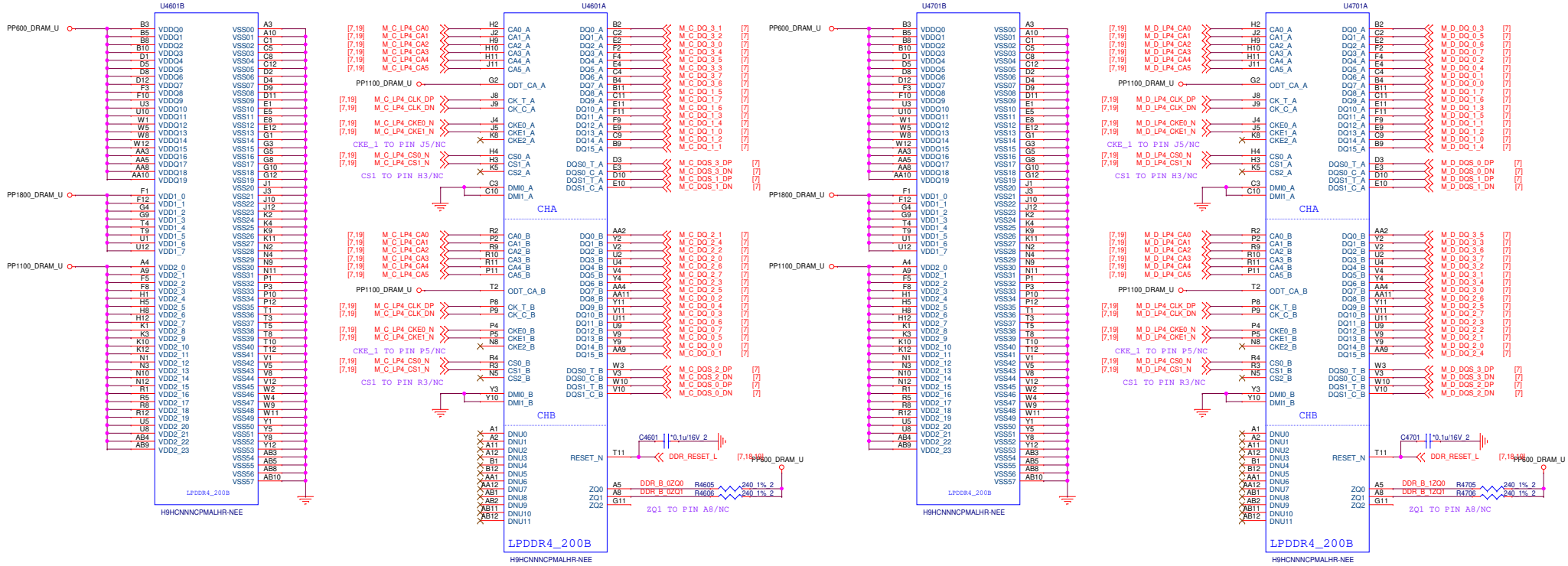
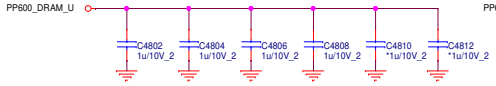
LPDDR4X 2933, 2GIB/PART

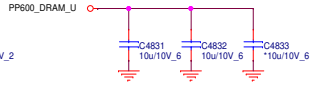
BIT SWAPPING IS ALLOWED WITHIN EACH BYTE

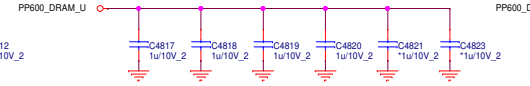


CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM

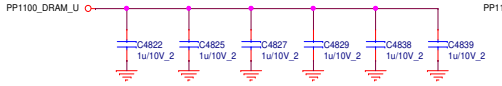


CAD NOTE: DISTRIBUTE EVENLY, 1 FOR EACH DRAM

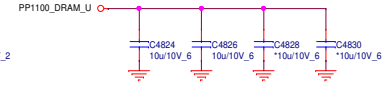


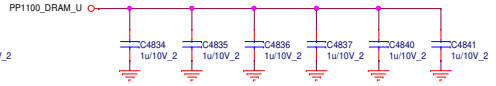


CAD NOTE: DISTRIBUTE EVENLY, 6 FOR EACH DRAM

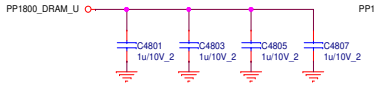


CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM

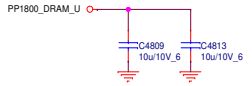




CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM

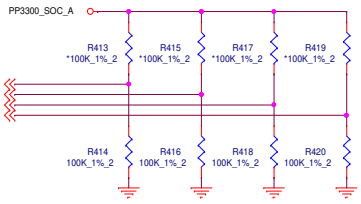


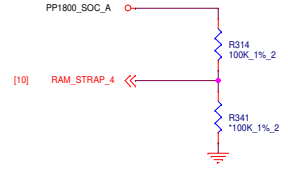
CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM



STRAPS				MPN
3	2	1	0	
0	0	0	0	MT53E512M32D2NP-046 WT:E,K4U6E3S4AA-MGCR,H9HCNNNBKMMLXR-NEE
0	0	0	1	MT53E1G32D2NP-046 WT:A
0	0	1	0	K4UBE3D4AA-MGCR
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

RAM_STRAP_4: 0=SINGLE-CHANNEL, 1=DUAL-CHANNEL





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PROJECT : Magolor

Size	Document Number	Rev
	LPDDR4X: CH C+D	1A

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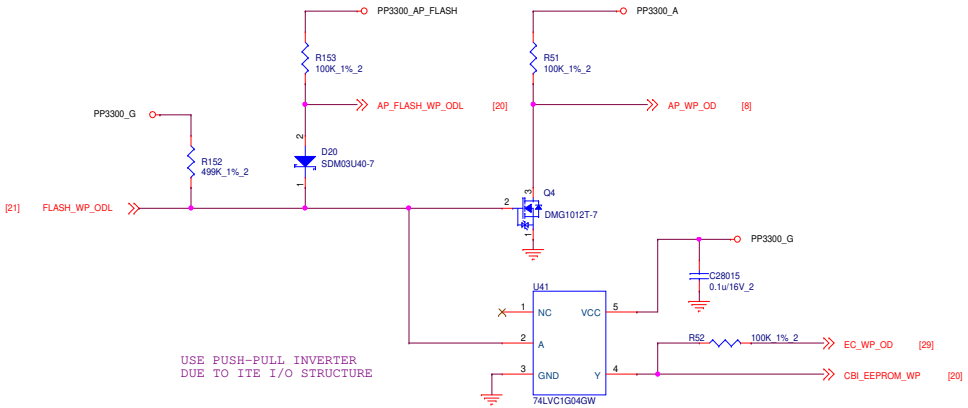
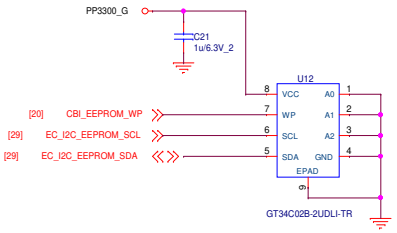
WP TREE

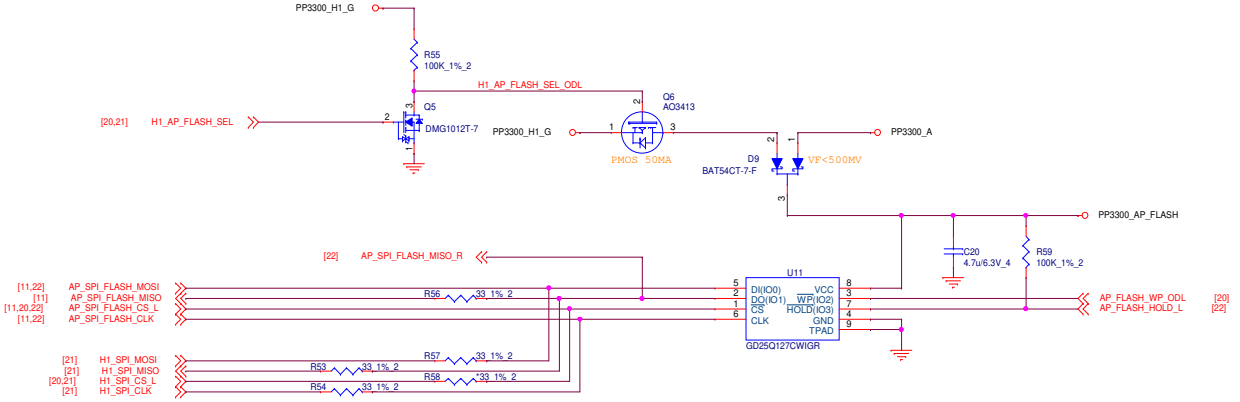


USE PUSH-PULL INVERTER
DUE TO ITE I/O STRUCTURE

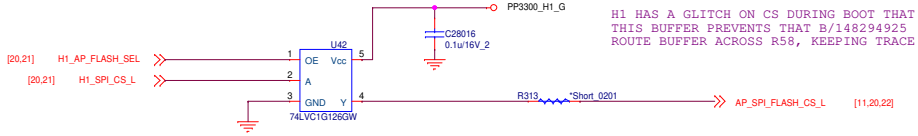
CBI EEPROM



SPI ROM



KEEP STUBS TO H1 SHORT



H1 HAS A GLITCH ON CS DURING BOOT THAT CAUSES LEAKAGE INTO THE PCH
THIS BUFFER PREVENTS THAT B/148294925
ROUTE BUFFER ACROSS R58, KEEPING TRACE LENGTH AS SHORT AS POSSIBLE

Quanta Computer Inc.
PROJECT : Magolor

Size	Document Number	Rev
	WP, CBI EEPROM, SPI ROM	1A

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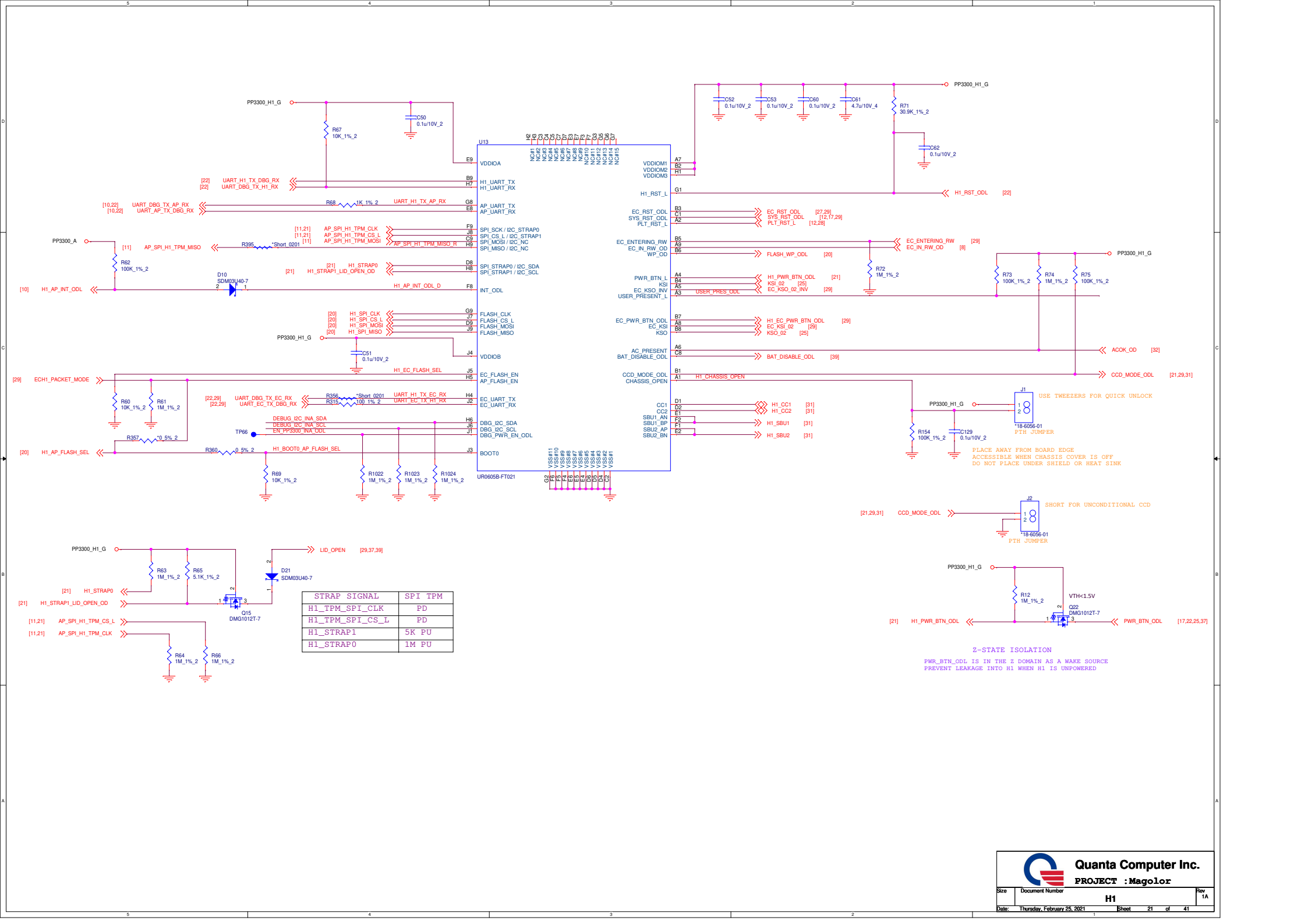

STRAP SIGNAL	SPI TPM
H1_TPM_SPI_CLK	PD
H1_TPM_SPI_CS_L	PD
H1_STRAP1	5K PU
H1_STRAP0	1M PU

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PROJECT : Magolor

Size	Document Number	Rev
	H1	1A

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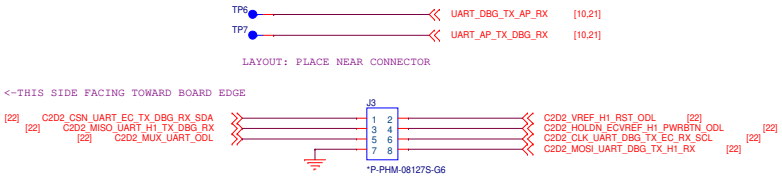
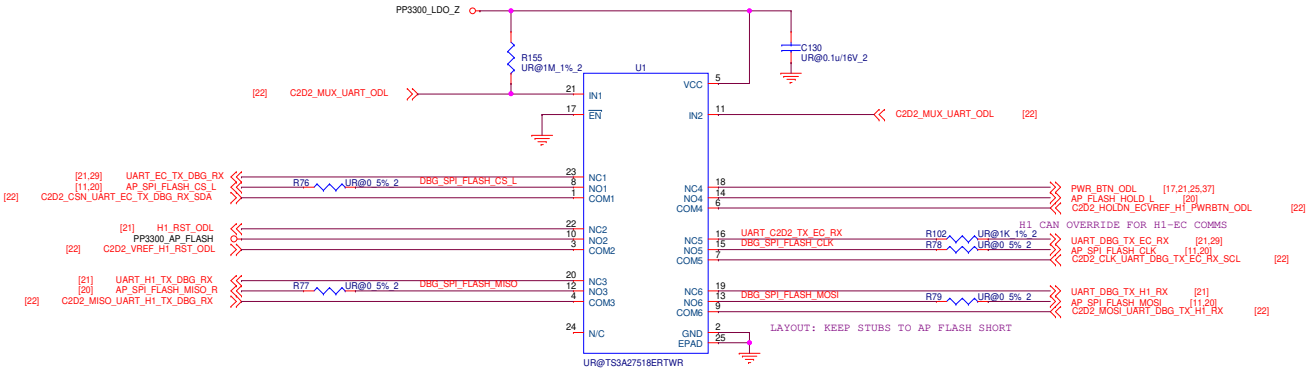
DNS ENTIRE PAGE IN DVT/PVT (EXCEPT LAB UNITS)



IF SHROUDED CONNECTOR IS UNAVAILABLE, USE UNSHROUDED FTSH-104-01-F-DV (OR EQUIV) WITH KEY MARKING IN SILK
PLACEMENT: PLACE NEAR MUX, SPI FLASH, AND H1 TO KEEP SPI TRACES AS SHORT AS POSSIBLE. CAN BE PLACED IN CENTER OF BOARD



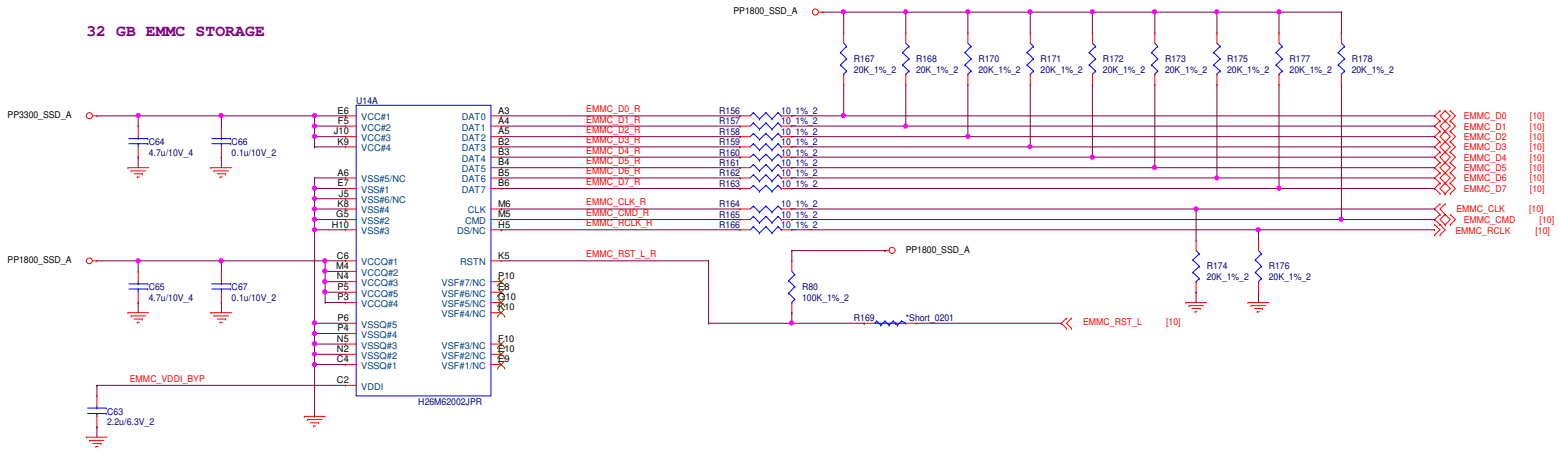
FOR SYSTEMS WITH I2C-FLASHED ECS, WHERE H1_VDDIOA=H1_VDDIOB=3.3V

SYSTEMS WITH SPI- OR UART-FLASHED ECS DO NOT REQUIRE THE EXTRA MUXING BASED ON H1_EC_FLASH_SEL

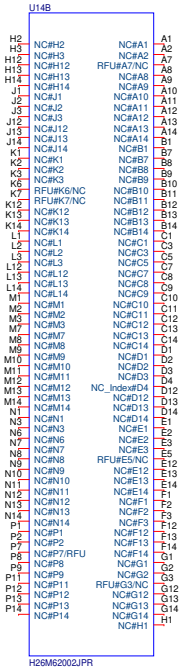
SYSTEMS WITH H1_VDDIOA!=3.3V NEED LEVEL SHIFTING ON H1_RST_ODL

SYSTEMS WITH H1_VDDIOB!=3.3V NEED LEVEL SHIFTING ON PWR_BTN_ODL

32 GB EMMC STORAGE



NOTE MOST EMMC 5.1 PART REQUIRES > 1 UF ON VDDI



NC/RFU/VSF LEAVE FLOATING

Quanta Computer Inc.		
PROJECT : Magolor		
Size	Document Number: STORAGE: EMMC	Rev 1A
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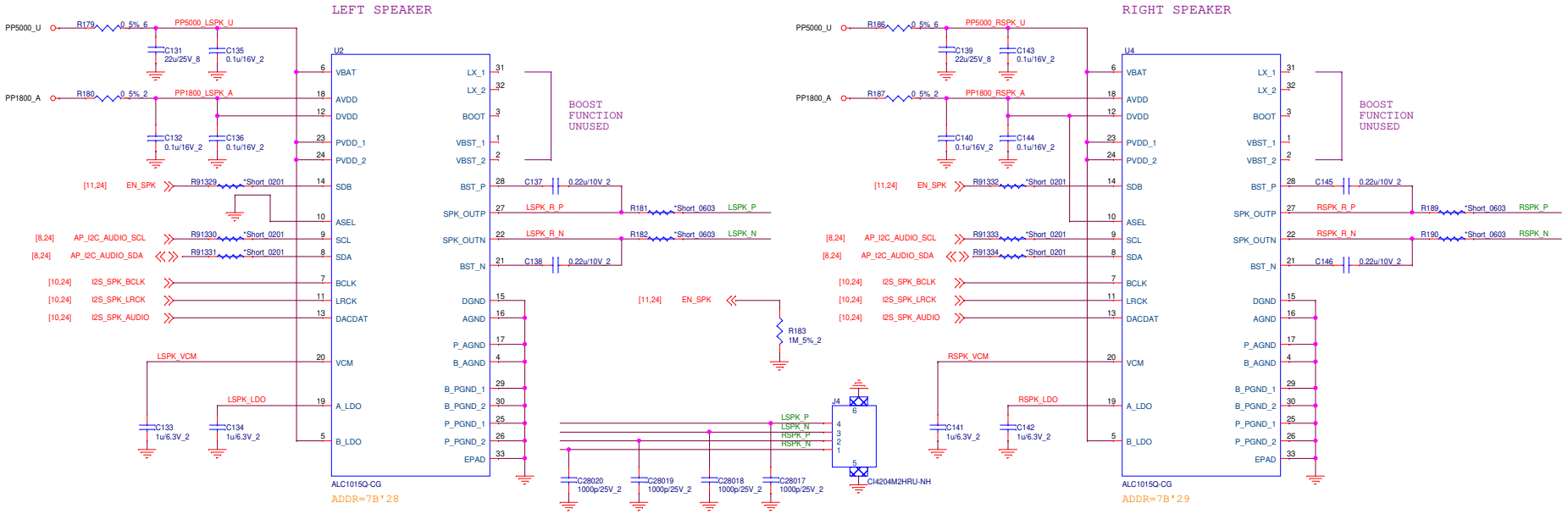

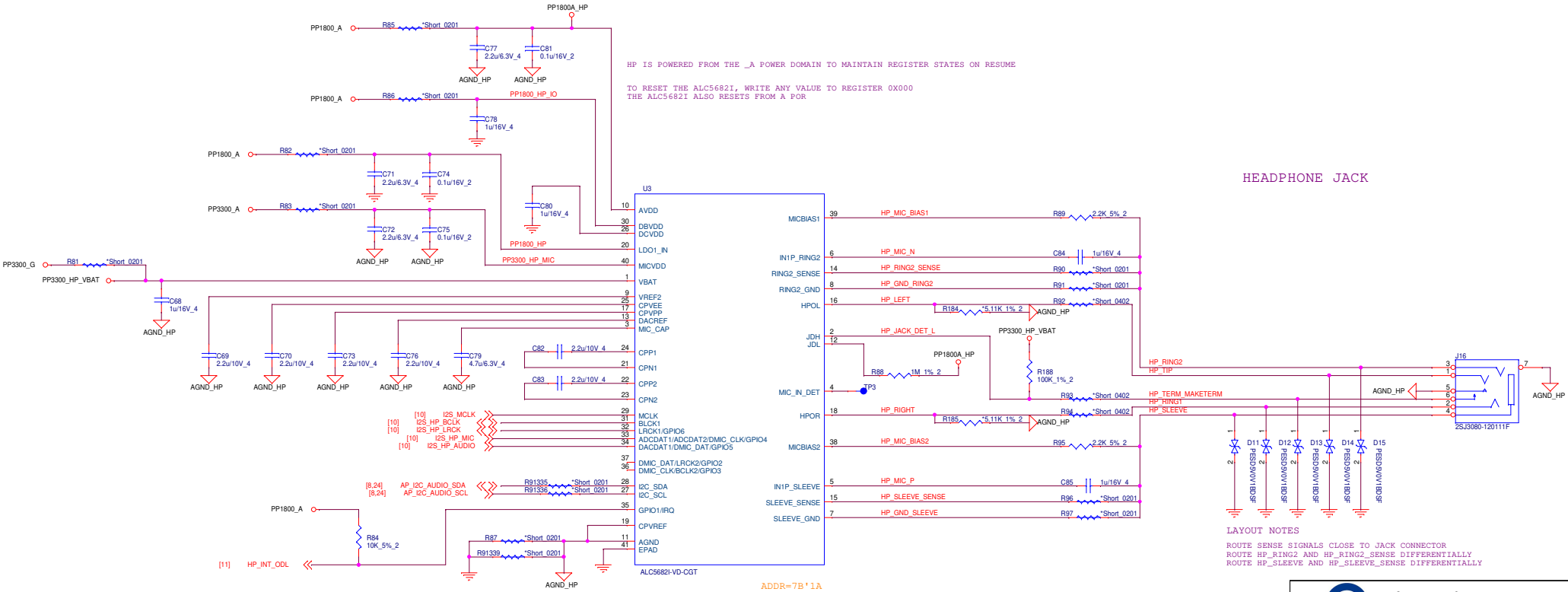

Quanta Computer Inc.

PROJECT : Magolor

Size	Document Number	Rev
	AUDIO	1A
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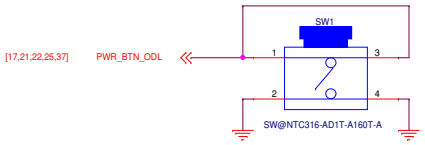
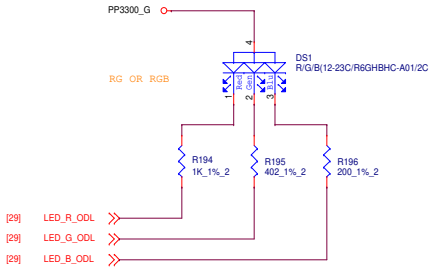
BUTTONS (IF ON MLB)

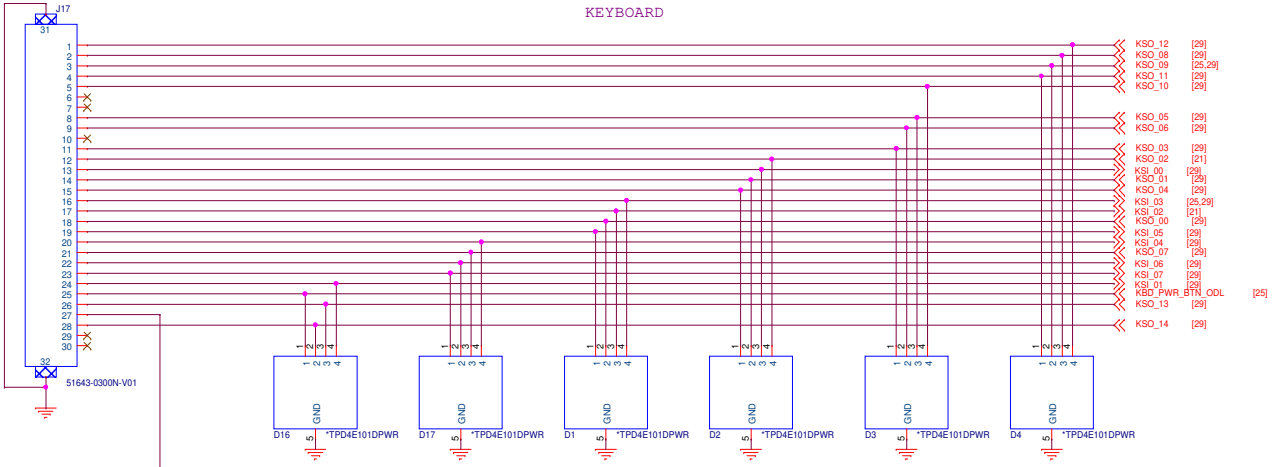


LEDS

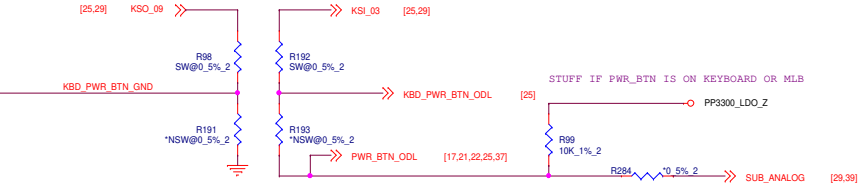
ADJUST RESISTORS TO MATCH SELECTED LED



KEYBOARD



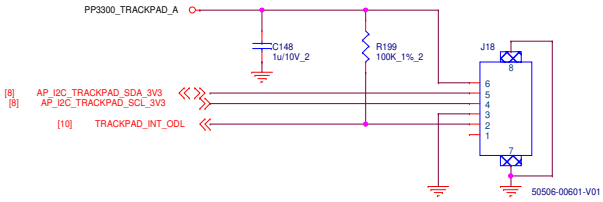
STUFF THESE FOR KEYBOARD LOCK BUTTON (CONVERTIBLES)



STUFF THESE FOR KEYBOARD POWER BUTTON

PWR BTN	R98	R192	R191	R193	R99	R284
ON KBD	DNS	DNS	0R	0R	10K	DNS
ON MLB	0R	0R	DNS	DNS	10K	DNS
SUB_ANA	0R	0R	DNS	DNS	DNS	0R
SUB_DIG	0R	0R	DNS	DNS	10K	DNS

TRACKPAD



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PROJECT : Magolor

Size	Document Number	Rev
	KB,BTNS,LEDS,TRACKPAD	1A

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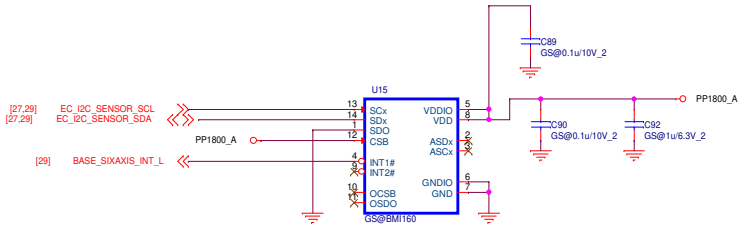
SIXAXIS

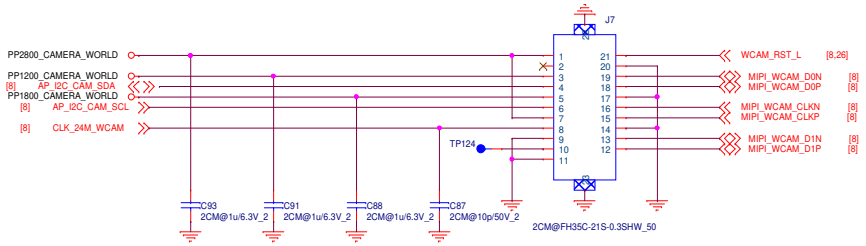


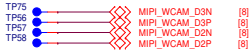
PLACE AS CLOSE TO WCAM AS POSSIBLE

WORLD-FACING CAMERA

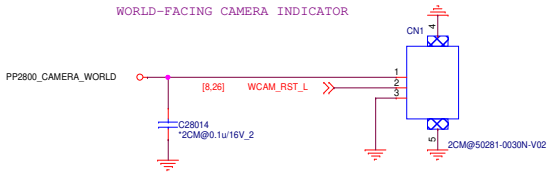
ADDRESS = 0X??

PLACEHOLDER/CONNECTOR DOESN'T MATCH ANYTHING

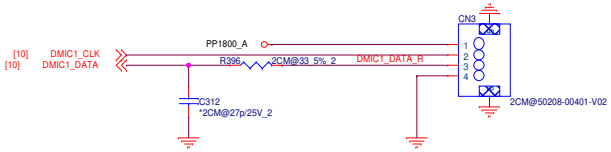




WORLD-FACING CAMERA INDICATOR



TO WORLD-FACING MIC MODULE



Quanta Computer Inc.

PROJECT : Magolor

Size	Document Number	Rev
	SENSORS	1A
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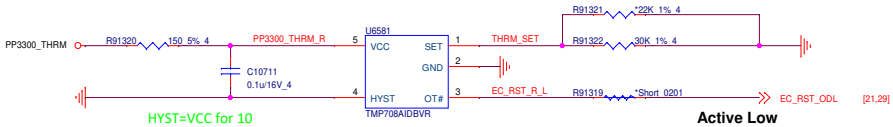
Thermal Protector

[OEM] BOM option

Rset(Kohm)=0.0012T*T-0.9308T+96.147



HYST=VCC for 10 degree Hys.
HYST=GND for 30 degree Hys.

Active Low

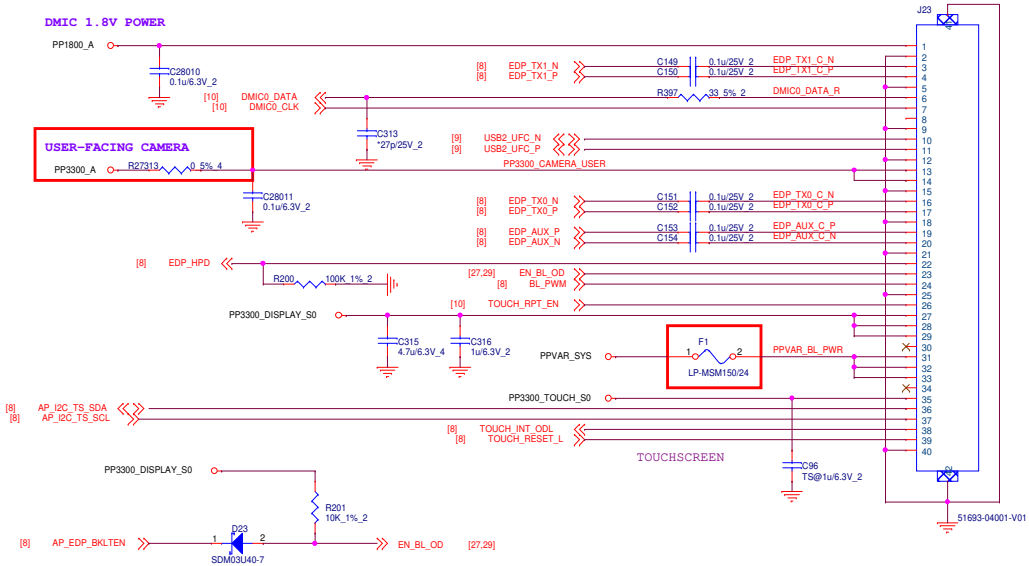
DISPLAY CONNECTOR GO HERE

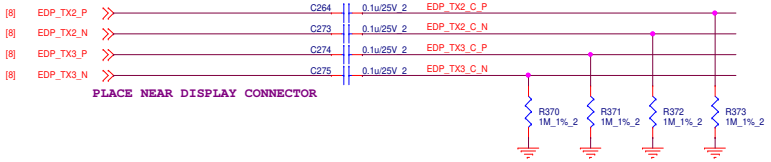
PLACEHOLDER CONNECTOR

DMIC 1.8V POWER

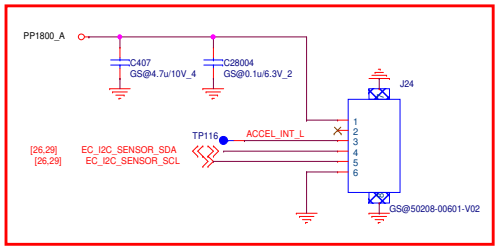
USER-FACING CAMERA

TOUCHSCREEN





PLACE NEAR DISPLAY CONNECTOR



Quanta Computer Inc.

PROJECT : Magolor

Size	Document Number	Rev
	LID: DISPLAY, CAMERA, SENSORS	1A

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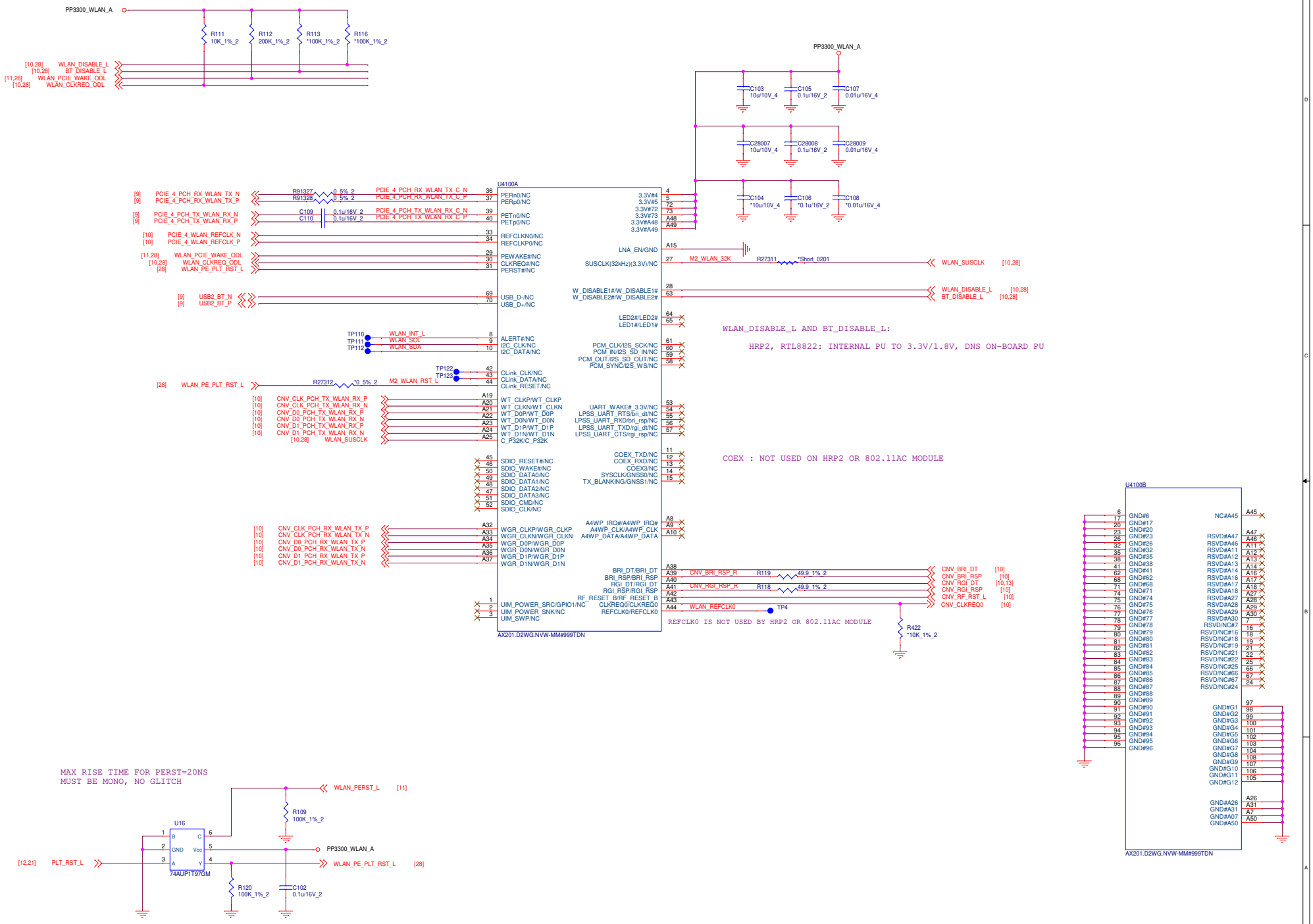

Quanta Computer Inc.			
PROJECT : Magolor			
Size	Document Number		Rev
	WIFI, BT		1A
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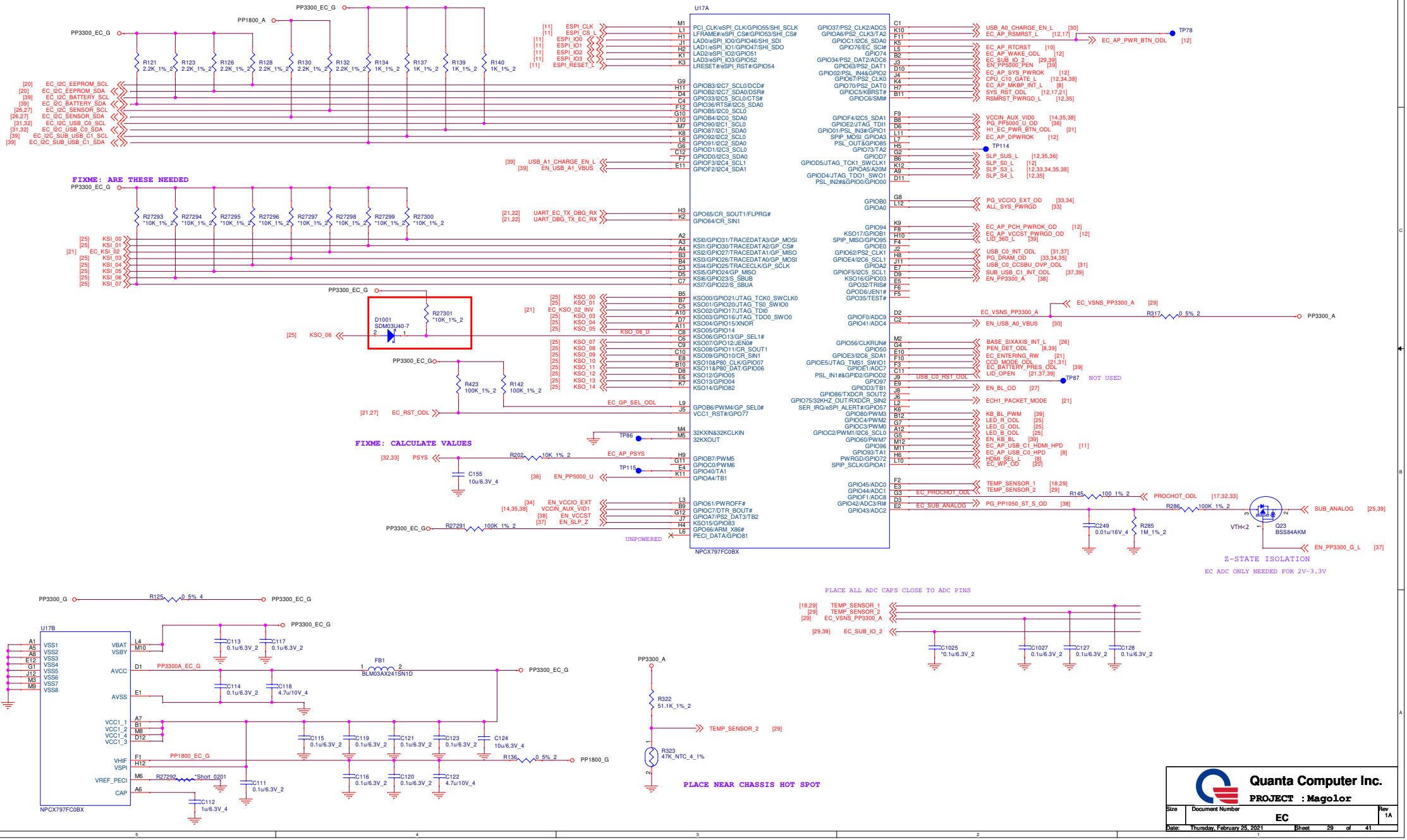
U17A
NPCX797FC0BX
FIXME: ARE THESE NEEDED
FIXME: CALCULATE VALUES
UNPOWERED
TP78
TP114
TP86
TP115
TP87
NOT USED
Z-STATE ISOLATION
EC ADC ONLY NEEDED FOR 2V-3.3V
PLACE ALL ADC CAPS CLOSE TO ADC PINS
PLACE NEAR CHASSIS HOT SPOT
U17B
NPCX797FC0BX
Quanta Computer Inc.
PROJECT : Magolor
Size
Document Number
EC
Rev
1A
Date: Thursday, February 25, 2021
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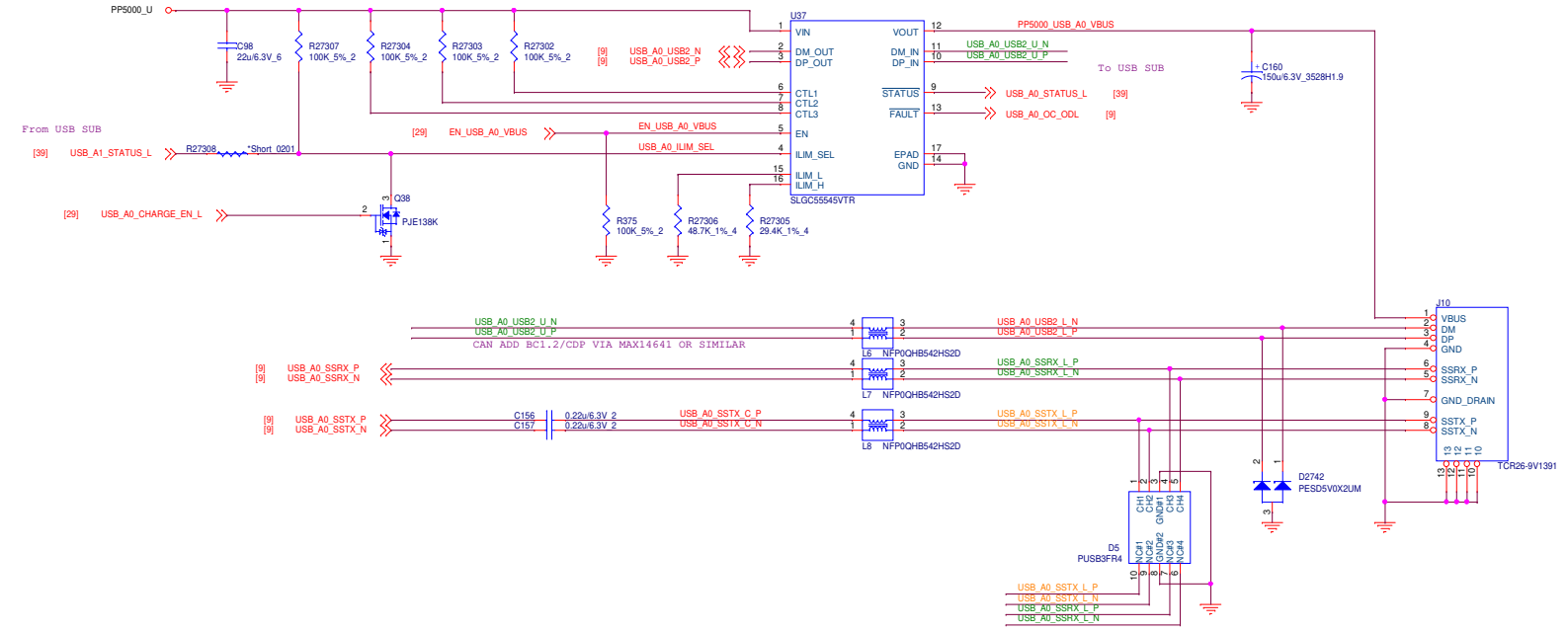

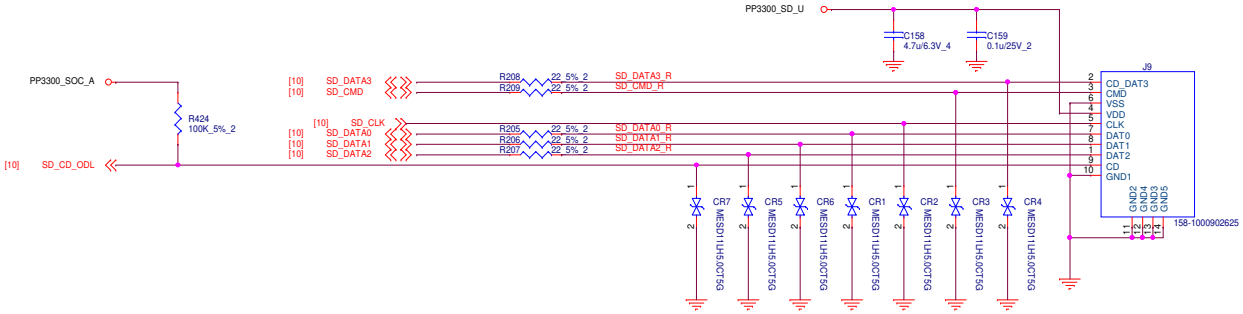

Quanta Computer Inc.		
PROJECT : Magolor		
Size	Document Number: USB-A, SD	Rev: 1A
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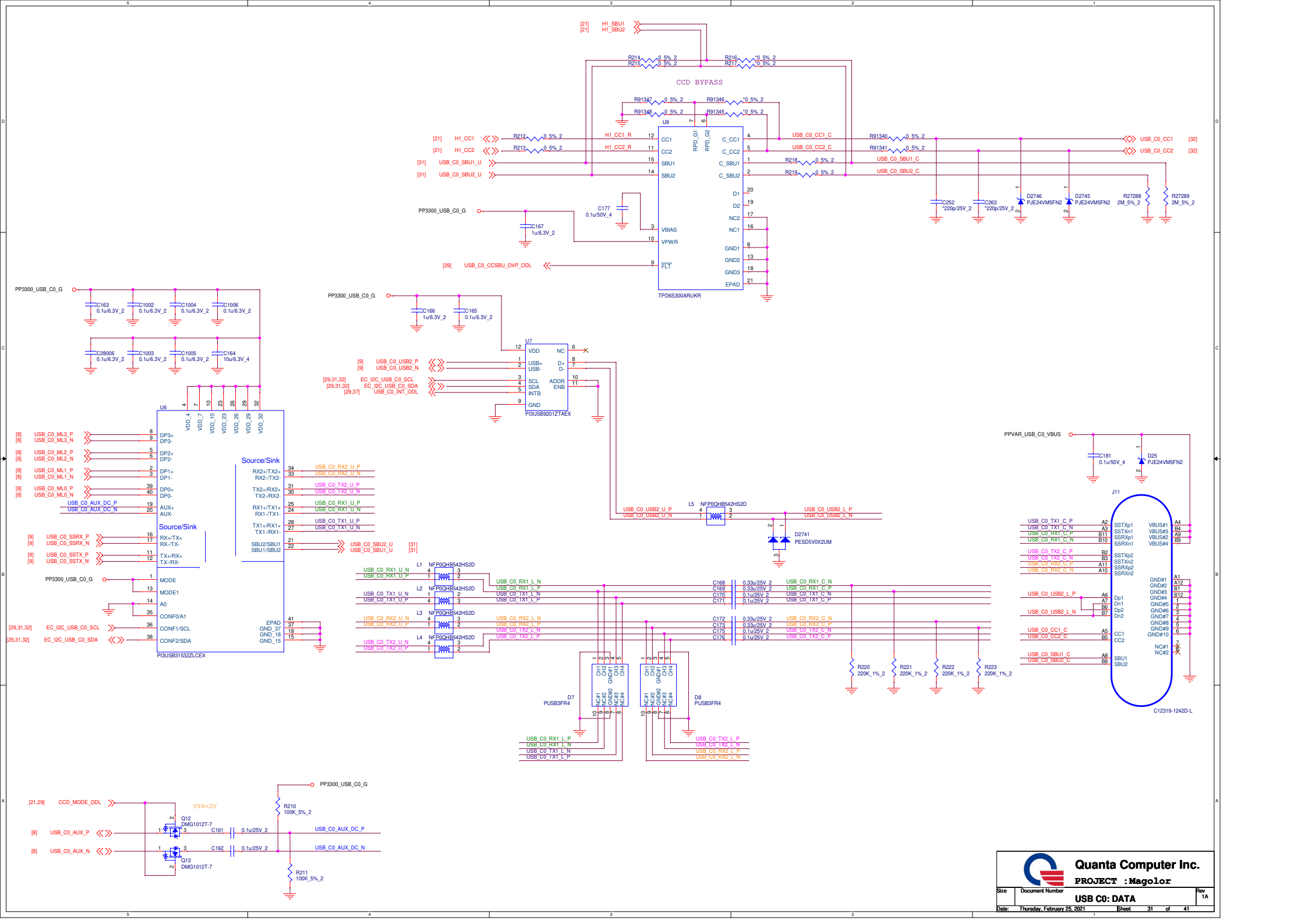
CCD BYPASS
TPD6S300ARUKR
PI3USB9201ZTAEX
PI3USB31532ZLCEX
PUSB3FR4
PUSB3FR4
C12319-1242D-L
Source/Sink
Source/Sink
VTH<2V
Quanta Computer Inc.
PROJECT : Magolor
USB C0: DATA
Rev 1A
Thursday, February 25, 2021
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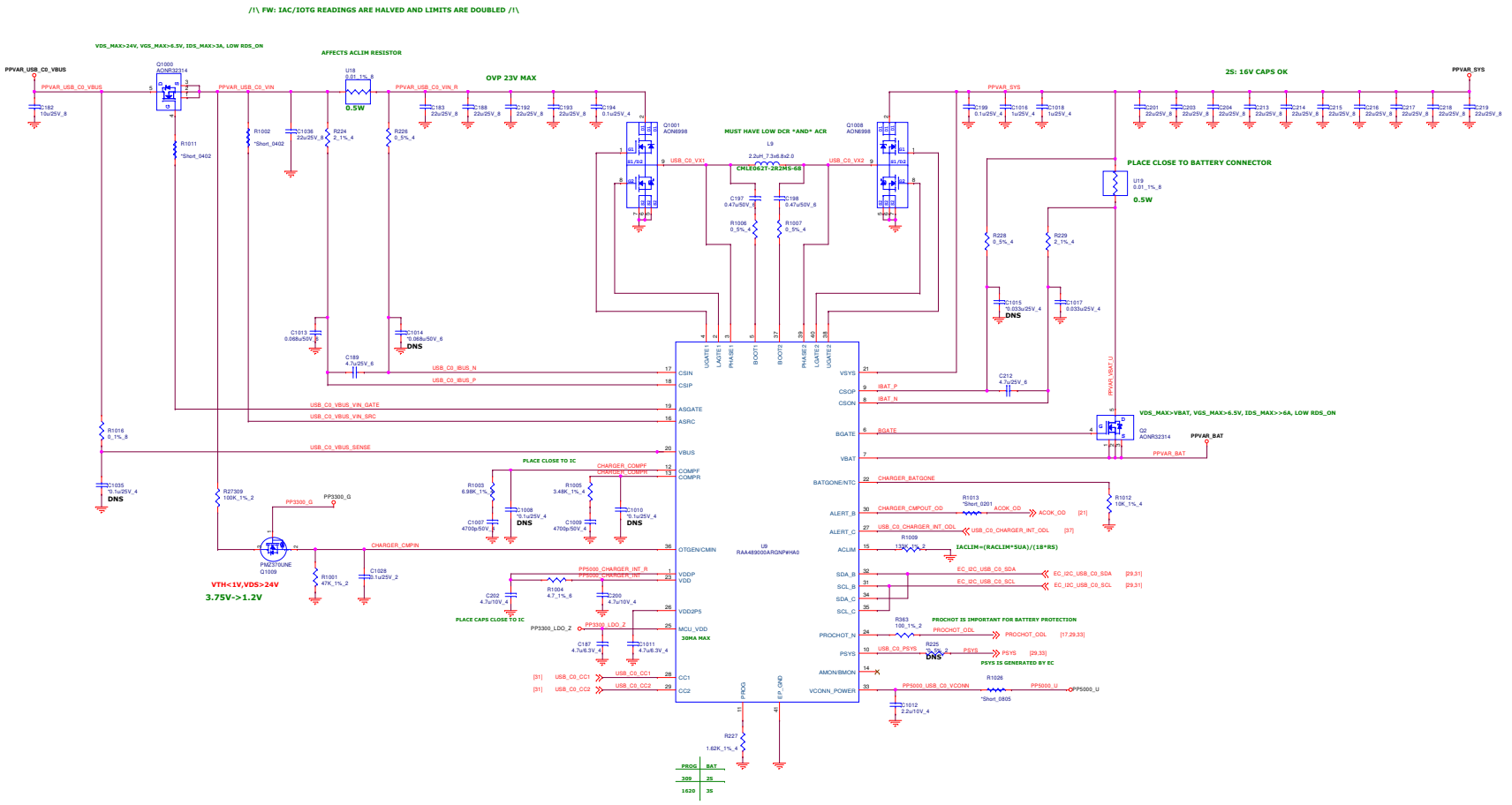
/!\ FW: IAC/IOTG READINGS ARE HALVED AND LIMITS ARE DOUBLED /!\
VDS_MAX>24V, VGS_MAX>6.5V, IDS_MAX>3A, LOW RDS_ON
AFFECTS ACLIM RESISTOR
OVP 23V MAX
MUST HAVE LOW DCR *AND* ACR
2S: 16V CAPS OK
PLACE CLOSE TO BATTERY CONNECTOR
VDS_MAX>VBAT, VGS_MAX>6.5V, IDS_MAX>>6A, LOW RDS_ON
PLACE CLOSE TO IC
PLACE CAPS CLOSE TO IC
PROCHOT IS IMPORTANT FOR BATTERY PROTECTION
PSYS IS GENERATED BY EC
VTH<1V,VDS>24V
3.75V->1.2V
PPVAR_USB_C0_VBUS
PPVAR_USB_C0_VIN
PPVAR_USB_C0_VIN_R
PPVAR_SYS
PPVAR_BAT
PPVAR_VBAT_U
PP3300_G
PP3300_LDO_2
PP5000_CHARGER_INT
PP5000_USB_C0_VCONN
CHARGER_CMPIN
CHARGER_COMPF
CHARGER_CMPR
USB_C0_IBUS_N
USB_C0_IBUS_P
USB_C0_VBUS_VIN_GATE
USB_C0_VBUS_VIN_SRC
USB_C0_VBUS_SENSE
USB_C0_VX1
USB_C0_VX2
CHARGER_BATGONE
IBAT_P
IBAT_N
BGATE
ACOK_OD
USB_C0_CHARGER_INT_ODL
EC_I2C_USB_C0_SDA
EC_I2C_USB_C0_SCL
PROCHOT_ODL
USB_C0_PSYS
PSYS
USB_C0_CC1
USB_C0_CC2
Q1000 AONR32314
Q1001 AON6998
Q1008 AON6998
Q2 AONR32314
Q1009 PMZ370UNE
U8 RAA489000ARGNP#HA0
U18 0.01_1%_8
U19 0.01_1%_8
L9 2.2uH_7.3x6.8x2.0 CMLE062T-2R2MS-68
R1011 *Short_0402
R1002 *Short_0402
R1013 *Short_0201
R1012 10K_1%_4
R1009 150K_1%_2
R363 100_1%_2
R225 0_5%_2 DNS
R1026 *Short_0805
R27309 100K_1%_2
R1001 47K_1%_2
R1004 4.7_1%_8
R1003 6.98K_1%
R1005 3.48K_1%_4
R227 1.62K_1%_4
C1035 *0.1u25V_4 DNS
C1028 0.1u25V_2
C1013 0.068u50V_6
C1014 *0.068u50V_6 DNS
C189 4.7u25V_6
C212 4.7u25V_6
C1015 *0.033u25V_4 DNS
C1017 0.033u25V_4
C1007 4700p50V_4
C1008 *0.1u25V_4 DNS
C1009 4700p50V_4
C1010 *0.1u25V_4 DNS
C202 4.7u10V_4
C200 4.7u10V_4
C187 4.7u6.3V_4
C1011 4.7u6.3V_4
C1012 2.2u10V_4
C197 0.47u50V_6
C198 0.47u50V_6
R1006 0_5%_4
R1007 0_5%_4
R228 0_5%_4
R229 2_1%_4
PROG BAT
309 2S
1620 3S
Quanta Computer Inc.
PROJECT : Magolor
USB C0: BATTERY CHARGER
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VCCIN IMVP 9 CONTROLLER

COMPONENT VALUES NEED TO BE TUNED FOR EACH NEW DESIGN BASED ON VRTT TEST RESULTS!

RT3612EGGQW

Vendor:follow data sheet 6.2 ohm

IF L27202 change to CYN PCMB103T-R24MS1R107
R429 change from 1.5K to 1.82K
R427 change from 1.5K to 9.09K

RICHTEK RECOMMENDS 0603 RESISTORS TO REDUCE VCR EFFECT

LL/IMON COMPENSATION
PLACE CLOSE TO PHASE 1 INDUCTOR

PLACE CLOSE TO PHASE 1 MOSFET

PSYS GENERATED BY EC

FOR FIVR VCCIO

PARAMETER	SETTING
OUTPUT VOLTAGE	VID SELECTABLE
LOAD CURRENT	35 A
OCP	56 A
FREQUENCY	564 KHZ @ TDC
SOFT START	NA
LOAD LINE	2 MOHM

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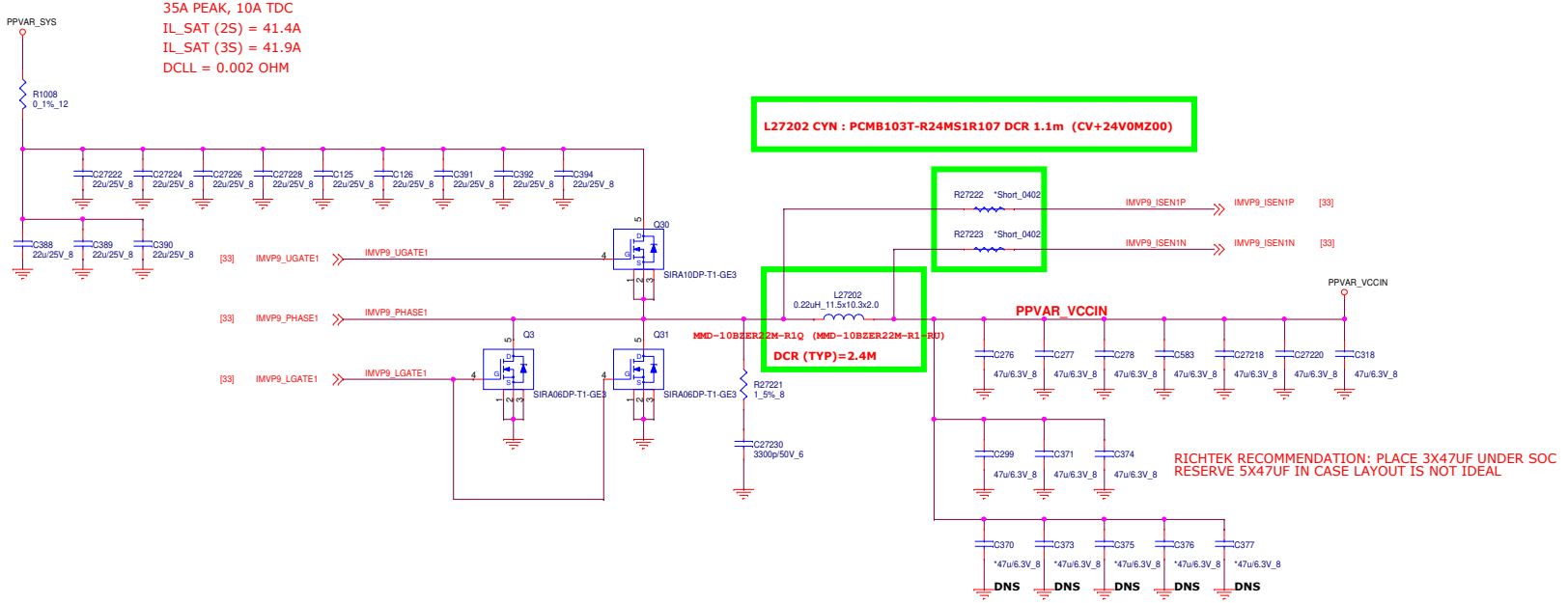
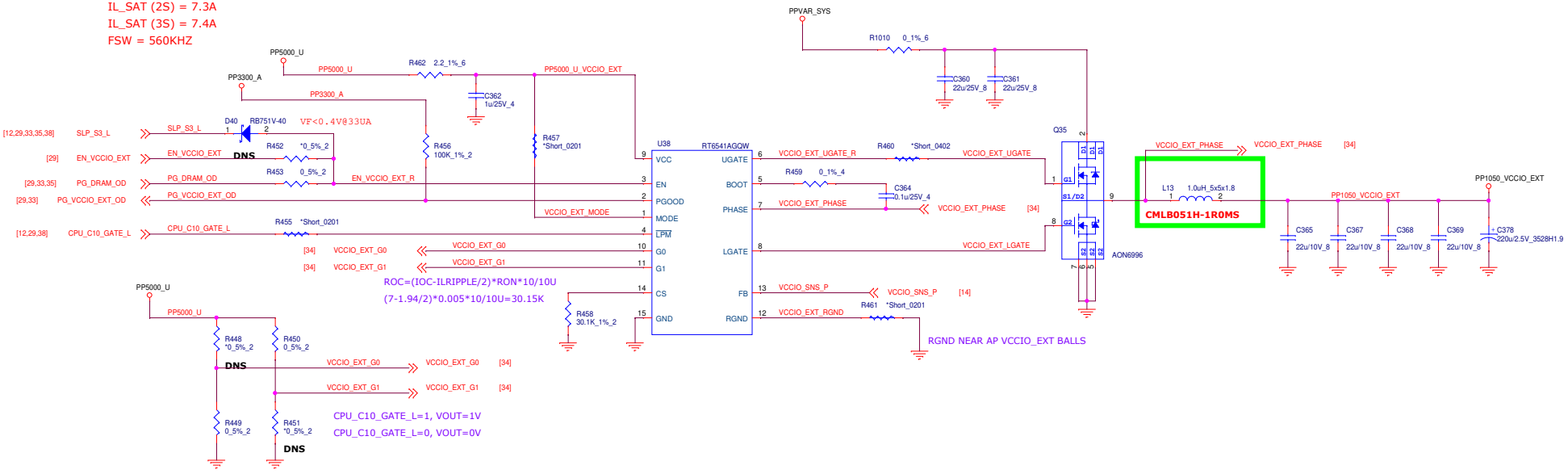
VCCIN POWER CONVERSION

35A PEAK, 10A TDC
IL_SAT (2S) = 41.4A
IL_SAT (3S) = 41.9A
DCLL = 0.002 OHM



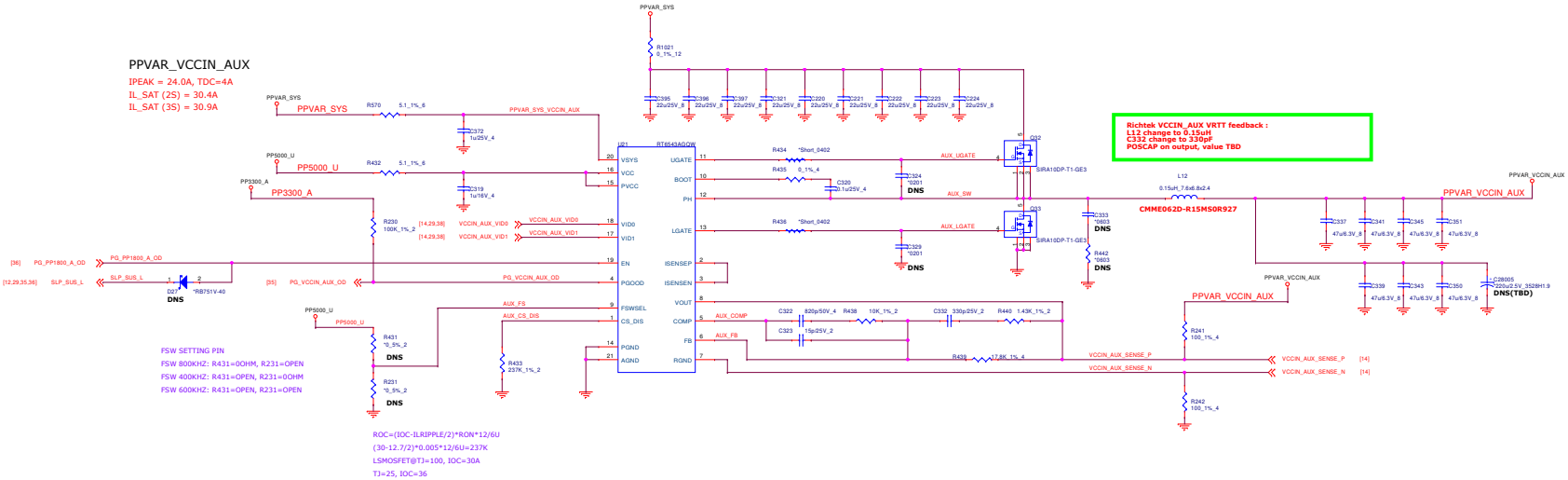
VCCIO_EXT

IPEAK = 6.5A
IL_SAT (2S) = 7.3A
IL_SAT (3S) = 7.4A
FSW = 560KHZ



PPVAR_VCCIN_AUX

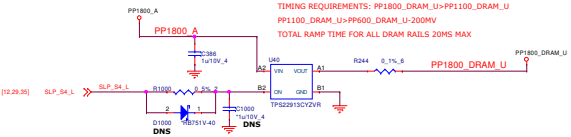
IPEAK = 24.0A, TDC=4A
IL_SAT (2S) = 30.4A
IL_SAT (3S) = 30.9A



Richtek VCCIN_AUX VRTT feedback :
L12 change to 0.15uH
C332 change to 330pF
POSCAP on output, value TBD

PP1800_DRAM_U

IPEAK = 0.3A



USE RC IF POWER-DOWN TIMING IS NOT CORRECT

PP1100_DRAM_U

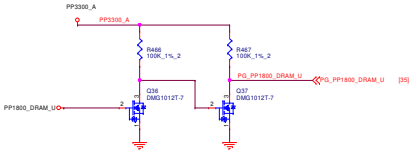
IPEAK = 6.51A
IL_SAT (2S/3S) = 7.9A

TIMING REQUIREMENTS: PP1800_DRAM_U>PP1100_DRAM_U
PP1100_DRAM_U>PP600_DRAM_U-200MV
TOTAL RAMP TIME FOR ALL DRAM RAILS 20MS MAX

CAN USE ANY LOAD SWITCH WITH TON<=1MS

PP600_DRAM_U

IPEAK = 0.99A

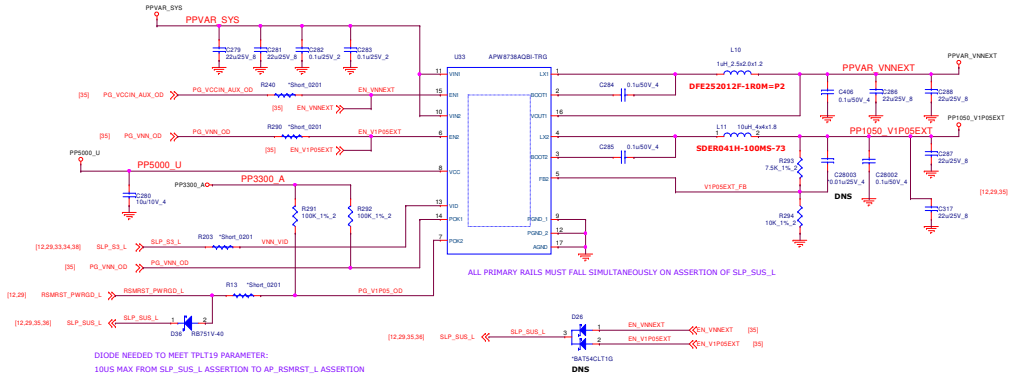


OPTIONAL CIRCUIT IN CASE 1.8V->1.1V TIMING IS NOT CORRECT

PPVAR_VNNEXT & PP1050_V1P05EXT BYPASS RAILS

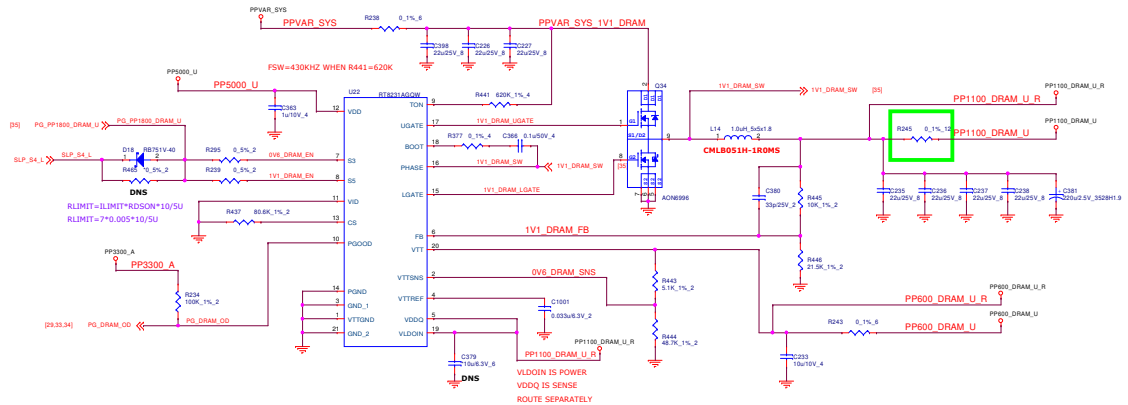
IMAX = 0.5A
IL_SAT (2S/3S) = 1A
FSW = 800KHZ

IMAX = 0.5A
IL_SAT (2S/3S) = 0.6A
FSW = 800KHZ



ALL PRIMARY RAILS MUST FALL SIMULTANEOUSLY ON ASSERTION OF SLP_SUS_L

DIODE NEEDED TO MEET TPLT19 PARAMETER:
10US MAX FROM SLP_SUS_L ASSERTION TO AP_RSMRST_L ASSERTION



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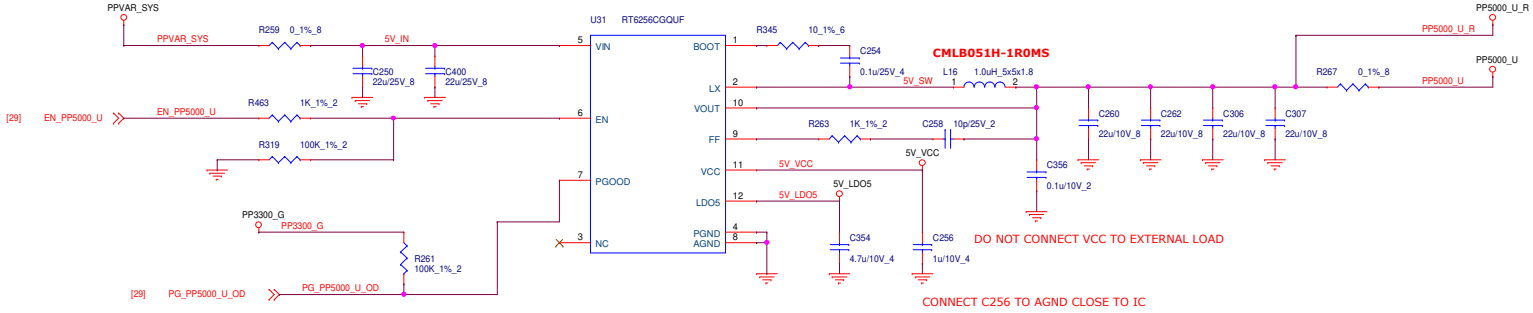
PP5000_U

PEAK CURRENT: 3.3A
IL_SAT (2S): 4.99A
IL_SAT (3S): 5.74A

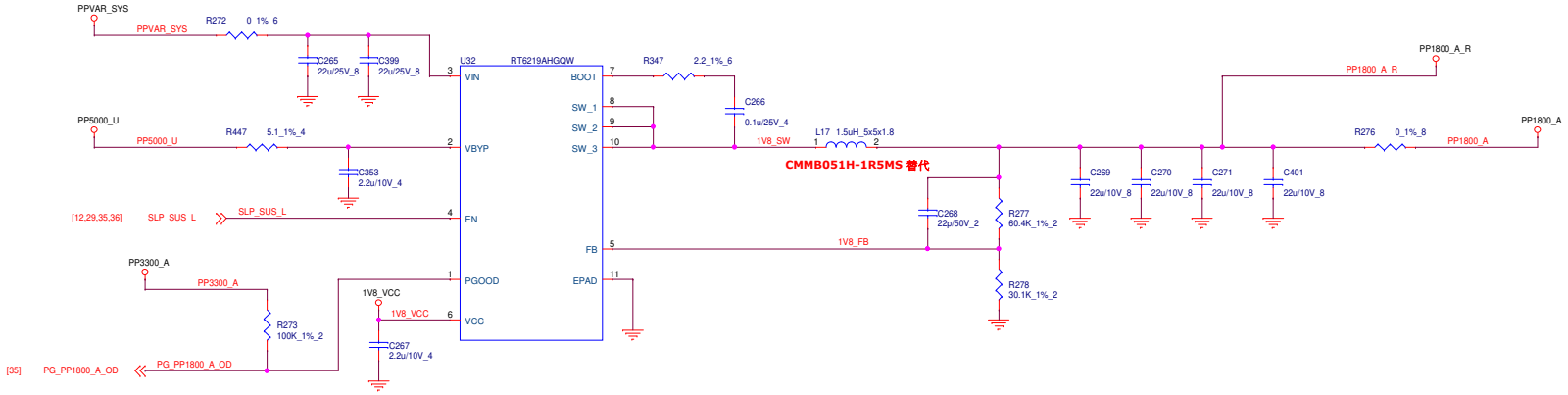
IF USING BC1.2
PEAK CURRENT: 4A
IL_SAT (2S): 5.69A
IL_SAT (3S): 6.44A

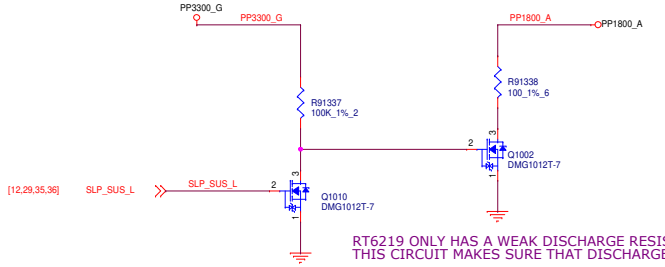
FIXME: THIS SHOULD BE RENAMED TO PP5000_A ON FUTURE PLATFORMS



PP1800_A

PEAK CURRENT: 2.94A
IL_SAT (2S): 4.06A
IL_SAT (3S): 4.16A

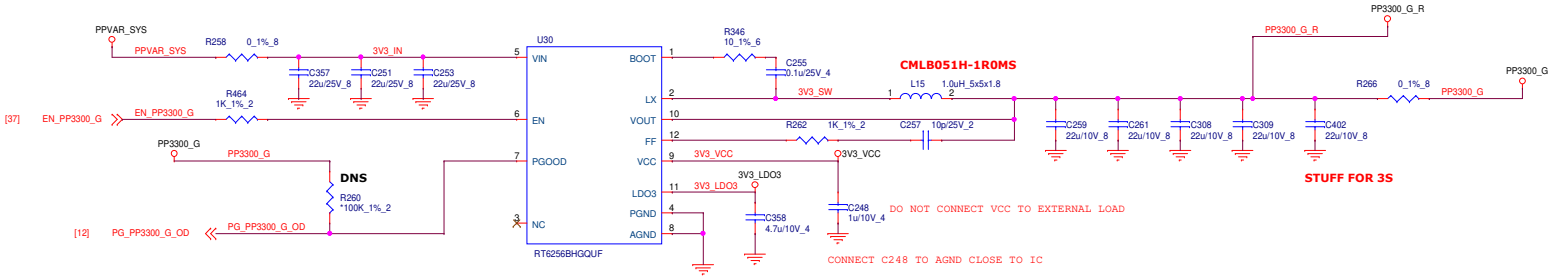




RT6219 ONLY HAS A WEAK DISCHARGE RESISTANCE (5K) WHEN DISABLED
THIS CIRCUIT MAKES SURE THAT DISCHARGE HAPPENS IN <100MS

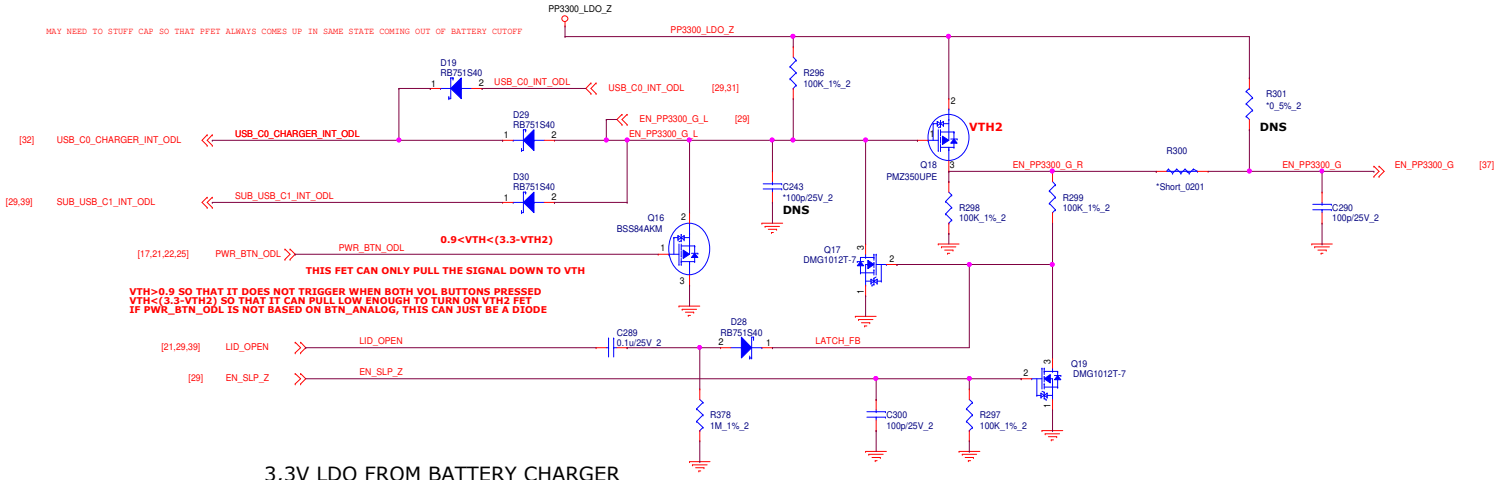
PP3300_G

PEAK CURRENT: 4.06A
IL_SAT (2S): 6.47A
IL_SAT (3S): 6.96A



Z SLEEP STATE LOGIC

SUPER LOW POWER STATE WITH ONLY AP RTC ON. WAKES FROM PWR BTN, LID, USB-C EVENT



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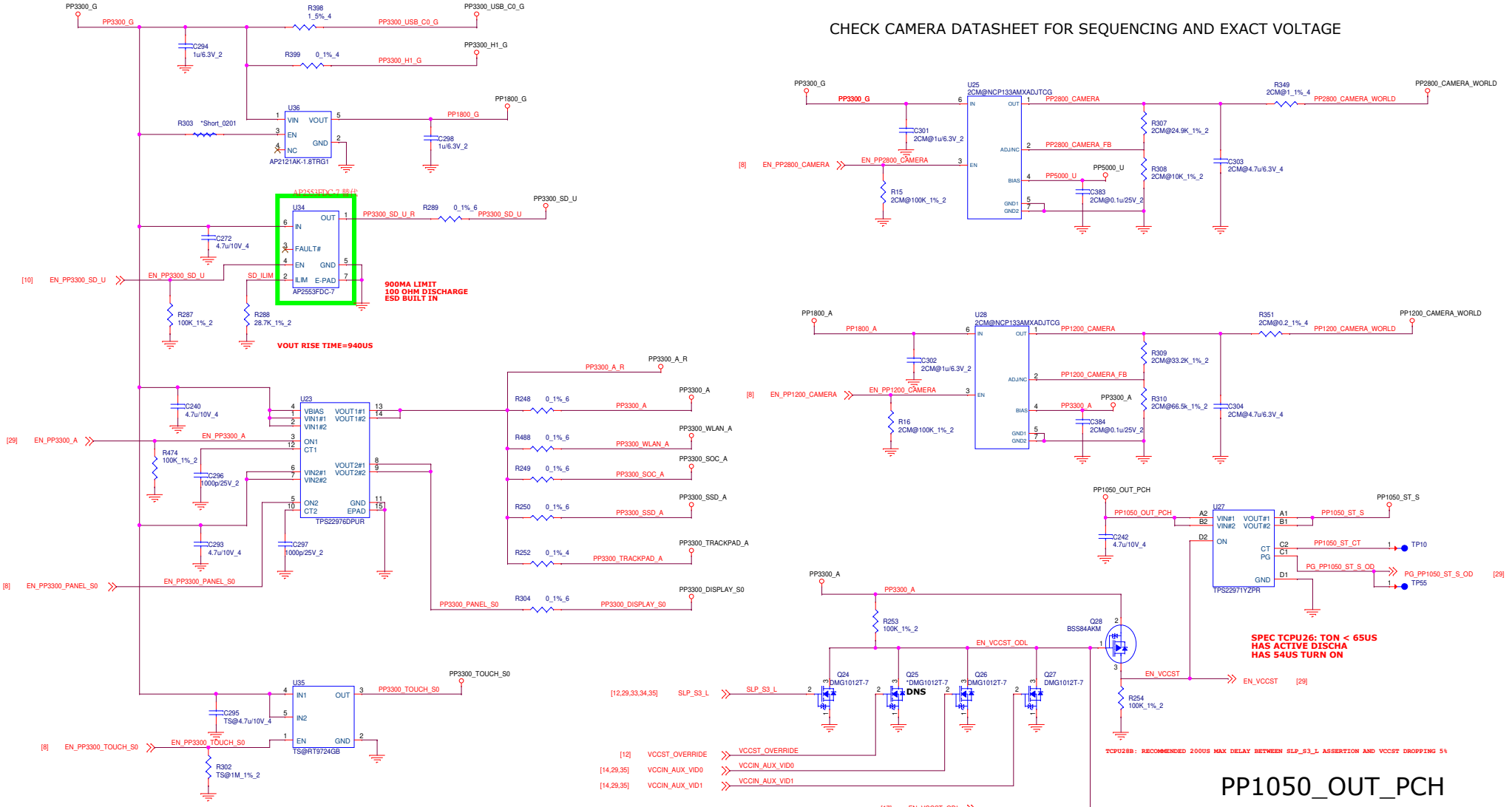
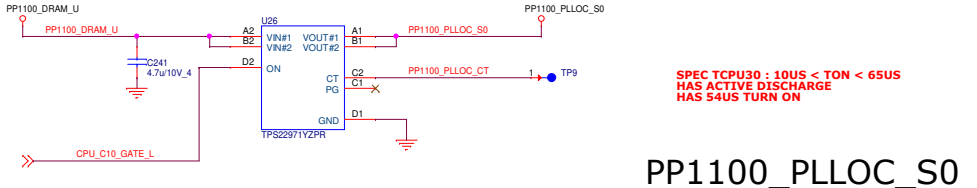
CHECK CAMERA DATASHEET FOR SEQUENCING AND EXACT VOLTAGE





PP3300_G

PP1050_OUT_PCH

PP1800_A

PP1100_PLLOC_S0

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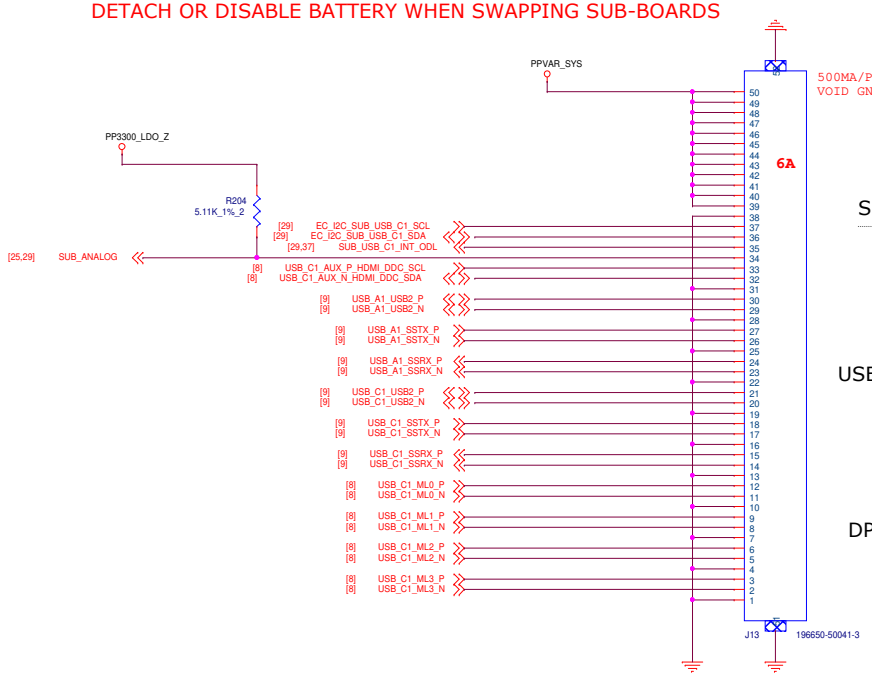
SUB-BOARD CONNECTOR

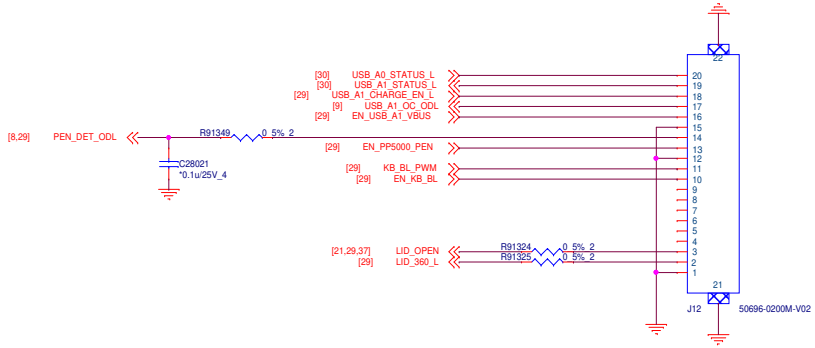
DETACH OR DISABLE BATTERY WHEN SWAPPING SUB-BOARDS



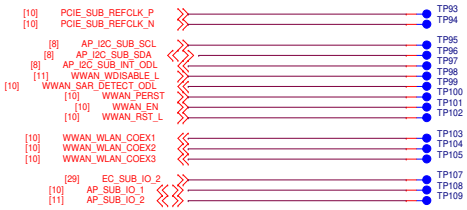
SUB-BOARD	SUB_ANALOG
USB-C	BTN_ANALOG
HDMI	HDMI_HPD_ODL

USB-A SS PINS ARE ALSO PCIE

DP PINS ARE ALSO HDMI



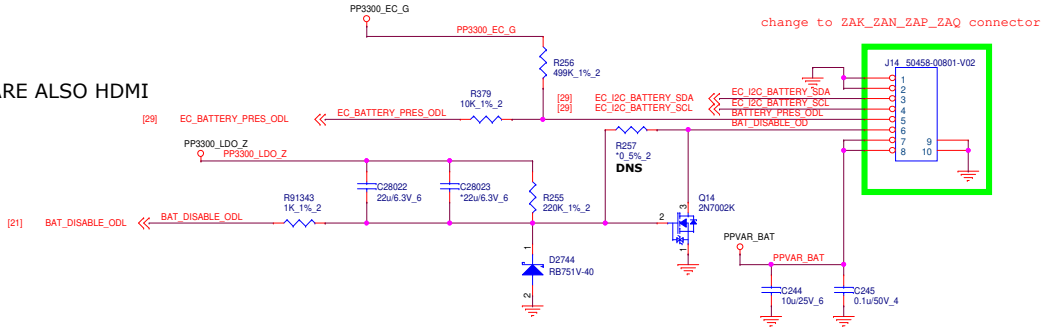
SUB-BOARD WWAN/EXTRA CONNECTOR



SMART BATTERY

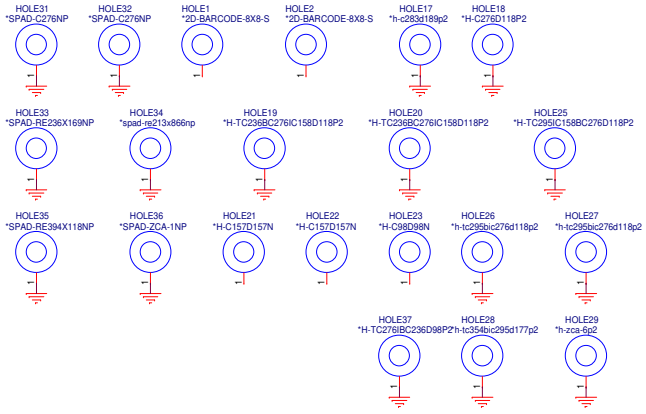
MAY NEED WEAKER PULL-UP IF BATTERY THERMISTOR IS GREATER THAN 100K

change to ZAK_ZAN_ZAP_ZAQ connector



EC_BATT_PRES SERIES R PREVENTS PARTIALLY-CONNECTED BATTERY FROM USING THE EC AS HIGH-CURRENT GROUND RETURN

Hole



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Data	Page	Item
6/9	7	DNS C314
6/9	22,29,21	With Nuvoton EC, U20 is not needed. Please delete U20 and rewire C2D2 port as is done on Waddledoo. Watch closely wiring on H1 (Balls H4, J2, H6, J6) and make sure 1M pulldowns are added to balls H6, J6, J1 of H1
6/9	29	This should only route from EC to CBI EEPROM and should *not* route to H1
6/9	39	Del J12.
6/9	29	Routes directly from Nuvoton EC to U1 (Please refer to Waddledoo schematic). UART_DBG_TX_EC_RX has a series resistor
6/9	29	stuff R202, C155
6/10	8	DNS R148 & R149 if not using HDMI
6/10	31	Vconn can be applied to USB CC1 and CC2 signals through the Renesas Charger; U39 is not needed and should be deleted
6/10	31	Add discrete ESD protection D2741 to USB_C0_USB2_L_P/N and disconnect from U8
6/11	9,30	Connect USB_A0_OC_ODL to U1JSL #CR27
6/11	29	Del TP81-TP85 and R27290
6/11	39	Swap J13 pin define for layout routing
6/12	18,19	Swap M_D_DQ_3_*,M_D_DQ_1_*,M_C_DQ_3_*,M_B_DQ_2_*,M_A_DQ_2_*,M_A_DQ_0_*,M_C_DQ_1_*,M_B_DQ_3_*,M_A_DQ_1_* for layout routing
6/12	28	Change WIFI to AX201 1216 soldered down module
6/15	8,9,27,38	Change UFC to USB2 I/F and combine with LCD connector include DMIC, add TP TP113, del R348,R350, W1
6/15	25,29	Del SW2 and SW3 due to vol up/down button place on USB/B, add TP114, TP115
6/15	27	Add thermal protect circuit
6/16	9,39	[USB A] "USB_A1_OC_ODL" that use 0 ohm connect to CPU JSP ball#CL30 for over current
6/16	28	Pins 36 & 37 (PERn0 and PERp0) each need a 0.1uF DC blocking cap for the PCIe lane.
6/16	19	Swap M_C_DQ_0_* for layout routing
6/23	27	Modify J24 pin define, add " ACCEL_INT_L" for G-sensor/B.
6/23	26	Add CN1 LED connector for WFC indicator
6/23	26	Del U29, add connector CN2 to GMR/B
6/23	25,39	Move PEN GARAGE connector to USB/B, combine PEN signal with To USB/B 20pin connector
6/23	26	Del U5, add connector CN3 to DMIC module
6/30	26,39	Move GMR circuit to USB/B
6/30	39	Add 20pin connector to USB/B
6/30	25,29	Del J19 (KB backlight), add TP117
6/30	8,27,38	Del J20 (EMR stylus), del R306, add TP118,TP119,TP120,TP121
7/1	24	Fix ALC1015 I2C address
7/1	39	Add note for R256
7/2	20	Update to 128Mbit flash
7/2	33	Add stuffing option for controlling VCCIN_EN with PG_VCCIO_EXT_OD Make PG_VCCIO_EXT_OD stuffing the default for VCCIN_EN Add D39 criteria: Vf<0.3V@33uA Updated D39 note: FOR FIVR VCCIO
7/2	34	Add diode to pull PG_DRAM_OD low by SLP_S3_L Remove R454 Move D40 to VCCIO page Add D40 criteria: Vf<0.4V@33uA Stuff R453 for PG_DRAM_OD control of VCCIO
7/2	32	Change VBUS threshold to 3.75V and add voltage protection (add Q1009/ R1001change from 43.2K to 47K) Add cap to PPVAR_USB_C0_VIN to reduce inrush (Add R1016 & C1035) Add placeholder filters for VBUS and VCONN inputs (Add C1036 & R1026) For 3S battery R227 change from 309 to 1.62K
7/3	31	Swap L1/L2/L3/L4 pin for layout routing
7/3	19	Update RAM ID table
7/6	30	Swap L7/L8 pin for layout routing
7/8	2	Update block diagram
7/8	34	L13 change to CMLB051H-1R0MS 5*5*1.8
7/9	18	DNS C4301
7/9	37	Stuff C402 for 3S
7/17	10,28	Refer to RVP, connect CNV_RF_RST_L from U1JSL CJ49 to CB24 Change C28012,C28013 to 0 ohm (R91327,R91328) ; DNS R422 ; add TP122,TP123
7/20	39	Modify J14 Pin1 &2 to GND
7/20	29,30,39	USB_A0_CHARGE_EN_L to EC GPIO37 ; USB_A1_CHARGE_EN_L to EC GPIOF3 ; EN_USB_A1_VBUS to EC GPIOF2
7/22	31	Swap L5 for layout routing
7/23	10	To use ball#CJ49 as CNV_RF_RST_L that same as WDoo/WDee
7/23	19	Modify RAM STRAP table
7/27	31	Swap D7/L1 pin for layout routing
7/29	32	Change Q2,Q1000 from AON7752 to AONR32314 due to AON7752 EOL
8/25	29,39	Correct net name EN_PP3300_PEN to EN_PP5000_PEN
8/25	20	Due to ITE8320 I/O structure, put in a push-pull inverter for EEPROM WP, this replaces Q29 and R313 DNS R58 and add tri-state buffer across R58 to prevent H1 startup glitch b/148294925
8/26	31	Change U6 from PI3USB31532ZLEX to PI3USB31532ZLCEX for soldering issue
8/27	20	Change U12 from AT24C02C-MAHM-T to GT34C02B-2UDLI-TR for shortage issue
9/1	24	Vendor suggest to add 0 ohm on I2C and EN pin for debug.

Data	Page	Item
9/1	10	Change C4104,C4103 to 15pF, C4101,C4102 to 12pF for crystal vendor measure result.
9/4	12	Change R368 from 1M to 100k (prevents AP_DWPROK from turning on during EC programming); will be on schematic release 0.11
9/4	10	Change R9 from 2M to 100k; pin leakage was inducing a voltage on Q20 and Q21 gates; this change will be on schematic release 0.11
9/4	12	Change R355 from DNS to 100k; removes runt pulse on CPU_C10_GATE_L
9/4	37	DNS R260 to avoid runt pulse on AP_DPWROK; this change will be on schematic release 0.11
9/7	33	Change R275 to 13.7K for IMON fine tune
9/23	13,17	Stuff R405, R407, R408, R409, R410, R411, R412 with the 1k resistor for INTEL JSL PDG
11/2	17	Remove TODO comment about MIPI60 connections
11/2	10	Add note to AP crystals page that adjusting caps may be necessary
11/2	13	Update R4F23 to 100k to match phase
11/2	10	Remove R312 and D37
11/2	24	Removed stale comment about Realtek Codec
11/2	33	Added note that VCCIN components will need to be tuned based on VRTT test results
11/2	13,17,38	Rejigger MIPI60 header for ease of removal from designs
11/3	26,29	Remove camera VSYNC signal
11/3	10,11,39	Rename WWAN signals
11/3	30,31	Change L5, L6 from PCMF1USB3S to NFP0QHB542HS2D, add PESD5V0X2UM for USB_A0_USB2_L
11/3	28	Change U16 from TI SN74AUP1T97YZPR (BGA) to NXP 74AUP1T97GM (SOT886)
11/11	24	Add 1000pF to ground on each of these signals, LSPK_P, LSPK_N, RSPK_P, RSPK_N for EMI. Add one 0 ohm resistor between GND and AGND_HP.
11/11	2,29	Change EC from NPCX796FC0BX to NPCX797FC0BX
11/25	29,39	Connect keyboard backlight signal to EC (KB_BL_PWM to GPIO80/PWM3, EN_KB_BL to GPIO60/PWM7)
12/2	32	Change R1009 from 110K ohm to 121K ohm for ACLIM
12/23	31	Wire the RAA489000 CC pins directly to the USBC connector
1/8	17	D31 can be DNS/EMPTY as part of MIPI60 circuitry
1/12	10	Add 0 ohm (DNS for now) between GP_C22 (ball CE13) on SoC and AP_PEN_DET_ODL signal. The second GPIO on the SoC is needed to permit the system to know which input was responsible to WAKE the system.
1/12	39	Add 0 ohm between J12.14 and PEN_DET_ODL. This resistor may be needed for tuning for current limiting the discharge of a capacitor, so you may not wish to replace with a metal short for PVT. Add 0402 DNS capacitor between PEN_DET_ODL and GND.
1/12	31	The RAA489000 TCPC has built in Rd pulldowns for the dead battery case. with U8 pins connecting RPD_G1 and RPD_G2 to CC(2:1) instead of Ground, there are two parallel Rd pulldowns for the dead battery case. To remove the TPD6S300 Rd pulldown, you may consider tying RPD_G1 and RPD_G2 each to ground.
1/12	31	Attach C252 to USB_C0_CC1 instead of USB_C0_CC1_C. Attach C263 to USB_C0_CC2 instead of USB_C0_CC2_C This will place the cap on the USB PD negotiation path, which is between the USBC connector J11 and the RAA4890000 TCPC.
1/12	39	1.Add R91343 / C28022/D2744 2.R255 change from 100K to 220K
1/13	39	Replacing (Q14) DMG1012T-7 with the 2N7002 will give a longer pulse on BAT_DISABLE_OD.
1/13	25	LED limit resistor change: Blue to 200ohm, Amber to 1Kohm
1/18	39	R91343 change to 1K ohm, stuff D2744
2/25	32	Change R1009 from 121Kohm to 133K ohm for IACLIM setting

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