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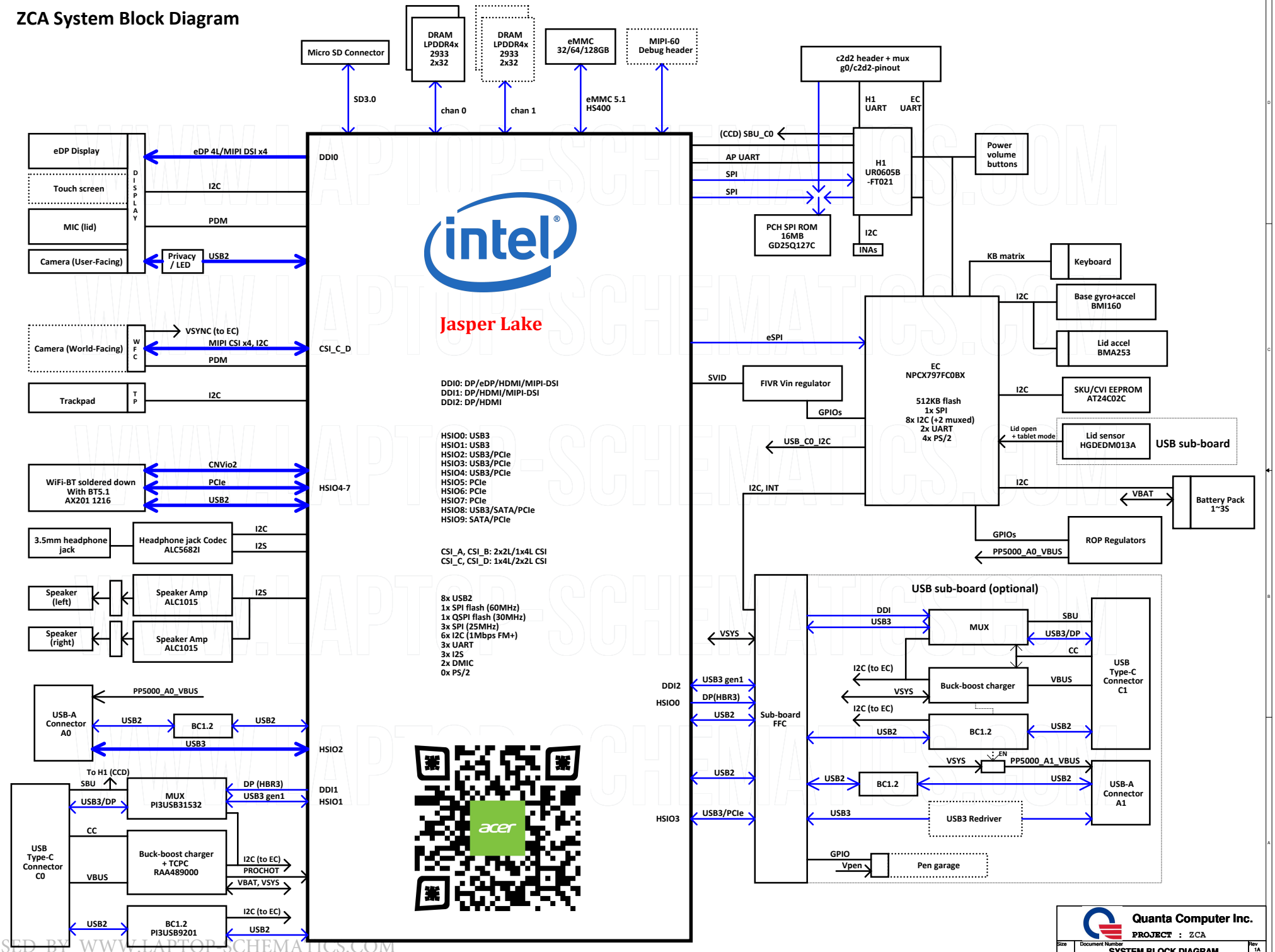
ZCA System Block Diagram

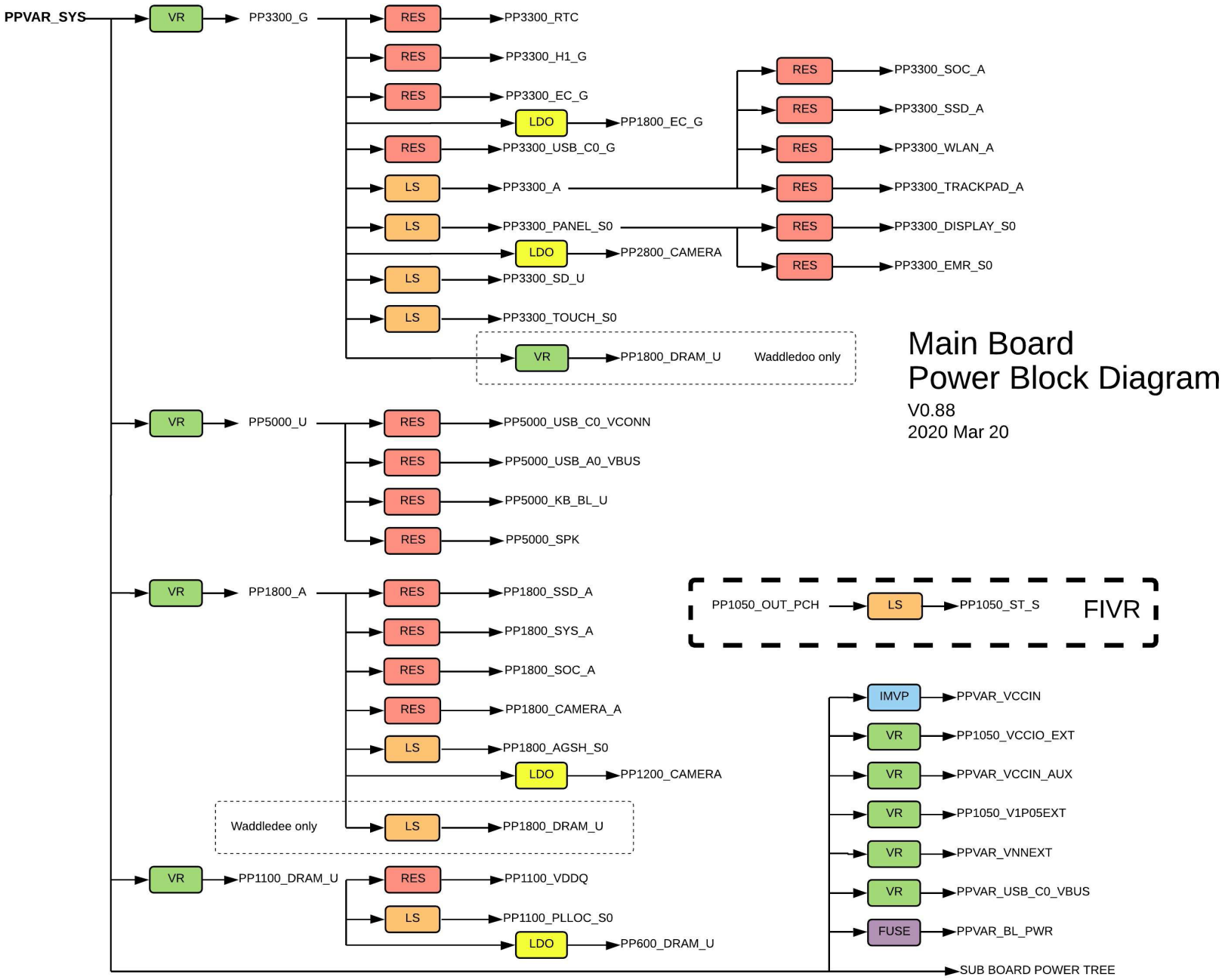


Quanta Computer Inc.

PROJECT : ZCA

Size	Document Number	Rev
	SYSTEM BLOCK DIAGRAM	1A

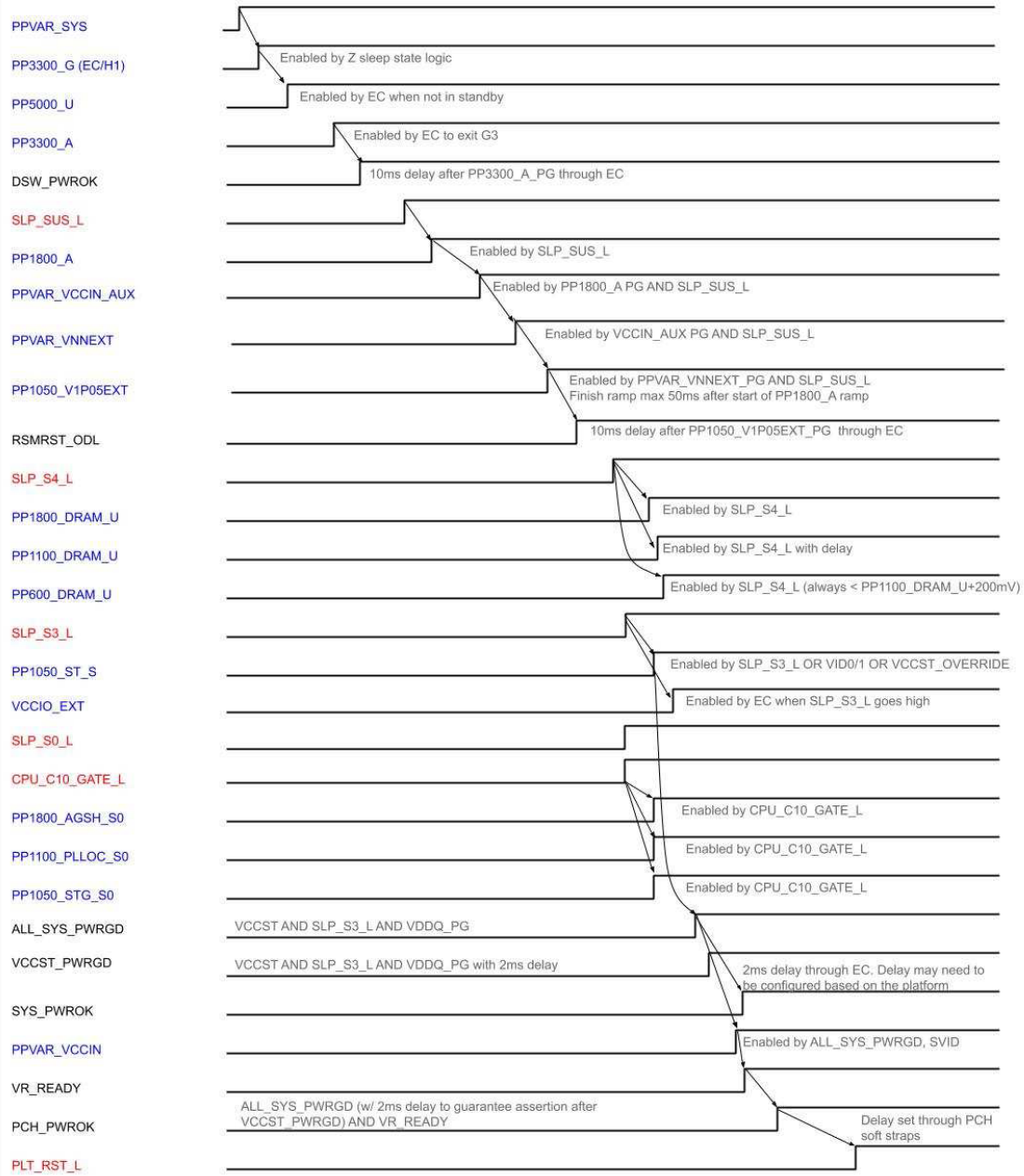
Date: Wednesday, March 10, 2021 Sheet 2 of 41



Main Board
Power Block Diagram

V0.88
2020 Mar 20

Quanta Computer Inc.
PROJECT : ZCA
Size | Document Number | Rev 1A
POWER TREE
Date: Wednesday, February 17, 2021 | Sheet 3 of 41



Power Rail
Signal from PCH
Signal from Platform

Power Sequencing

Updated: 6/06/2020

W

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PROJECT : ZCA

Size	Document Number	Rev
	RESERVED	1A

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Master	Port	Voltage Domain	Bus name	Bus Speed	Slave Device	7-bit Addr(s)	Int Priority	Note
AP(JSL+)	0	PP1800_A	AP_I2C_TP	400KHz	Trackpad	Project-specific	0	Trackpad
	1	PP3300_EMR_S0	AP_I2C_EMR	400KHz	SUBE-xxxxxMI	0x09	0	EMR pen
					HPDxxxx-920	?	0	EMR pen
	2	PP3300_TOUCH_S0	AP_I2C_TS	400KHz	Touchscreen	Project-specific	0	Touchsreen
					Panel	Project-specific	-	MIPI Panel
	3	PP1800_A	AP_I2C_CAMERA	400KHz	UFC	Project-specific	-	MIPI UFC
					WFC	Project-specific	-	MIPI WFC
	4	PP1800_A	AP_I2C_AUDIO	400KHz	ALC1015	0x28(left),0x29(right)	-	Speakers
					ALC5682I	0x1A	0	Headphone
					DA7219	0x1A	0	Headphone
	5	TBD	AP_I2C_SUB	400KHz	TBD	-	-	Expansion

Master	Port	Voltage Domain	Bus name	Bus Speed	Slave Device	7-bit Addr(s)	Int Priority	Note
EC	IT8320: 0 NPCX796: 7	PP3300_G	EC_I2C_EEPROM	1MHz	AT24C02D, GT34C02B, N24C02	0x30(PSWP),0x50(memory)	-	CBI EEPROM
					IT8320	0x35,0x5A,0x79	-	EC flash
					INA3221	0x40 ~ 0x43	-	INA
					INA231	0x44 ~ 0x4F	-	INA
	IT8320: 1 NPCX796: 5	PP3300_G	EC_I2C_BATTERY	100KHz	Smart battery	Pack-specific	-	Fuel gauge
	IT8320: 2 NPCX796: 0	PP1800_A	EC_I2C_SENSOR	400KHz	BMI160	0x68	-	Gyro/accel
					LSM6DS3TR	0x6A	-	Gyro/accel
					BMA253	0x18	-	Lid accel
					LIS2DE12	0x18	-	Lid accel
					KB backlight	Project-specific	-	KB backlight
					IMVP9	Project-specific	-	IMVP9
	IT8320: 5 NPCX796: 1	PP3300_G	EC_I2C_USB_C0	1MHz	SM5803	0x30,0x31,0x32	1	Charger
					SM5804	TBD	0	Charger+TCPC
					RAA489000	0x09(+0x0C SMBus ARA)	1	Charger
					RAA489000	0x22	0	TCPC
					ANX3447	0x2C,0x3F,0x3D,0x42,0x39,0x38	0	TCPC+MUX
					IT5205	0x48	-	MUX
					PI3USB31532	0x54	-	MUX
					PI3USB9201	0x5F	2	BC1.2
	IT8320: 4 NPCX796: 2	PP3300_G	EC_I2C_SUB_USB_C1	1MHz	SM5803	0x30,0x31,0x32	1	Charger
					SM5804	TBD	0	Charger+TCPC
					RAA489000	0x90(+0x0C SMBus ARA)	1	Charger
					RAA489000	0x22	0	TCPC
					ANX3447	0x2C,0x3F,0x3D,0x42,0x39,0x38	0	TCPC+MUX
					IT5205	0x48	-	MUX
					PI3USB31532	0x54	-	MUX
					PI3USB9201	0x5F	2	BC1.2
					TUSB544	0x44	-	Redriver
					NB7VPQ904M	0x19	-	Redriver
					PS8743	0x11	-	MUX+Redriver

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PROJECT : ZCA

Size	Document Number	Rev
	I2C MAP	1A

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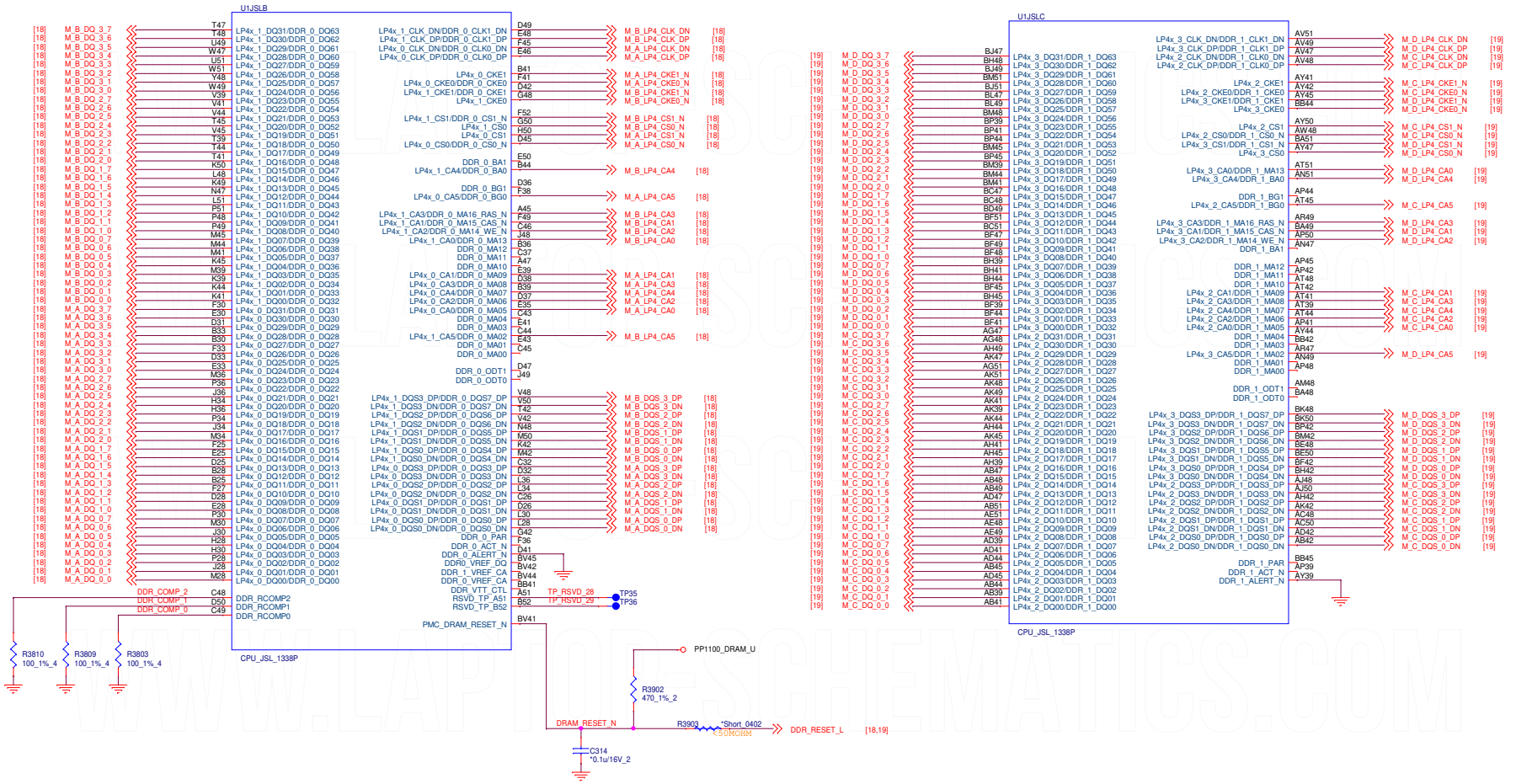
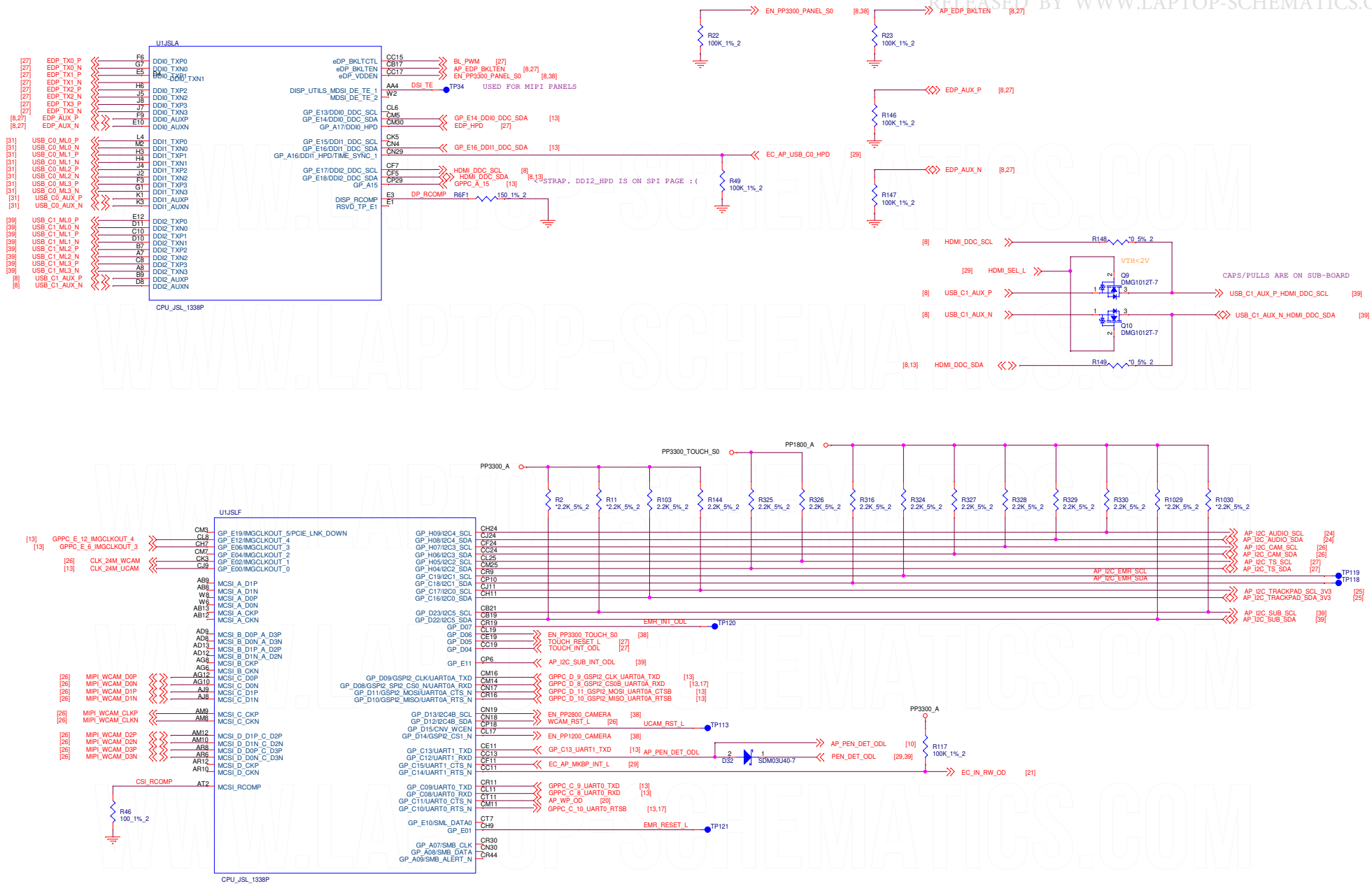


Quanta Computer Inc.			
PROJECT : ZCA			
Size	Document Number	JSL+: MEMORY	Rev 1A
Date: Wednesday, February 17, 2021	Sheet 7 of 41		

PCH GLITCH MITIGATION

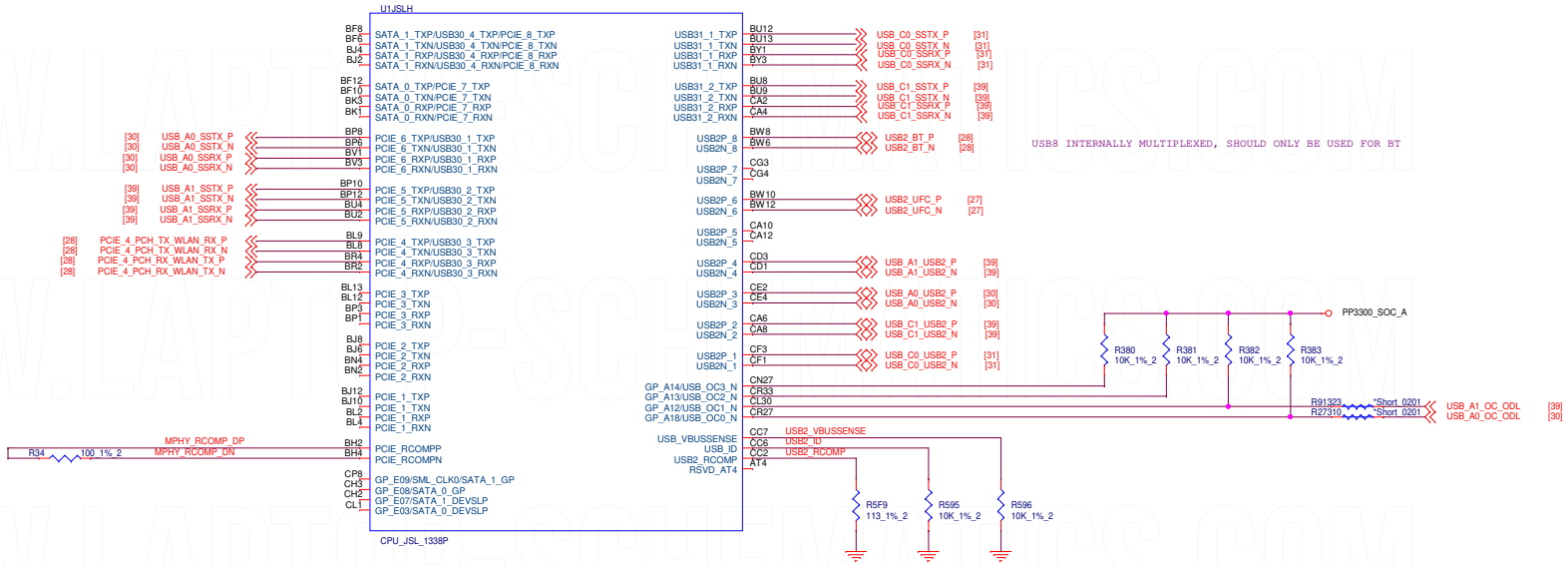


Quanta Computer Inc.

PROJECT : ZCA

Size	Document Number	Rev
	JSL+: DISPLAY, CAMERA, I2C	1A

Date: Wednesday, February 17, 2021 Sheet 8 of 41



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PROJECT : ZCA

Size	Document Number	Rev
	JSL+: USB, PCIE, CNVI	1A

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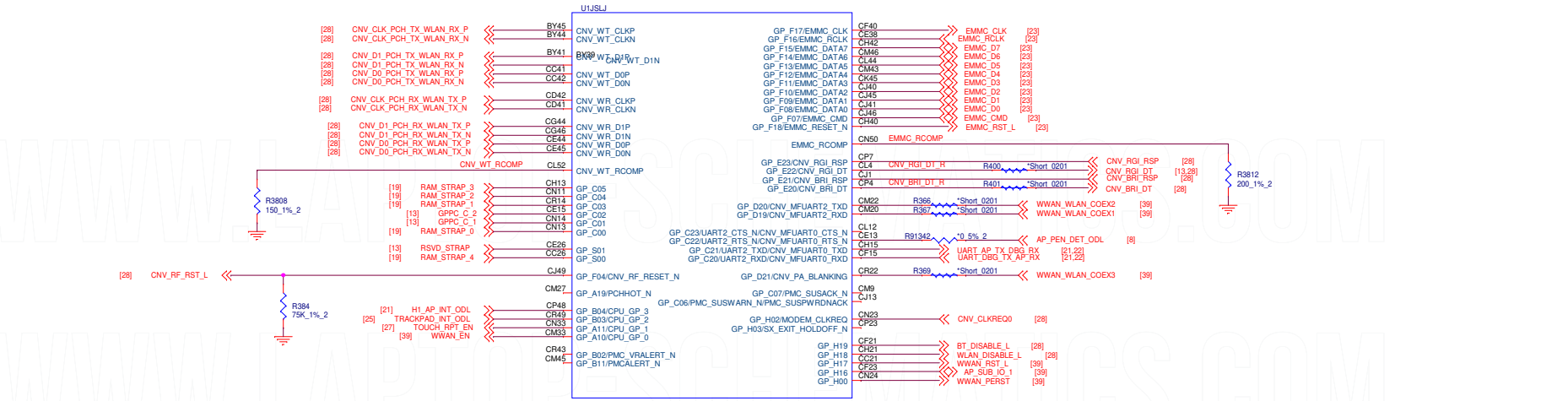

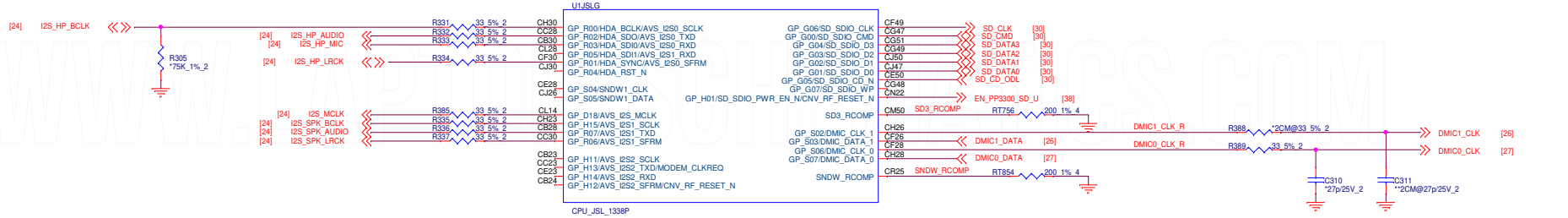

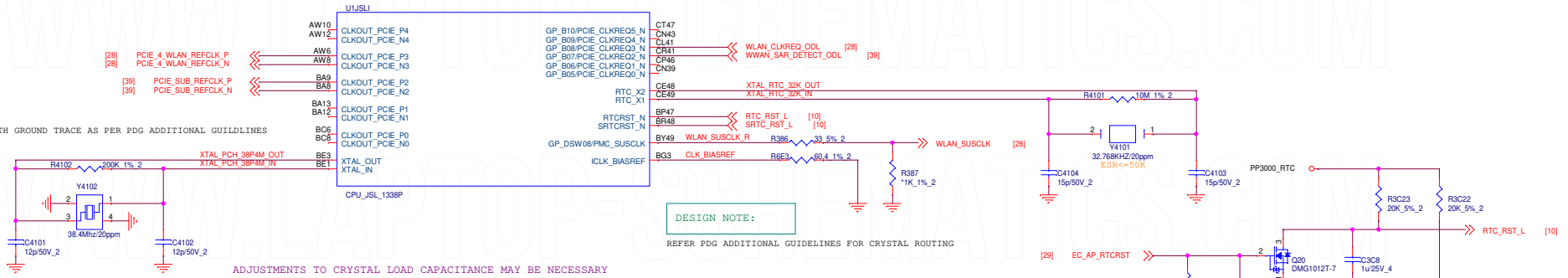

CAD NOTE:

GUARD THE CRYSTAL INOUT WITH GROUND TRACE AS PER PDG ADDITIONAL GUILDLINES

DESIGN NOTE:

REFER PDG ADDITIONAL GUIDELINES FOR CRYSTAL ROUTING

ADJUSTMENTS TO CRYSTAL LOAD CAPACITANCE MAY BE NECESSARY

DESIGN NOTE:

XTAL ESR = 30 OHM MAX, CL = 10PF, C0 = 3PF, MAX DRIVE = 300UW

Quanta Computer Inc.		
PROJECT : ZCA		
Size	Document Number: JSL+: AUDIO, SD, EMMC, CNVI, CLOCKS	Rev 1A
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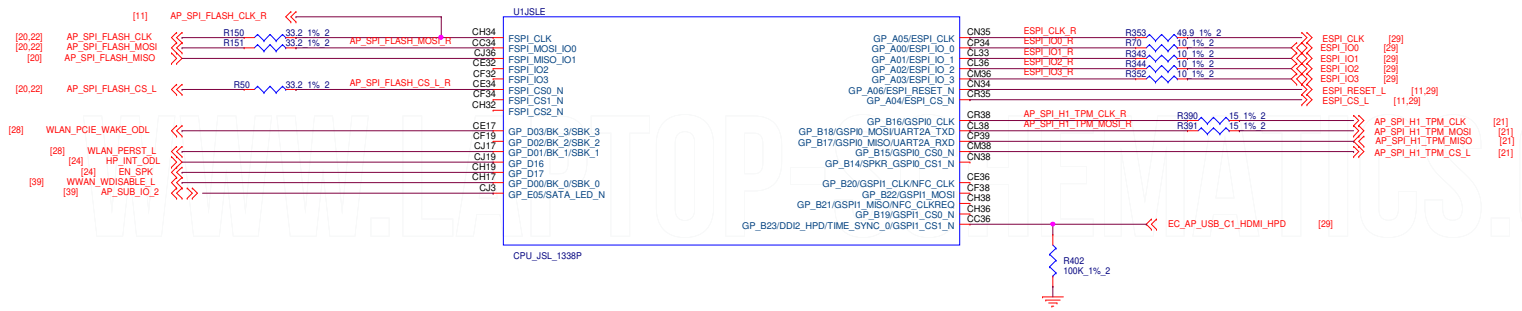
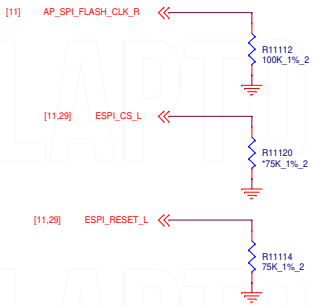


PCH GLITCH MITIGATION



Quanta Computer Inc.		
PROJECT : ZCA		
Size	Document Number	Rev
	JSL+: ESPI, SPI	1A
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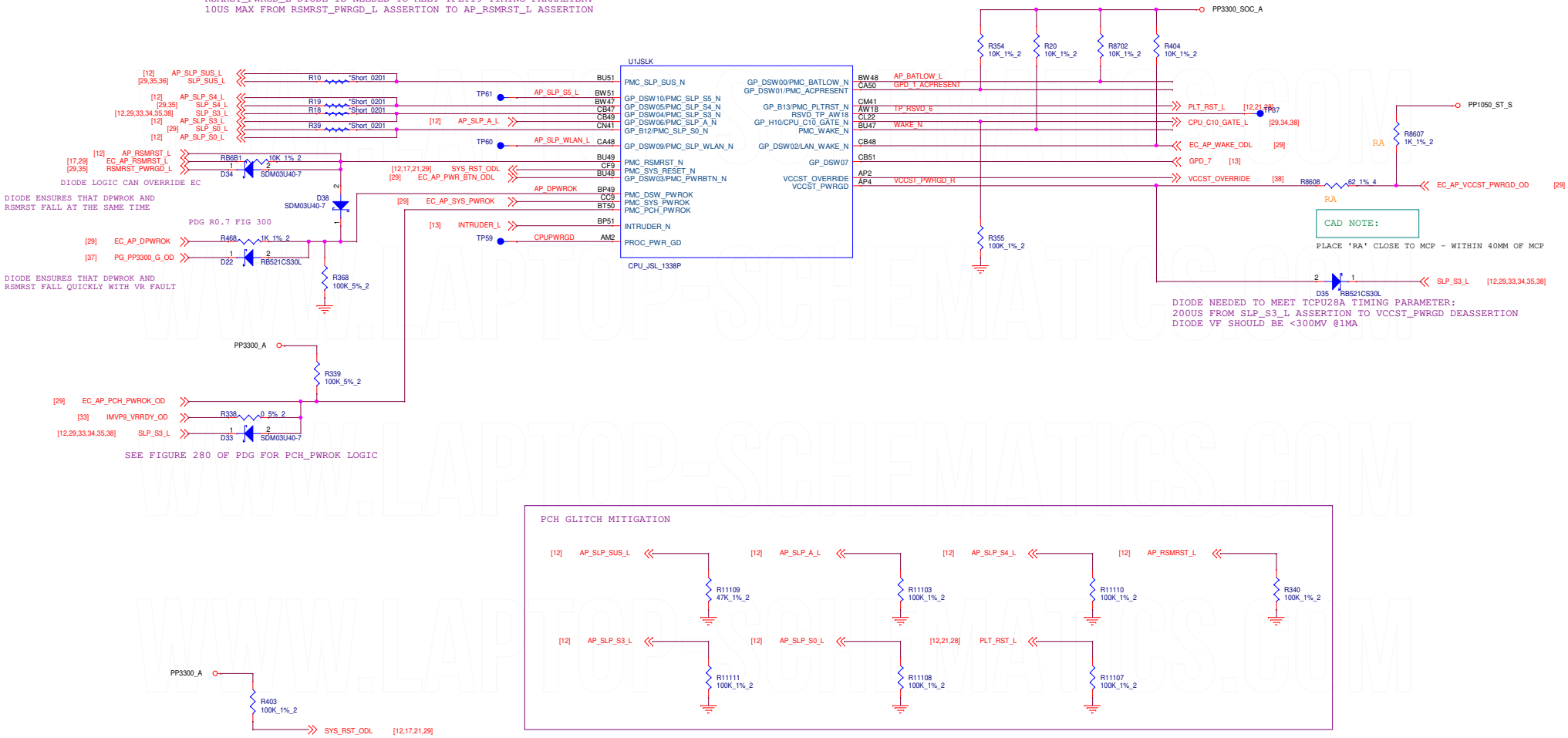
RSMRST_PWRGD_L DIODE IS NEEDED TO MEET TPLT19 TIMING PARAMETER:
10US MAX FROM RSMRST_PWRGD_L ASSERTION TO AP_RSMRST_L ASSERTION



Quanta Computer Inc.
PROJECT : ZCA

Size	Document Number	Rev
	JSL+: POWER SEQUENCING	1A

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DISPLAY PORT PRESENCE STRAP

CFG4

0: ENABLED

AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

1: DISABLED; (DEFAULT)

NO PHYSICAL DISPLAY PORT ATTACHED TO THE EMBEDDED DISPLAY PORT

[17] MIPI60_CFG4_N — R5M19 1K_1%_2

TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

PP3300_SOC_A — R7D35 *4.7K_1%_2 — [10] GPPC_C_1

NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

PP3300_SOC_A — R8A7 *4.7K_1%_2 — [10] GPPC_C_2

TLS CONFIDENTIALITY

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

PP3300_SOC_A — R7D25 *4.7K_1%_2 — [8] GPPC_C_8_UART0_RXD

MAF/SAF STRAP

LOW-> MAF ENABLE
HIGH-> SAF ENABLE

WEAK INTERNAL PD 20K

PP3300_SOC_A — R1H18 *2.2K_1%_2 — [8] GPPC_D_11_GSPI2_MOSI_UART0A_CTSB

BOOT HALT

HIGH - DISABLED
LOW- ENABLED

NO INTERNAL PU/PD
SAMPLING - RSMRSTB

CHANGE PU TO 100K STARTING DVT

PP3300_SOC_A — R4F23 100K_1%_2 — R_DVT=100K — [8,17] GPPC_C_10_UART0_RTSB — R4F20 *20K_1%_2

FLASH DESCRIPTOR SECURITY OVERRIDE

HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

PP3300_SOC_A — R3C14 *4.7K_1%_2 — [8] GPPC_A_15

???

PP3300_SOC_A — R6C1 100K_1%_2 — [8] GPPC_E_6_IMGCLKOUT_3

CPUNSSC CLOCK FREQ

HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)

LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

PP3300_SOC_A — R4E63 *4.7K_1%_2 — [8] GP_C13_UART1_TXD

RESERVED

PP3300_SOC_A — R1G3 100K_1%_2 — [8] GPPC_D_9_GSPI2_CLK_UART0A_TXD — R1G1 *4.7K_1%_2

PP3300_SOC_A — R6D34 100K_1%_2 — [8,17] GPPC_D_8_GSPI2_CS0B_UART0A_RXD — R6D29 *4.7K_1%_2

RESERVED FOR CHROMEOS

PP1800_SOC_A — R105 *4.7K_1%_2 — [10] RSVD_STRAP — R107 100K_1%_2

XTAL SEL1

LOW: 38.4/19.2MHZ (DEFAULT)
HIGH = 24MHZ

(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

PP1800_SOC_A — R6D67 *4.7K_1%_2
PP3300_SOC_A — R6D66 *4.7K_1%_2
[8] CLK_24M_UCAM

M.2 CNVI MODES

LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE

NO INTERNAL PU/PD
SAMPLING - RSMRSTB

PP1800_SOC_A — R6D85 *20K_1%_2
PP3300_SOC_A — R6D84 20K_1%_2
[10,28] CNV_RGI_DT — R6D82 *4.7K_1%_2

1K PULLDOWN ON M.2 MODULE

RESERVED

THIS STRAP HAS A 20K INTERNAL PULL-DOWN

DO NOT PULL THIS PIN HIGH ON BOARD

PP3300_SOC_A — R6D41 *4.7K_1%_2 — [8] GPPC_D_10_GSPI2_MISO_UART0A_RTSB — R6D38 *20K_1%_2

RESERVED

THIS STRAP HAS A 20K INTERNAL PULL-DOWN

PP3300_SOC_A — R7D26 *4.7K_1%_2 — [12] GPD_7 — R7D24 *20K_1%_2

ESPI OR EC LESS

HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED

WEAK INTERNAL PD 20K

PP3300_SOC_A — R7D40 *4.7K_1%_2 — [8] GPPC_C_9_UART0_TXD

RESERVED

PP1050_OUT_PCH — R37 1K_1%_2 — [17] DBG_PMODE — R5G69 *1K_1%_2

THIS STRAP HAS A 20K INTERNAL PULL-UP

SPI VCCSIO CONFIGURATION

LOW: 3.3V

HIGH: 1.8V

NO INTERNAL PU/PD

SAMPLING - DSW_PWROK

PP3000_RTC — R3C18 *1M_1%_2 — [12] INTRUDER_L — R2C20 10K_1%_2

RESET SEQUENCE STALL

LOW: STALL

HIGH: NO STALL

INTERNAL PU(?)

STALLS AFTER PCU PLL LOCK UNTIL DEASSERTED

PP1050_VCCIO_EXT — R405 1K_1%_2 — [17] MIPI60_CFG0_N — R406 *1K_1%_2

BSSB LSX #0 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

PP3300_SOC_A — R6D46 *4.7K_1%_2 — [8] GP_E14_DDI0_DDC_SDA

BSSB LSX #1 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

PP3300_SOC_A — R6D42 *4.7K_1%_2 — [8] GP_E16_DDI1_DDC_SDA

BSSB LSX #2 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

PP3300_SOC_A — R6D40 *4.7K_1%_2 — [8] HDMI_DDC_SDA

BSSB LSX #3 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

PP3300_SOC_A — R6D39 *4.7K_1%_2 — [8] GPPC_E_12_IMGCLKOUT_4

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PROJECT : ZCA

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	JSL+: STRAPS	1A

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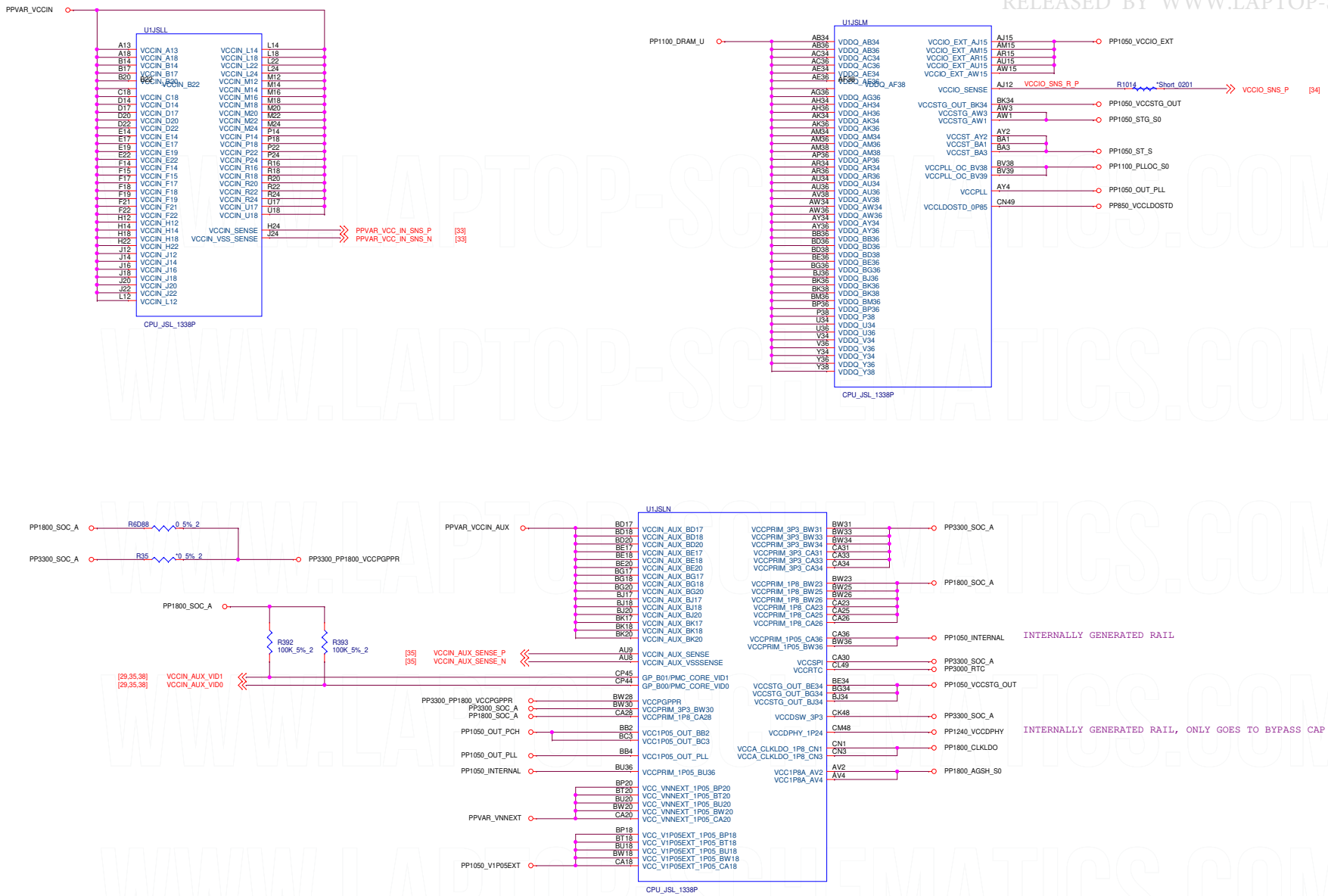

Quanta Computer Inc.		
PROJECT : ZCA		
Size	Document Number: JSL+: CPU AND PCH POWER	Rev 1A
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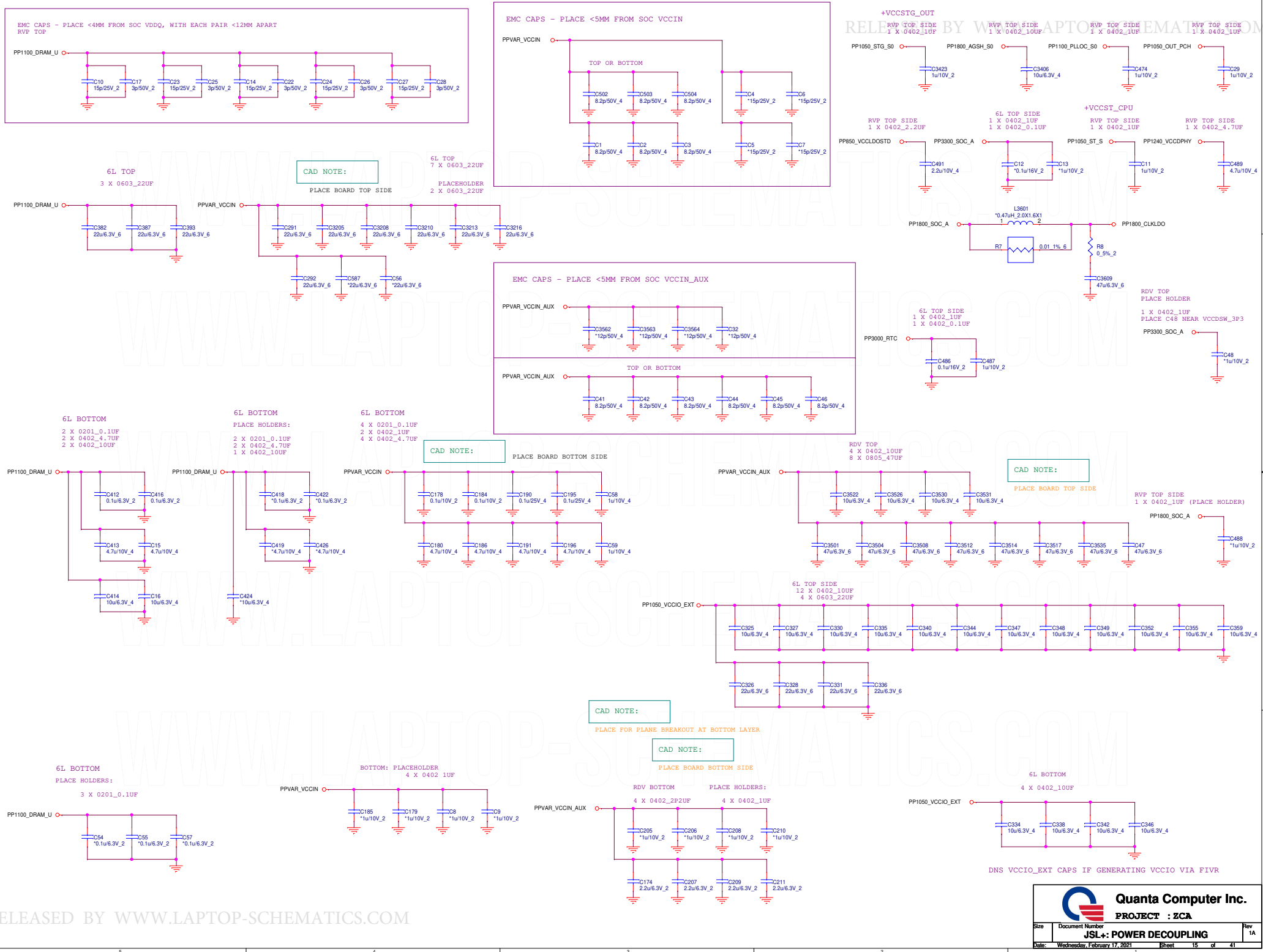

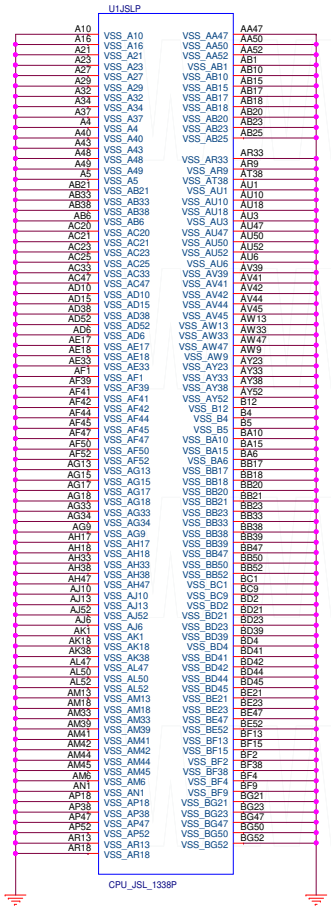

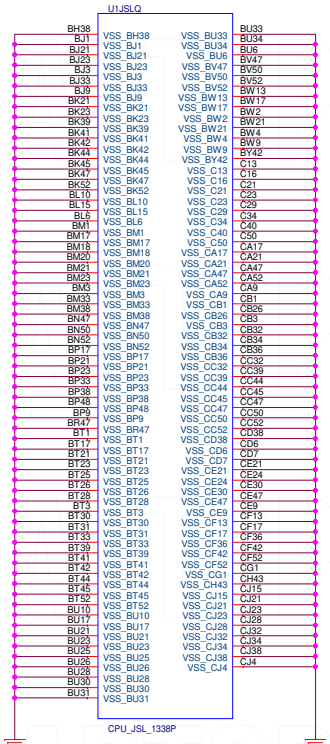

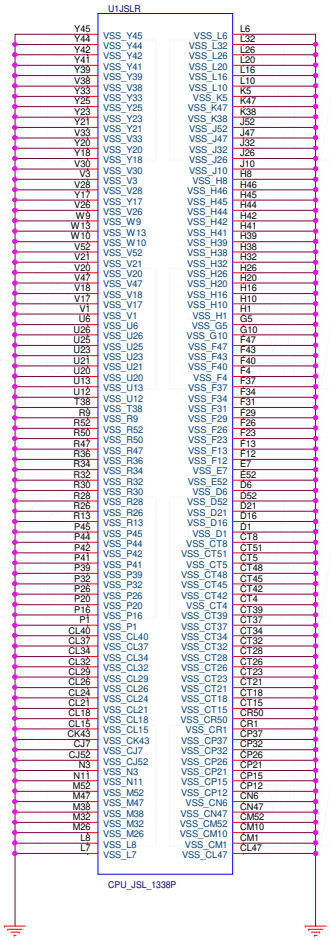

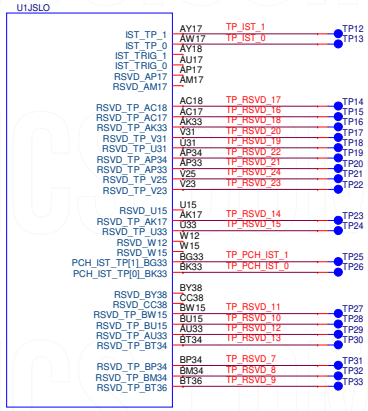

Quanta Computer Inc.

PROJECT : ZCA

Size	Document Number	Rev
	JSL+: GROUND, RESERVED	1A

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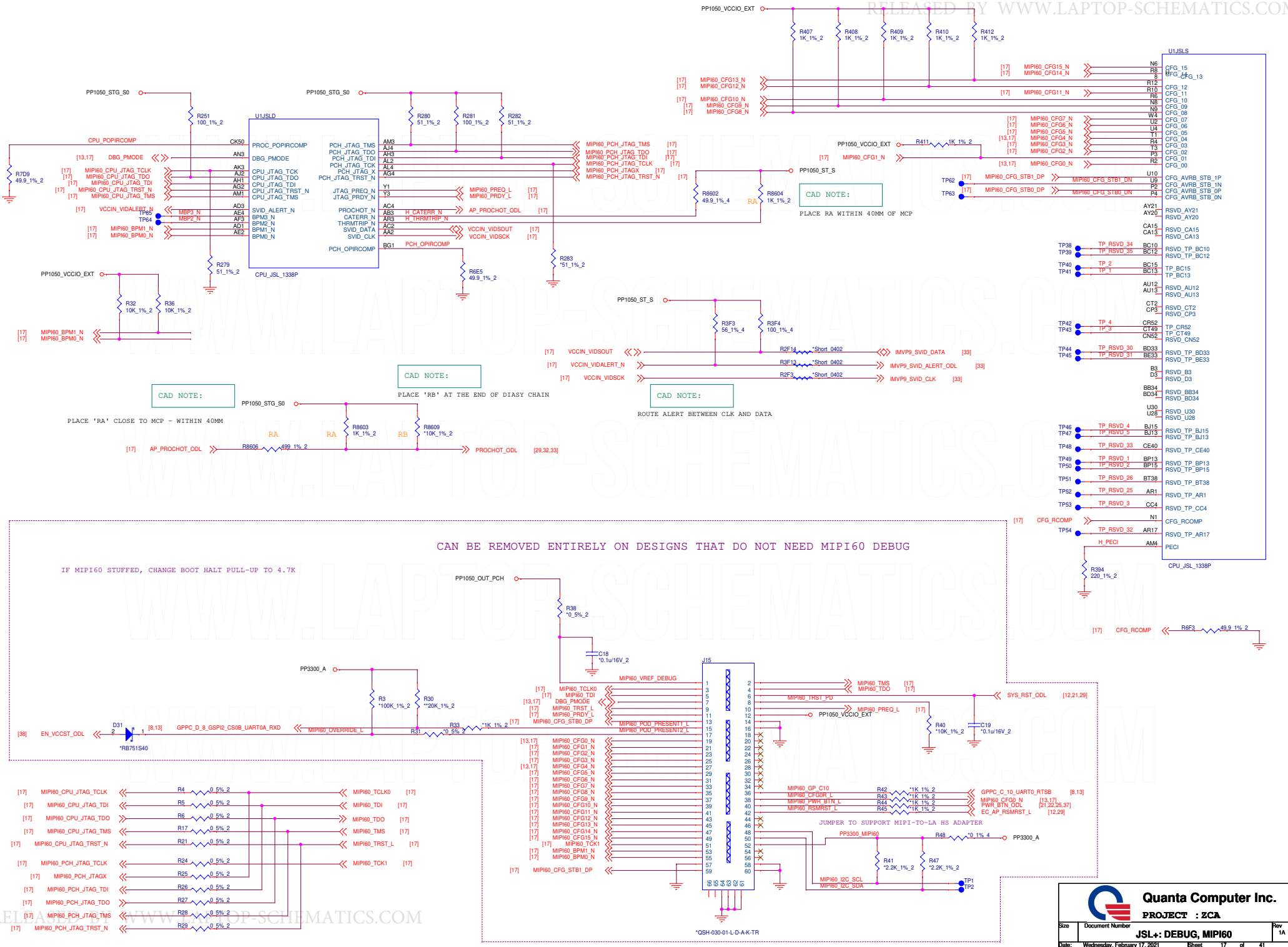
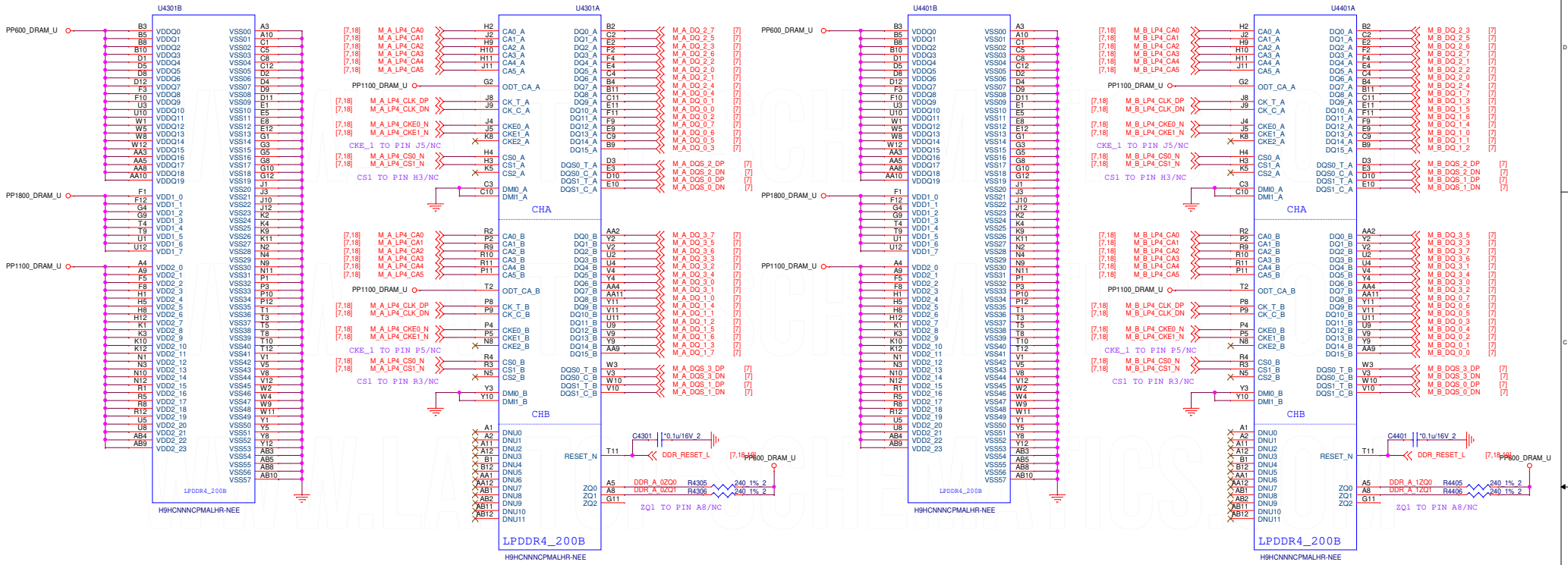
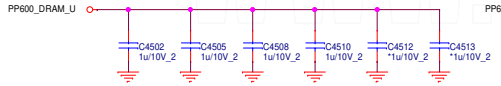


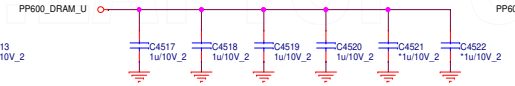
LPDDR4X 2933, 2GIB/PART

BIT SWAPPING IS ALLOWED WITHIN EACH BYTE

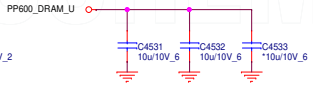


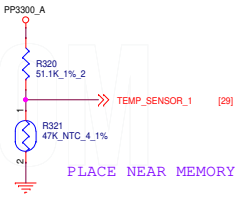
CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM



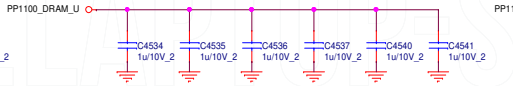


CAD NOTE: DISTRIBUTE EVENLY, 1 FOR EACH DRAM

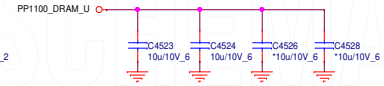




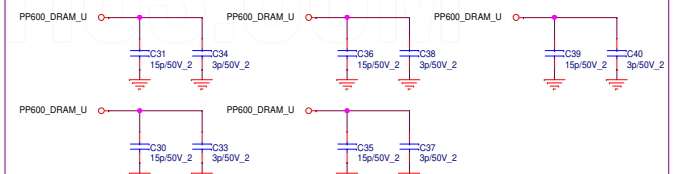
CAD NOTE: DISTRIBUTE EVENLY, 6 FOR EACH DRAM



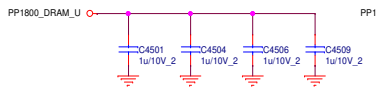
CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM

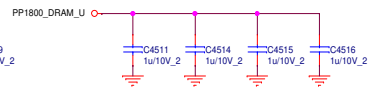


EMC CAPS - PLACE <4MM FROM MEMORY VDDQ, WITH EACH PAIR <12MM APART

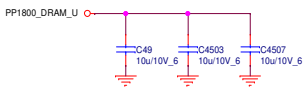


CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM





CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM



Quanta Computer Inc.

PROJECT : ZCA

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	LPDDR4X: CH A+B	1A

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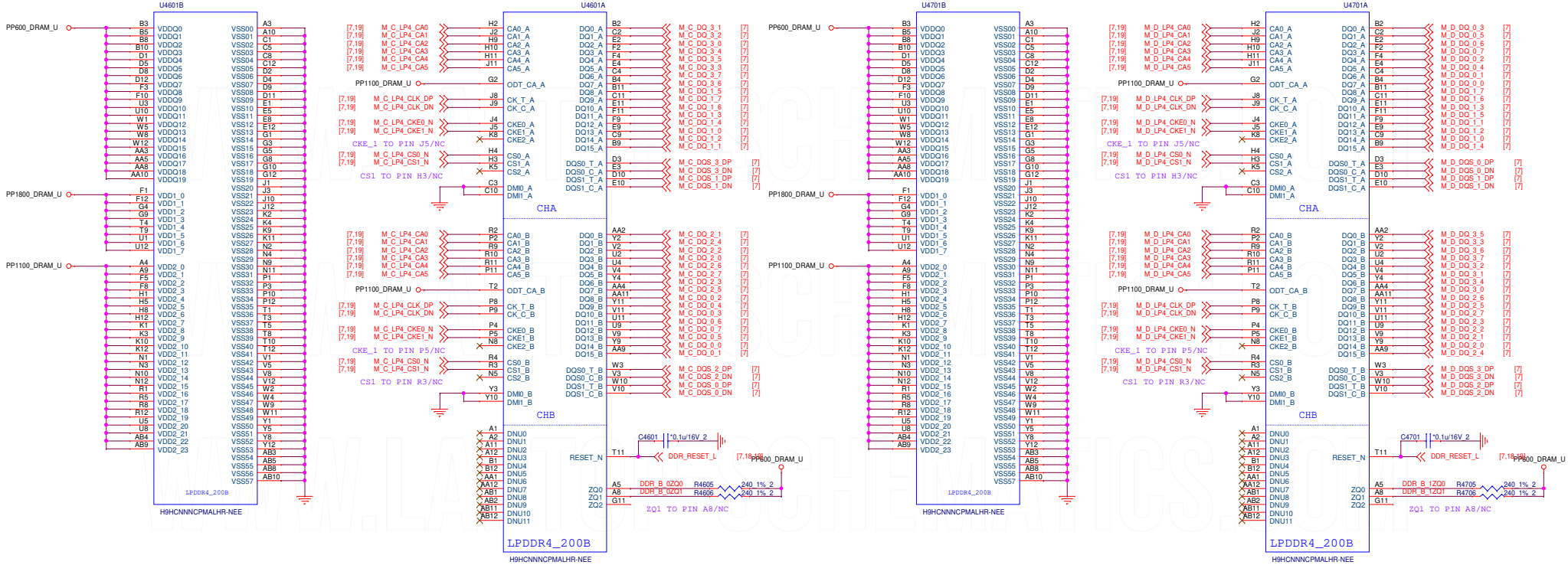
LPDDR4X 2933, 2GIB/PART

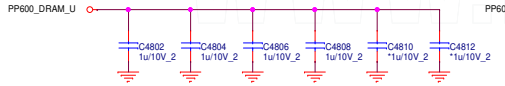
BIT SWAPPING IS ALLOWED WITHIN EACH BYTE

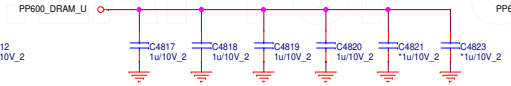


STRAPS				MPN
3	2	1	0	
0	0	0	0	MT53E512M32D2NP-046 WT:E,K4U6E3S4AA-MGCR,H9HCNNNBKMMLXR-NEE
0	0	0	1	MT53E1G32D2NP-046 WT:A
0	0	1	0	K4UBE3D4AA-MGCR
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

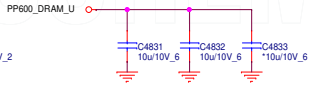
RAM_STRAP_4: 0=SINGLE-CHANNEL, 1=DUAL-CHANNEL

CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM

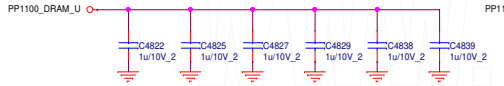


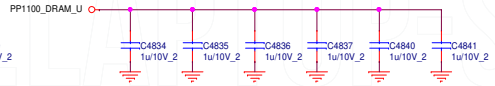


CAD NOTE: DISTRIBUTE EVENLY, 1 FOR EACH DRAM

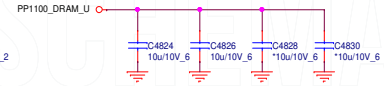


CAD NOTE: DISTRIBUTE EVENLY, 6 FOR EACH DRAM

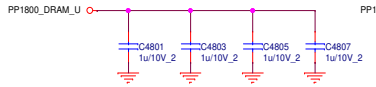


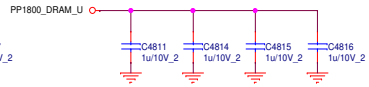


CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM

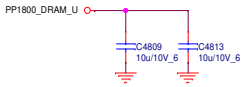


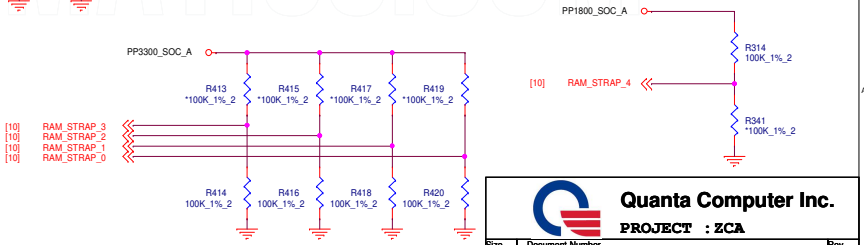
CAD NOTE: DISTRIBUTE EVENLY, 4 FOR EACH DRAM





CAD NOTE: DISTRIBUTE EVENLY FOR EACH DRAM





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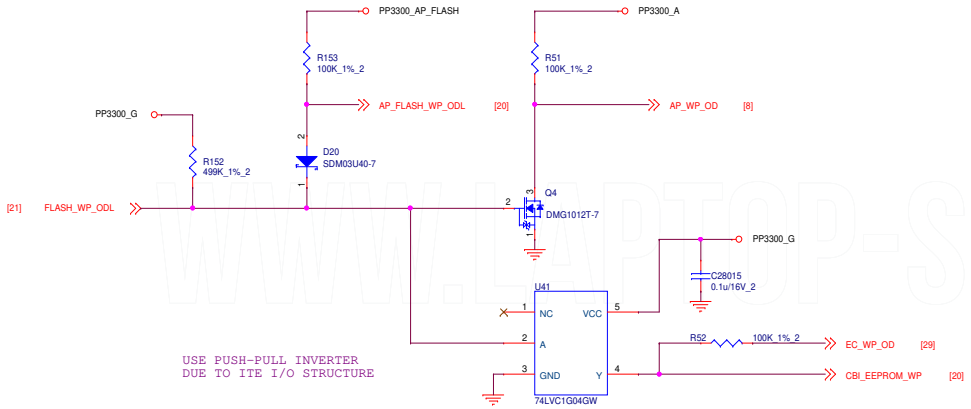
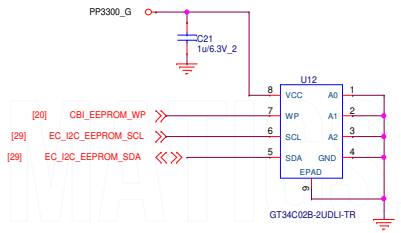
WP TREE

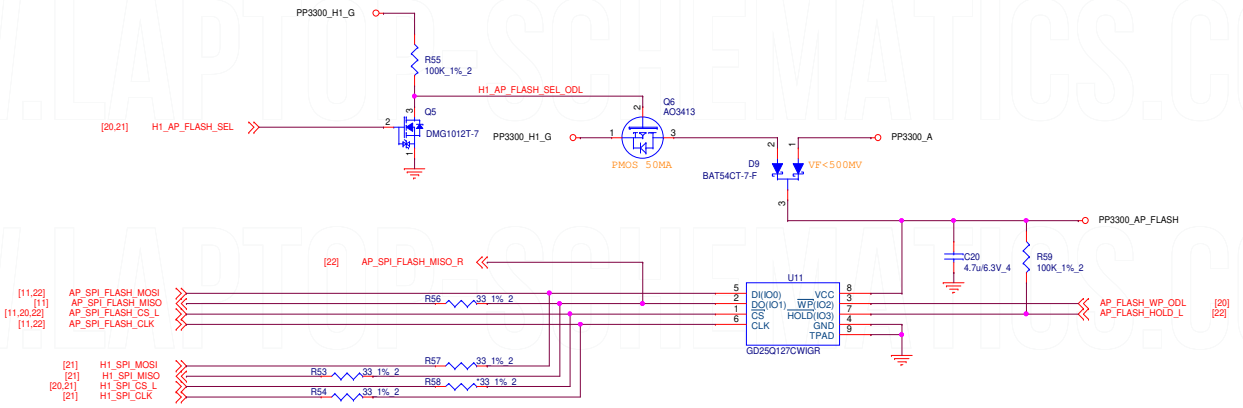


USE PUSH-PULL INVERTER
DUE TO ITE I/O STRUCTURE

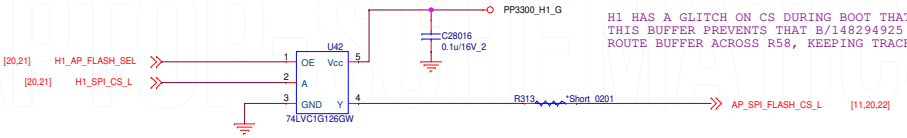
CBI EEPROM



SPI ROM



KEEP STUBS TO H1 SHORT



H1 HAS A GLITCH ON CS DURING BOOT THAT CAUSES LEAKAGE INTO THE PCH
THIS BUFFER PREVENTS THAT B/148294925
ROUTE BUFFER ACROSS R58, KEEPING TRACE LENGTH AS SHORT AS POSSIBLE

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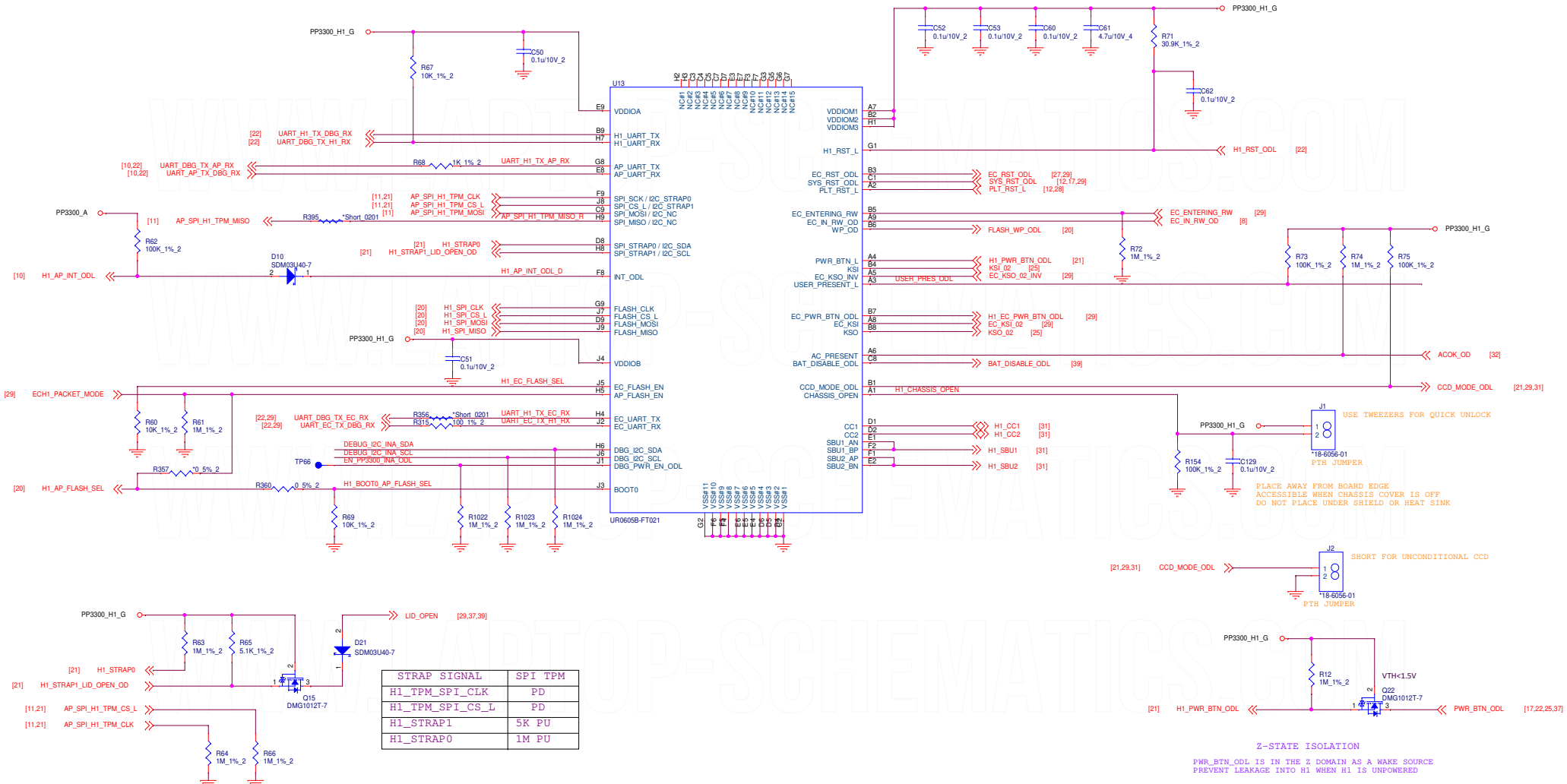

STRAP SIGNAL	SPI TPM
H1_TPM_SPI_CLK	PD
H1_TPM_SPI_CS_L	PD
H1_STRAP1	5K PU
H1_STRAP0	1M PU

Quanta Computer Inc.

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Size	Document Number	Rev
	H1	1A

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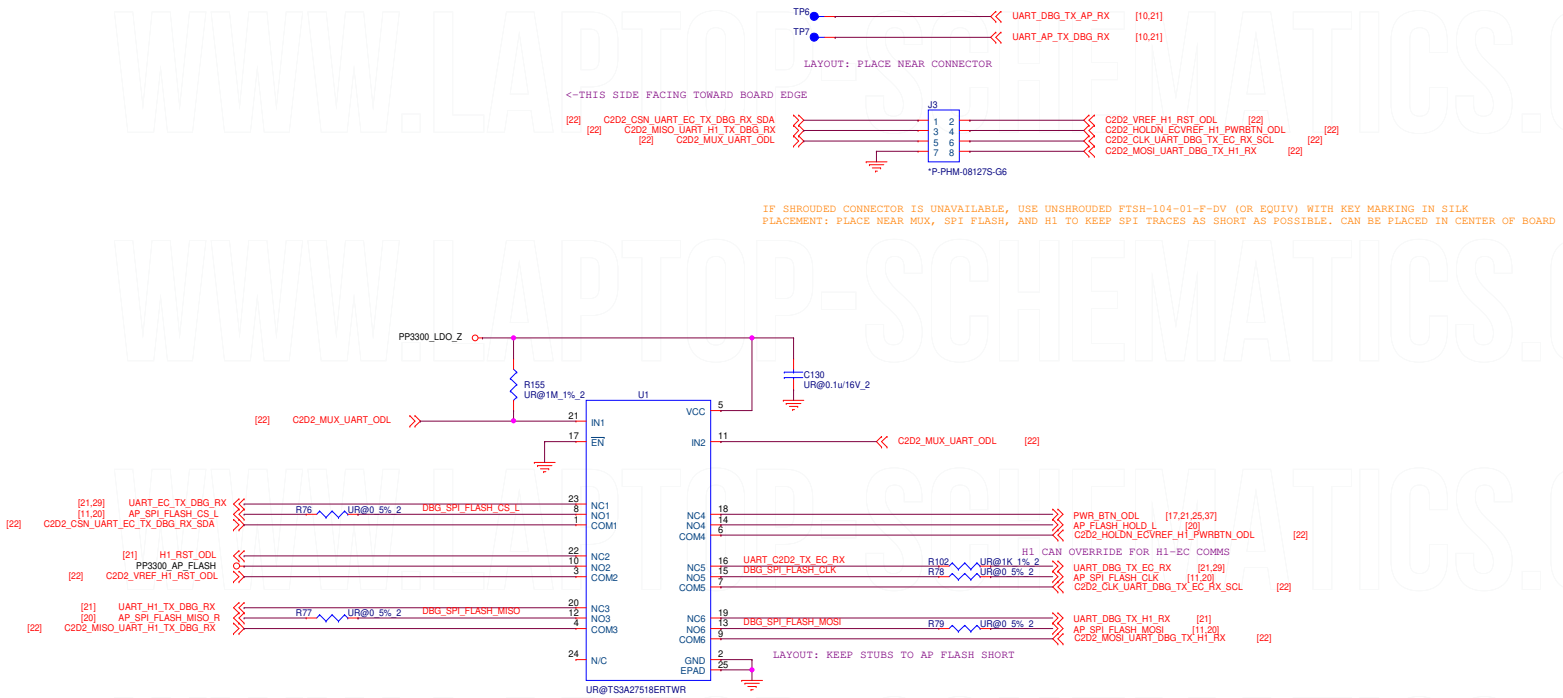
DNS ENTIRE PAGE IN DVT/PVT (EXCEPT LAB UNITS)



FOR SYSTEMS WITH I2C-FLASHED ECS, WHERE H1_VDDIOA=H1_VDDIOB=3.3V

SYSTEMS WITH SPI- OR UART-FLASHED ECS DO NOT REQUIRE THE EXTRA MUXING BASED ON H1_EC_FLASH_SEL

SYSTEMS WITH H1_VDDIOA!=3.3V NEED LEVEL SHIFTING ON H1_RST_ODL

SYSTEMS WITH H1_VDDIOB!=3.3V NEED LEVEL SHIFTING ON PWR_BTN_ODL

Quanta Computer Inc.

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	C2D2	1A

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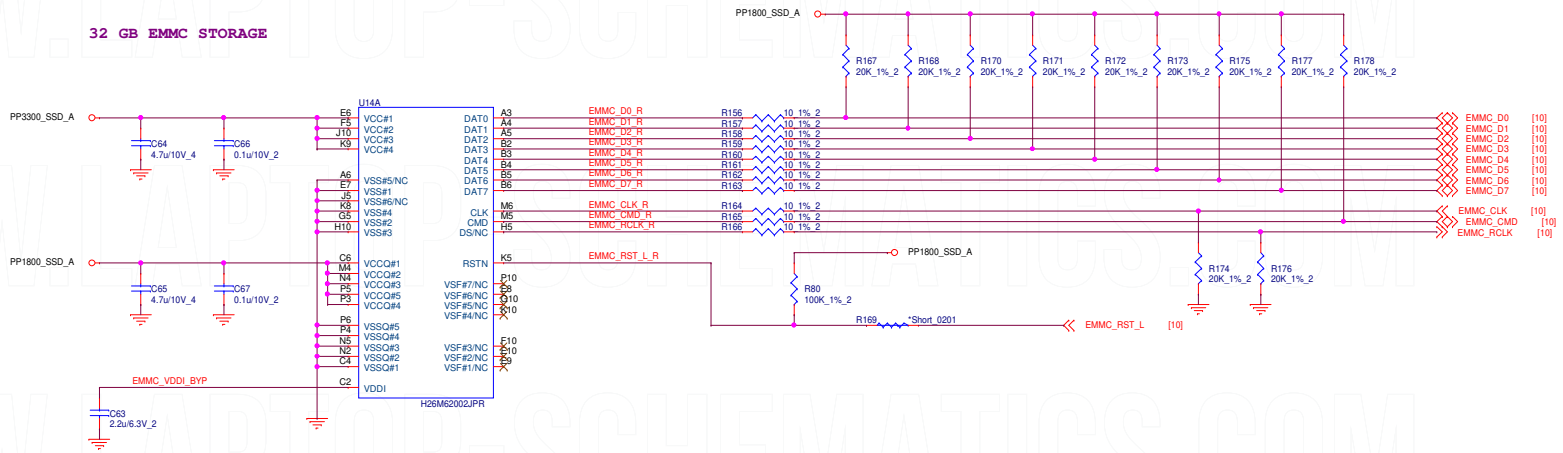
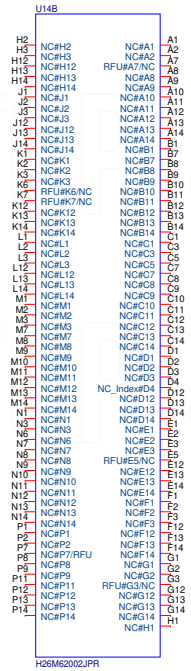
32 GB EMMC STORAGE



NOTE MOST EMMC 5.1 PART REQUIRES > 1 UF ON VDDI



NC/RFU/VSF LEAVE FLOATING

Quanta Computer Inc.		
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LEFT SPEAKER

PP5000_U — R179 0_5%_6 — PP5000_LSPK_U — C131 22u/25V_8 — C135 0.1u/16V_2
PP1800_A — R180 0_5%_2 — PP1800_LSPK_A — C132 0.1u/16V_2 — C136 0.1u/16V_2

U2 (ALC1015Q-CG, ADDR=7B'28)

Pin	Signal
6	VBAT
18	AVDD
12	DVDD
23	PVDD_1
24	PVDD_2
14	SDB
10	ASEL
9	SCL
8	SDA
7	BCLK
11	LRCK
13	DACDAT
20	VCM
19	A_LDO
5	B_LDO
31	LX_1
32	LX_2
3	BOOT
1	VBST_1
2	VBST_2
28	BST_P
27	SPK_OUTP
22	SPK_OUTN
21	BST_N
15	DGND
16	AGND
17	P_AGND
4	B_AGND
29	B_PGND_1
30	B_PGND_2
25	P_PGND_1
26	P_PGND_2
33	EPAD

BOOST FUNCTION UNUSED

[11,24] EN_SPK — R91329 *Short_0201
[8,24] AP_I2C_AUDIO_SCL — R91330 *Short_0201
[8,24] AP_I2C_AUDIO_SDA — R91331 *Short_0201
[10,24] I2S_SPK_BCLK
[10,24] I2S_SPK_LRCK
[10,24] I2S_SPK_AUDIO
LSPK_VCM — C133 1u/6.3V_2
LSPK_LDO — C134 1u/6.3V_2

LSPK_R_P — C137 0.22u/10V_2 — R181 *Short_0603 — LSPK_P
LSPK_R_N — C138 0.22u/10V_2 — R182 *Short_0603 — LSPK_N
[11,24] EN_SPK — R183 1M_5%_2

J4 (CI4204M2HRU-NH): LSPK_P, LSPK_N, RSPK_P, RSPK_N
C28020 1000p/25V_2 — C28019 1000p/25V_2 — C28018 1000p/25V_2 — C28017 1000p/25V_2

RIGHT SPEAKER

PP5000_U — R186 0_5%_6 — PP5000_RSPK_U — C139 22u/25V_8 — C143 0.1u/16V_2
PP1800_A — R187 0_5%_2 — PP1800_RSPK_A — C140 0.1u/16V_2 — C144 0.1u/16V_2

U4 (ALC1015Q-CG, ADDR=7B'29)

Pin	Signal
6	VBAT
18	AVDD
12	DVDD
23	PVDD_1
24	PVDD_2
14	SDB
10	ASEL
9	SCL
8	SDA
7	BCLK
11	LRCK
13	DACDAT
20	VCM
19	A_LDO
5	B_LDO
31	LX_1
32	LX_2
3	BOOT
1	VBST_1
2	VBST_2
28	BST_P
27	SPK_OUTP
22	SPK_OUTN
21	BST_N
15	DGND
16	AGND
17	P_AGND
4	B_AGND
29	B_PGND_1
30	B_PGND_2
25	P_PGND_1
26	P_PGND_2
33	EPAD

BOOST FUNCTION UNUSED

[11,24] EN_SPK — R91332 *Short_0201
[8,24] AP_I2C_AUDIO_SCL — R91333 *Short_0201
[8,24] AP_I2C_AUDIO_SDA — R91334 *Short_0201
[10,24] I2S_SPK_BCLK
[10,24] I2S_SPK_LRCK
[10,24] I2S_SPK_AUDIO
RSPK_VCM — C141 1u/6.3V_2
RSPK_LDO — C142 1u/6.3V_2

RSPK_R_P — C145 0.22u/10V_2 — R189 *Short_0603 — RSPK_P
RSPK_R_N — C146 0.22u/10V_2 — R190 *Short_0603 — RSPK_N

PP1800A_HP
PP1800_A — R85 *Short_0201 — C77 2.2u/6.3V_4 — C81 0.1u/16V_2 — AGND_HP
PP1800_A — R86 *Short_0201 — PP1800_HP_IO — C78 1u/16V_4
PP1800_A — R82 *Short_0201 — C71 2.2u/6.3V_4 — C74 0.1u/16V_2
PP3300_A — R83 *Short_0201 — C72 2.2u/6.3V_4 — C75 0.1u/16V_2 — AGND_HP
C80 1u/16V_4
PP3300_G — R81 *Short_0201 — PP3300_HP_VBAT — C68 1u/16V_4 — AGND_HP

HP IS POWERED FROM THE _A POWER DOMAIN TO MAINTAIN REGISTER STATES ON RESUME

TO RESET THE ALC5682I, WRITE ANY VALUE TO REGISTER 0X000
THE ALC5682I ALSO RESETS FROM A POR

U3 (ALC5682I-VD-CGT, ADDR=7B'1A)

Pin	Signal
10	AVDD
30	DBVDD
26	DCVDD
20	LDO1_IN
40	MICVDD
1	VBAT
9	VREF2
25	CPVEE
17	CPVPP
13	DACREF
3	MIC_CAP
24	CPP1
21	CPN1
22	CPP2
23	CPN2
29	MCLK
31	BLCK1
32	LRCK1/GPIO6
33	ADCDAT1/ADCDAT2/DMIC_CLK/GPIO4
34	DACDAT1/DMIC_DAT/GPIO5
37	DMIC_DAT/LRCK2/GPIO2
36	DMIC_CLK/BCLK2/GPIO3
28	I2C_SDA
27	I2C_SCL
35	GPIO1/IRQ
19	CPVREF
11	AGND
41	EPAD
39	MICBIAS1
6	IN1P_RING2
14	RING2_SENSE
8	RING2_GND
16	HPOL
2	JDH
12	JDL
4	MIC_IN_DET
18	HPOR
38	MICBIAS2
5	IN1P_SLEEVE
15	SLEEVE_SENSE
7	SLEEVE_GND

[10] I2S_MCLK
[10] I2S_HP_BCLK
[10] I2S_HP_LRCK
[10] I2S_HP_MIC
[10] I2S_HP_AUDIO
[8,24] AP_I2C_AUDIO_SDA — R91335 *Short_0201
[8,24] AP_I2C_AUDIO_SCL — R91336 *Short_0201
PP1800_A — R84 10K_5%_2
[11] HP_INT_ODL
R87 *Short_0201 — R91339 *Short_0201 — AGND_HP

C82 2.2u/10V_4 — C83 2.2u/10V_4
C69 2.2u/10V_4 — C70 2.2u/10V_4 — C73 2.2u/10V_4 — C76 2.2u/10V_4 — C79 4.7u/6.3V_4 — AGND_HP

HP_MIC_BIAS1 — R89 2.2K_5%_2
HP_MIC_N — C84 1u/16V_4
HP_RING2_SENSE — R90 *Short_0201
HP_GND_RING2 — R91 *Short_0201
HP_LEFT — R92 *Short_0402 — R184 *5.11K_1%_2 — AGND_HP
HP_JACK_DET_L — R88 1M_1%_2 — PP1800A_HP — P3
PP3300_HP_VBAT — R188 100K_1%_2
HP_RIGHT — R94 *Short_0402 — R185 *5.11K_1%_2 — AGND_HP
HP_MIC_BIAS2 — R95 2.2K_5%_2
HP_MIC_P — C85 1u/16V_4
HP_SLEEVE_SENSE — R96 *Short_0201
HP_GND_SLEEVE — R97 *Short_0201

HEADPHONE JACK

HP_RING2 — HP_TIP — R93 *Short_0402 — HP_TERM_MAKETERM — HP_RING1 — HP_SLEEVE
J16 (2SJ3080-123111F): G/M, L, R, M/G — AGND_HP
D11 PESD5V0V1BDSF — D12 PESD5V0V1BDSF — D13 PESD5V0V1BDSF — D14 PESD5V0V1BDSF — D15 PESD5V0V1BDSF

LAYOUT NOTES

ROUTE SENSE SIGNALS CLOSE TO JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE DIFFERENTIALLY
ROUTE HP_SLEEVE AND HP_SLEEVE_SENSE DIFFERENTIALLY

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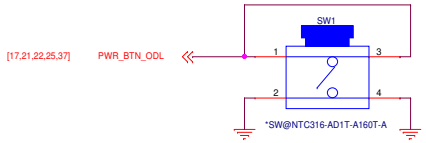
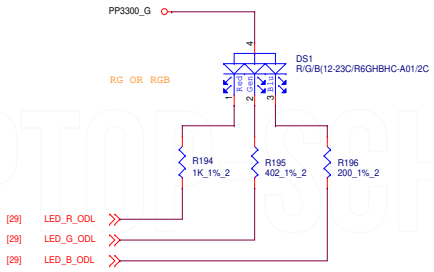
BUTTONS (IF ON MLB)

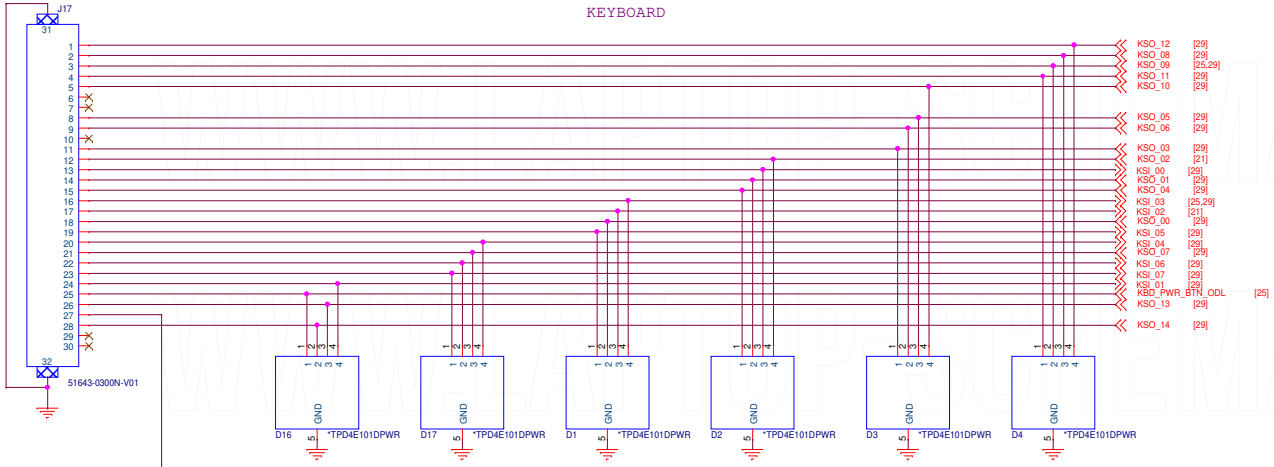


LEDS

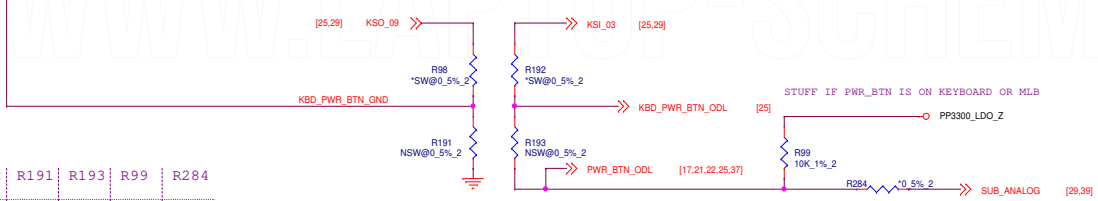
ADJUST RESISTORS TO MATCH SELECTED LED



KEYBOARD



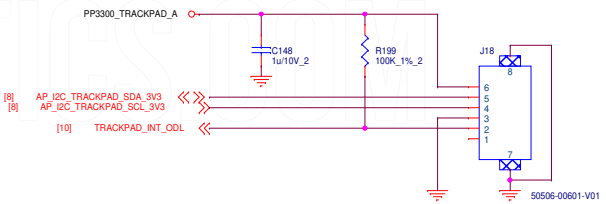
STUFF THESE FOR KEYBOARD LOCK BUTTON (CONVERTIBLES)



STUFF THESE FOR KEYBOARD POWER BUTTON

PWR BTN	R98	R192	R191	R193	R99	R284
ON KBD	DNS	DNS	0R	0R	10K	DNS
ON MLB	0R	0R	DNS	DNS	10K	DNS
SUB_ANA	0R	0R	DNS	DNS	DNS	0R
SUB_DIG	0R	0R	DNS	DNS	10K	DNS

TRACKPAD



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	KB,BTNS,LEDS,TRACKPAD	1A

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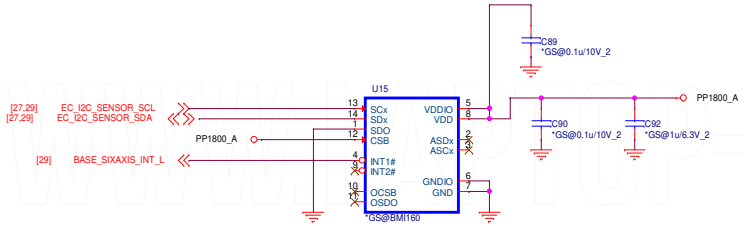
SIXAXIS

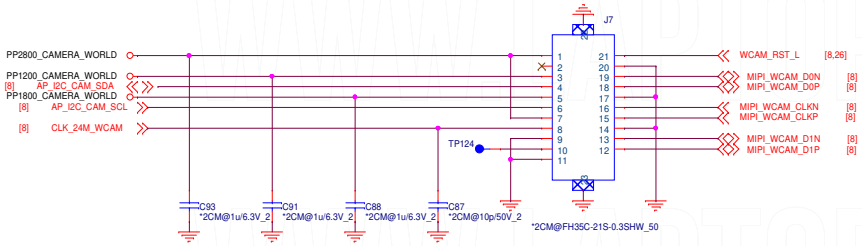


PLACE AS CLOSE TO WCAM AS POSSIBLE

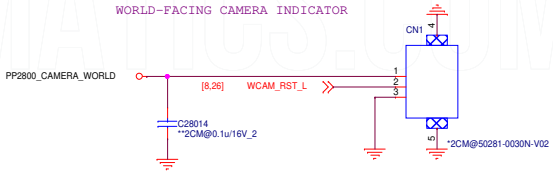
WORLD-FACING CAMERA

ADDRESS = 0X??

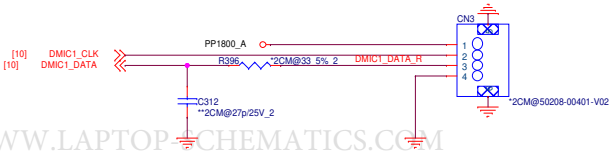
PLACEHOLDER/CONNECTOR DOESN'T MATCH ANYTHING



WORLD-FACING CAMERA INDICATOR



TO WORLD-FACING MIC MODULE



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	SENSORS	1A

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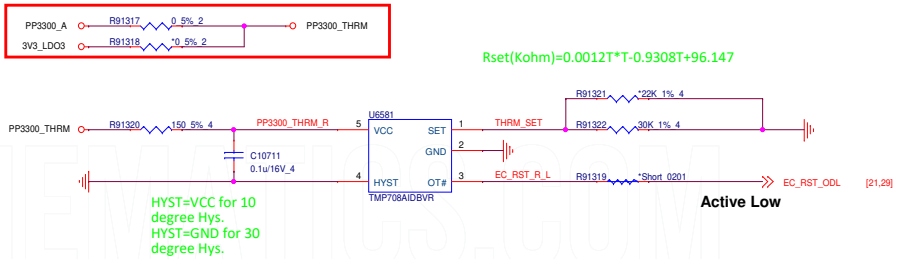
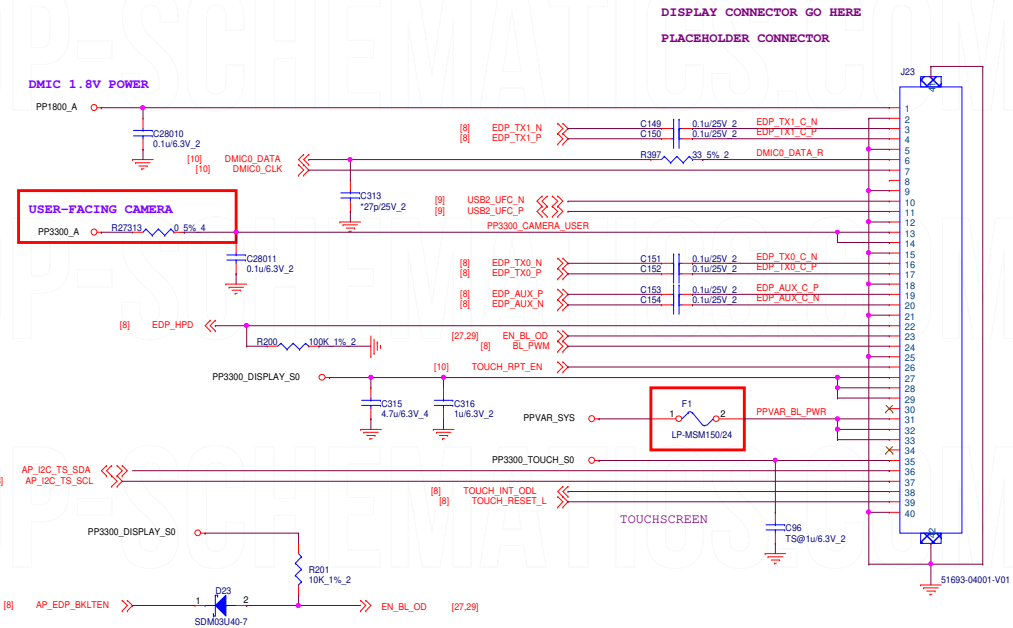
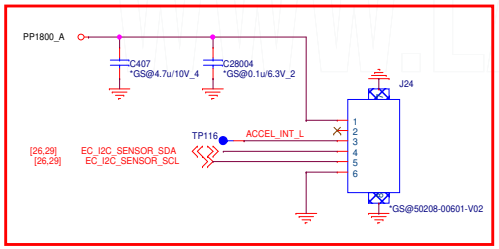
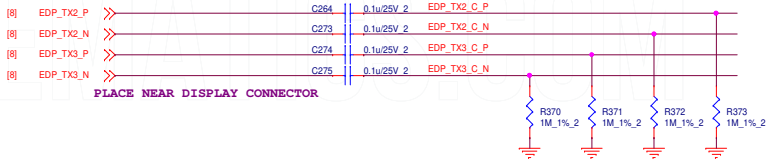
Thermal Protector

[OEM] BOM option

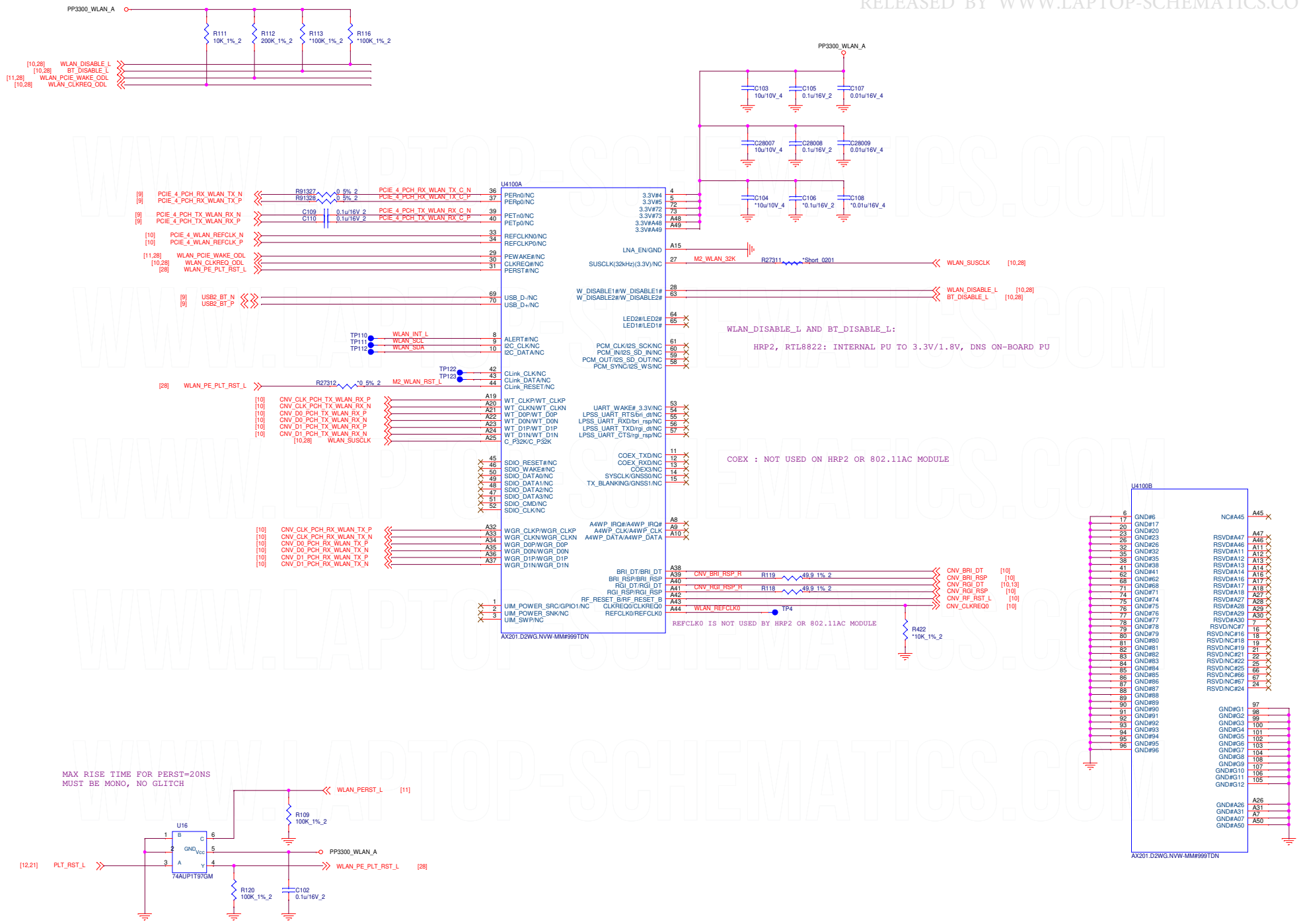








Quanta Computer Inc.		
PROJECT : ZCA		
Size	Document Number: LID: DISPLAY, CAMERA, SENSORS	Rev 1A
Date: Wednesday, February 17, 2021	Sheet 27 of 41	



Quanta Computer Inc.

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Size	Document Number	Rev
	WIFI, BT	1A

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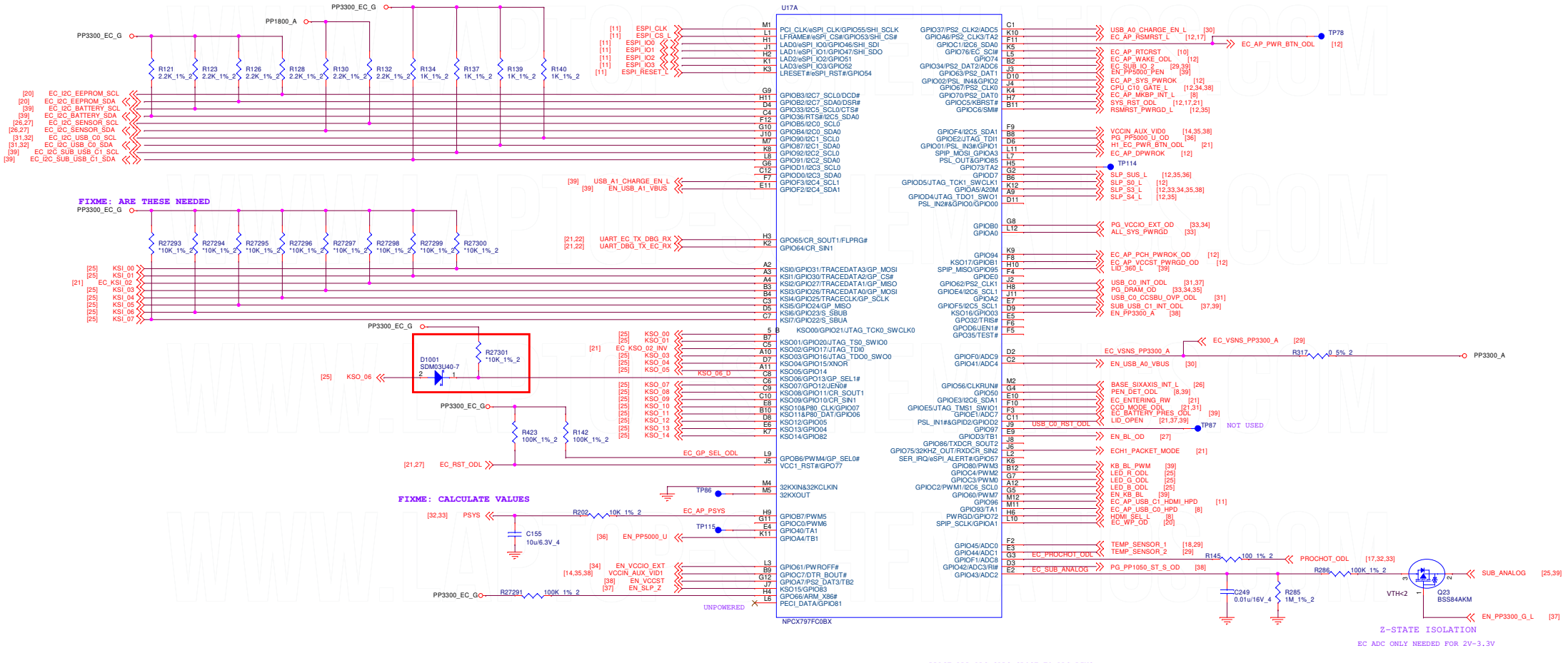

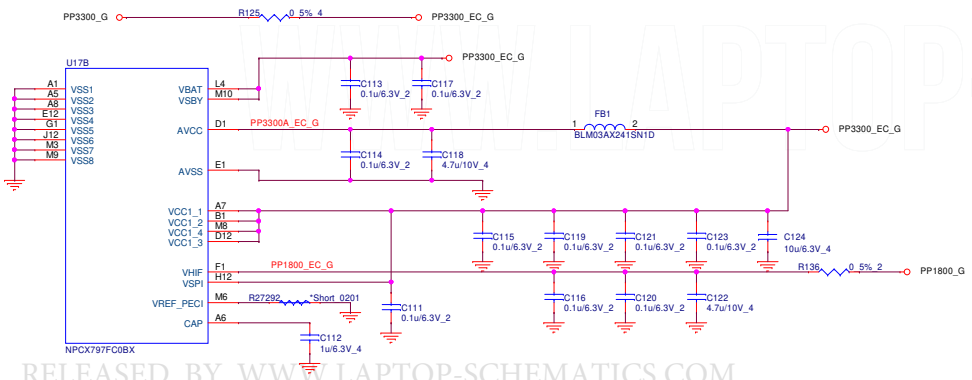

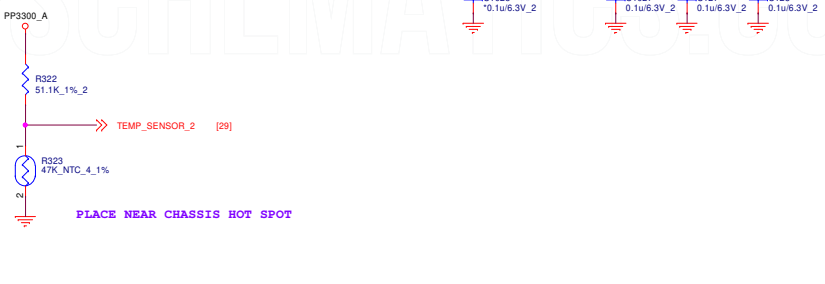

Quanta Computer Inc.			
PROJECT : ZCA			
Size	Document Number		Rev
	EC		1A
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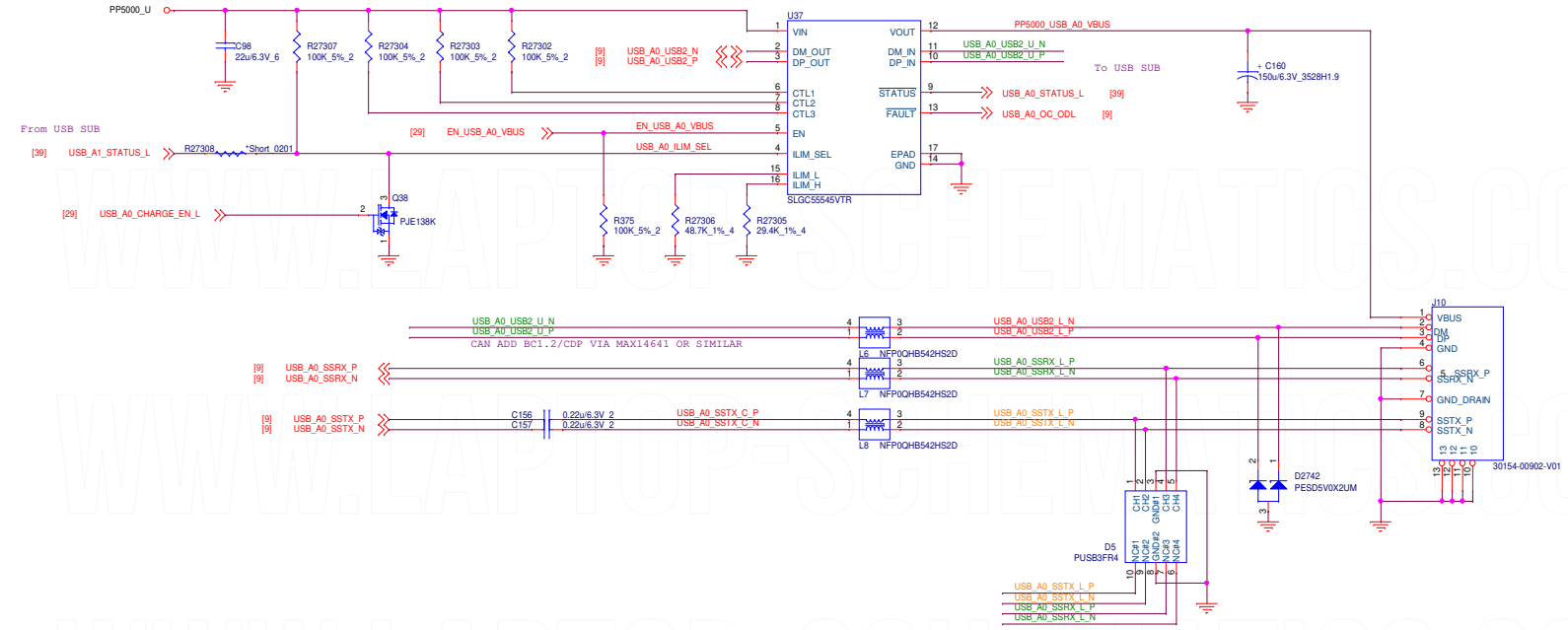

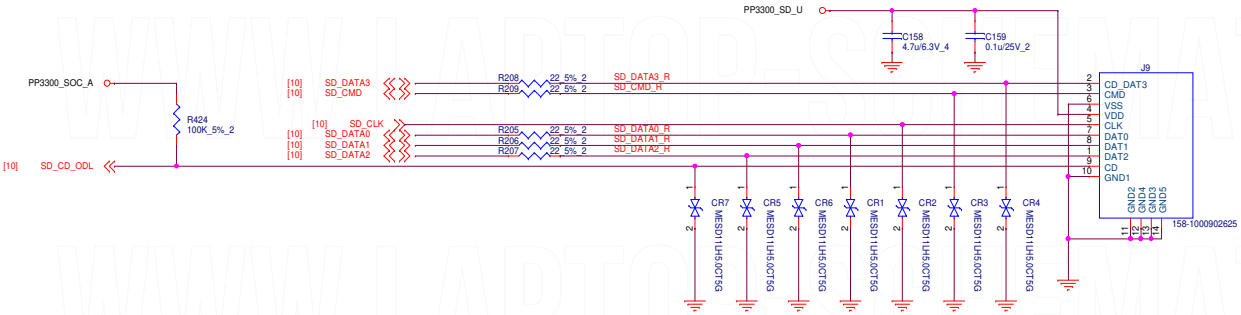

Quanta Computer Inc.

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Size	Document Number	Rev
	USB-A, SD	1A

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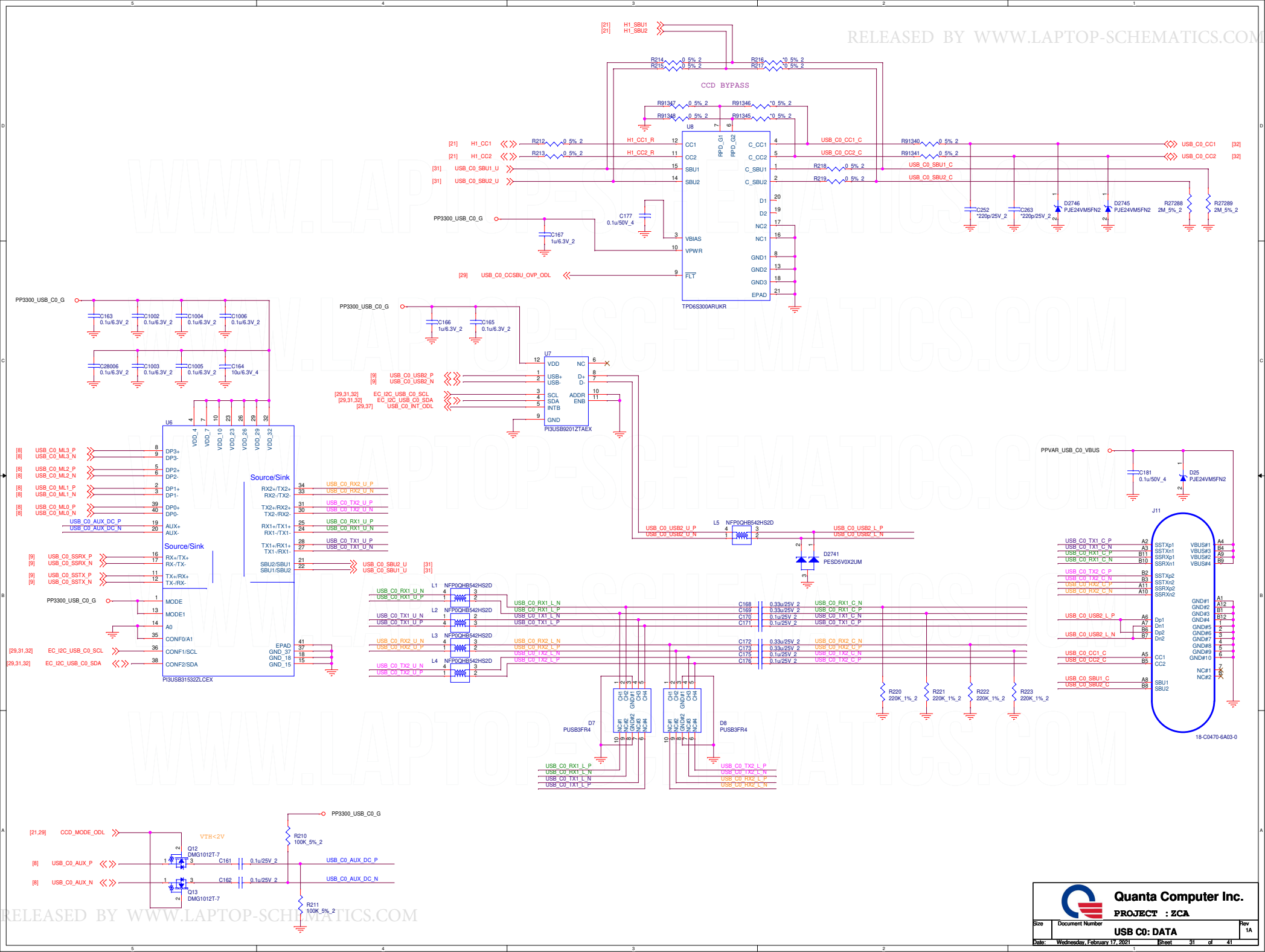

Quanta Computer Inc.

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Size	Document Number	Rev
	USB C0: DATA	1A

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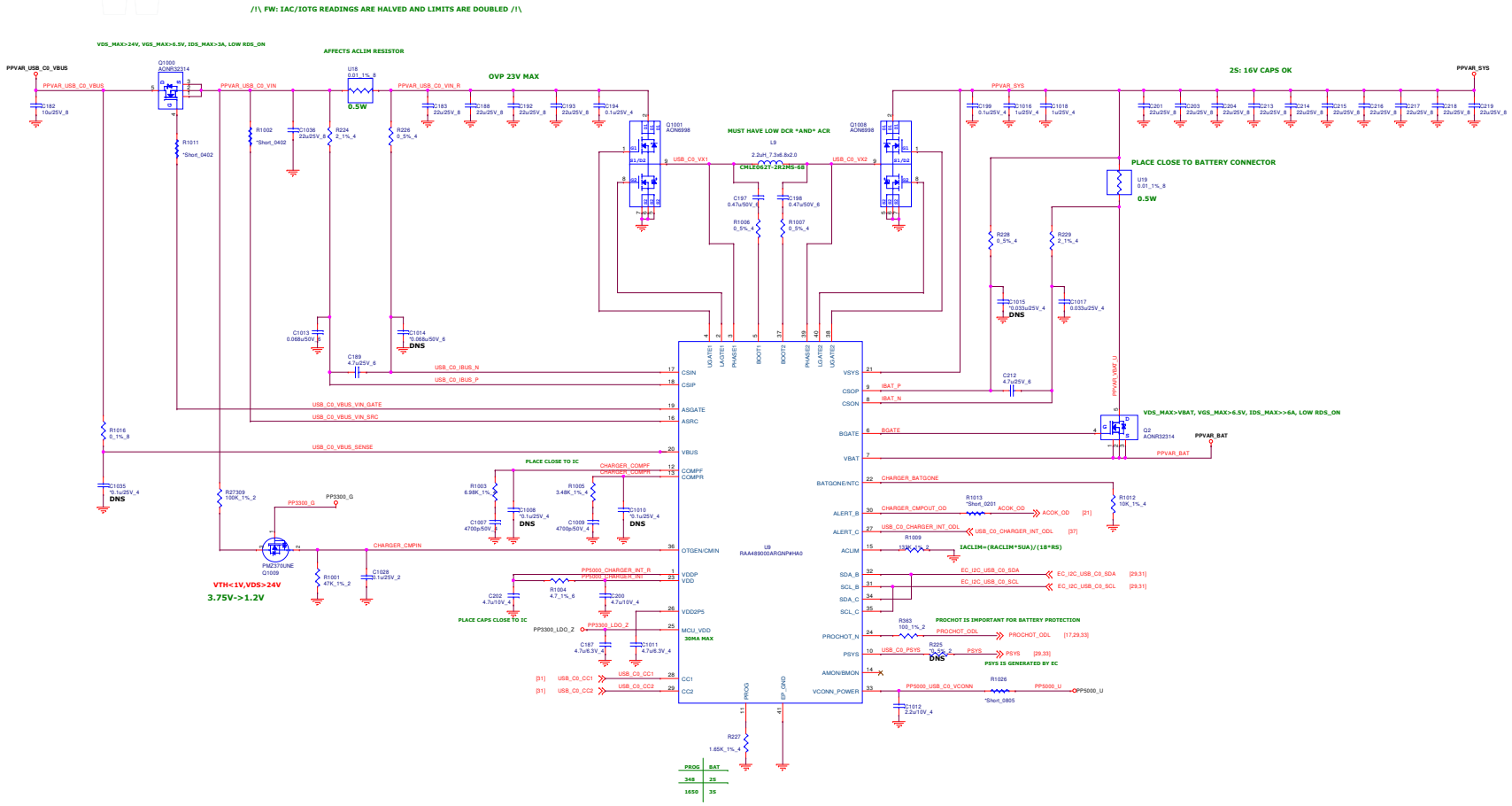

Quanta Computer Inc.

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	USB C0: BATTERY CHARGER	1A

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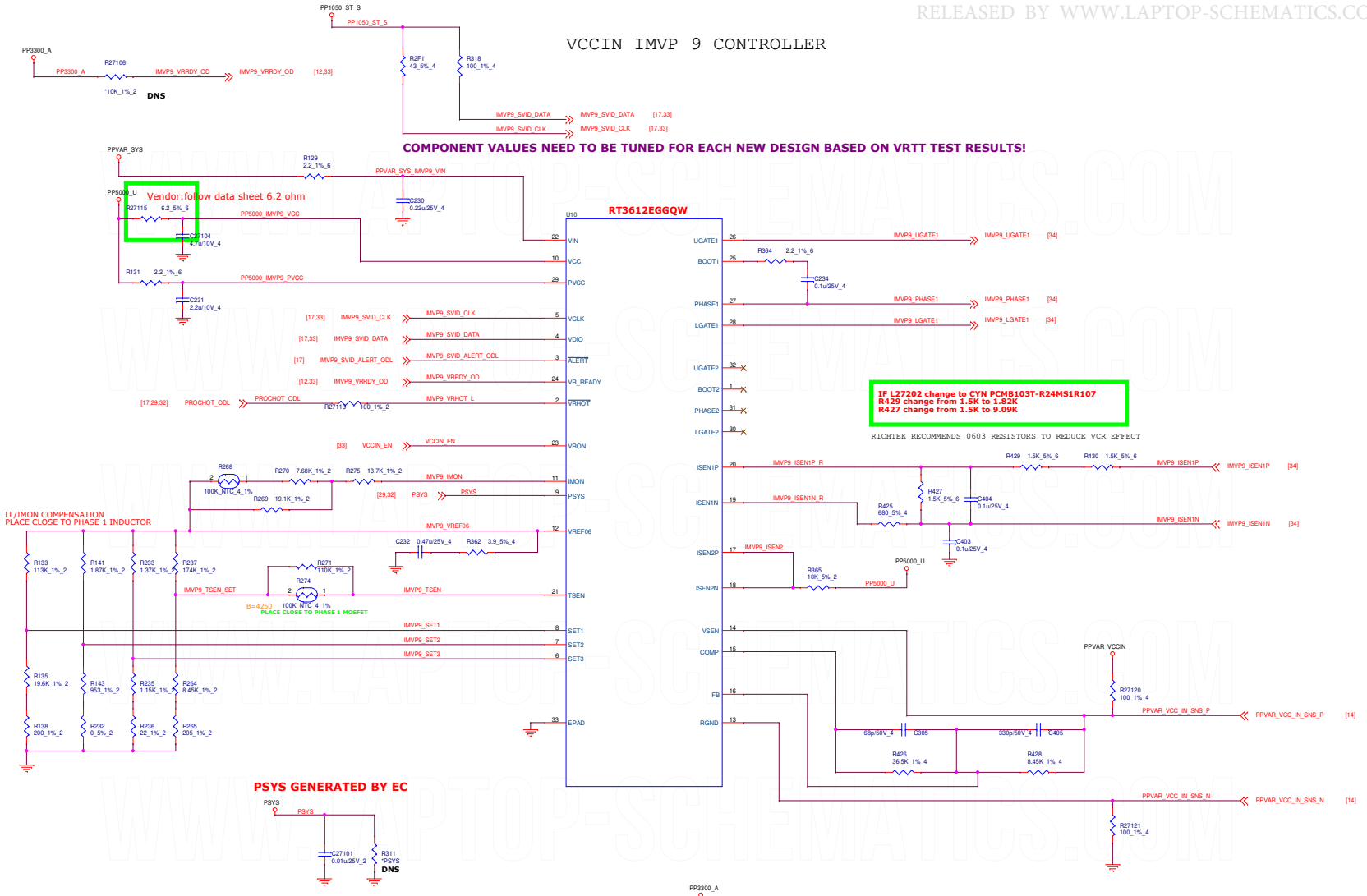
VCCIN IMVP 9 CONTROLLER



PARAMETER	SETTING
OUTPUT VOLTAGE	VID SELECTABLE
LOAD CURRENT	35 A
OCP	56 A
FREQUENCY	564 KHZ @ TDC
SOFT START	NA
LOAD LINE	2 MOHM

Quanta Computer Inc.

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POWER: SOC RAILS 1 | 1A

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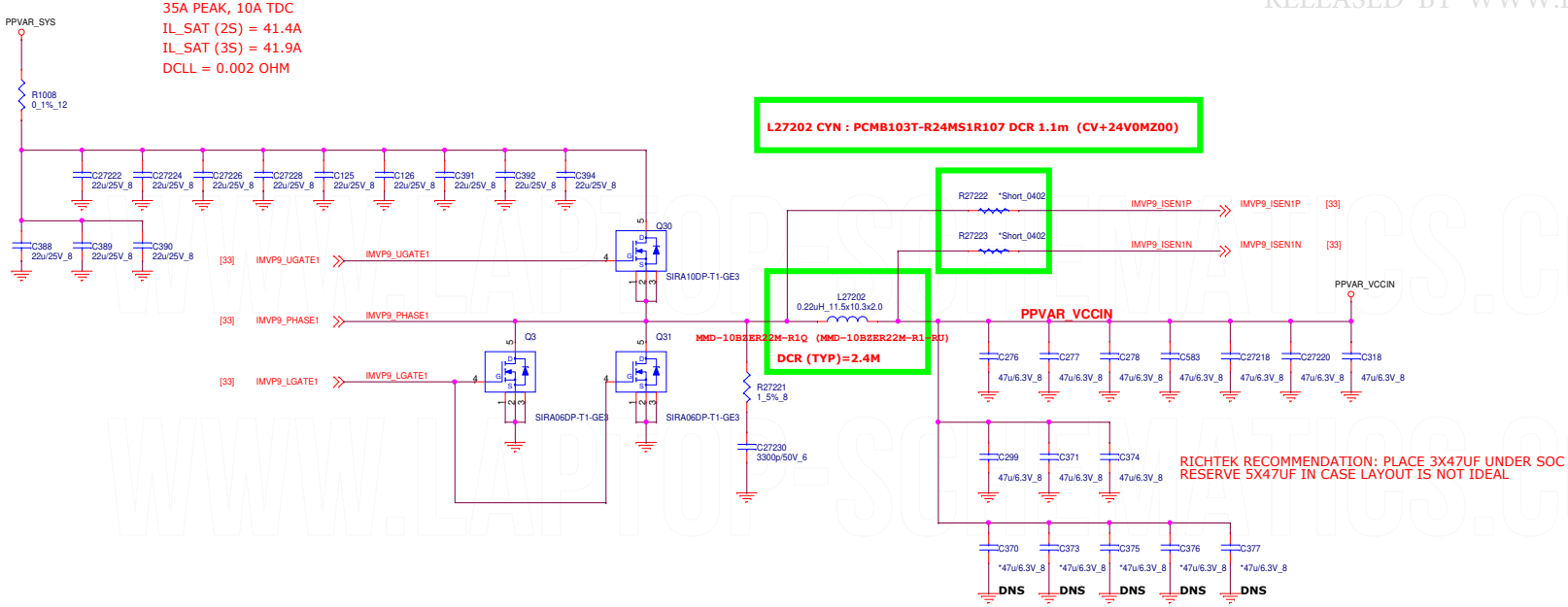
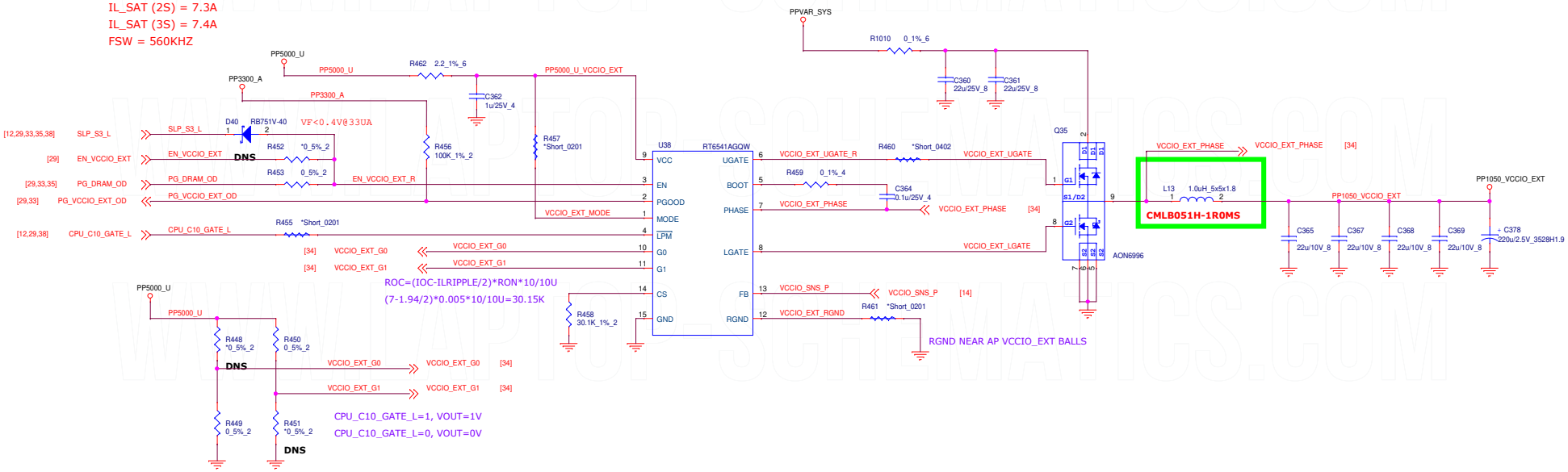
VCCIN POWER CONVERSION

35A PEAK, 10A TDC
IL_SAT (2S) = 41.4A
IL_SAT (3S) = 41.9A
DCLL = 0.002 OHM



VCCIO_EXT

IPEAK = 6.5A
IL_SAT (2S) = 7.3A
IL_SAT (3S) = 7.4A
FSW = 560KHZ



Quanta Computer Inc.			
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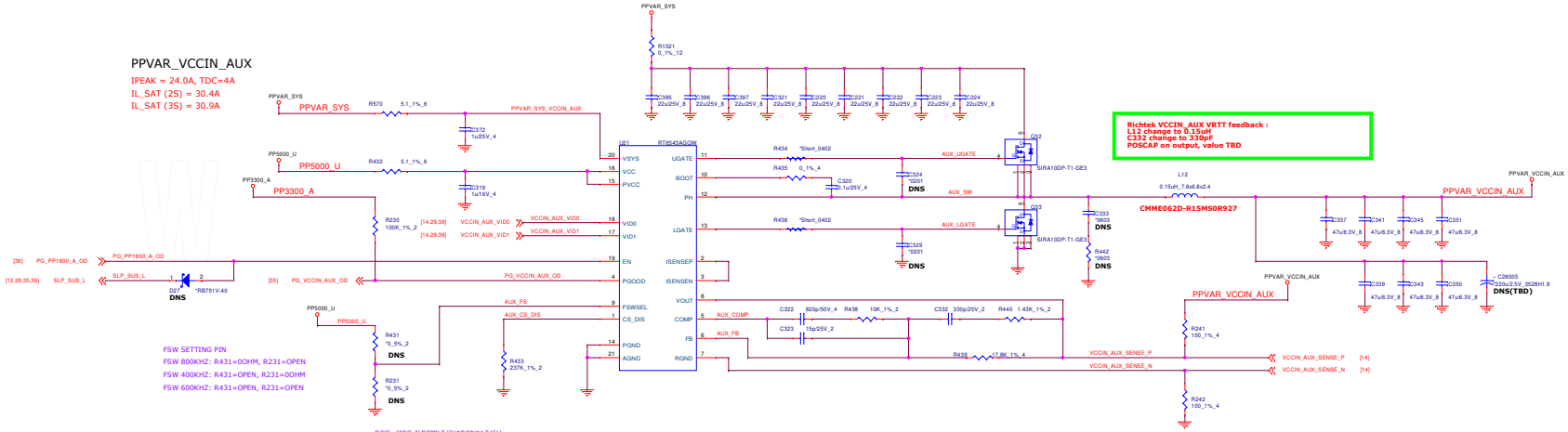
PPVAR_VCCIN_AUX

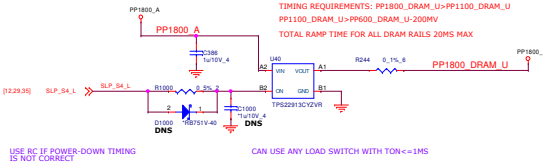
IPEAK = 24.0A, TDC=4A
IL_SAT (2S) = 30.4A
IL_SAT (3S) = 30.9A



Richtek VCCIN_AUX VRTT feedback :
L12 change to 0.15uH
C332 change to 330pF
POSCAP on output, value TBD

PP1800_DRAM_U

IPEAK = 0.3A



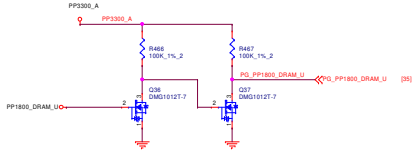
PP1100_DRAM_U

IPEAK = 6.51A
IL_SAT (2S/3S) = 7.9A

TIMING REQUIREMENTS: PP1800_DRAM_U>PP1100_DRAM_U
PP1100_DRAM_U>PP600_DRAM_U-200MV
TOTAL RAMP TIME FOR ALL DRAM RAILS 20MS MAX

PP600_DRAM_U

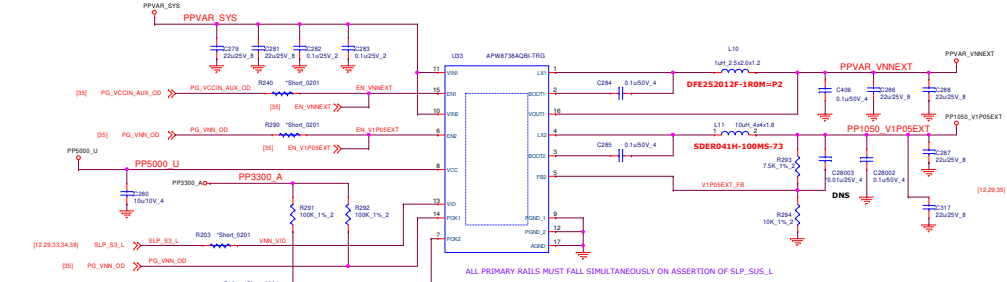
IPEAK = 0.99A

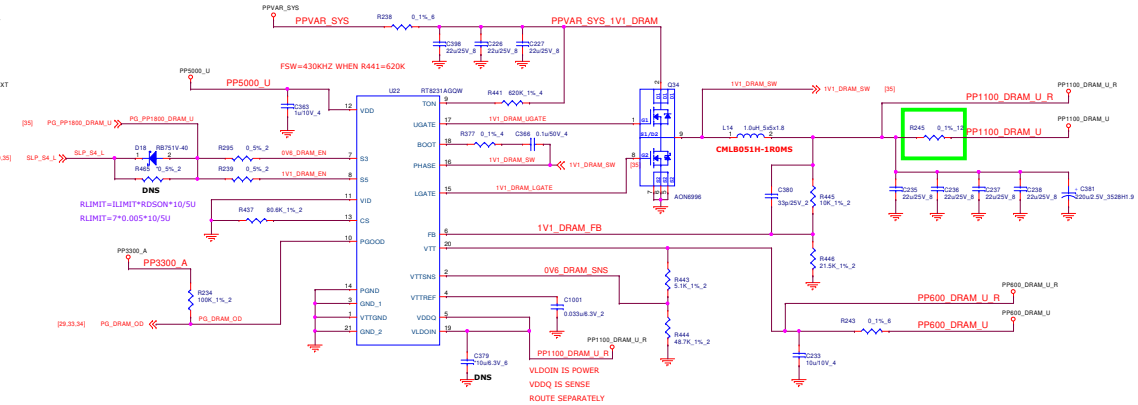


PPVAR_VNNEXT & PP1050_V1P05EXT BYPASS RAILS

IMAX = 0.5A
IL_SAT (2S/3S) = 1A
FSW = 800KHZ

IMAX = 0.5A
IL_SAT (2S/3S) = 0.6A
FSW = 800KHZ



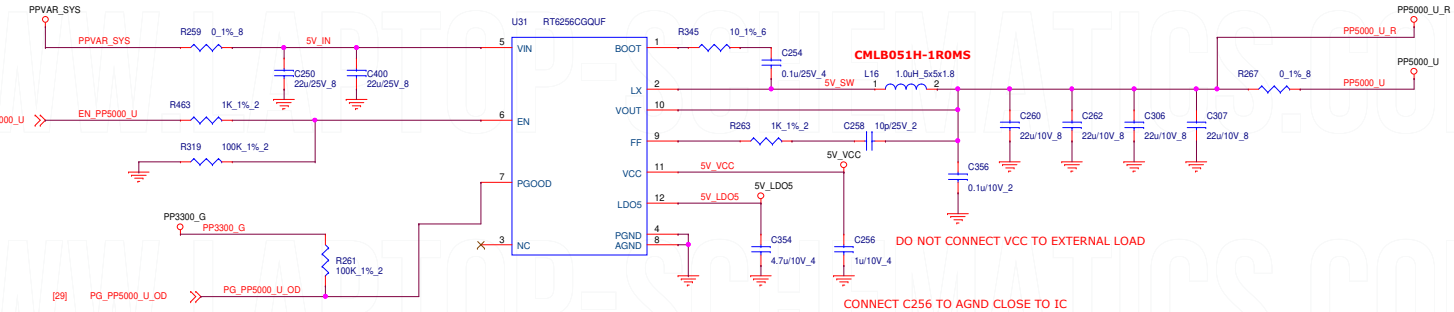


PP5000_U

PEAK CURRENT: 3.3A
IL_SAT (2S): 4.99A
IL_SAT (3S): 5.74A

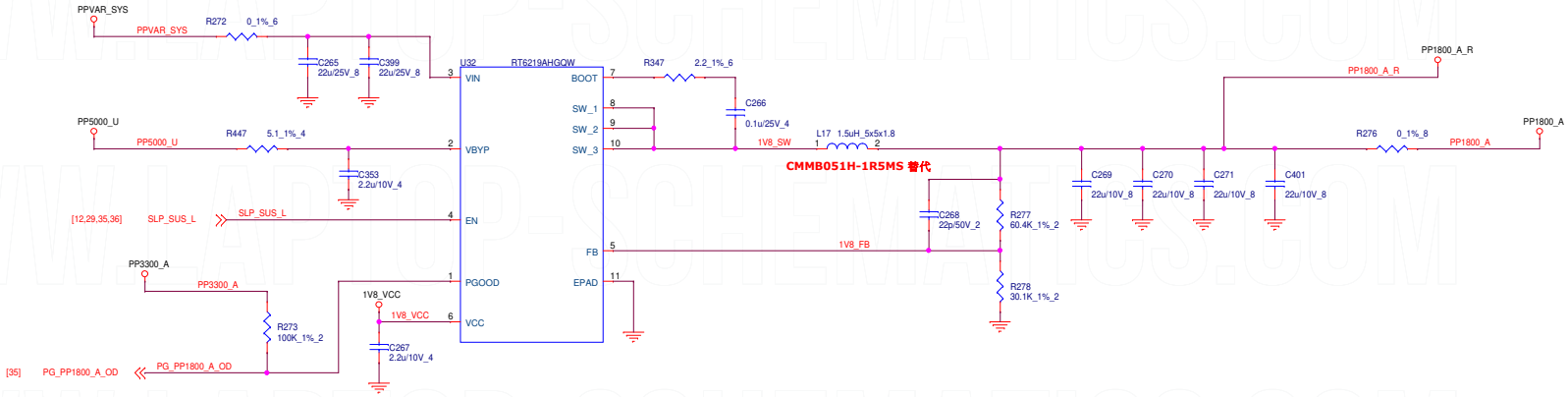
IF USING BC1.2
PEAK CURRENT: 4A
IL_SAT (2S): 5.69A
IL_SAT (3S): 6.44A

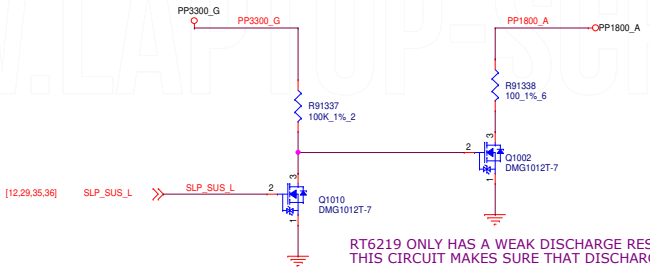
FIXME: THIS SHOULD BE RENAMED TO PP5000_A ON FUTURE PLATFORMS



PP1800_A

PEAK CURRENT: 2.94A
IL_SAT (2S): 4.06A
IL_SAT (3S): 4.16A





RT6219 ONLY HAS A WEAK DISCHARGE RESISTANCE (5K) WHEN DISABLED
THIS CIRCUIT MAKES SURE THAT DISCHARGE HAPPENS IN <100MS

Quanta Computer Inc.		
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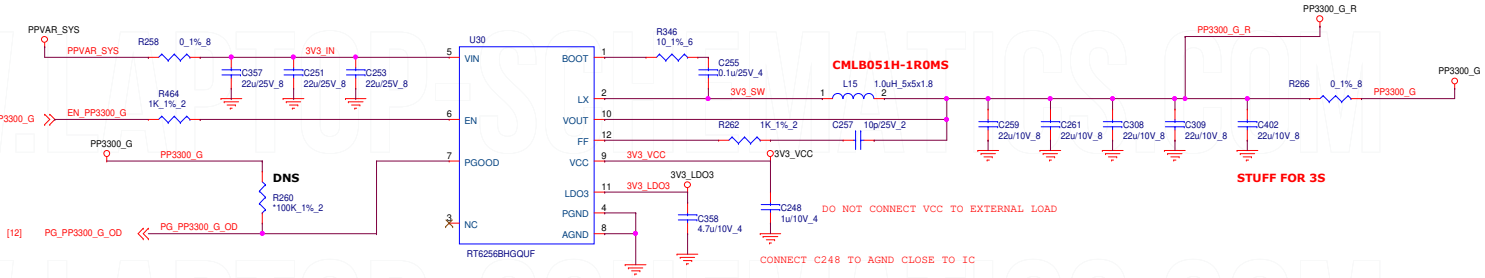
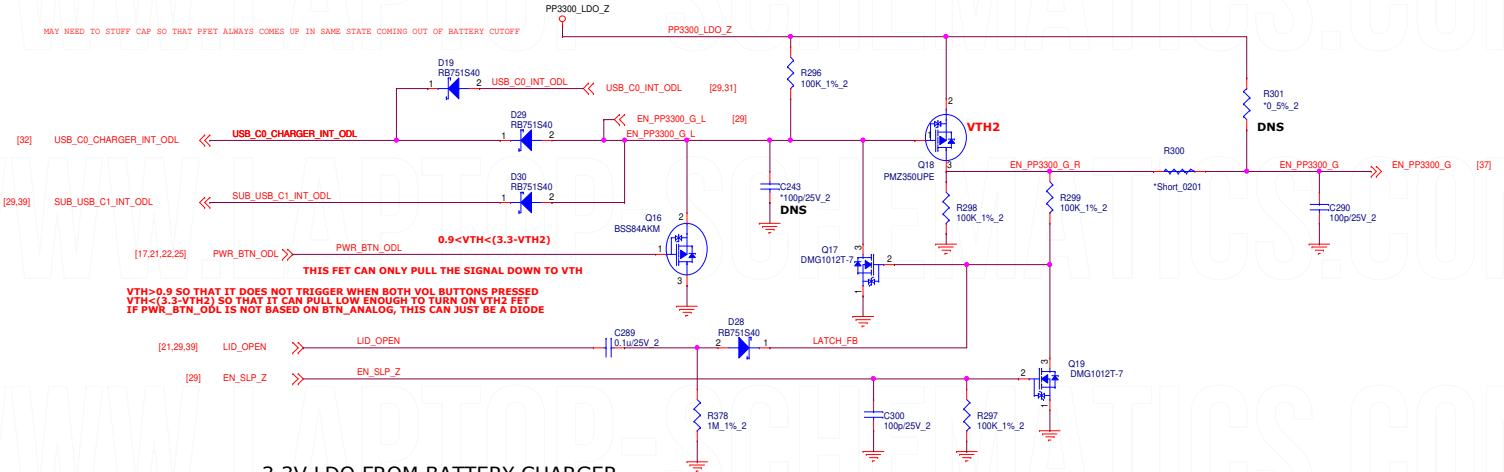
PP3300_G

PEAK CURRENT: 4.06A
IL_SAT (2S): 6.47A
IL_SAT (3S): 6.96A

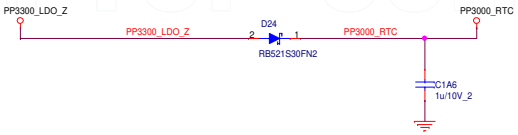


Z SLEEP STATE LOGIC

SUPER LOW POWER STATE WITH ONLY AP RTC ON. WAKES FROM PWR BTN, LID, USB-C EVENT



3,3V LDO FROM BATTERY CHARGER



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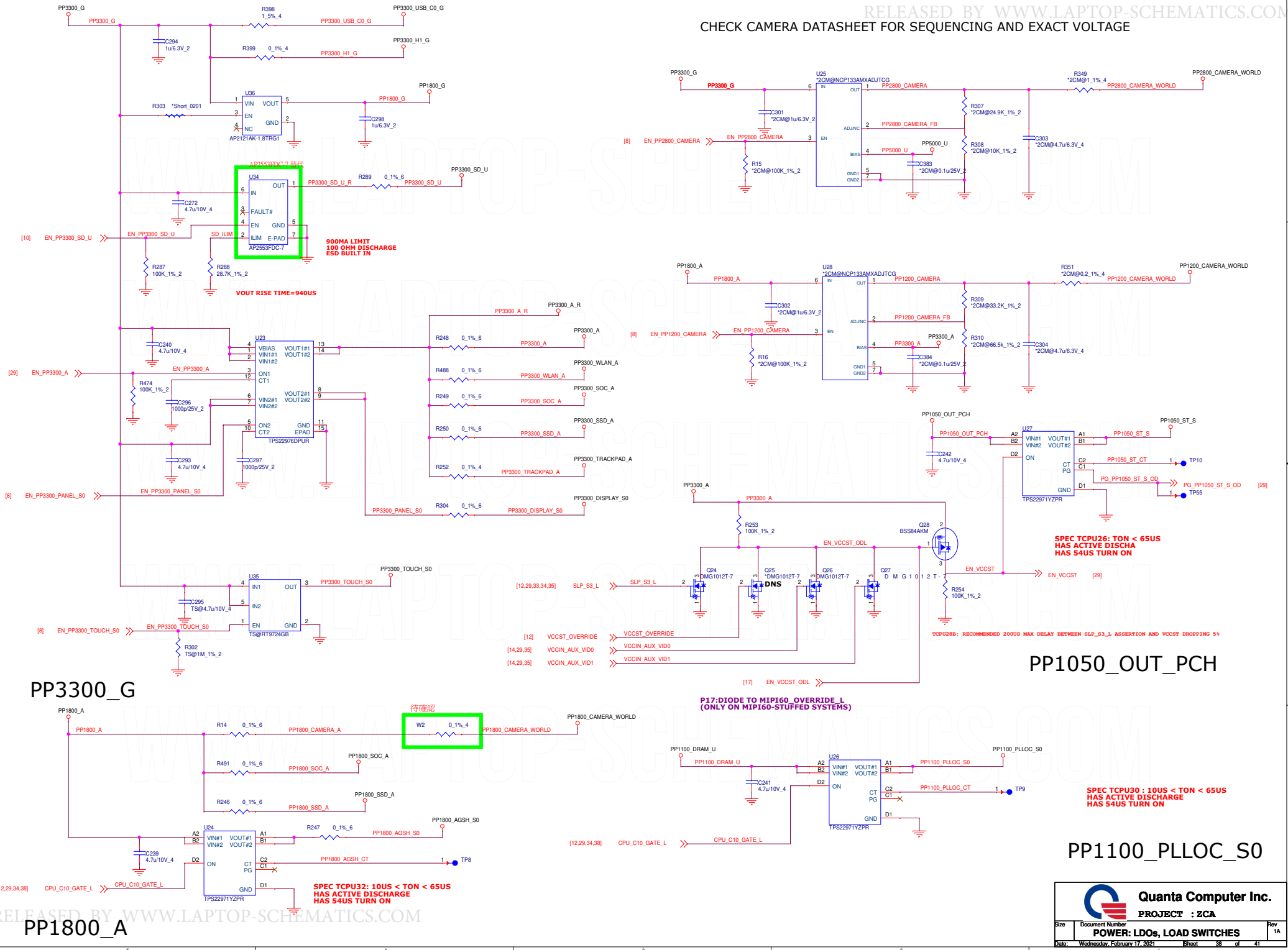
CHECK CAMERA DATASHEET FOR SEQUENCING AND EXACT VOLTAGE



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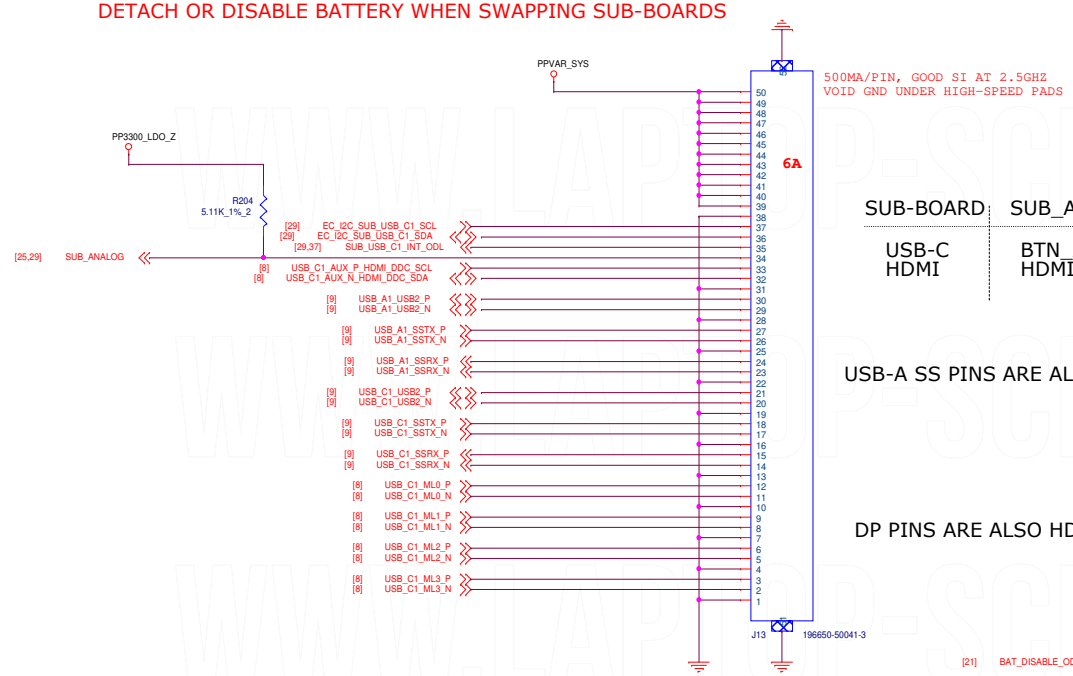
SUB-BOARD CONNECTOR

DETACH OR DISABLE BATTERY WHEN SWAPPING SUB-BOARDS



500MA/PIN, GOOD SI AT 2.5GHZ
VOID GND UNDER HIGH-SPEED PADS

SUB-BOARD	SUB_ANALOG
USB-C	BTN_ANALOG
HDMI	HDMI_HPD_ODL

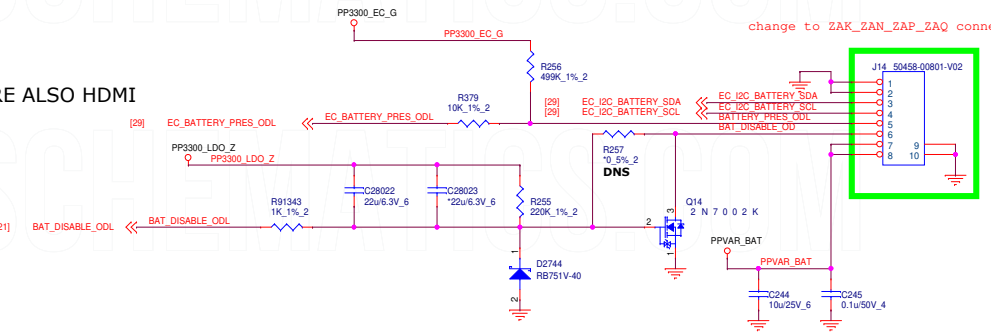
USB-A SS PINS ARE ALSO PCIE

DP PINS ARE ALSO HDMI

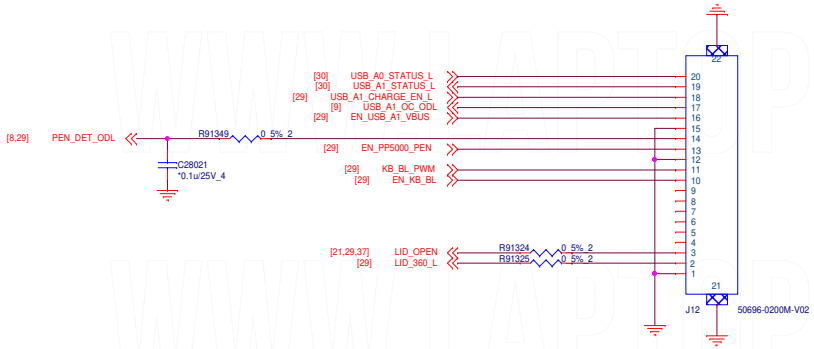
SMART BATTERY

MAY NEED WEAKER PULL-UP IF BATTERY THERMISTOR IS GREATER THAN 100K

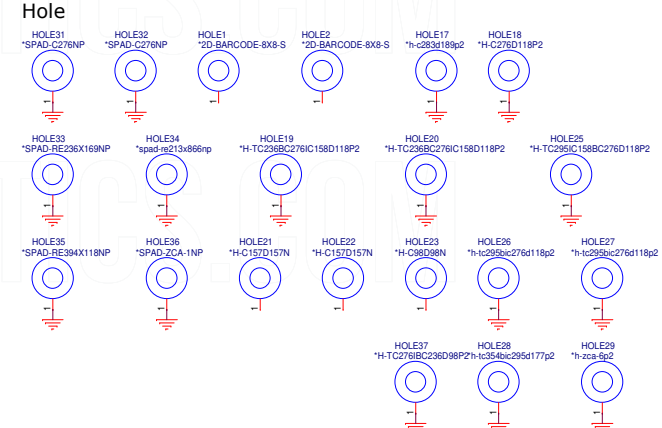
change to ZAK_ZAN_ZAP_ZAQ connector



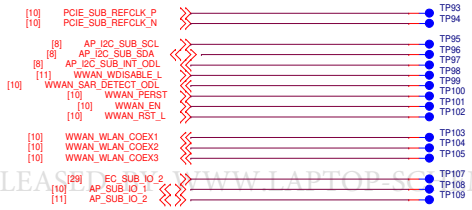
EC_BATT_PRES SERIES R PREVENTS PARTIALLY-CONNECTED BATTERY FROM USING THE EC AS HIGH-CURRENT GROUND RETURN



Hole



SUB-BOARD WWAN/EXTRA CONNECTOR



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PROJECT : ZCA

Size	Document Number	Rev
	RESERVED	1A

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Quanta Computer Inc.

PROJECT : ZCA

Size	Document Number	Rev
	RESERVED	1A

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