

ZSA MB Schematic Document

2018.07.26

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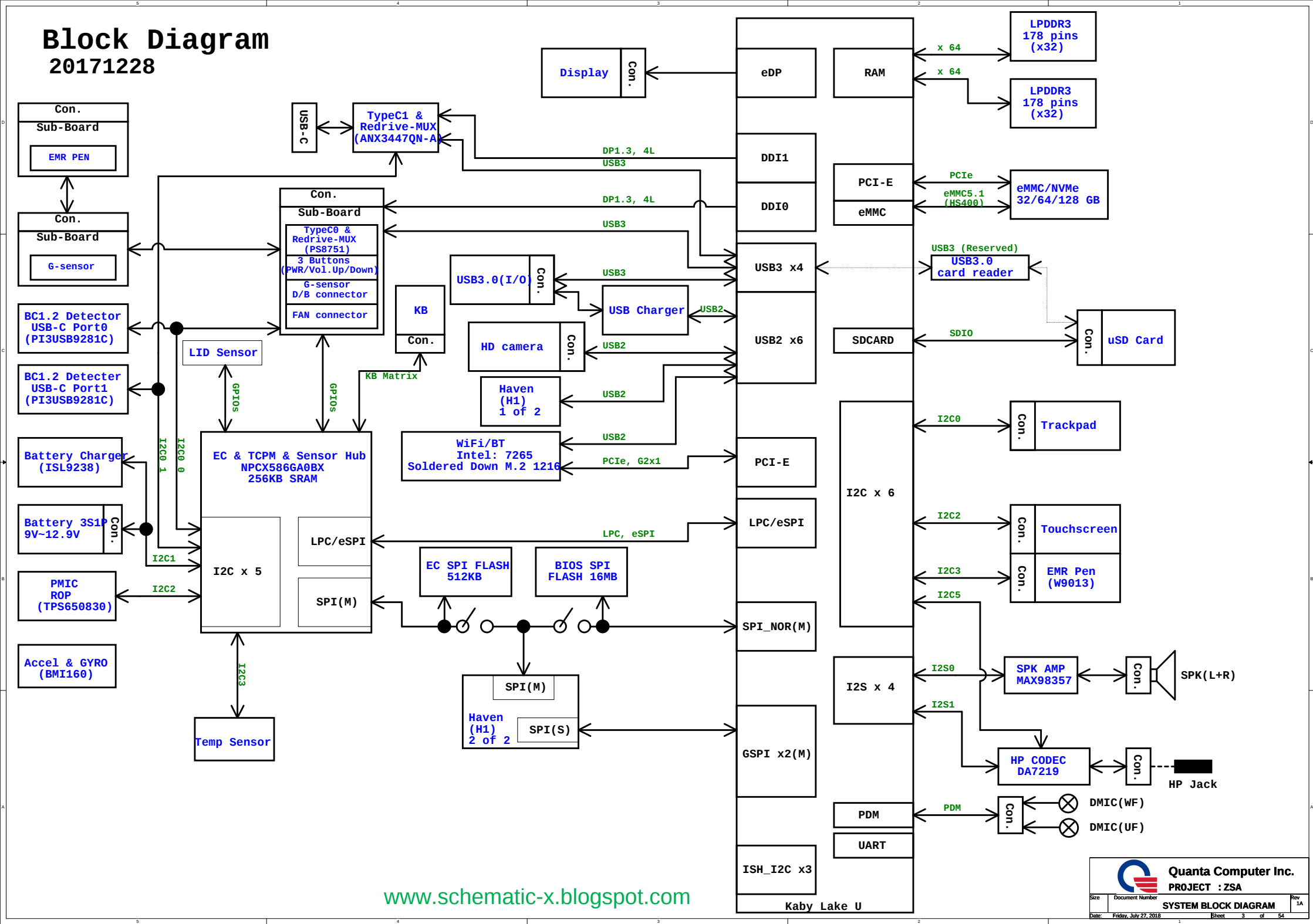
Trackpad/Thermal

GMR/Srew

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Block Diagram

20171228



Intel KBL-U Platform		KBL-U Chromebook (EQA04)		
HSIO Port	Capable	Port Allocation	PCIE CLK & CLKREQ	Note
1	USB3 #1	USB3 Type-C port 1		SUB/B
2	USB3 #2	USB3 Type-C port 2		M/B
3	USB3 #3	USB3 Type-A		M/B
4	USB3 #4	SD card reader		M/B
5	PCIE #1	NA		
6	PCIE #2	NA		
7	PCIE #3	NA		
8	PCIE #4	WLAN + BT Intel 7265	PCIE CLK1	M/B
9	PCIE #5	NA		
10	PCIE #6	NA		
11	SATA#6/PCIE #7	NA		
12	SATA#1/PCIE #8	NA		
13	PCIE#9	On board NVMe	PCIE CLK2	Reserved
14	PCIE#10	On board NVMe	PCIE CLK2	Reserved
15	PCIE#11	NA		
16	PCIE#12	NA		

Intel KBL-U Platform		KBL-U Chromebook (EQA04)	
USB Port	Capable	Port Allocation	Note
1	USB2 #1	USB3 Type-C port 1	SUB/B
2	USB2 #2	USB3 Type-C port 2	M/B
3	USB2 #3	USB3 Type-A	M/B
4	USB2 #4	SD card reader	M/B
5	USB2 #5	WLAN + BT Intel 7265	M/B
6	USB2 #6	NA	
7	USB2 #7	CAMERA	SUB/B
8	USB2 #8	NA	
9	USB2 #9	NA	
10	USB2 #10	NA	
Intel KBL-U Platform		KBL-U Chromebook (EQA04)	
DDI Port	Capable	Port Allocation	Note
1	DDI #1	USB3 Type-C port 2	M/B
2	DDI #2	USB3 Type-C port 1	SUB/B

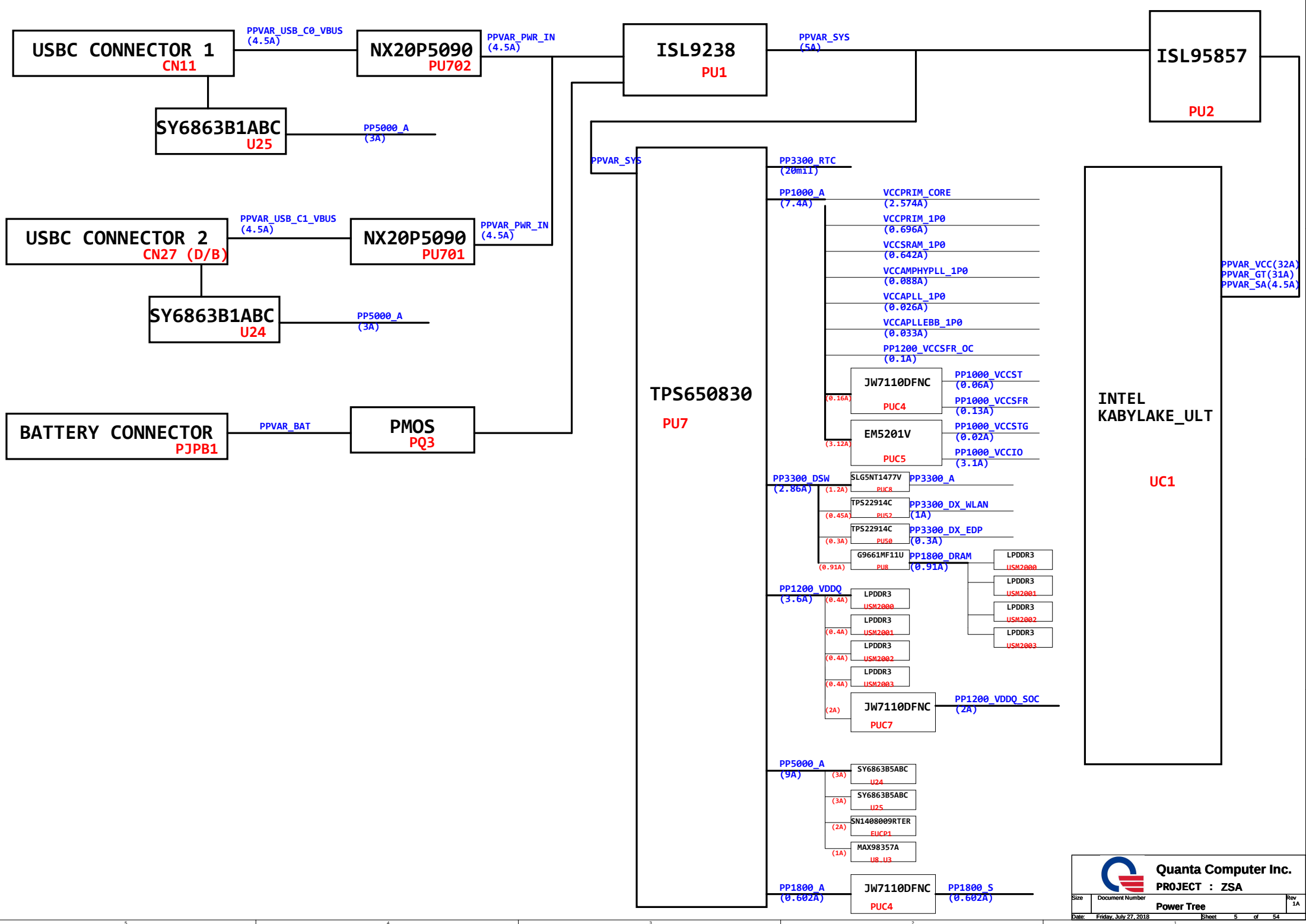
SOC			
I2C Port	Voltage level	Device	Address(7bit)
I2C_0	3.3V	Touch Screen	
I2C_1	3.3V	Tricapad	0011001
I2C_2	1.8V	Active pen	
I2C_3	1.8V	Headphone codec	0011010
I2C_4	1.8V	HI(Reserve)	

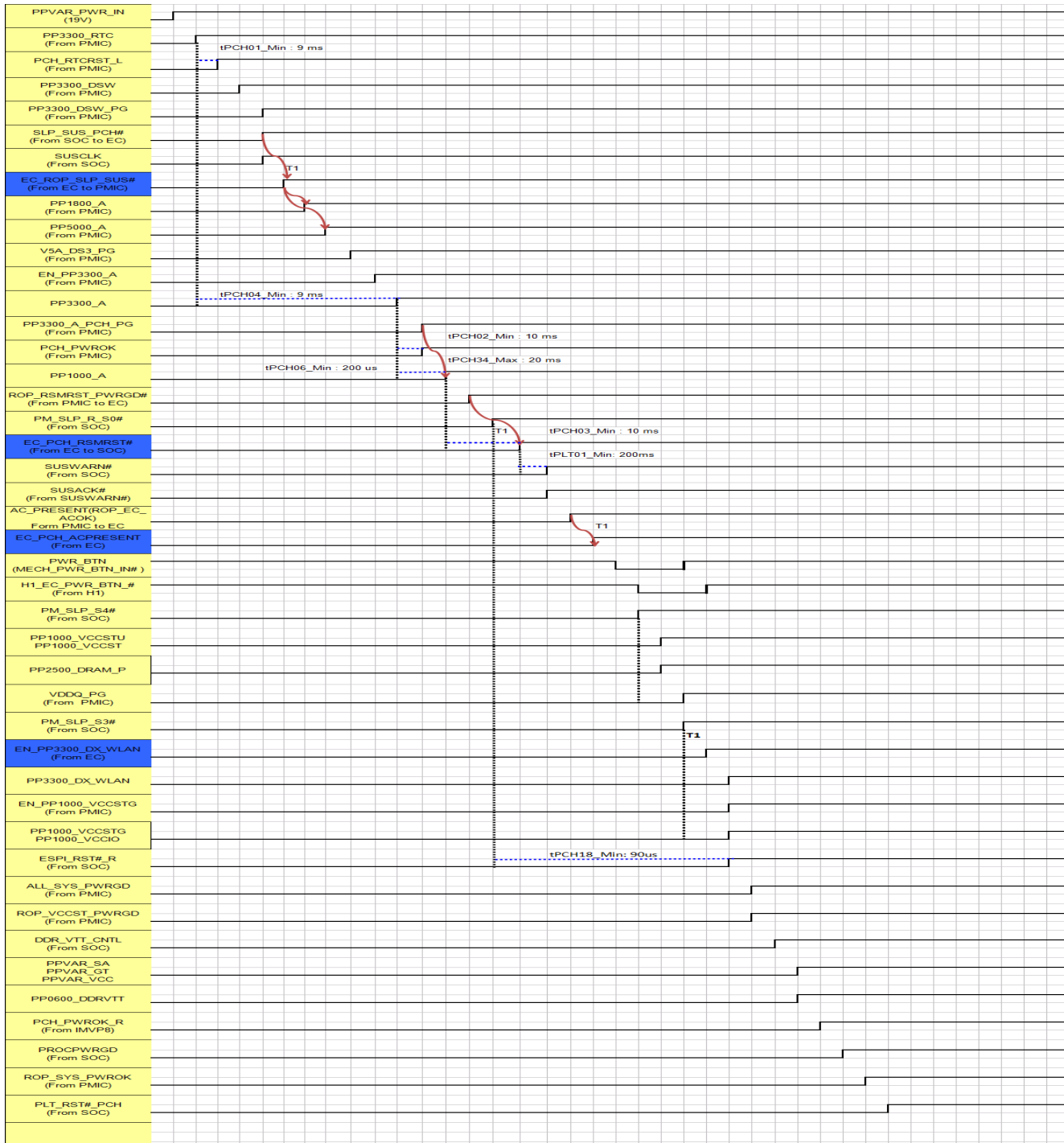
SOC	
GPIO group	Voltage level
A	1.8V
B	3.3V
C	3.3V
D	1.8V
E	3.3V
F	1.8V
G	3.3V

EC			
I2C Port	Voltage level	Device	Address(7bit)
I2C_0	3.3V	BC1.2 Detector (USB-C Port 1)	0100101
		TPCPC & Redrive-MUX (USB-C Port 1)	0001011
I2C0_1	3.3V	BC1.2 Detector (USB-C Port 2)	0100101
		TPCPC & Redrive-MUX (USB-C Port 2)	0001011
I2C_1	3.3V	Battery	0010110
		Battery Charger	0001001
I2C_2	3.3V	MB Back Light(LN3509)	0110110
		PMIC	0110000
I2C_3	3.3V	6-axis Accel & Gyro	1101000
		G-sensor	0011000
		Thermal Sensor(F76303M_MSOP10)	1001100

CPU	MB(7447)	DB(8761)	MB(7447)	DB(8761)
DDI_TX*	SOC_DP1*		SOC_DP1*	SOC_DP0*
DDI_TX**	SOC_DP1*	SOC_DP0*		SOC_DP0*
DDI_AUX*	SOC_DP1_AUX*		SOC_DP1_AUX*	
DDI_AUX**		SOC_DP0_AUX**		SOC_DP0_AUX**
USB3_1		USB3_1		USB3_1
USB3_2		USB3_2		USB3_2
USB2_1		USB2_1		USB2_1
USB2_2		USB2_2		USB2_2
HSIO	USB_C1_DP_HPD_S0C(PN1L0)		USB_C0_DP_HPD_S0C(PN1L0)	
HSIO		USB_C0_DP_HPD_S0C(PN1L7)		USB_C1_DP_HPD_S0C(PN1L7)
EC	MB(7447)	DB(8761)	MB(7447)	DB(8761)
OPD04	USB_C1_PD_HPD_EC		USB_C0_PD_HPD_EC	
OPD4S	USB_C0_DP_HPD_EC		USB_C1_DP_HPD_EC	
OPD0B	USB_C1_PD_RST_ODL			USB_C1_PD_HPD_EC
OPD0C	USB_C0_PD_RST_ODL	USB_C0_PD_RST_ODL	USB_C1_PD_RST_ODL	USB_C0_PD_RST_ODL
OPD0F	USB_C1_PD_RST_ODL	USB_C0_PD_RST_ODL	USB_C1_PD_RST_ODL	USB_C0_PD_RST_ODL
OPD07	USB_C1_PD_RST_ODL	USB_C0_PD_RST_ODL	USB_C0_PD_RST_ODL	USB_C0_PD_RST_ODL
OPD0D	USB_C1_BC12_RTW	USB_C0_BC12_RTW	USB_C1_BC12_RTW	USB_C0_BC12_RTW
OPD0C	USB_C1_VBUS_DET#	USB_C0_VBUS_DET#	USB_C1_VBUS_DET#	USB_C0_BC12_RTW
OPD07		USB_C0_VBUS_DET#		USB_C0_VBUS_DET#
EC0_S0A0	EC_D0C_1_S0A	EC_D0C_1_S0A	EC_D0C_1_S0A	EC_D0C_1_S0A
EC0_S0A0	EC_D0C_1_S0A	EC_D0C_1_S0A	EC_D0C_1_S0A	EC_D0C_1_S0A
EC0_S0A1	EC_D0C_1_S0A	EC_D0C_1_S0A	EC_D0C_1_S0A	EC_D0C_1_S0A
CONNECTOR	MB(7447)	DB(8761)	MB(7447)	DB(8761)
VBUS	PPVAR_USB_C1_VBUS	PPVAR_USB_C0_VBUS	PPVAR_USB_C1_VBUS	PPVAR_USB_C0_VBUS
DISCHARGE	USB_C1_DISCHARGE	USB_C0_DISCHARGE	VBUS_C1_DISCHG	NA

	Location	Address	Channel	Test Power Net Name	Test Point	Remark
INA3221AIROVR	PU35	10000000	CH1	PPVAR_SYS_PMIC_V1	PR127	0.01 1% 6
			CH2	PPVAR_BL_PWR	F101	0.5% 8
			CH3	+8.4VB_VCC1_VIN	PR87	0.01 1% 12
	PU36	10000001	CH1	PP5000_A	PR160	0.008 1% 12
			CH2	PPVAR_SYS_PMIC_V5	PR159	0.01 1% 8
			CH3	PP1800_A	PR137	0.5% 6
	PU37	10000010	CH1	PP1200_VDDQ	PR152	0.008 1% 12
			CH2	PP0600_DDRVTT	PR929	0.01 1% 6
			CH3	SYS_PPVAR_SYS_PMIC_V4	PR151	0.5% 6
	PU38	10000011	CH1	VINVR2-650830	PR1236	0.5% 4
			CH2	PP1200_VDDQ_DDRVTT1N	PR931	0.5% 4
			CH3	PPVAR_SYS_PMIC_V3	PR140	0.01 1% 8
INA219A1DCNRG4	PU39	10001000	CH1	+8.4VB_VCC2_VIN	PR92	0.01 1% 6
	PU40	10001010	CH1	PP3300_DSM	PR138	0.008 1% 12
	PU41	10010000	CH1	PPVAR_GT_VIN	PR97	0.01 1% 12
	PU42	10001011	CH1	PPVAR_BATT_R	PR11	0.01 1% 12
	PU44	10001001	CH1	PPVAR_SA_VIN	PR99	0.01 1% 12
	PU97	10010001	CH1	PP3300_S	PR4920	0.01 1% 6
	PU98	10010010	CH1	PP3300_OX_WLAN	PR381	0.01 1% 8
	PU99	10010011	CH1	PP1000_A	PR128	0.008 1% 12
	PU100	10011000	CH1	PP3300_OX_EDP	PR378	0.01 1% 6
	PU101	10011001	CH1	PP3300_DSM_EC	R401	2.2 6







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Size

Document Number

SKU PLAN

Rev

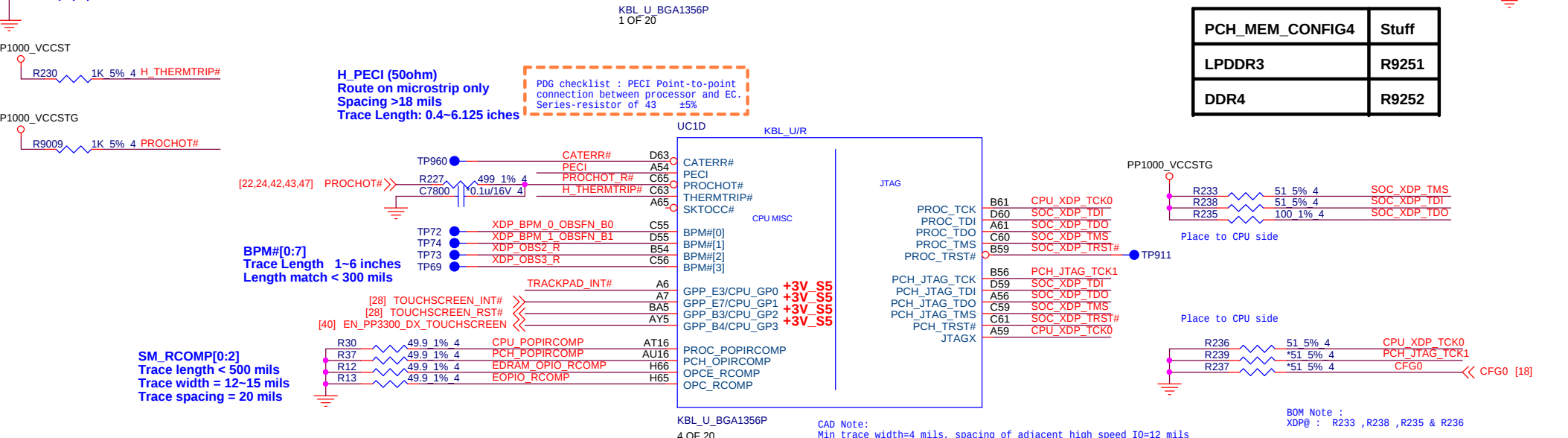
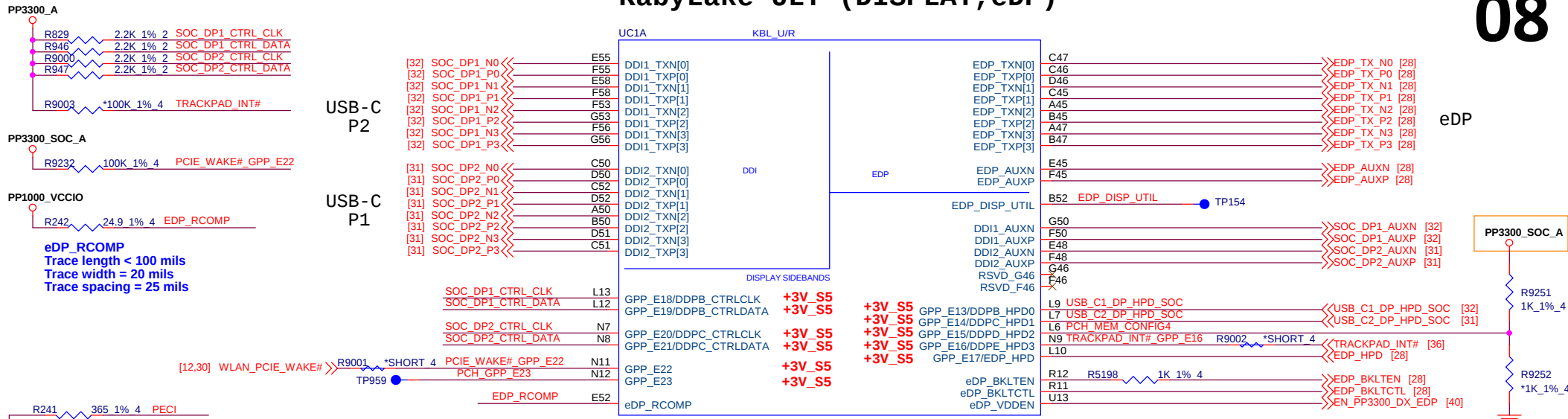
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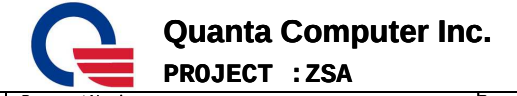
KabyLake ULT (DISPLAY, eDP)

08



BOM Note :
XDP@ : R233 ,R238 ,R235 & R236

CAD Note:
Min trace width=4 mils, spacing of adjacent high speed IO=12 mils



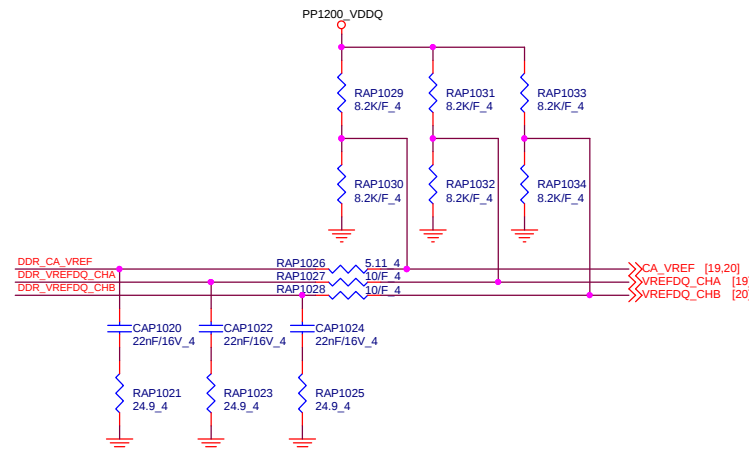
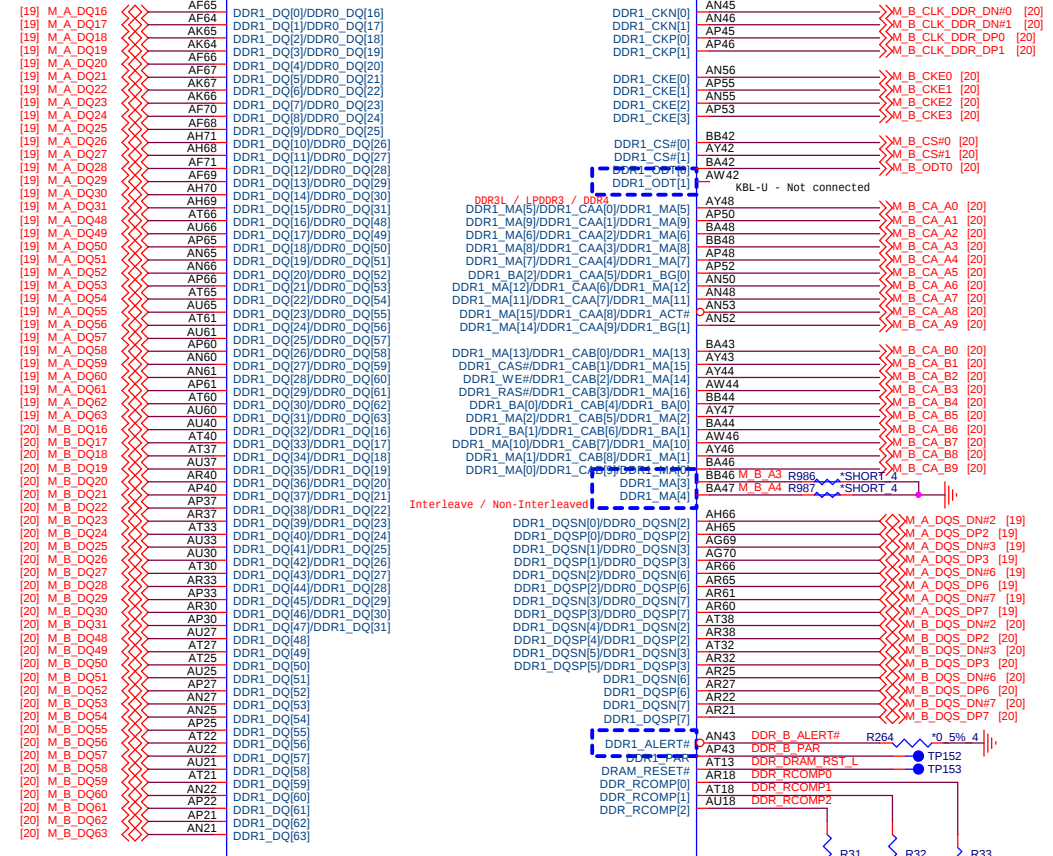
UC1B

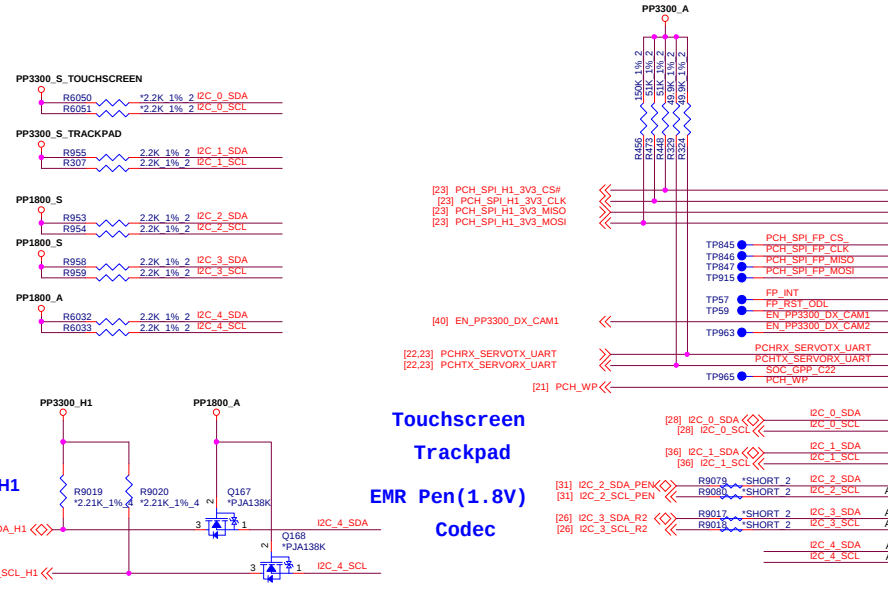
DDR4(IL)/LP3-DDR4 (NIL)



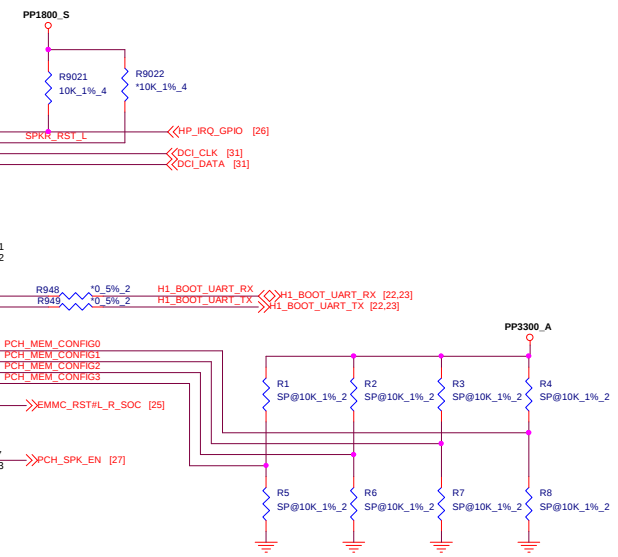
UC1C KBL_U/R

Interleave / Non-Interleaved





	UC1F		KBV_U1R				IS#
		LPSS					
N8		GPP_B18/GSPI0_C#	+3V S5				
P7		GPP_B18/GSPI0_CLK	+3V S5				GPP_D9
P8		GPP_B17/GSPI0_MISO	+3V S5			+1.8V S5	GPP_D10
P7		GPP_B18/GSPI0_MOSI	+3V S5			+1.8V S5	GPP_D11
		GPP_B18/GSPI0_MOSI	+3V S5			+1.8V S5	GPP_D12
M5		GPP_B18/GSPI1_C#	+3V S5				
N5		GPP_B20/GSPI1_CLK	+3V S5			+1.8V S5	GPP_D6/ISH_12C0_SDA
P5		GPP_B21/GSPI1_MISO	+3V S5			+1.8V S5	GPP_D6/ISH_12C0_SCL
P5		GPP_B22/GSPI1_MOSI	+3V S5				
						+1.8V S5	GPP_D7/ISH_12C1_SDA
						+1.8V S5	GPP_D8/ISH_12C1_SCL
B1		GPP_C8/UART0_RXD	+3V S5				
P1		GPP_C9/UART0_TXD	+3V S5				
P3		GPP_C10/UART0_RTS#	+3V S5			+1.8V S5	GPP_F10/12C5_SDA/ISH_12C2_SDA
B3		GPP_C10/UART0_CTS#	+3V S5			+1.8V S5	GPP_F11/12C5_SCL/ISH_12C2_SCL
D2		GPP_C20/UART2_RXD	+3V S5				
D2		GPP_C21/UART2_TXD	+3V S5			+1.8V S5	GPP_D13/ISH_UART0_RXD/SMLOBALDATA/12C48_SDA
D4		GPP_C22/UART2_RTS#	+3V S5			+1.8V S5	GPP_D14/ISH_UART0_TXD/SMLOBCK/12C48_SCL
		GPP_C22/UART2_CTS#	+3V S5			+1.8V S5	GPP_D15/ISH_UART0_RTS#
						+1.8V S5	GPP_D16/ISH_UART0_CTS#/SMLOBALERT#
U7		GPP_C16/12C0_SDA	+3V S5			+3V S5	GPP_C12/UART1_RXD/ISH_UART1_TXD
U8		GPP_C17/12C0_SCL	+3V S5			+3V S5	GPP_C13/UART1_TXD/ISH_UART1_TXD
U8		GPP_C18/12C1_SDA	+3V S5			+3V S5	GPP_C14/UART1_RTS#/ISH_UART1_RTS#
U9		GPP_C19/12C1_SCL	+3V S5			+3V S5	GPP_C15/UART1_CTS#/ISH_UART1_CTS#
H9		GPP_F4/12C2_SDA	+1.8V S5			+1.8V S5	GPP_A18/ISH_GP0
		GPP_F5/12C2_SCL	+1.8V S5			+1.8V S5	GPP_A19/ISH_GP1
						+1.8V S5	GPP_A20/ISH_GP2
						+1.8V S5	GPP_A21/ISH_GP3
11		GPP_F6/12C3_SDA	+1.8V S5			+1.8V S5	GPP_A22/ISH_GP4
12		GPP_F7/12C3_SCL	+1.8V S5			+1.8V S5	GPP_A23/ISH_GP5
						+1.8V S5	GPP_A24/ISH_GP6
11		GPP_F8/12C4_SDA	+1.8V S5			+1.8V S5	Sx_EXIT_HOLDOFF#/GPP_A12/EM_BUSY/ISH_GP6
12		GPP_F8/12C4_SCL	+1.8V S5				

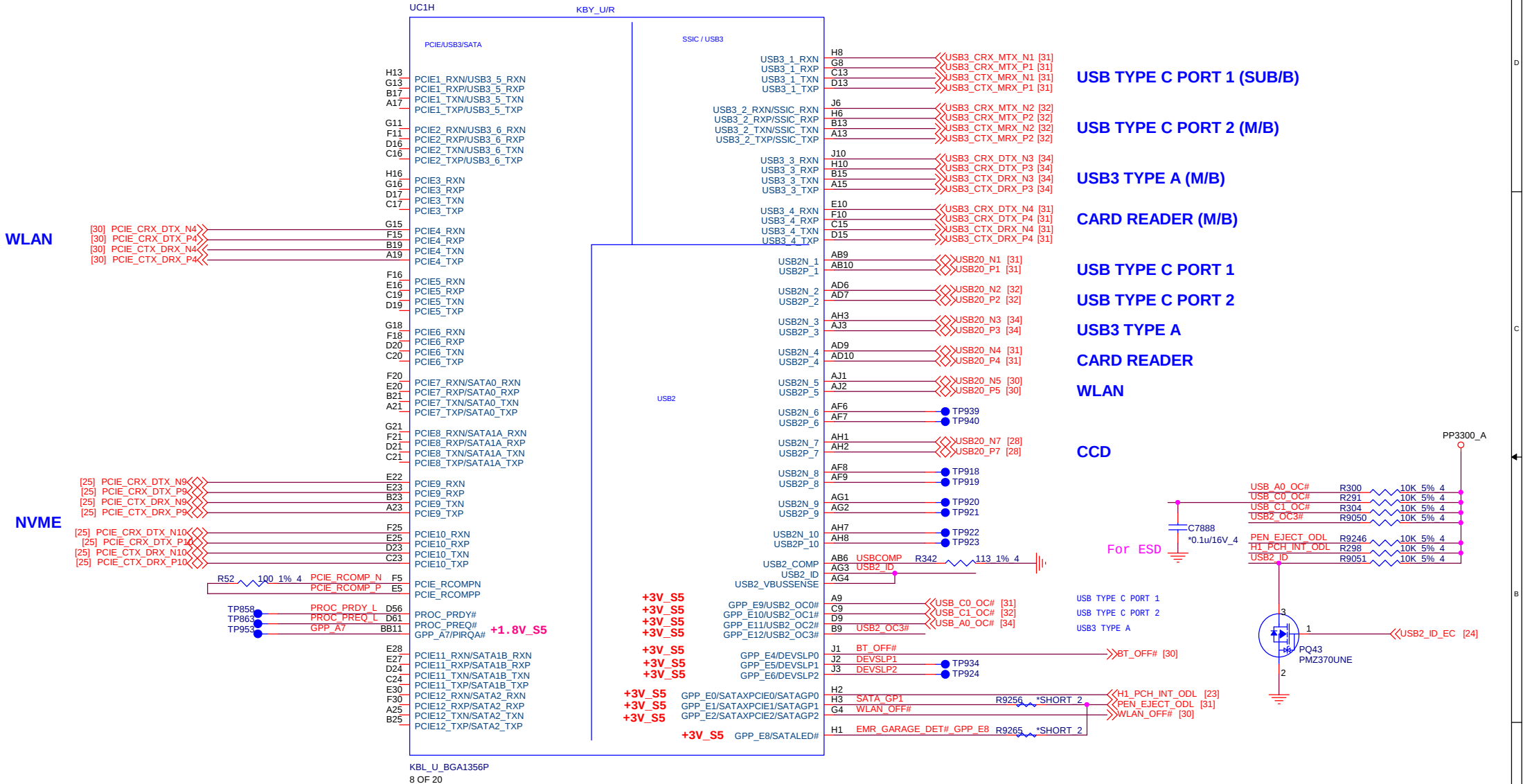


Pin Name	FUNCTION	INTENT
GPP_B_23/SML1ALERTB#	IPD = EXI BOOT STALL BYPASS DISABLE PU = EXI BOOT STALL BYPASS ENABLED	DISABLE
GPP_B18/GSPi0_MOSI	IPD = DISABLE NO REBOOT MODE PU = ENABLE NO REBOOT MODE	DISABLE
GPP_C2/SMBALERT#	IPD = DISABLE TLS CONFIDENTIALITY PU = ENABLE TLS CONFIDENTIALITY	DISABLE
GPP_B22/GSPi1_MOSI	IPD = BOOT FROM SPI PU = BOOT FROM LPC	SPI
GPP_C5/SML0ALERT#	IPD = LPC IS SELECTED FOR EC PU = ESPI IS SELECTED FOR EC	ESPI
GPP_E19/DDPB_CTRLDATA	IPD = DO NOT DETECT PORT B PU = DETECT PORT B	DETECT PORT B
GPP_E21/DDPC_CTRLDATA	IPD = DO NOT DETECT PORT C PU = DETECT PORT C	DETECT PORT C

Memory straps pin				
PCH_MEM_CFG[3:0]	MEMORY PN	QPN	Stuff	
0 0000	MT52L51M32D2PF-I07 WT:B	AKD5RW0TL12	R5, R6, R7, R8	
1 0001	MT52L256M32D1PF-I07 WT:B	AKD5QWSTL08	R4, R5, R6, R7	
2 0010	H9CCNNNB3TALAR-NUD	AKD5RW0TW72	R3, R5, R6, R8	
3 0011	H9CCNNNBGTALAR-NUD	AKD5QW0TW38	R3, R4, R5, R6	
4 0100	MT52L1G32D4PG-I07	AKD5SWSTL07	R2, R5, R7, R8	
5 0101	H9CCNNNCLGALAR-NUD	AKD5SW0TW46	R2, R4, R5, R7	
6 0110	NT6CL256T32CM-H1	AKD5QWSTF00	R2, R3, R5, R8	
7 0111			R2, R3, R4, R5	
8 1000				
9 1001			R1, R4, R6, R7	
10 1010				
11 1011			R1, R3, R4, R6	
12 1100				
13 1101			R1, R2, R4, R7	
14 1110				
15 1111				



KabyLake ULT (GPU, SATA , ODD, CLK ,USB2&3)

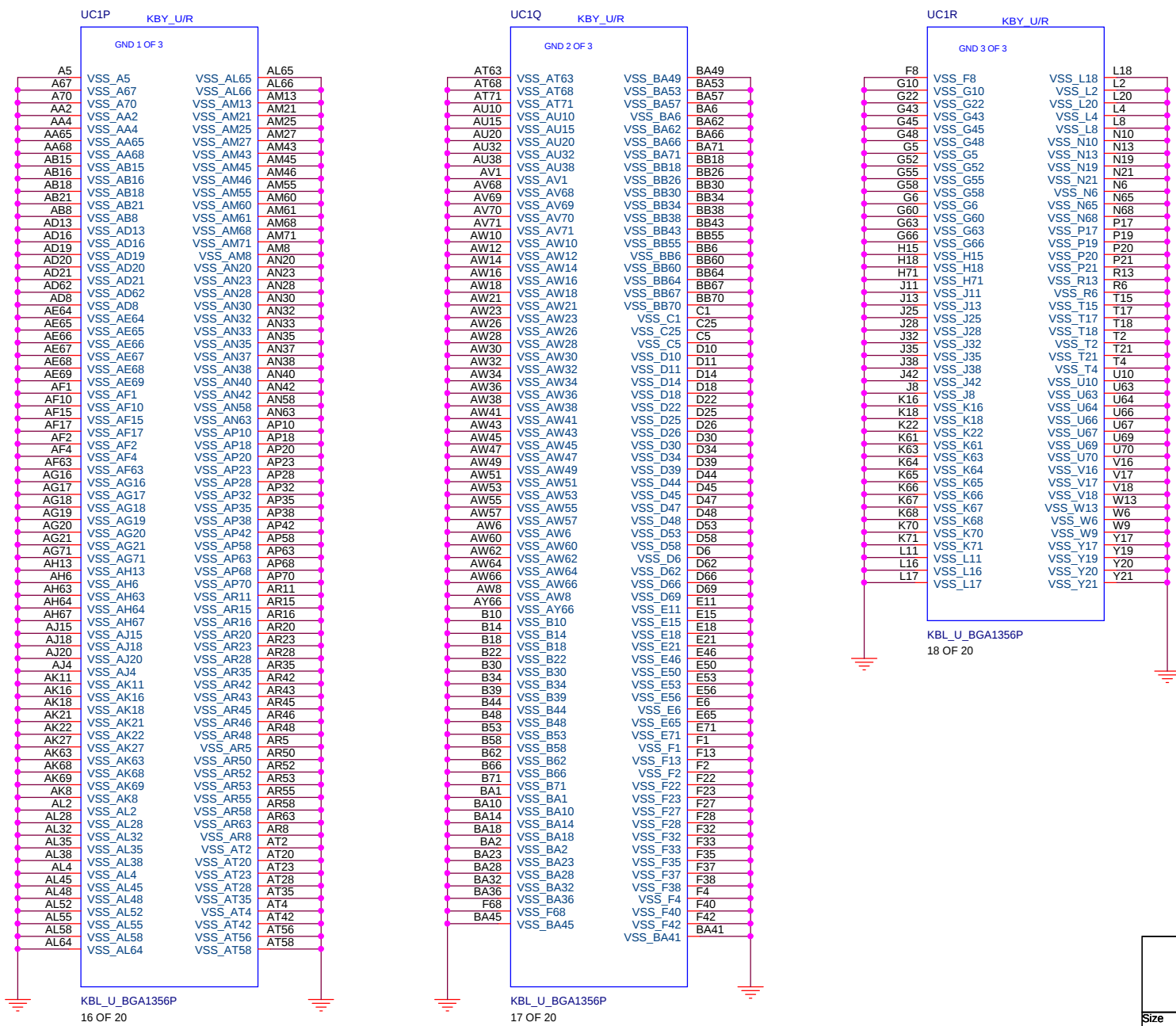


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	KabyLake PCIe/USB/SATA	1A
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KabyLake ULT (GND)



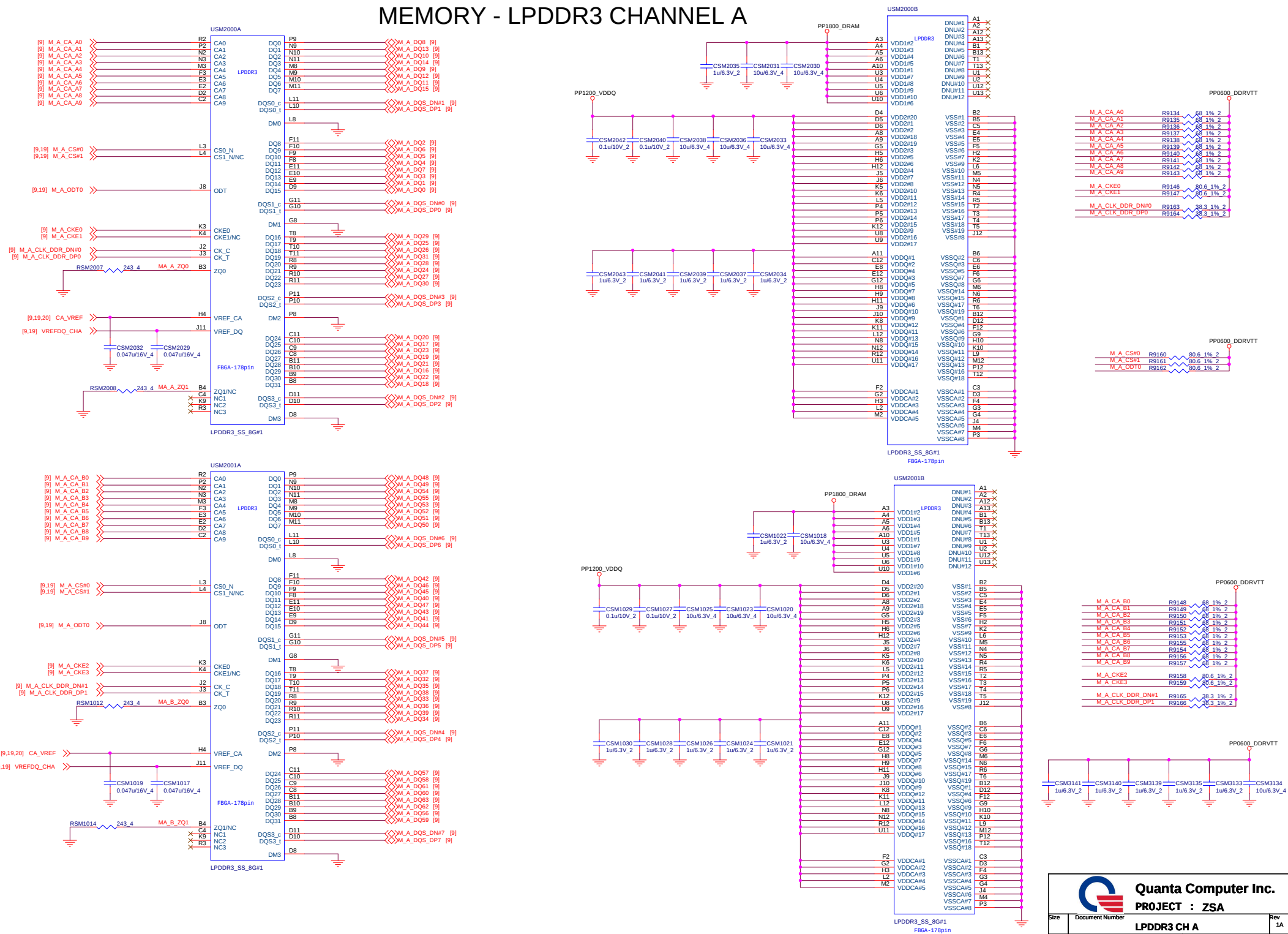


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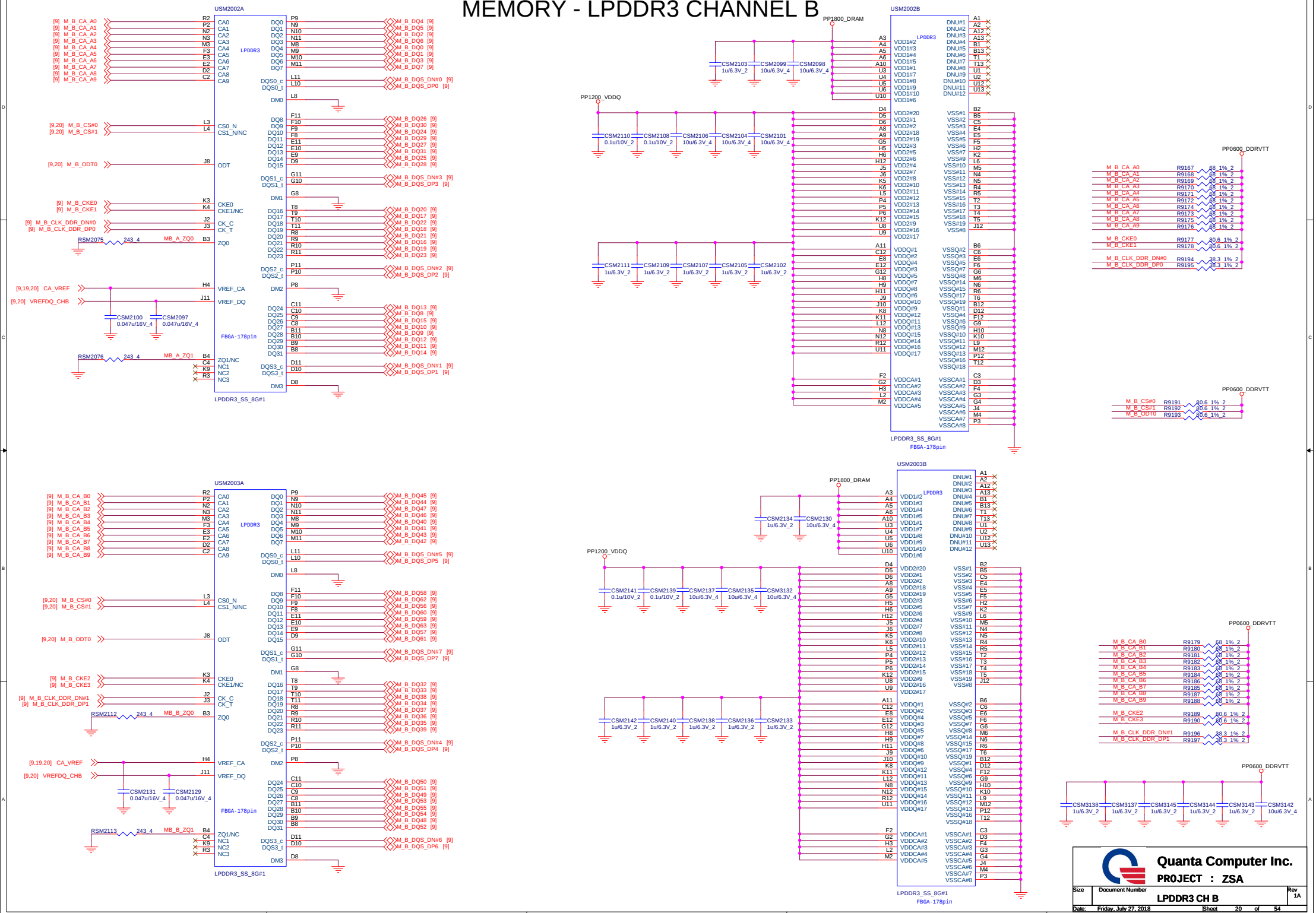
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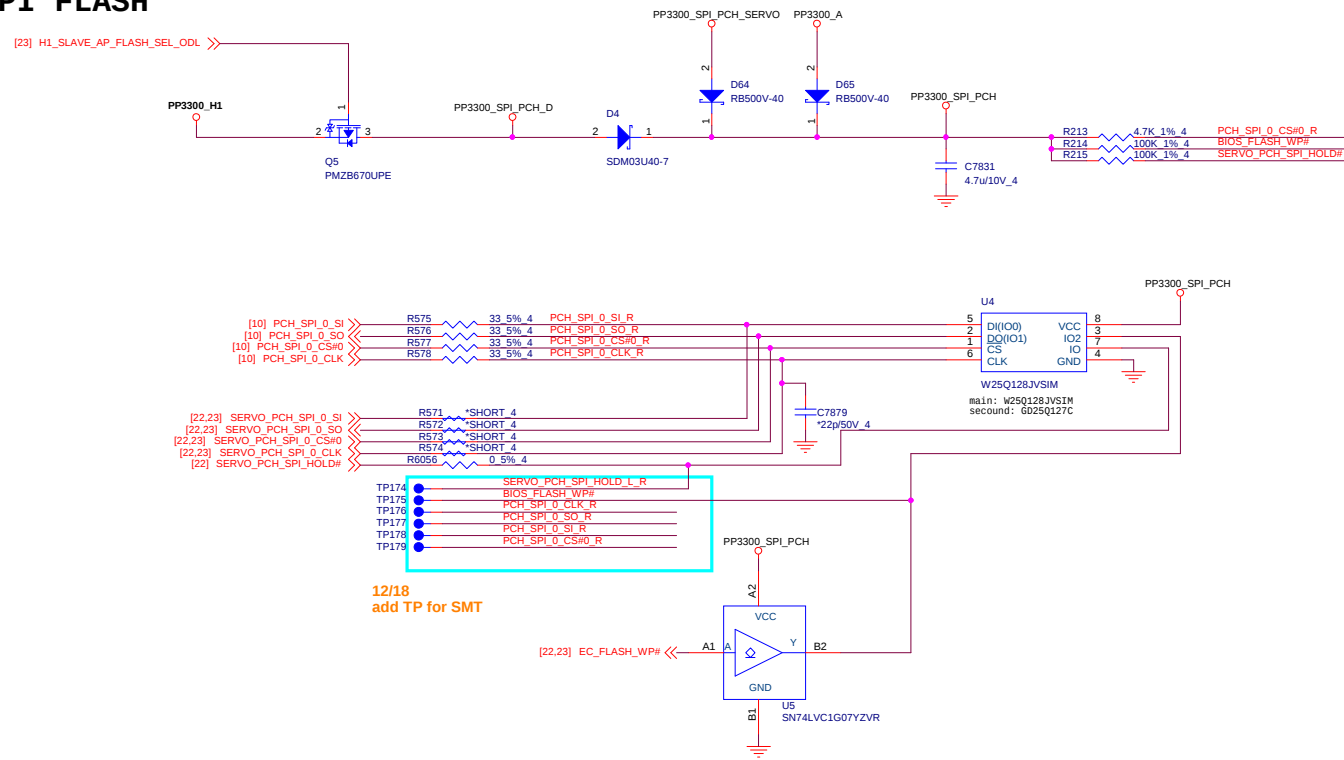
MEMORY - LPDDR3 CHANNEL A



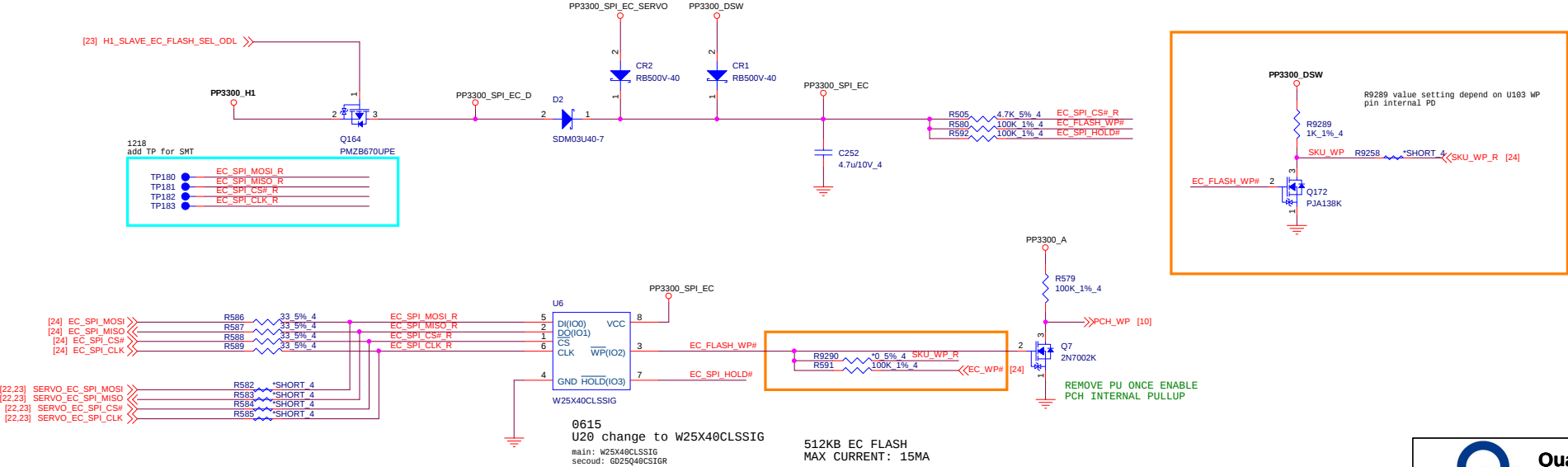
MEMORY - LPDDR3 CHANNEL B

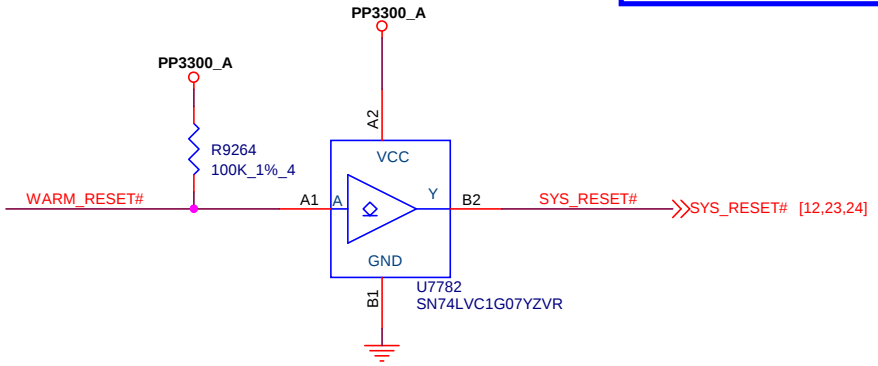
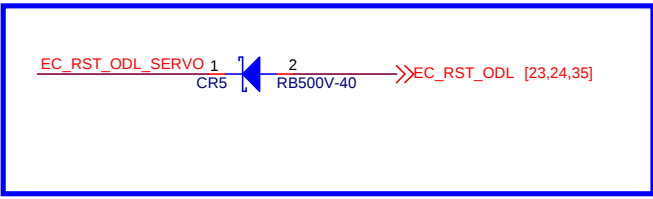
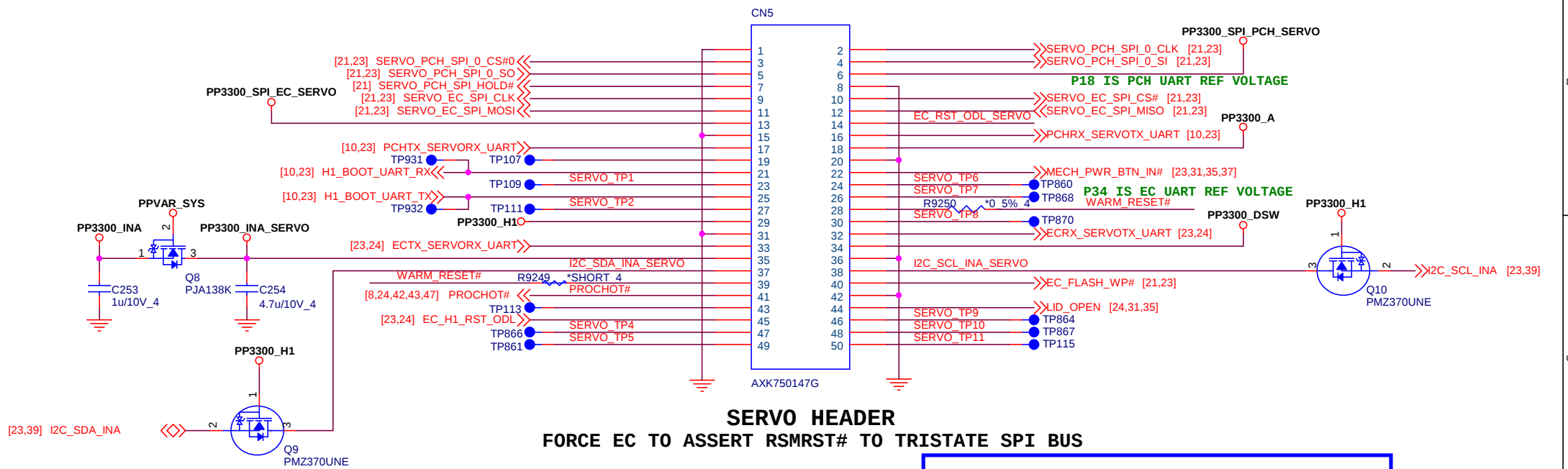


PCH SPI FLASH

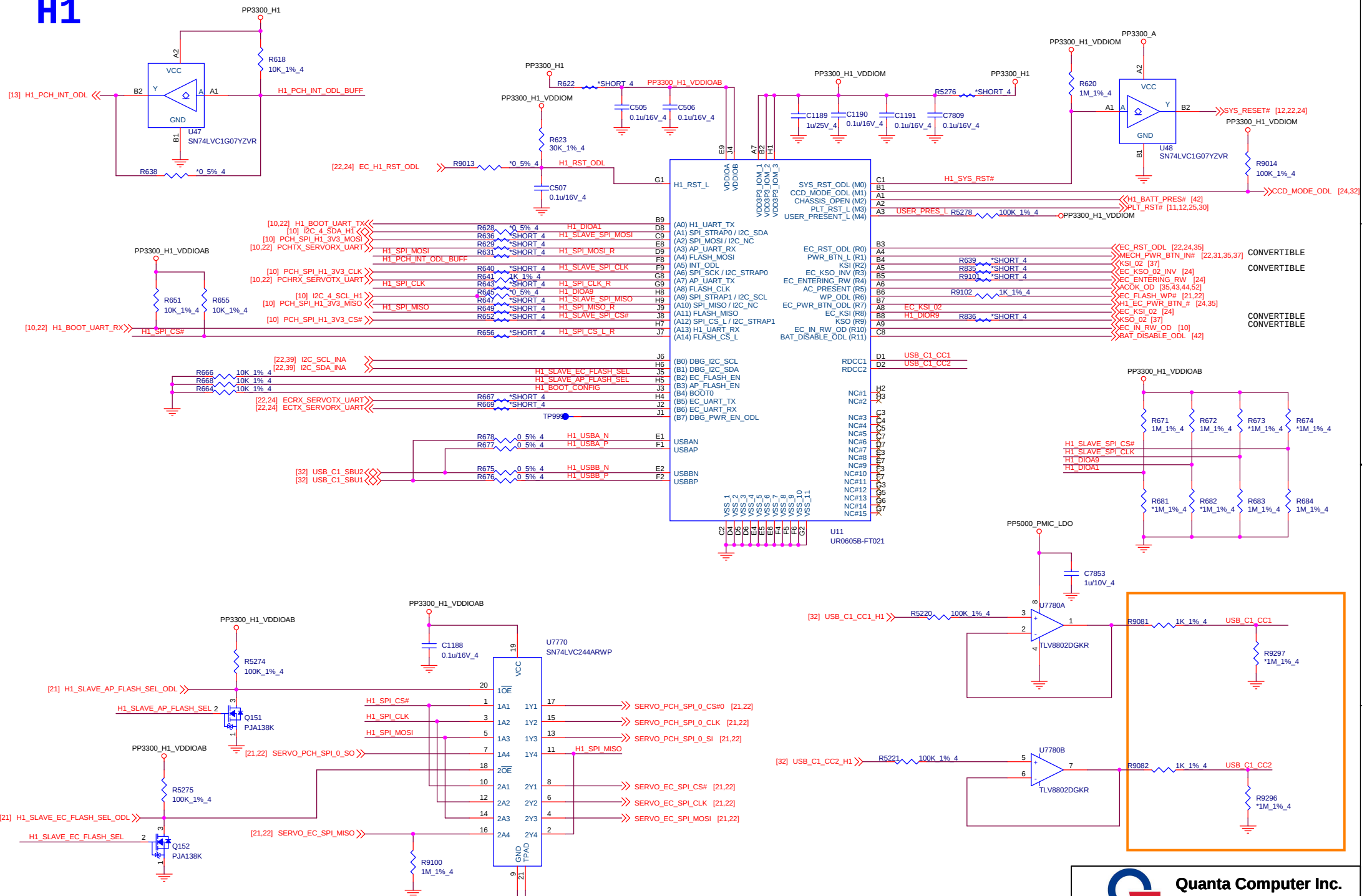


EC FLASH ROM



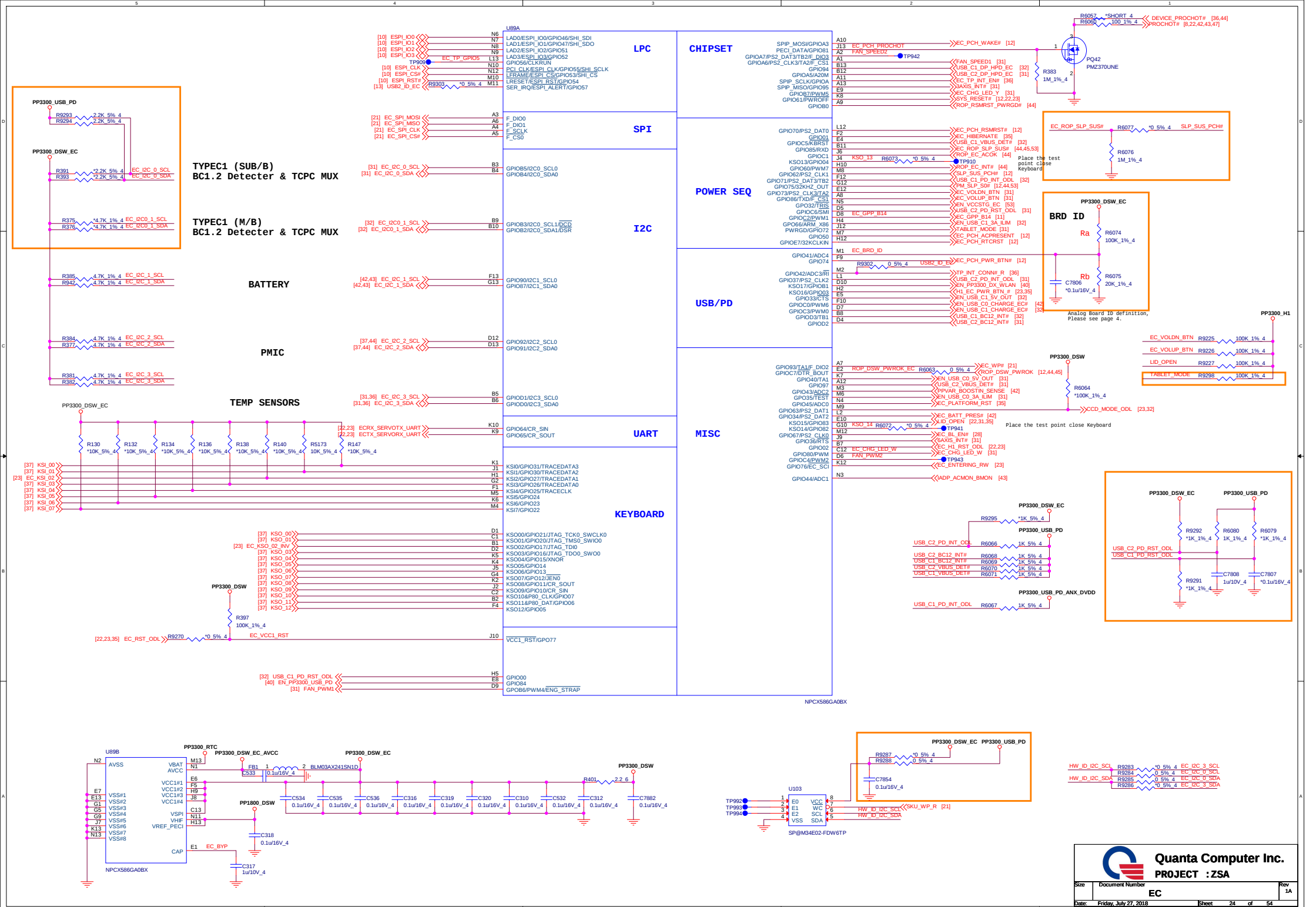


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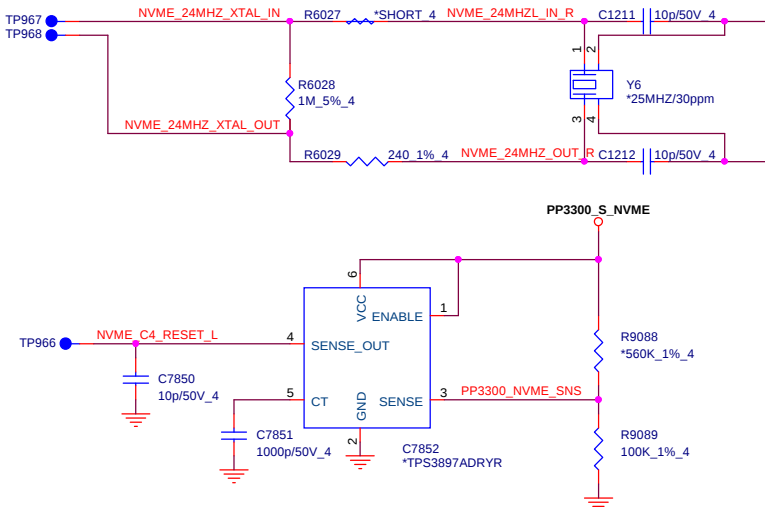
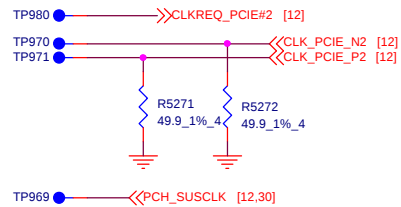
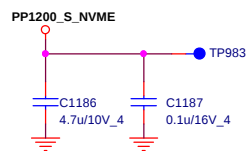
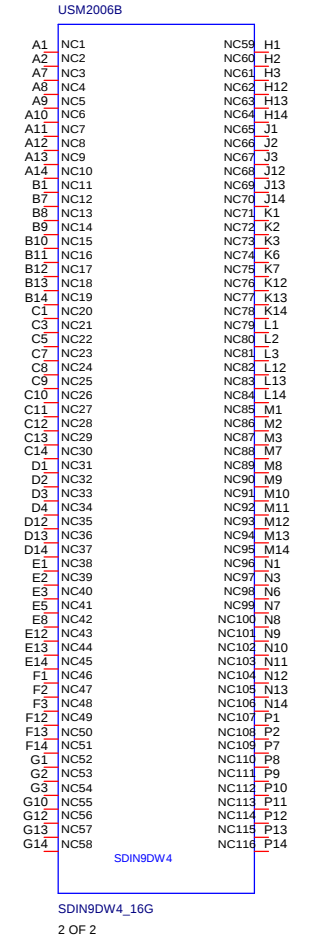


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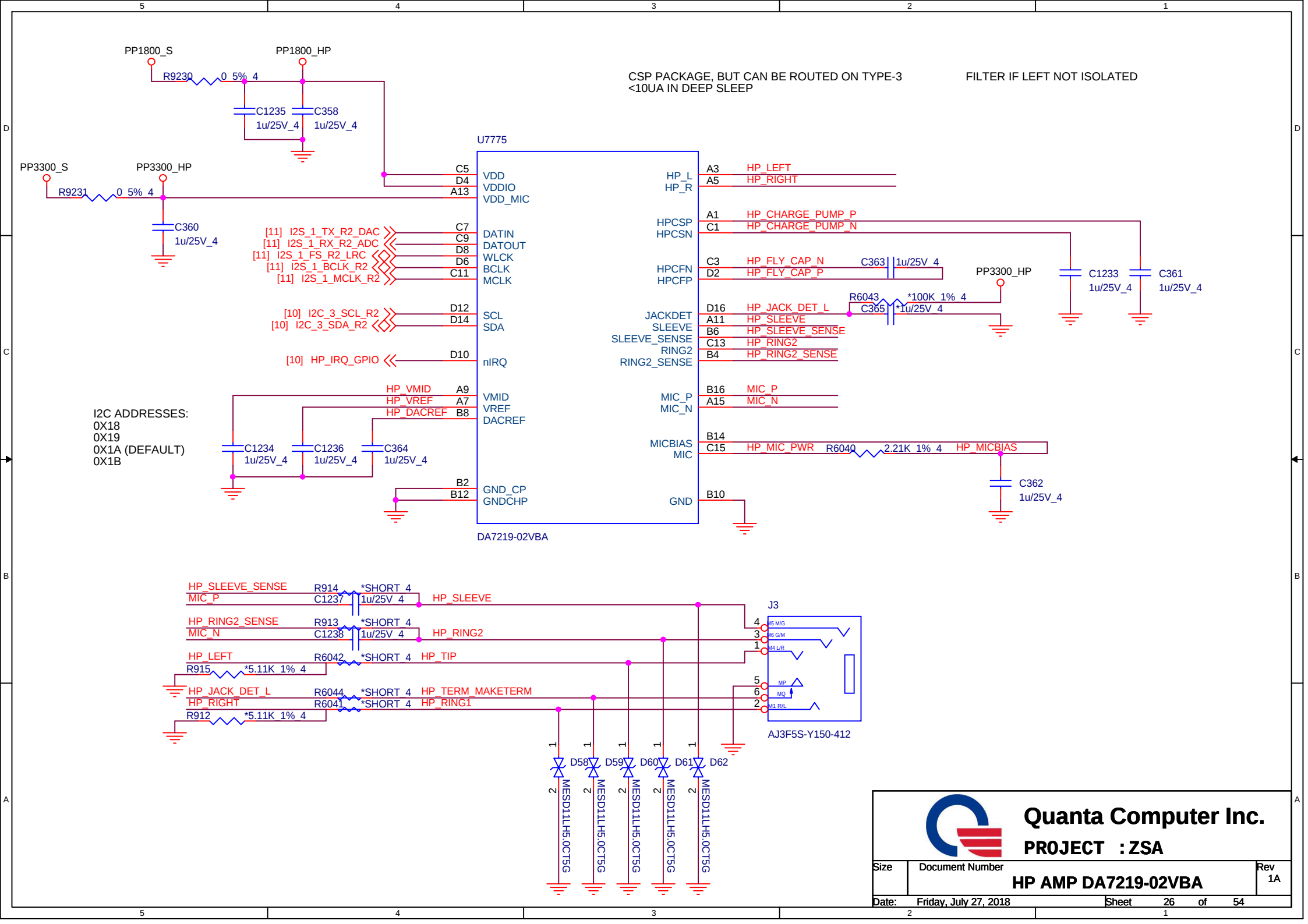
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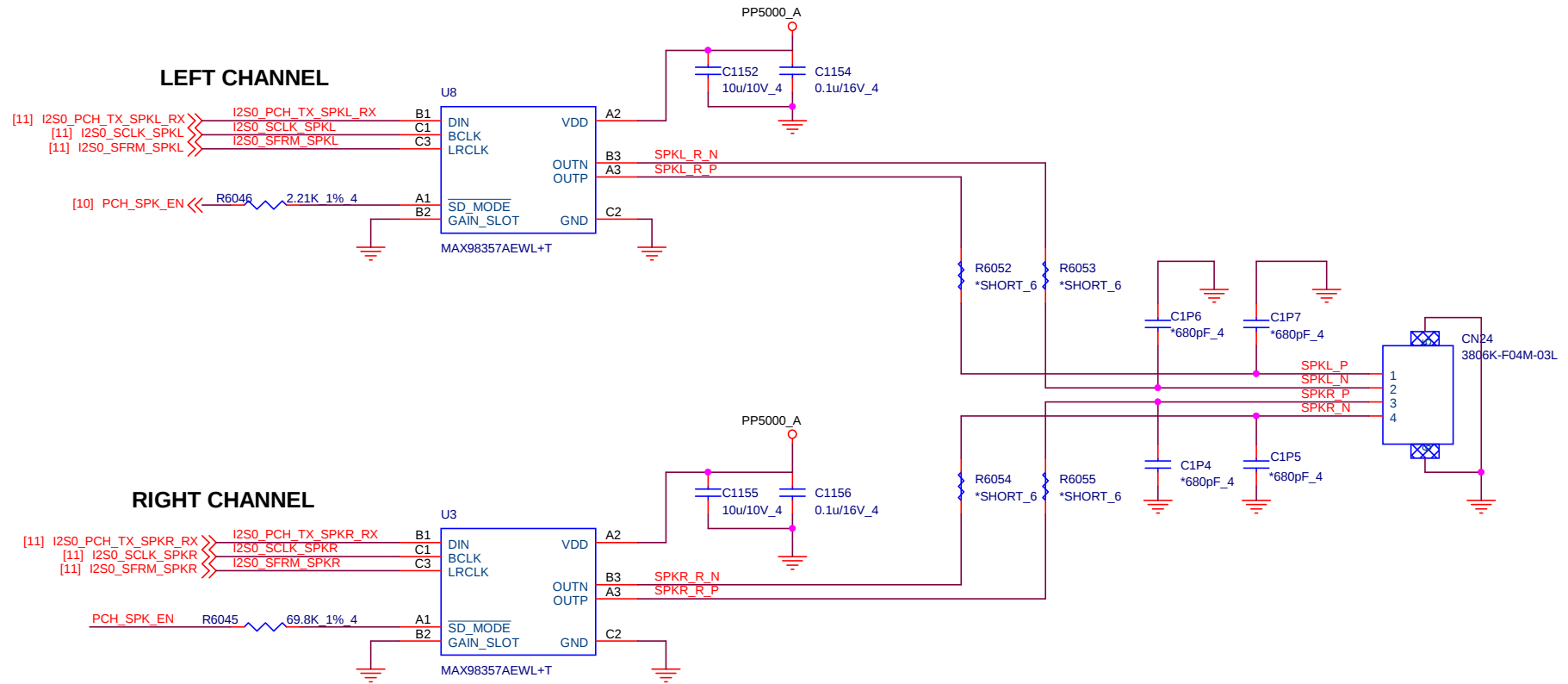
Reserved for NVME



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	EMMC/NVME	1A
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MAX98357A



LRCLK POLARITY

PART NUMBER	LRCLK POLARITY (LEFT CH)
MAX98357A	LOW
MAX98357B	HIGH

BCLK POLARITY

MODE	PART NUMBER	BCLK POLARITY
I2S	MAX98357A	Rising edge
Left Justified	MAX98357B	Rising edge
TDM	MAX98357A	Rising edge
	MAX98357B	Falling edge

GAIN TABLE

GAIN_SLOT	GAIN(dB)
PL 100K TO GND	15
PL TO GND	12
FLOATING	9
PU TO VDD	6
PU 100K TO VDD	3

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AUDIO - SPEAKER AMPS		
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Quanta Computer Inc.

PROJECT : ZSA

Size

Document Number

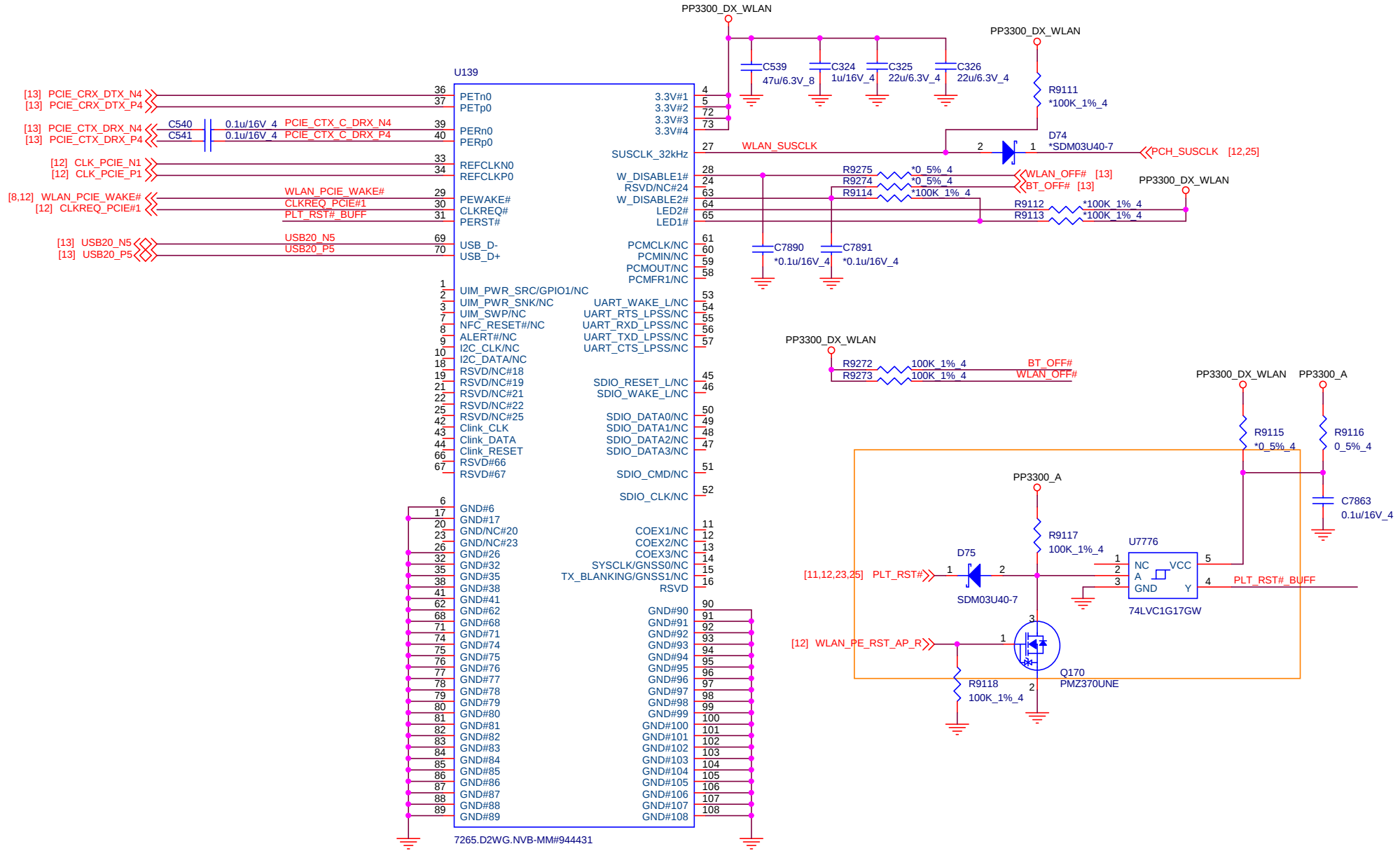
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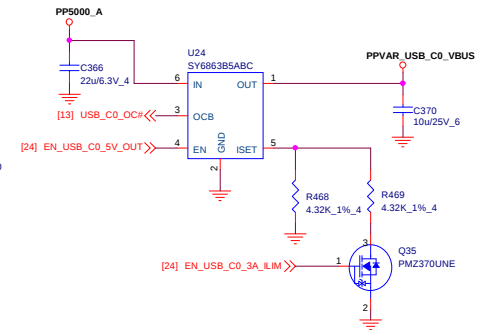
Date: Friday, July 27, 2018

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WLAN



FAN POWER

[illegible]

MICRO SD CARD

This schematic diagram illustrates the electrical connections for a Micro SD Card. The card's pins are connected to a PMOS supply and a Q53 MOSFET driver.

Micro SD Card Pins and Connections:

- Pin 1:** SD_DATA2_R (DAT2)
- Pin 2:** SD_DATA3_R (DAT3)
- Pin 3:** SD_CMD_R (CMD)
- Pin 4:** VDD
- Pin 5:** SD_CLK_R (CLK)
- Pin 6:** VSS
- Pin 7:** SD_DATA0_R (DAT0)
- Pin 8:** SD_DATA1_R (DAT1)
- Pin 9:** SD_CDZ_R (CD)
- Pin 10:** GND#3
- Pin 11:** GND#2
- Pin 12:** GND#1
- Pin 13:** GND#4
- Pin 14:** GND#5
- Pin 15:** CN16 A0528-0001

PMOS Supply and Biasing:

- PMOS:** Connected to the VDD pin (Pin 4).
- Resistors:** R9213 (10K_1%_4) and R9248 (0_5%_4) are connected in series between the PMOS supply and the SD_CDZ pin (Pin 9).
- Capacitors:** C491 (4.7u10V_4) and C492 (0.1u16V_4) are connected in parallel between the PMOS supply and the SD_CDZ pin (Pin 9).

Q53 MOSFET Driver:

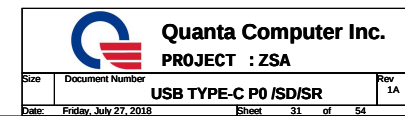
- Q53:** A MOSFET driver connected to the SD_CDZ pin (Pin 9).
- Gate:** Connected to the SD_CDZ pin (Pin 9).
- Source:** Connected to the SD_CDZ pin (Pin 9).
- Drain:** Connected to the SD_CDZ pin (Pin 9).

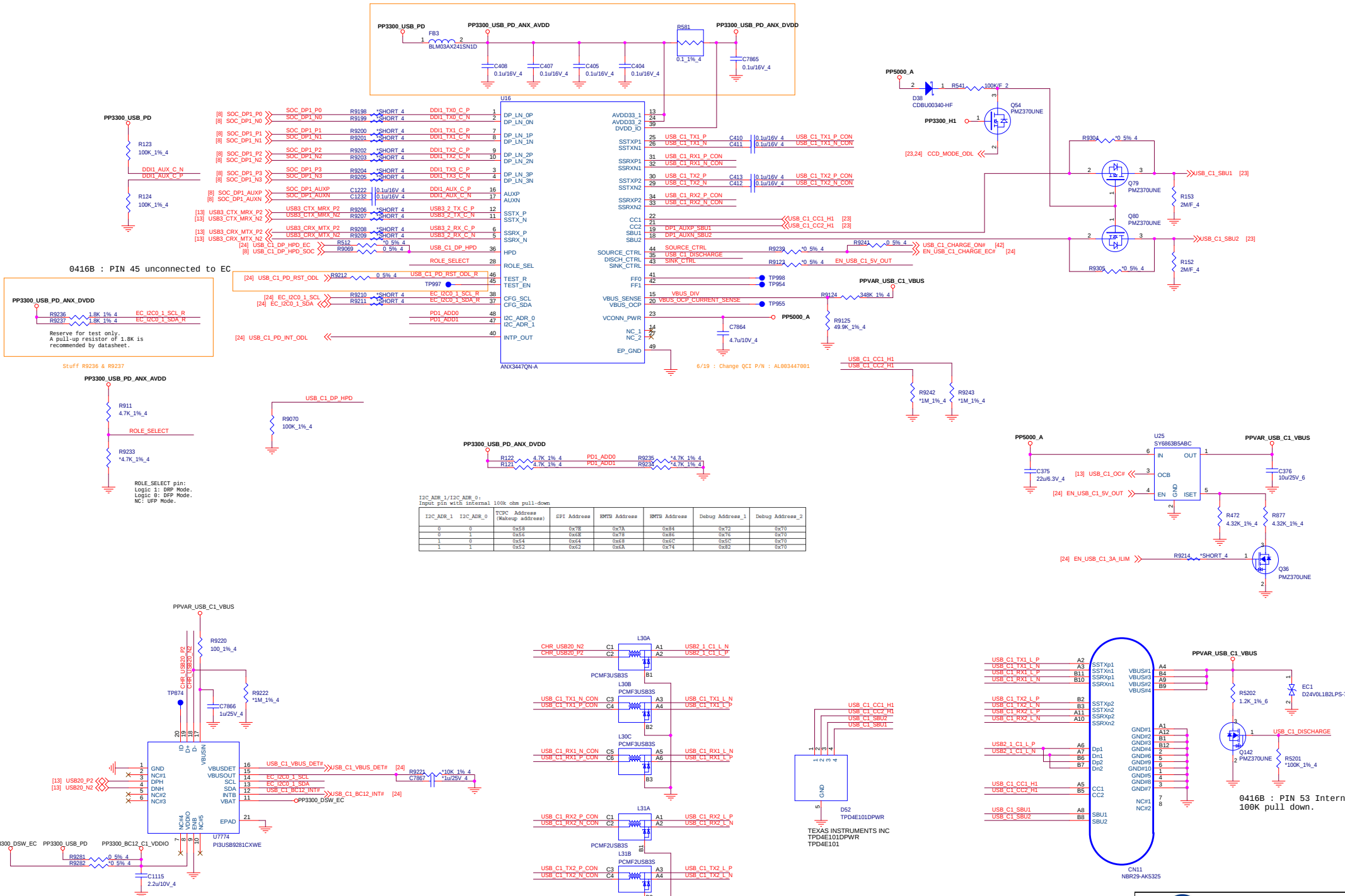
Confirm FP w/PDC.

PP3300_DSW PP3300_A PP3300_S PP3300_DX_SENSOR

EC_I2C_3_SDA
EC_I2C_3_SCL

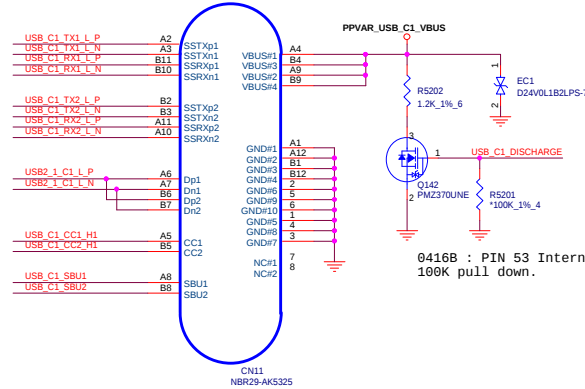
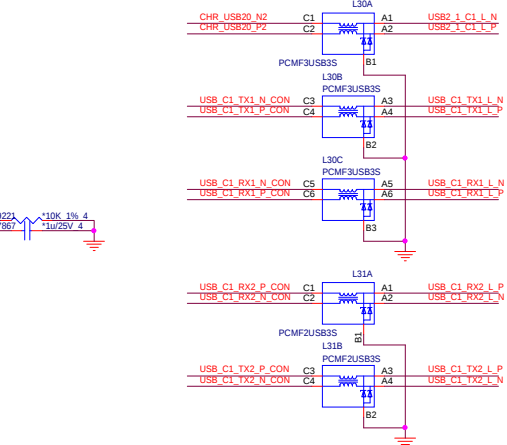
R6058 0.5% 4k
R9219 0.5% 4k
R5269 0.5% 4k





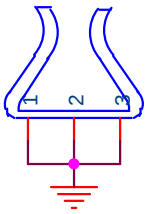
I2C_ADR_1/I2C_ADR_0:
Input pin with internal 100k ohm pull-down

I2C_ADR_1	I2C_ADR_0	I2C Address (Mainline address)	SPI Address	EMTB Address	EMTB Address	Debug Address_1	Debug Address_2
0	0	0x28	0x78	0x7A	0x72	0x70	0x70
0	1	0x48	0xA8	0x78	0xA6	0x76	0x70
1	0	0x44	0x64	0x6A	0x6C	0x60	0x60
1	1	0x2C	0x62	0x74	0x72	0x62	0x60

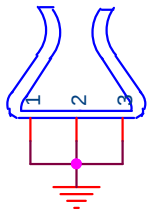


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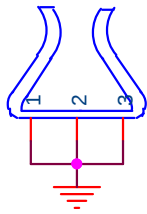
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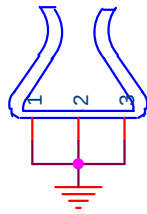
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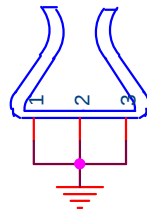
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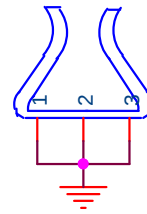
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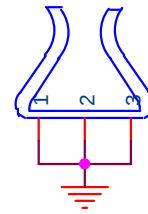
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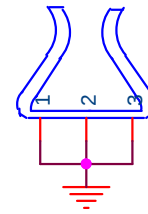
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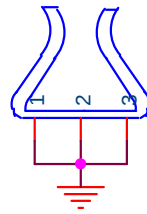
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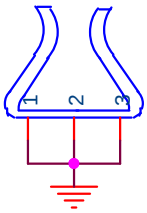
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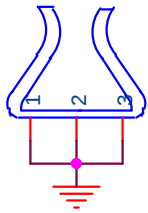
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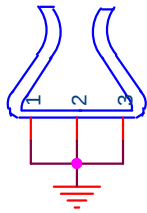
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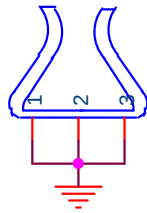
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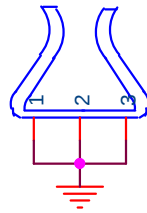
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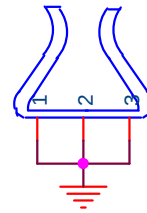
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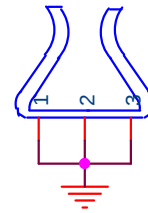
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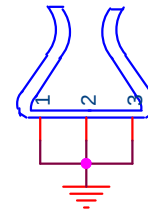
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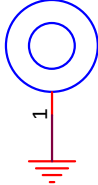
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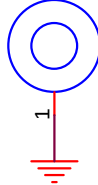
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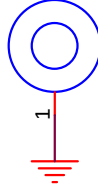
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*H-ZSA-2



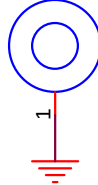
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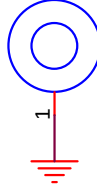
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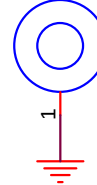
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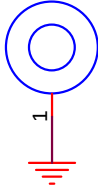
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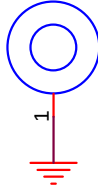
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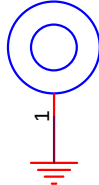
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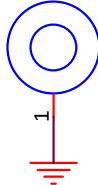
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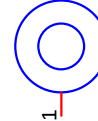
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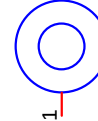
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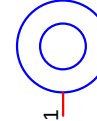
HOLE8
*H-C98D98N



HOLE16
*H-C177D177N



HOLE17
*H-O110X98D110X98N



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PCB, Screw, CLIP

Size

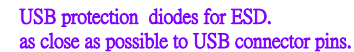
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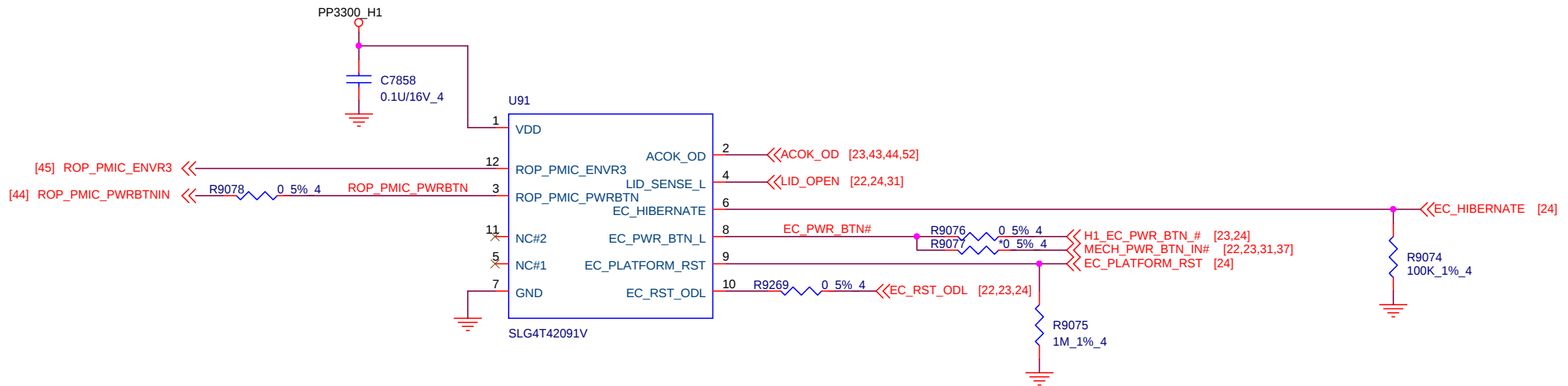
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Vbus discharge circuit



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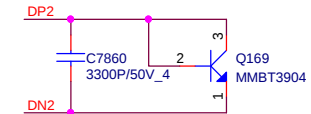
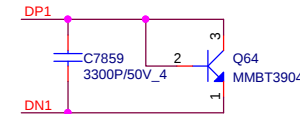
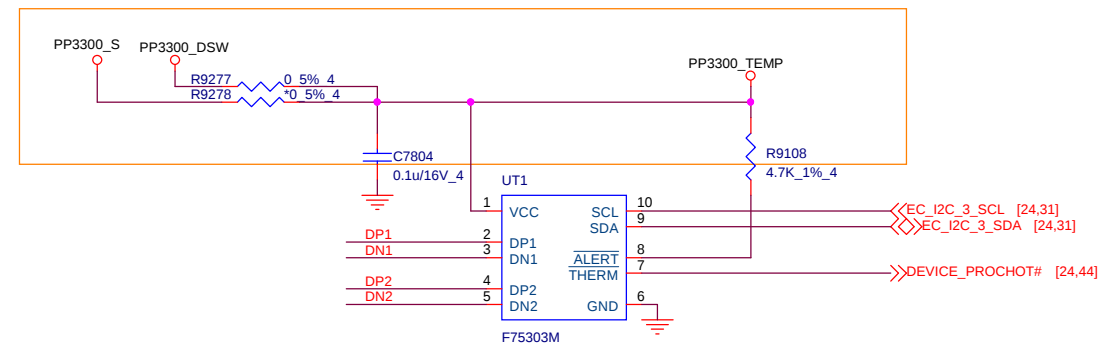
Pin Configuration

Pin#	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	ACOK_OD	Digital Input	Digital Input without Schmitt trigger	1M ohm pulldown
3	ROP_PMIC_PWRBTN	Digital Output	Open Drain NMOS 1X	floating
4	LID_SENSE_L	Digital Input	Digital Input without Schmitt trigger	100k ohm pullup
5	NC	--	Keep Floating or Connect to GND	--
6	EC_HIBERNATE	Digital Input	Digital Input without Schmitt trigger	floating
7	GND	GND	Ground	--
8	EC_PWR_BTN_L	Digital Input	Digital Input without Schmitt trigger	100k ohm pullup
9	EC_PLATFORM_RST	Digital Input	Digital Input without Schmitt trigger	floating
10	EC_RST_ODL	Digital Input	Digital Input without Schmitt trigger	100k ohm pullup
11	NC	--	Keep Floating or Connect to GND	--
12	ROP_PMIC_ENVR3	Digital Output	Open Drain NMOS 1X	floating


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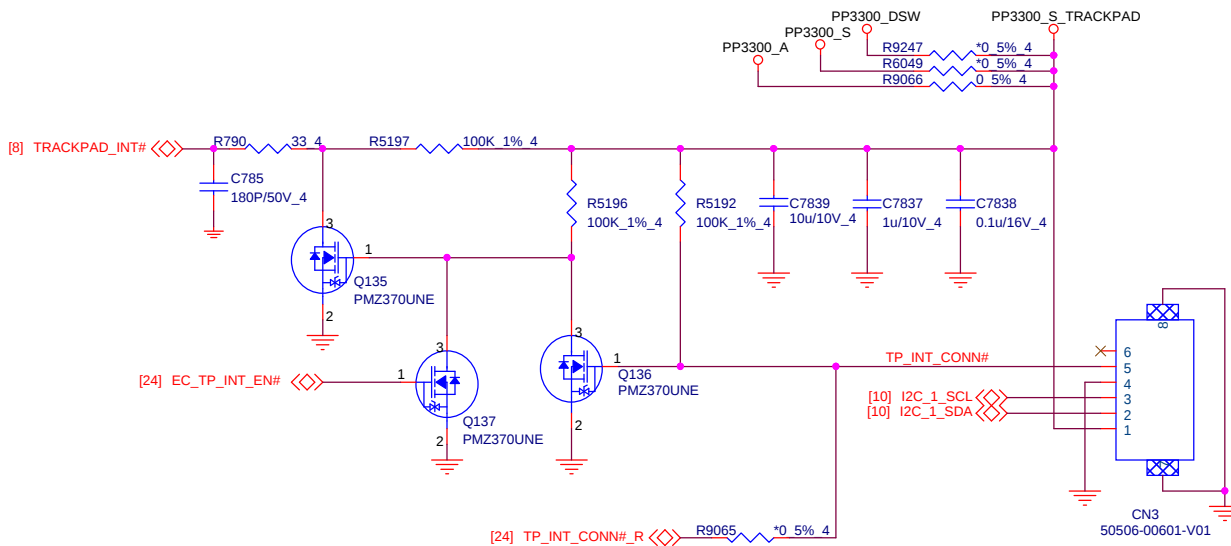
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	G3 WAKE	1A
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TEMP SENSORS



TRACKPAD CONNECTOR

Due to 3906 transistors is not common component in Quanta. Could we replace 3906 transistors by 3904 transistors? These two parts are substitute component in datasheet.



4.4 Pin Assignment

Pin Assignment and Description			
Pin #	Signal	I/O	Description
1	NC		NC
2	/SINT	O	Slave interrupt Indicates touchpad likes to send data to system (host)
3	GND	GND	Ground
4	I ² C_CLK	I/O	I ² C clock I _{Drive} or I _{Sink} : 8 mA max.
5	I ² C_DATA	I/O	I ² C data. I _{Drive} or I _{Sink} : 8 mA max.
6	VCC_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.



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	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	



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1A

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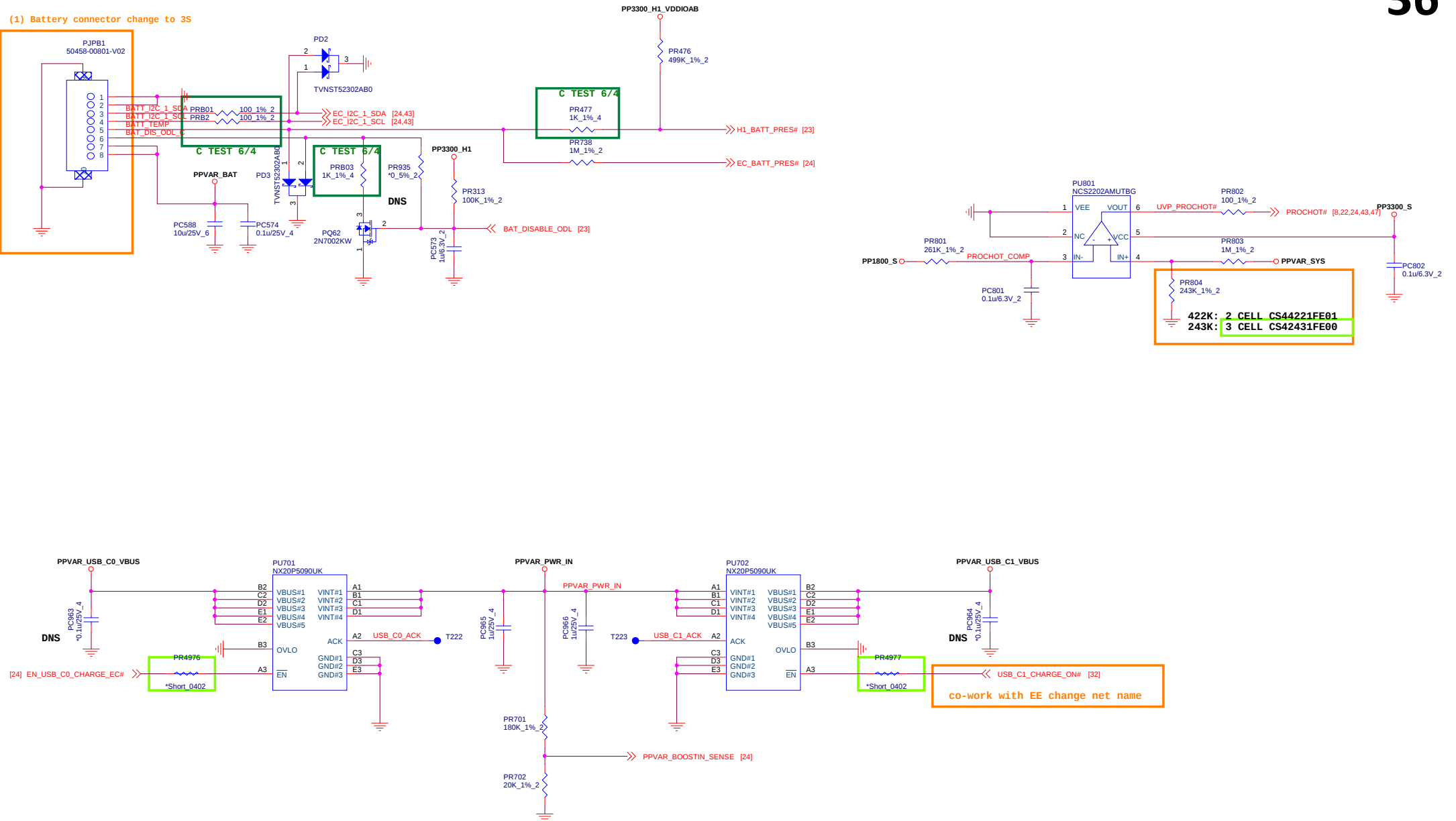
Rev

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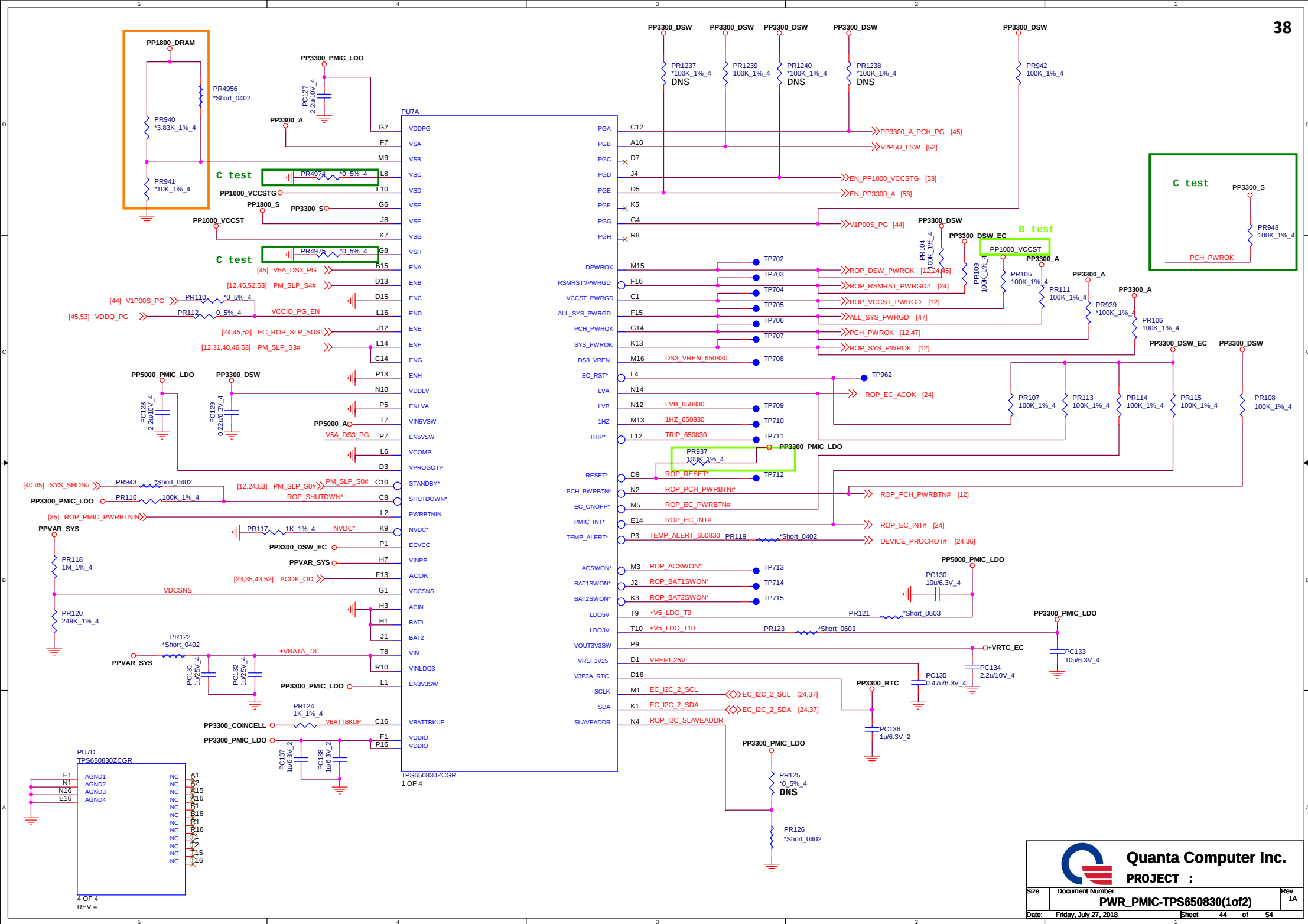
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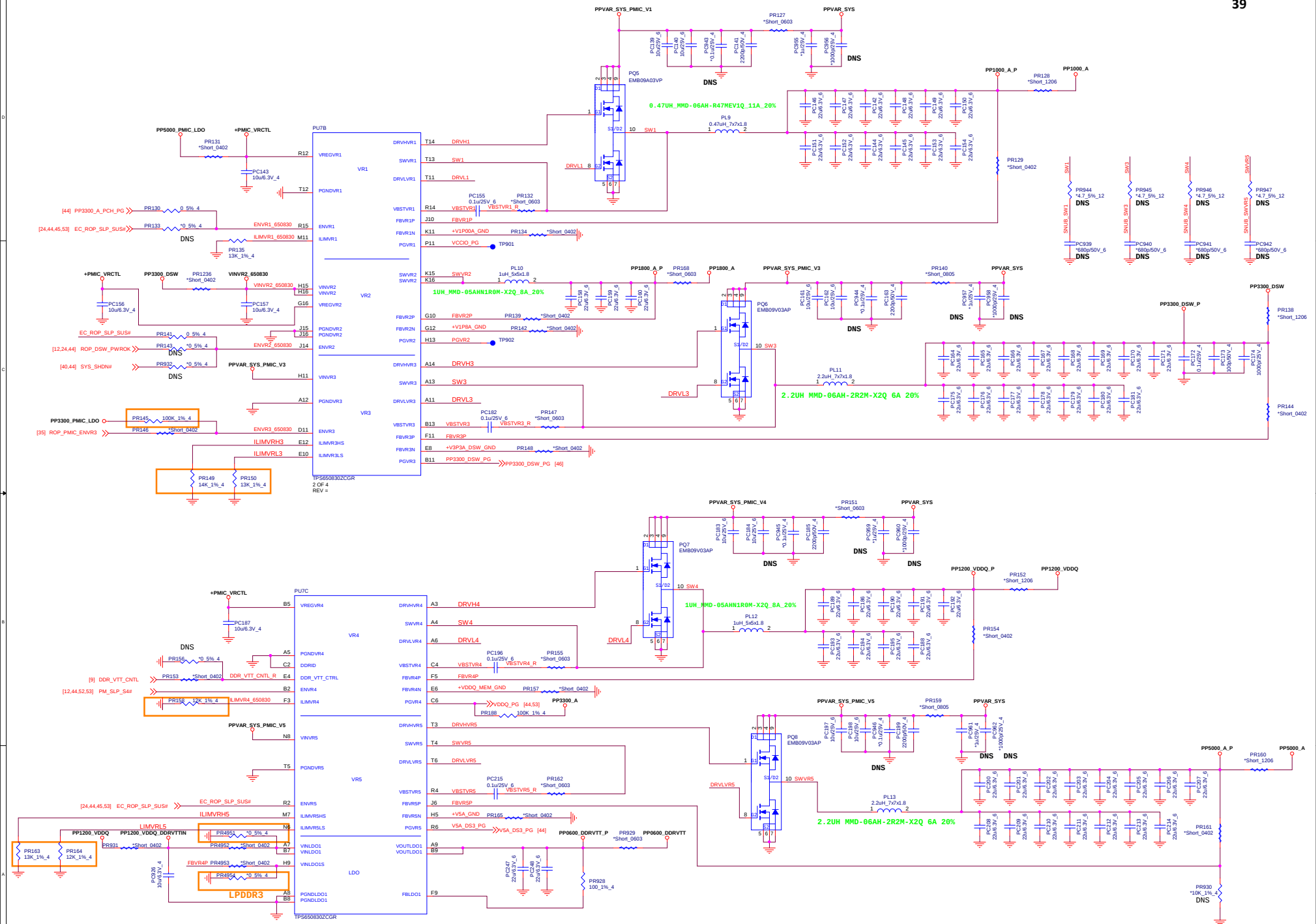
Sheet	41	of	35
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(1) Battery connector change to 3S

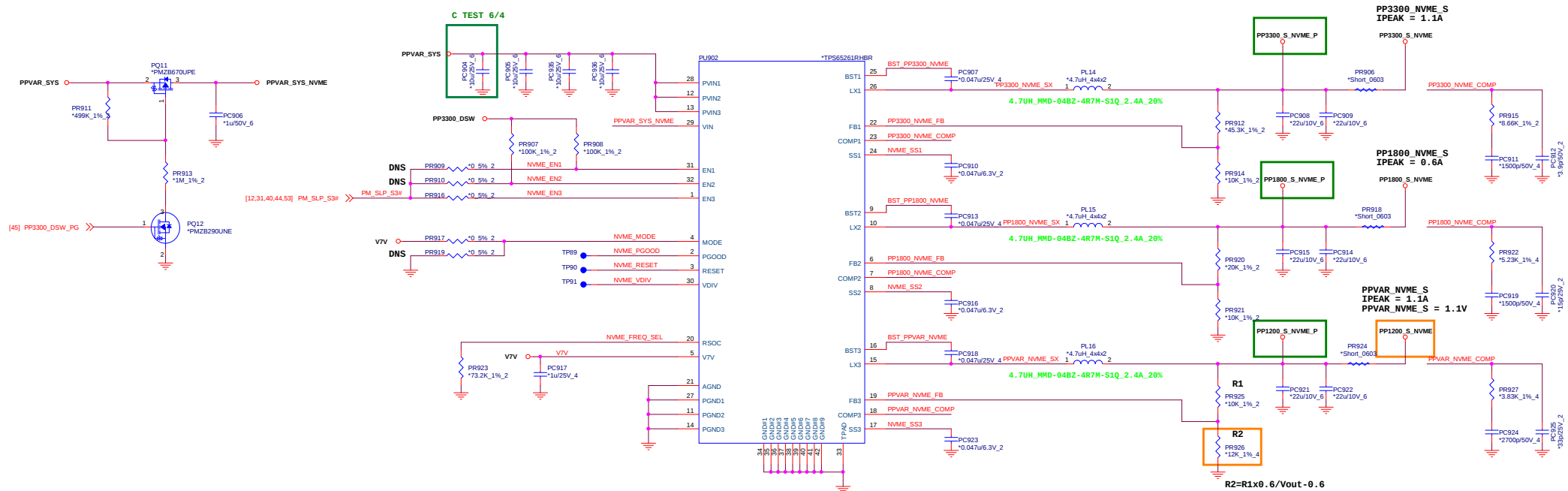


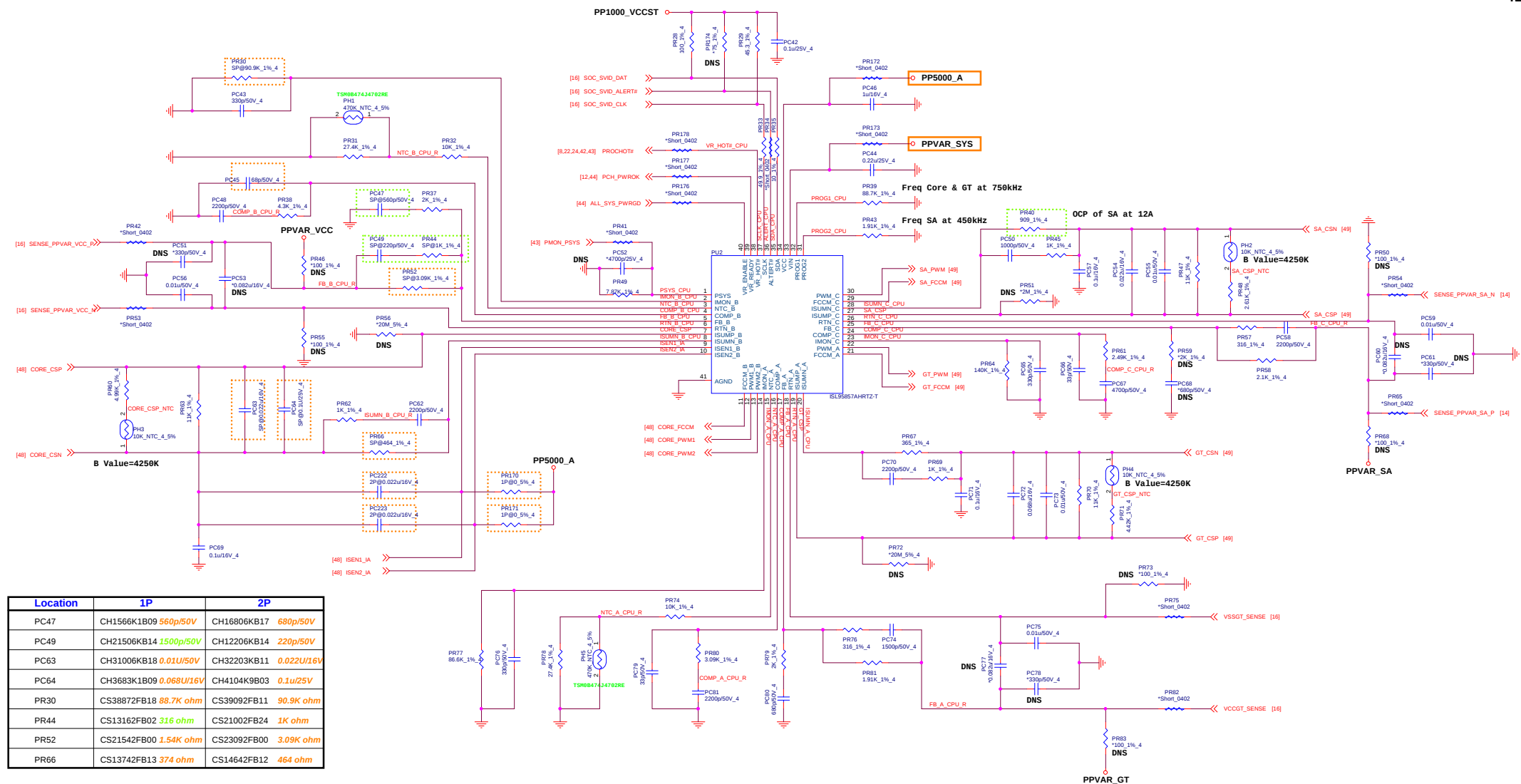






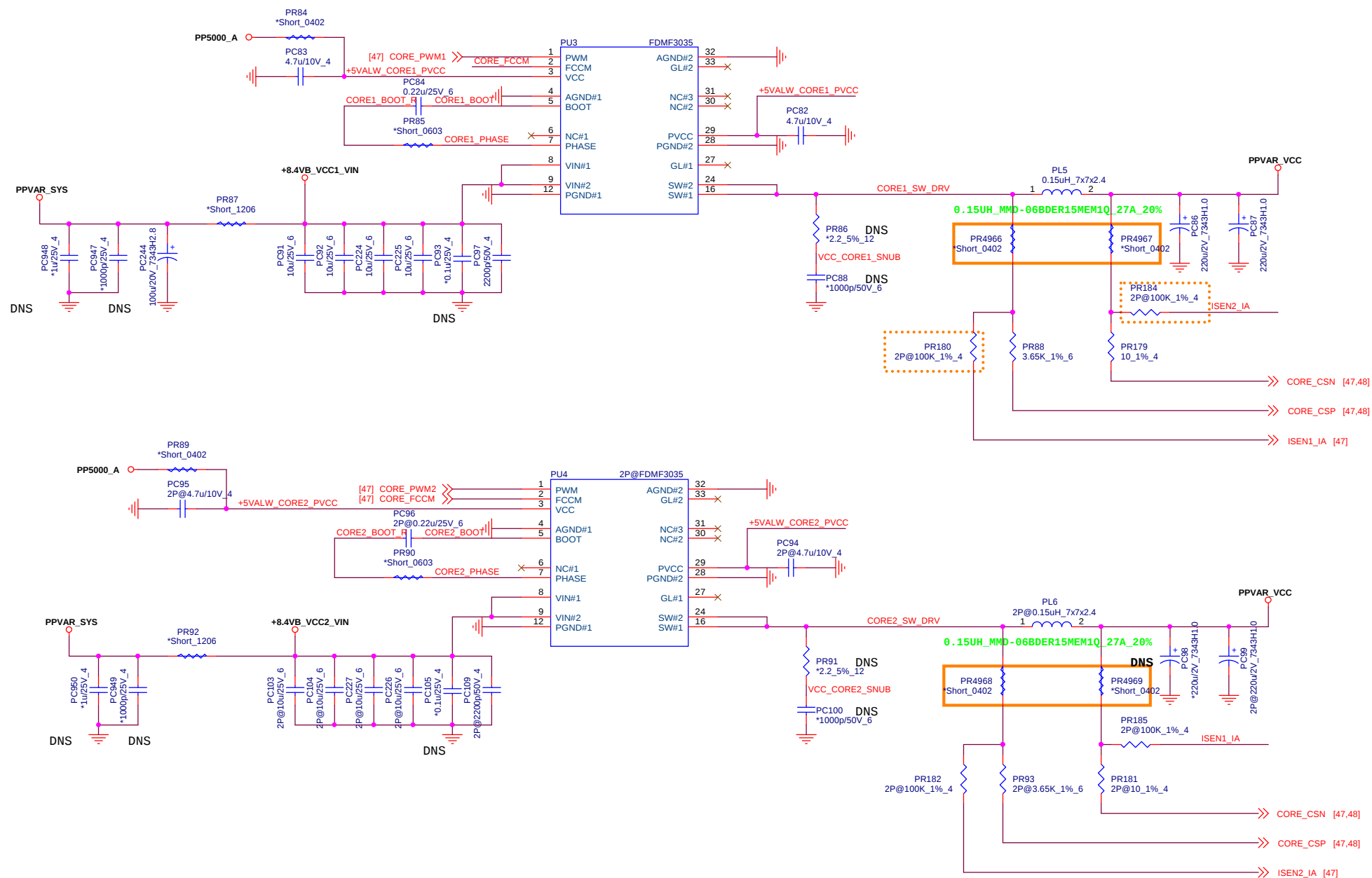
co-work with EE NVMe non staff

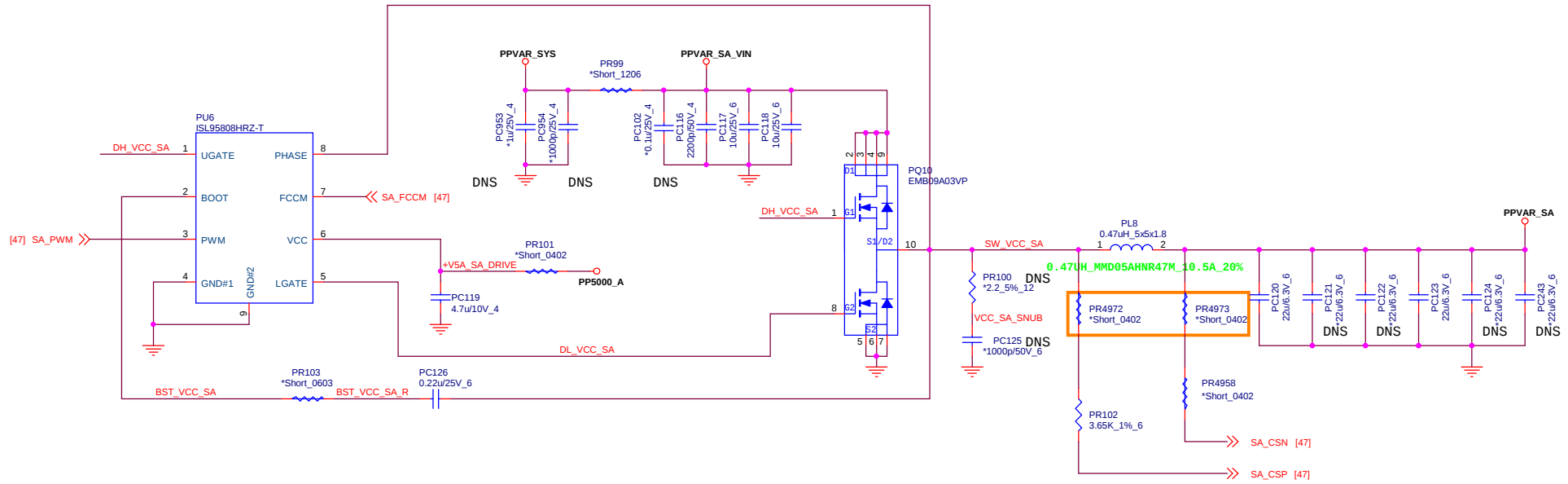
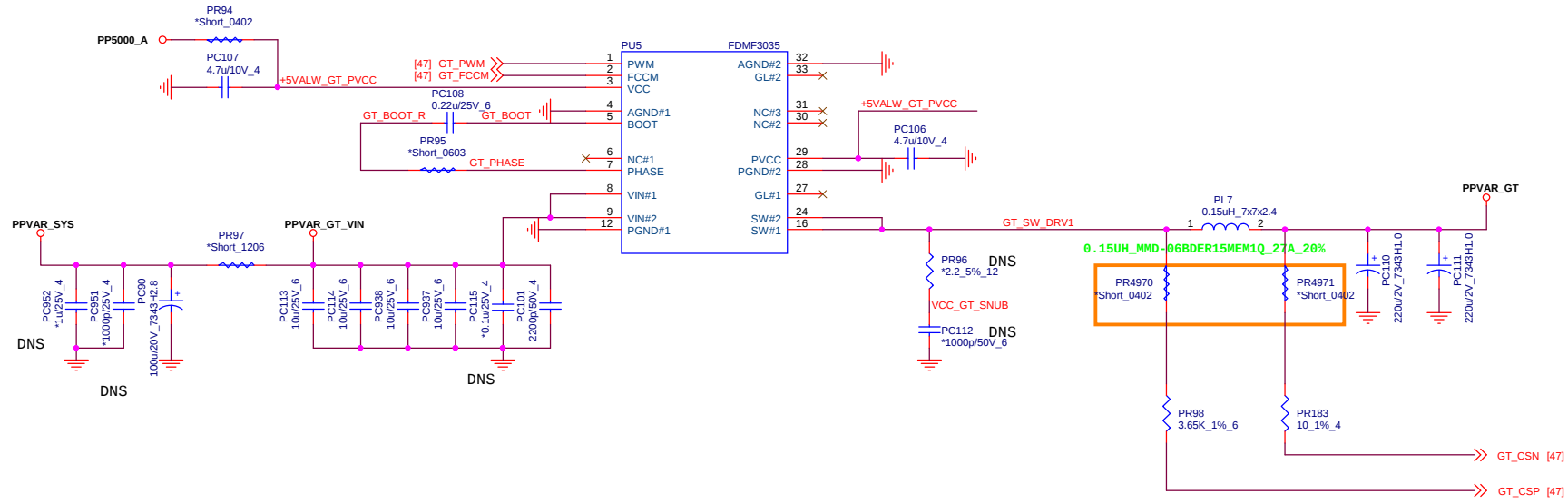




Location	1P	2P
PC47	CH1566K1B09 560p/50V	CH16806KB17 680p/50V
PC49	CH21506KB14 1500p/50V	CH12206KB14 220p/50V
PC63	CH31006KB18 0.01u/50V	CH32203KB11 0.022u/16V
PC64	CH3683K1B09 0.068u/16V	CH4104K9B03 0.1u/25V
PR30	CS38872FB18 88.7K ohm	CS39092FB11 90.9K ohm
PR44	CS13162FB02 316 ohm	CS21002FB24 1K ohm
PR52	CS21542FB00 1.54K ohm	CS23092FB00 3.09K ohm
PR66	CS13742FB13 374 ohm	CS14642FB12 464 ohm

Location	1P	2P
PC222	N/A	CH32203KB11 0.022u/16V
PC223	N/A	CH32203KB11 0.022u/16V
PR170	CS00002JB38 0 ohm	N/A
PR171	CS00002JB38 0 ohm	N/A







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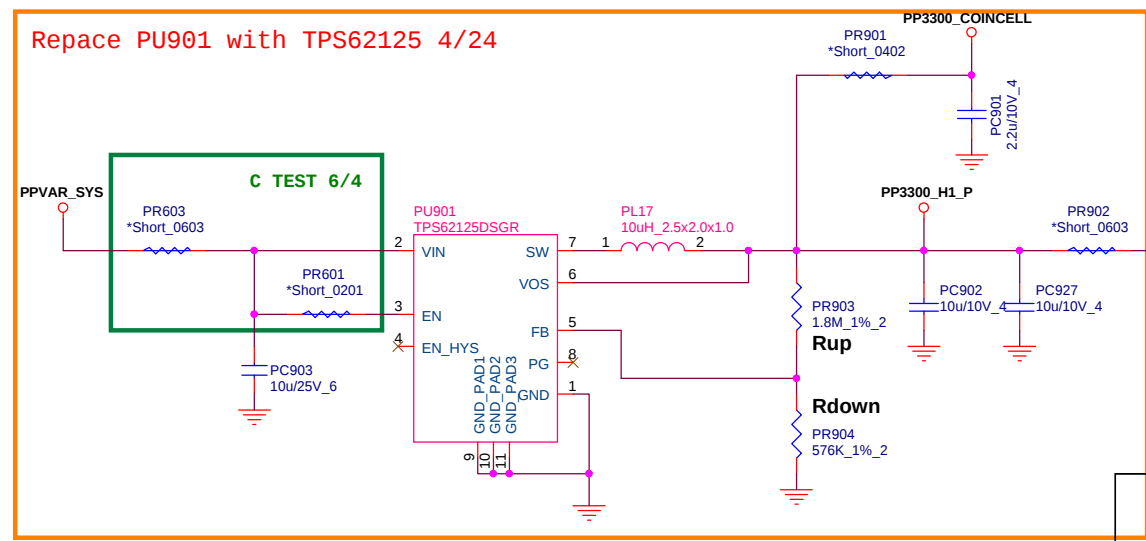
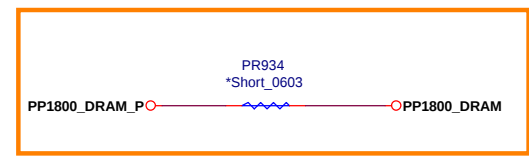
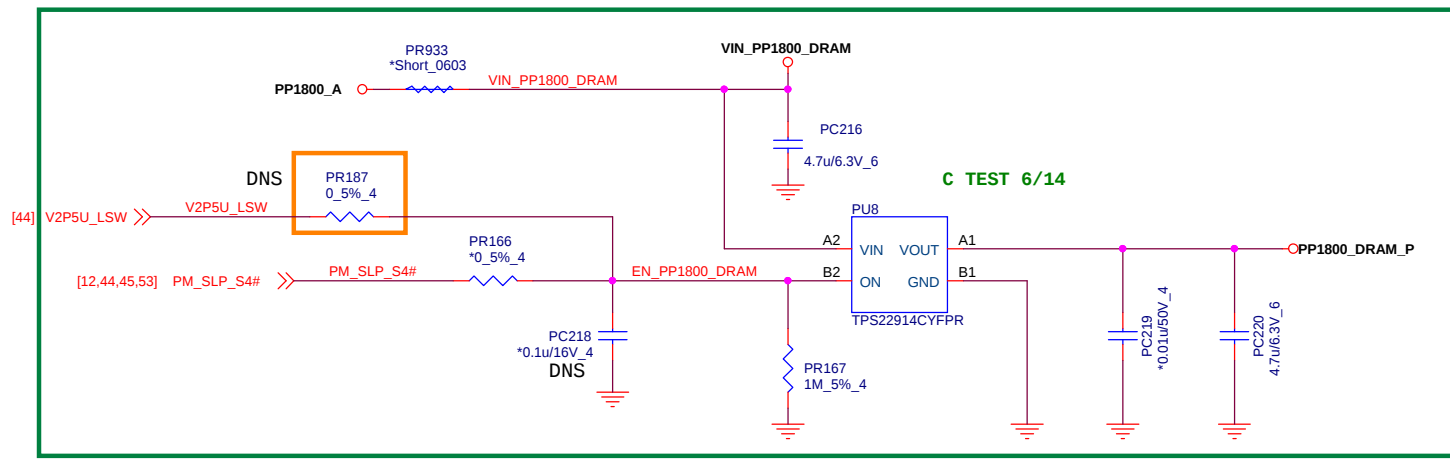
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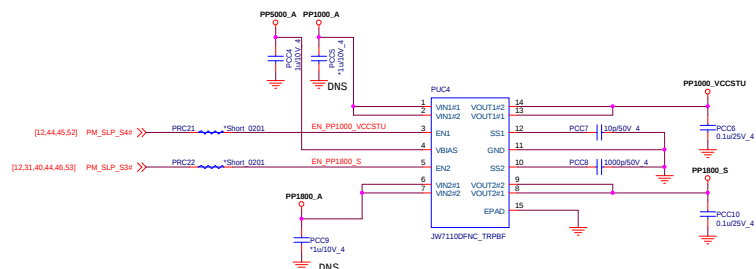
REV
1A

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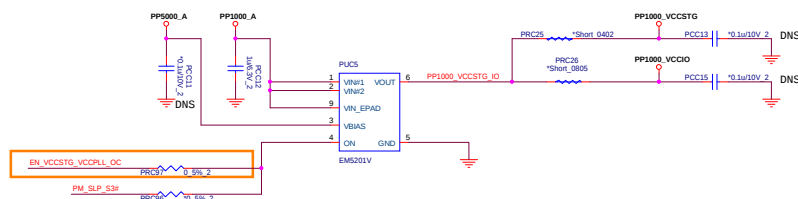


PP1000_A TO PP1000_VCCSTU

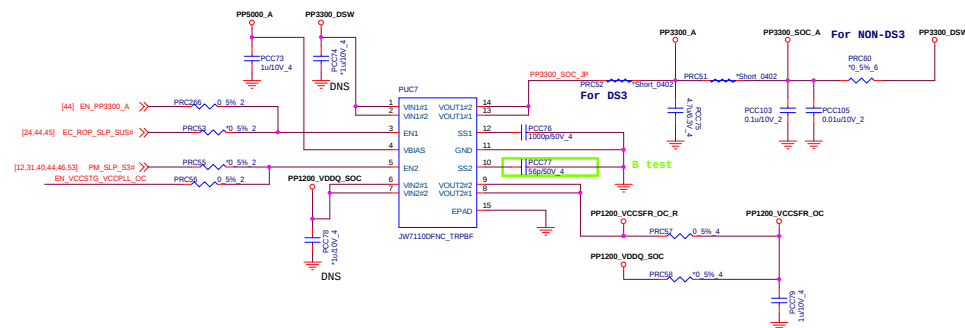


PP1800_A TO PP1800_S

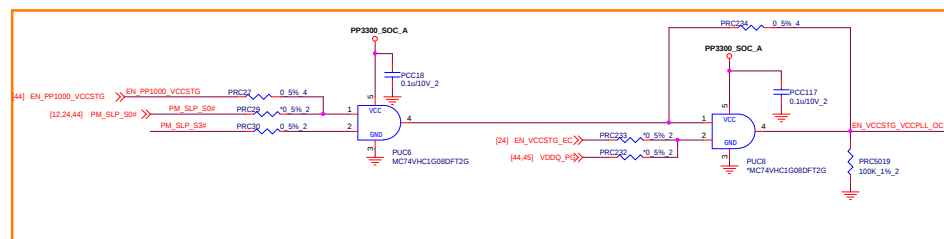
PP1000_A TO PP1000_STG / PP1000_VCCIO



PP3300_A TO PP3300_SOC_A



co-work with EE de1 PUC8



Model		Version	CHANGE LIST			
		1A	1. First release			
		1B	1. page 42: Change P1PB1 Battery connector for 3S Battery 2. page 43: PR22 from R2.5K change to 118K for 3S battery 3. page 44: Vendor suggest add PR4974 and PR4975 Connect VSC and VSH unused pins to GND better than let them floating 4. page 44: Add PR4955 for PP10B0DRAM 5. page 45: Add PR4951,PR4952,PR4953,PR4954 for LPDDR3_DRAM 6. page 47: Change net to correct form PP1000_ST change to PP1000_VCCST 7. page 47: Change net to correct PU2 PIN 33 VIN net to PPVAR_VS_PIN34 VCC net to PP5000_A 8. page 52: PR158 change to I2.7K for LPDDR3_DRAM 9. page 52: Net form PP2500_DRAM change to PP1800_DRAM, for LPDDR3_DRAM 10. MAG Inductor form xcl. change to xsQ (L&Q) inner code, Q is for Quanta ,L is for other customer) EE portion 1. page 13 : Remove R42 2. page 29 : Change NET name from EN_USB_A_5V to USB_A_5V_ODD Change NET name from +USB3_P4_VBUS to PPVAR_USB_CL_VBUS U16 change from P58751BQFN52GTR-A3 to ANX/447QN-A Add R9122 U25 change from NX3P3290UK to SY686B35ABC 3. page 9 : Remove R931 ,R922 ,R933 ,R934 ,C7817 & R934 4. page 10 : UCLAU13 Change connect from PP3300_DSW to PCH_BATLOWW 5. page 12 : UCLK20 & K21 Change connect to PP1000_VCCSTU UCLAM40 Change connect to PP1200_VDDQ_SOC 6. page 13 : UCLA119 Change connect to PP1800_A UCLA107 AD18 & AJ17 Change connect to PP3300_DSW UCLA1D15 Change connect to PP3300_SOC_A 7. page 28 : R984 Change connect to PMOS Add R9119 U24 change from NX3P3290UK to SY686B35ABC 8. page 11 : R984 Change connect to PMOS 9. page 27 : Correct wifi sch. . 10. page 31 : Q64 & Q169 Could we replace 2906 transistors by 3984 transistors? These two parts are substitute component in datasheet. 11. page 25 : Unstuff R6061 ,R6064 & R6077 12. page 7 :Correct memory sch. .			
		1C	EE portion 1. page 29 : add R9218, R9220, R9221, R9222, C7866, C7867 2. page 29 : change G sensor VDD to PP3300_A 3. page 28 : add R9219 4. page 21 : unstuff R628, R645 5. page 8 : unstuff Q167, Q168 Sch. Rev: 1C_0130			
		1D	1. page 8 : Add GPIO signal for LPDDR3 detection. Add pull up and pull down with GPP_E15. And unstuff pulldown 2. page 22 : Follow reference schematic ,delete pin 39 as WARM_RESET# 3. page 25 : Modify from NVME to eMMC schematic. 4. page 32 : Unstuff C7867 R9222 & R9221 5. page 30 : Unstuff Q170 6. page 31 : Unstuff R9073 , stuff R9072 7. page 36 : Unstuff R9106 & R9187 Sch. Rev: 1D			
		1E	1. Page 8 : 1. Add net name : PCH_EMMC_CONFIG 2. R9251 & R9252 Change to 10K PU. 3. Add table. 4 Stuff R9002 2. Page 32 : Unstuff R9239 and R9123 3. Page 53 : 1. DSX@ (PRC32 ,PRC76 & PCC73) change to stuff 2. DSX ,SDX@ (PRC27 & PCC73) change to stuff 3. MP@ (PRC26 ,PRC266 ,PRC25 & PRC51) change to stuff 4. XDP@ (R23 ,R236 ,R235 & R238) change to stuff 5. NDSX@ (PRC60 ,PRC55 ,PRC56 & PRC50) change to unstuff 6. Remove PUC8 related parts & circuit. 4. Page 19 : Del DDR Debug (Remove R24 & R48) 5. Page 31 : Add level shift (Q20 & Q171) 6. Page 39 : Keep layout and update INA address information 7. Page 13 : Connect GPP_E1 to PEN_EJECT_ODL 8. Page 21 : Correct part number for U4. Change part number to W25Q128JVSIM 9. Page 22 : Unstuff R9250 and stuff R9249 10. Page 30 : Stuff Q170 11. Page 24 : Revised U103 related parts & circuit. 12. Page 28 : R338 & R5286 connect to PP3300_S_TOUCHSCREEN			
		2A	EE portion 1. Page 36 : Add R79033 ohm) & C7857(100pf) for ESD 2. Page 13 & 15 : Add C7888 & C7889 (100nf) filter for enhance sensitive net ESD level 3. Page 24 : R401 change to 2.2 ohm for ESD 4. Page 24 : TOUCHSCREEN_D159 not need to connect to the panel side. 5. Page 13 : Follow reference schematic to add. R9265 6. Page 8 : Change R9251 to 1K ohm. 7. Page 22 : WARM_RESET# PU 100K ohm to PP3300_A PWR portion 1. Page 40 : Stuff PR960 with 0 ohm for wrong straping resistor 3. Page 42 : Add PR4976 and PR4977 with 0 ohm for measure 4. Page 43 : PC28,PC29 change to 0402 package 5. Page 44 : PR185 change pull high to PP1000_VCCST 6. Page 46 : Change PR696,PR918,PR924 location from beofore Divided resistor to After output MLCcs. 7. Page 47 : Make option table for U22 and U42 8. Page 53 : PRC77 change to 56p to meet SDIs sequence 9. Page 45 : Add PR1108 10. Page 44 : Unstuff PR110 11. Page 45 : PR127 & PR929 change to 0.01 ohm 12. Page 45 : Add PRC27 ,PUC8 ,PRC23 & PRC232 for power sequence adjustment			
		2B	1. Page 37 : Reverse CN18 for design change. 2. Page 29 : Change DMIL level shifter to FJA130KAVCS4b) 1.1 max (TXB0302DQMR: Waiting for vender spec for apply P/N & footprint.) 3. Page 16 : Follow latest review to remove TP11 ,TP12 & TP6 4. Page 23 : Stuff R678 and R677 5. Page 32 : USB_C1 ,SBU1 & USB_C1 ,SBU2 add related circuit. 6. Page 31 : GYRO change power source to PP3300_DSW 7. Page 17 : ADD PP3300_DSW to J10.37 for G-sensor 8. Page 31 : ADD PP1800_A in J10.13 for EMR 9. Page 32 : Stuff R9123 10. Page 25 & 46 : PP1100_S_NVME rename to PP1200_S_NVME 11. Page 24 : Add PRC233 for power sequence adjustment 12. Page 16 : Follow latest review that PPVAR ,GTX ,VCC change to PPVAR_VCC, and always stuff R6016 & R21			
		2C	1. Page 28 : Unstuff R9006 ,R9007 ,Q165 & Q166 and stuff R9215 & R9216 2. Page 24 : Reverse R9268. PWR portion 1. Page 40 : Change PC28 & PC29 from 1uF to 2.2uF 2. Page 40 : Unstuff PR385 and stuff PR960 3. Page 54 : PP3300_A INA is on the wrong address, it should be on tx40			
		2D	1. Page 52 : Replace PU961 with TPS62125 .			
		2E	1. Page 35 : Add R9269. 2. Page 24 : Add R9270. 3. Page 40 : Add PR4978 & PR4979 Change PU53 to TPS62915			
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