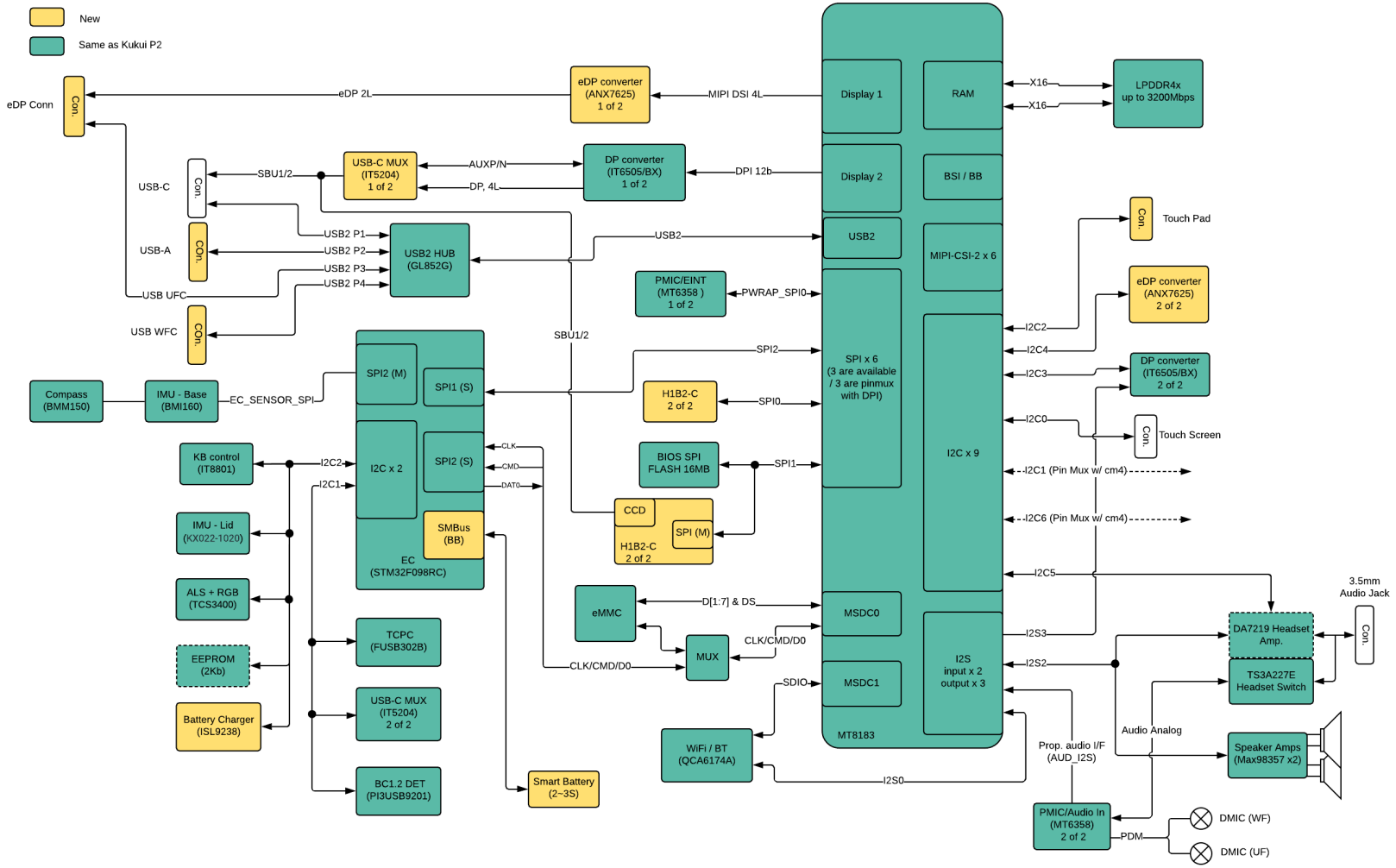
Jacuzzi Proto
MT8183 Chromebook Convertible
2019-12-16



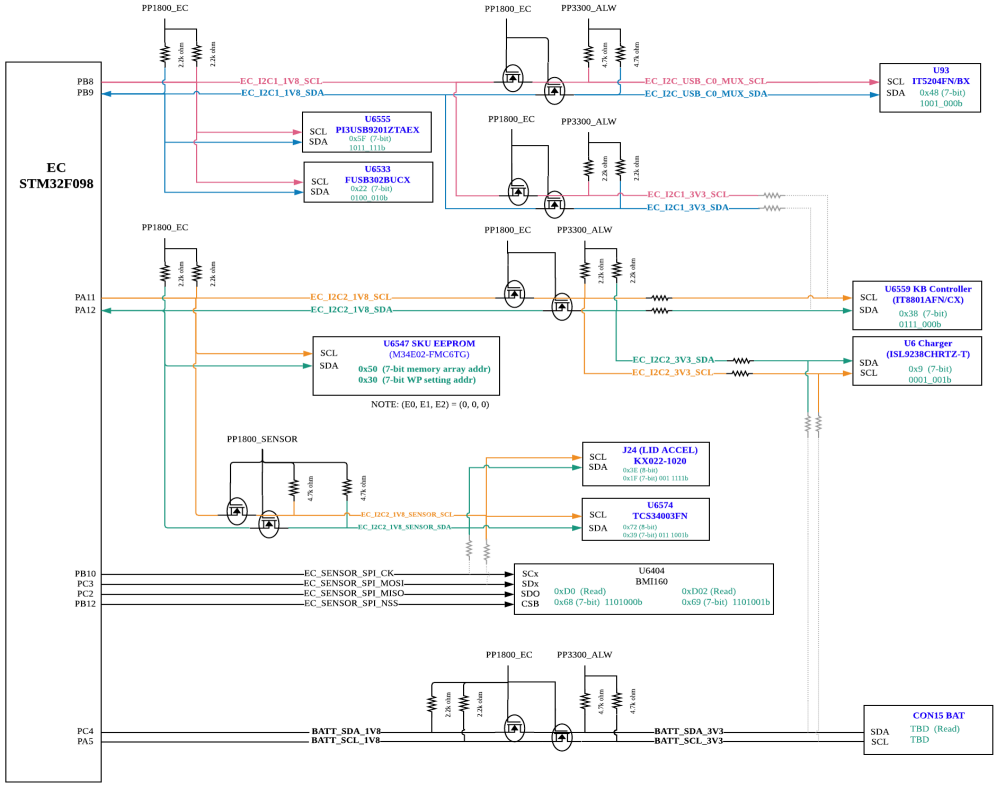
Quanta Computer Inc.
PROJECT : ZDE
Size | Document Number: 01_Block_Diagram | Rev: 1A
Date: Wednesday, May 06, 2020 | Sheet 1 of 39

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

EC_I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)	Note
I2C-1	IT5204FN/BX			0x90 (8-bit) ; 0x48 (7-bit)	
	PI3USB9201ZTAEX			0xBE (Read)	
	FUSB302BUCX			0x44 (Read)	
	IT8801BFN/CX			0x70 (8-bit) 0111_000b	Default NC
I2C-2	IT8801BFN/CX			0x70 (8-bit) 0111_000b	
	ISL9238CHRTZ-T			0x12 (8-bit) 0001_001b	
	BATTERY			0x?? (Read) ????_???b	
	KX022-1020			0x3E (8-bit) ; 0x1F (7-bit) 001 1111b	
	TCS34003FN			0x72 (8-bit) ; 0x39 (7-bit) 011 1001b	
	M34E02-FMC6TG			Memory area select code: 0xa0, PSWP: 0x60	
	BMI160			0xD0 (Read) 0x68 (7-bit) 1101000b 0xD02 (Read) 0x69 (7-bit) 1101001b	Default NC

I2C	AP, SCP	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)	Note
I2C-0	AP	CTP		Yes.	0X10	
I2C-1 (I3C)	TBD	-		Yes.	-	
		-		Yes.	-	
I2C-2 (I3C)	AP	Track Pad		Yes.		
I2C-3	AP	IT6505		Yes.	0x5C	
I2C-4 (I3C)	AP	ANX7625BN-AC-R		Yes.		
I2C-5	AP	DA7219		Yes.	0x1A	Default NC
		TS3A227EYFFR		Yes.	0x3B	
I2C-6	TBD	-		Yes.	-	

Jacuzzi EC I2C Block Diagram



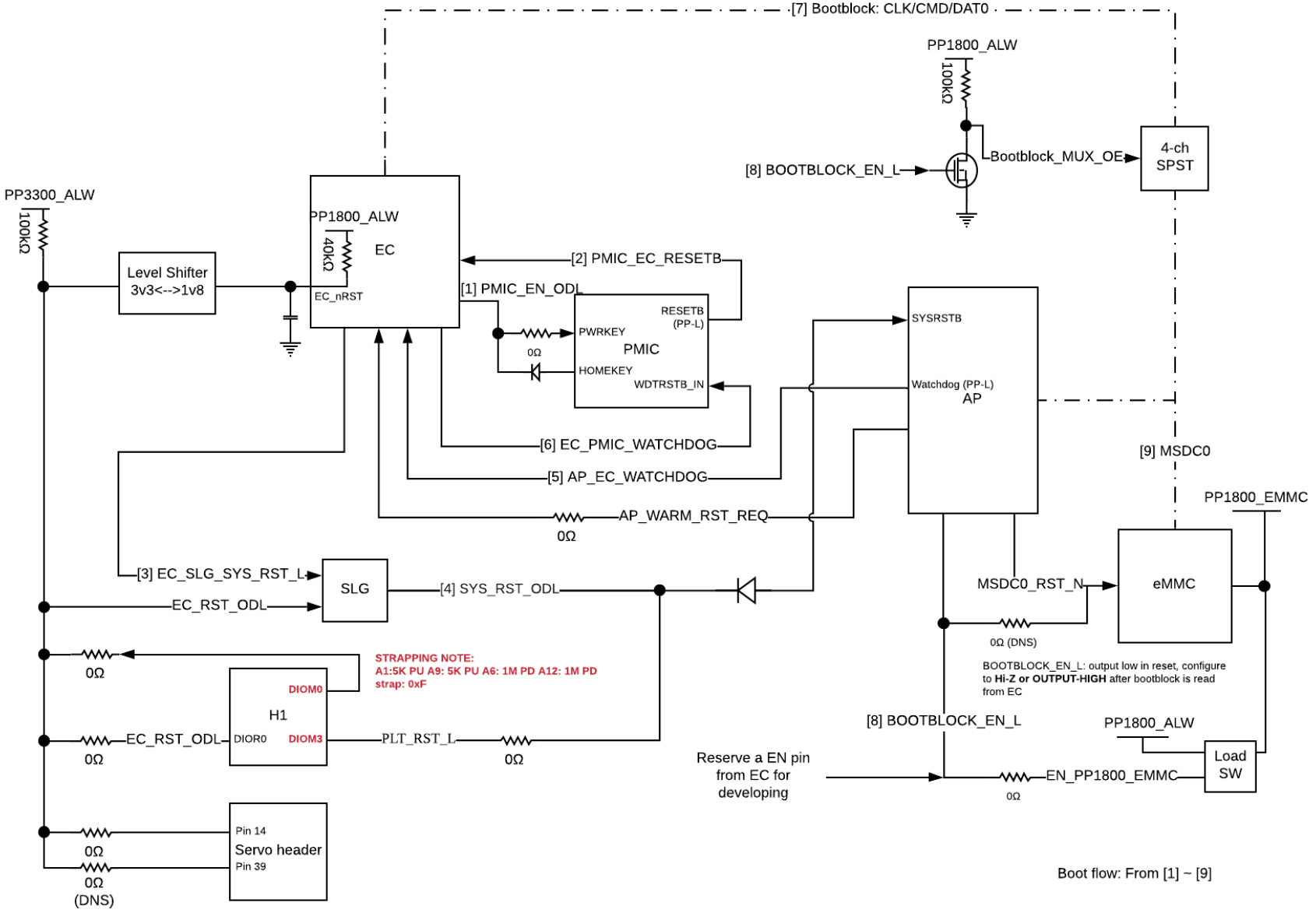
I2S	Device	Function
I2S2_MCK I2S2_BCK I2S2_LRCK I2S2_DI I2S3_DO	DA7219	Earphone
	MAX98357AEWL+T	Speaker AMP
I2S5_BCK I2S5_LRCK I2S0_DI I2S5_DO	U69H025.XX	Wifi Module BT
I2S3_TDM_BCK I2S3_TDM_LRCK I2S3_TDM_D0 I2S3_TDM_D1 I2S3_TDM_D2 I2S3_TDM_D3	IT6505	DPI to DP bridge audio

SPI		
Net Name	**Master**	**Slave**
AP_SPI_FLASH_CS_L AP_SPI_FLASH_CLK AP_SPI_FLASH_MOSI AP_SPI_FLASH_MISO	**AP**	**NOR FLASH**
SPI_AP_EC_CS_L SPI_AP_EC_CLK SPI_AP_EC_MOSI SPI_AP_EC_MISO	**AP**	**EC**
DEBUG_SPI_FLASH_CS_L DEBUG_SPI_FLASH_CLK DEBUG_SPI_FLASH_MOSI DEBUG_SPI_FLASH_MISO	**H1 or Servo**	**NOR FLASH**

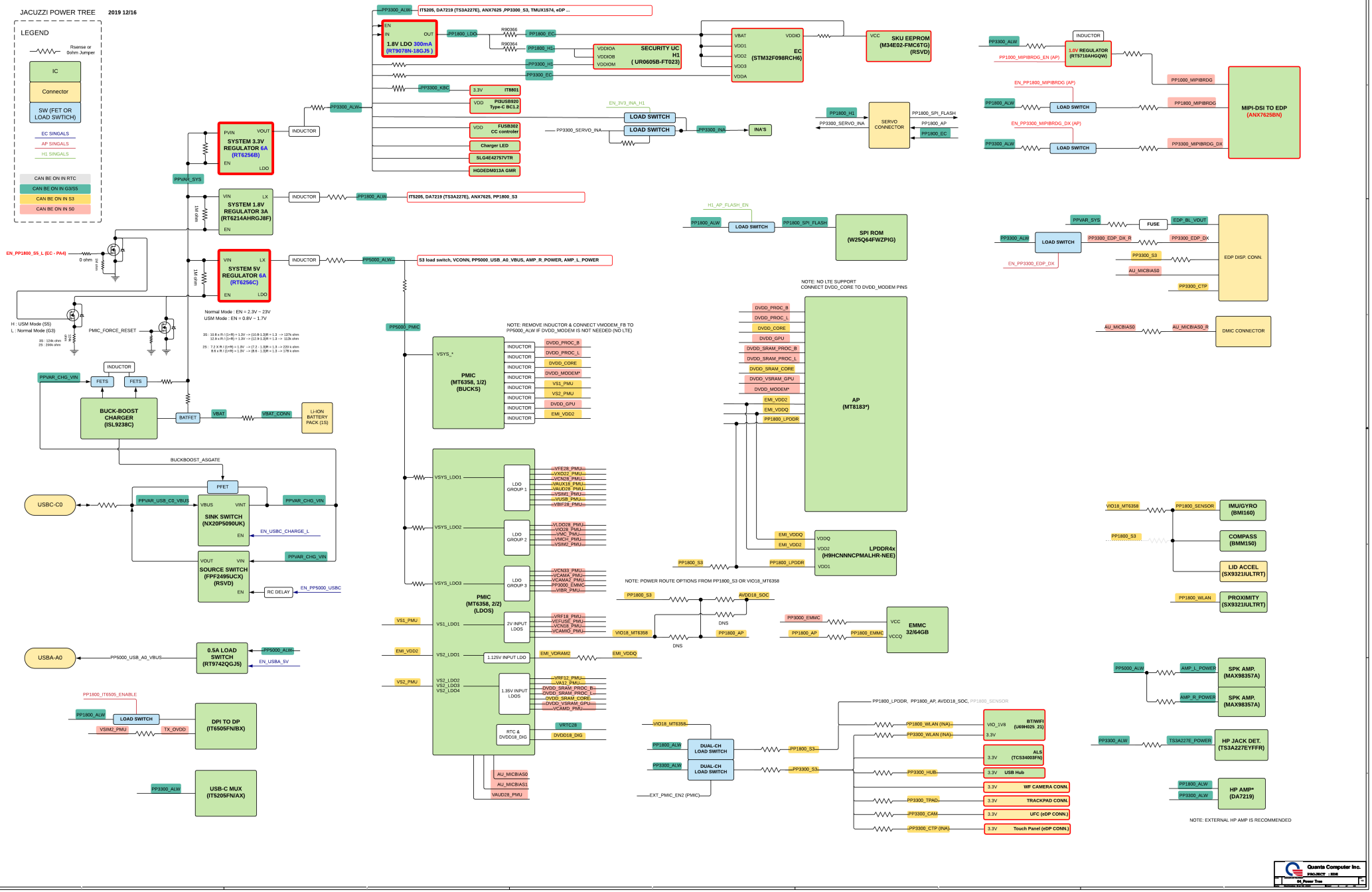
BOM value option	
ALS@	Ambient Light Sensor (*default non)
GMR@	GMR Sensor (*default non, GMR is on SUB-BOARD)
2CM@	2nd camera (*default non)
ECO@	E-compass (*default non)

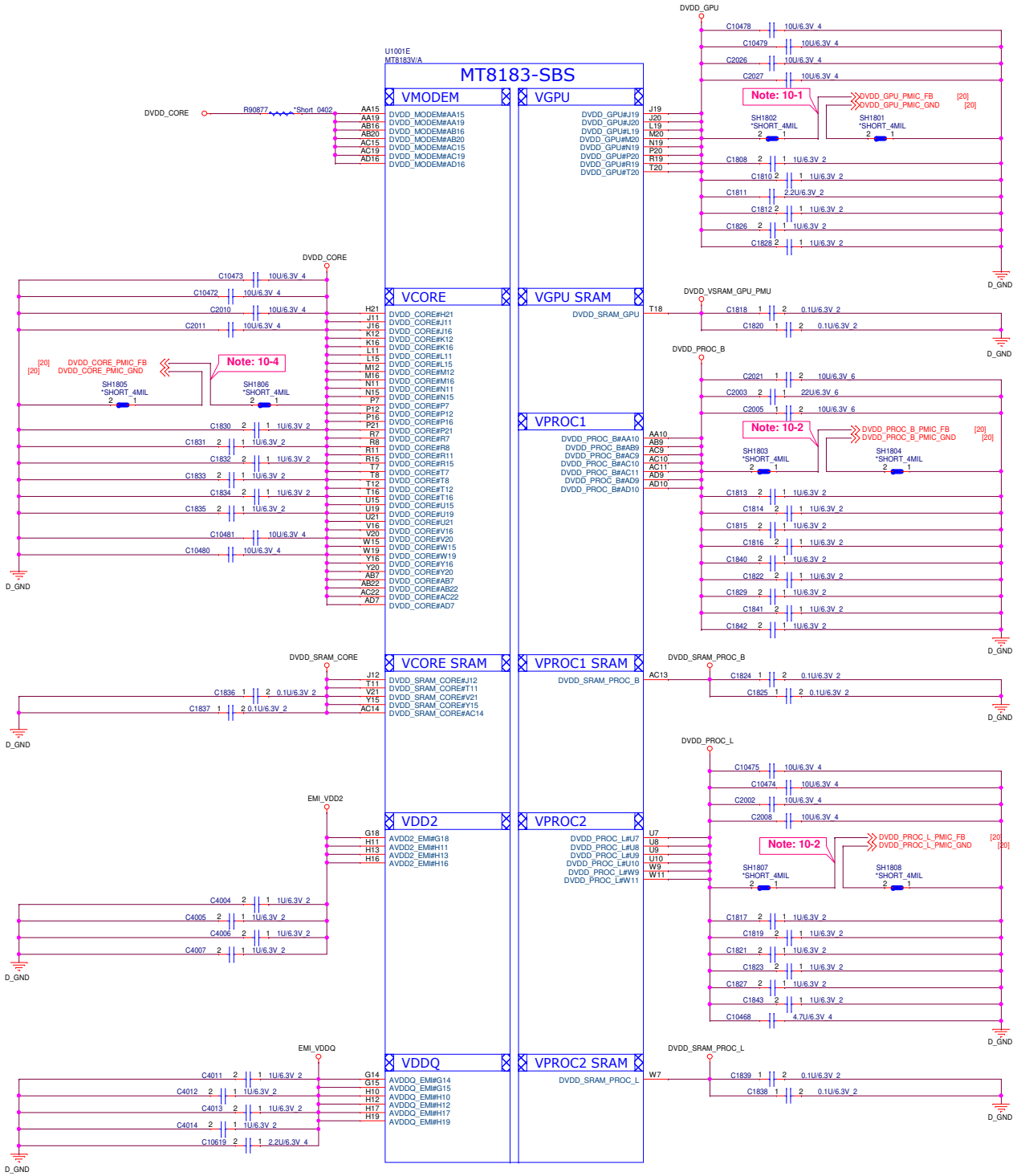
Quanta Computer Inc.
PROJECT : ZDE
Size | Document Number | Rev
02_Interface_Overview | 1A
Date: Wednesday, May 09, 2020 | Sheet 8 of 39

Reset Map
Ver2.3



Quanta Computer Inc.		
PROJECT : ZDE		
Size	Document Number: 03_EC_Reset_Map	Rev 1A
Date: Wednesday, May 06, 2020	Sheet 3 of 39	


JACUZZI POWER TREE
2019 12/16
LEGEND
Rsense or 0ohm Jumper
IC
Connector
SW (FET OR LOAD SWTICH)
EC SINGALS
AP SINGALS
H1 SINGALS
CAN BE ON IN RTC
CAN BE ON IN G3/S5
CAN BE ON IN S3
CAN BE ON IN S0
PP3300_ALW
IT5205, DA7219 (TS3A227E), ANX7625 ,PP3300 ,S3, TMUX1574, eDP ...
1.8V LDO 300mA (RT9078N-18GJ5)
PP1800_LDO
R90366
R90364
PP1800_EC
PP1800_H1
PP3300_H1
PP3300_EC
SECURITY UC H1 (UR0605B-FT023)
EC (STM32F098RCH6)
SKU EEPROM (M34E02-FMC6TG) (RSVD)
PP3300_KBC
3.3V IT8801
VDD PI3USB920 Type-C BC1.2
VDD FUSB302 CC controler
Charger LED
SLG4E42757VTR
HGDEDM013A GMR
EN_3V3_INA_H1
LOAD SWITCH
LOAD SWITCH
PP3300_SERVO_INA
PP3300_INA
INA'S
PP1800_H1
PP3300_SERVO_INA
SERVO CONNECTOR
PP1800_SPI_FLASH
PP1800_AP
PP1800_EC
PP3300_ALW
INDUCTOR
1.0V REGULATOR (RT5710AHGQW)
PP1000_MIPIBRDG_EN (AP)
PP1000_MIPIBRDG
EN_PP1800_MIPIBRDG (AP)
PP1800_ALW
LOAD SWITCH
PP1800_MIPIBRDG
MIPI-DSI TO EDP (ANX7625BN)
EN_PP3300_MIPIBRDG_DX (AP)
PP3300_ALW
LOAD SWITCH
PP3300_MIPIBRDG_DX
PVIN VOUT
SYSTEM 3.3V REGULATOR 6A (RT6256B)
EN LDO
INDUCTOR
PPVAR_SYS
VIN LX
SYSTEM 1.8V REGULATOR 3A (RT6214AHRGJ8F)
EN
INDUCTOR
PP1800_ALW
IT5205, DA7219 (TS3A227E), ANX7625, PP1800_S3
1.8V_PWR
EN_PP1800_S5_L (EC - PA4)
0 ohm
VIN LX
SYSTEM 5V REGULATOR 6A (RT6256C)
EN LDO
INDUCTOR
PP5000_ALW
S3 load switch, VCONN, PP5000_USB_A0_VBUS, AMP_R_POWER, AMP_L_POWER
5V_PWR
Normal Mode : EN = 2.3V ~ 23V
USM Mode : EN = 0.8V ~ 1.7V
H : USM Mode (S5)
L : Normal Mode (G3)
PMIC_FORCE_RESET
3S : 10.8 x R / (1+R) = 1.3V --> (10.8-1.3)R = 1.3 --> 137k ohm
12.9 x R / (1+R) = 1.3V --> (12.9-1.3)R = 1.3 --> 112k ohm
2S : 7.2 X R / (1+R) = 1.3V --> (7.2 - 1.3)R = 1.3 --> 220 k ohm
8.6 x R / (1+R) = 1.3V --> (8.6 - 1.3)R = 1.3 --> 178 k ohm
INDUCTOR
PPVAR_CHG_VIN
FETS
FETS
BUCK-BOOST CHARGER (ISL9238C)
BATFET
VBAT
VBAT_CONN
LI-ION BATTERY PACK (1S)
BUCKBOOST_ASGATE
PFET
USBC-C0
PPVAR_USB_C0_VBUS
VBUS VINT
SINK SWITCH (NX20P5090UK)
EN
EN_USBC_CHARGE_L
PPVAR_CHG_VIN
VOUT VIN
SOURCE SWITCH (FPF2495UCX) (RSVD)
EN
RC DELAY
EN_PP5000_USBC
USBA-A0
PP5000_USB_A0_VBUS
0.5A LOAD SWITCH (RT9742QGJ5)
PP5000_ALW
EN_USBA_5V
PP1800_IT6505_ENABLE
PP1800_ALW
LOAD SWITCH
VSIM2_PMU
TX_OVDD
DPI TO DP (IT6505FN/BX)
PP3300_ALW
USB-C MUX (IT5205FN/AX)
PP5000_PMIC
VSYS_*
PMIC (MT6358, 1/2) (BUCKS)
INDUCTOR
DVDD_PROC_B
DVDD_PROC_L
DVDD_CORE
DVDD_MODEM*
VS1_PMU
VS2_PMU
DVDD_GPU
EMI_VDD2
NOTE: REMOVE INDUCTOR & CONNECT VMODEM_FB TO PP5000_ALW IF DVDD_MODEM IS NOT NEEDED (NO LTE)
VSYS_LDO1
VSYS_LDO2
VSYS_LDO3
LDO GROUP 1
LDO GROUP 2
LDO GROUP 3
VTFE28_PMU
VYX022_PMU
VCN28_PMU
VAUX18_PMU
VAUD28_PMU
VSIM1_PMU
VUSB_PMU
VIBF28_PMU
VLDO28_PMU
VIO28_PMU
VMC_PMU
VMCH_PMU
VSIM2_PMU
VCN33_PMU
VCAMA_PMU
VCAMA2_PMU
PP3000_EMMC
VIBR_PMU
PMIC (MT6358, 2/2) (LDOS)
VS1_PMU
VS1_LDO1
2V INPUT LDOS
VRF18_PMU
VEFUSE_PMU
VCN18_PMU
VCAMIO_PMU
EMI_VDD2
VS2_LDO1
1.125V INPUT LDO
EMI_VDRAM2
EMI_VDDQ
VS2_PMU
VS2_LDO2
VS2_LDO3
VS2_LDO4
1.35V INPUT LDOS
VRF12_PMU
VA12_PMU
DVDD_SRAM_PROC_B
DVDD_SRAM_PROC_L
DVDD_SRAM_CORE
DVDD_VSRAM_GPU
VCAMD_PMU
RTC & DVDD18_DIG
VRTC28
DVDD18_DIG
AU_MICBIAS0
AU_MICBIAS1
VAUD28_PMU
NOTE: NO LTE SUPPORT
CONNECT DVDD_CORE TO DVDD_MODEM PINS
AP (MT8183*)
EMI_VDD2
EMI_VDDQ
PP1800_LPDDR
LPDDR4x (H9HCNNNCPMALHR-NEE)
EMI_VDDQ
EMI_VDD2
PP1800_S3
PP1800_LPDDR
NOTE: POWER ROUTE OPTIONS FROM PP1800_S3 OR VIO18_MT6358
PP1800_S3
AVDD18_SOC
DNS
VIO18_MT6358
PP1800_AP
DNS
PP3000_EMMC
PP1800_AP
PP1800_EMMC
EMMC 32/64GB
VCC
VCCQ
VIO18_MT6358
PP1800_ALW
DUAL-CH LOAD SWITCH
PP3300_ALW
DUAL-CH LOAD SWITCH
PP1800_S3
PP3300_S3
EXT_PMIC_EN2 (PMIC)
PP1800_LPDDR, PP1800_AP, AVDD18_SOC, PP1800_SENSOR
PP1800_WLAN (INA)
PP3300_WLAN (INA)
VIO_1V8
3.3V
BT/WIFI (U69H025_21)
3.3V
ALS (TCS34003FN)
3.3V
USB Hub
PP3300_HUB
3.3V
WF CAMERA CONN.
PP3300_TPAD
3.3V
TRACKPAD CONN.
PP3300_CAM
3.3V
UFC (eDP CONN.)
PP3300_CTP (INA)
3.3V
Touch Panel (eDP CONN.)
H1_AP_FLASH_EN
PP1800_ALW
LOAD SWITCH
PP1800_SPI_FLASH
SPI ROM (W25Q64FWZPIG)
PPVAR_SYS
FUSE
EDP_BL_VOUT
PP3300_ALW
LOAD SWITCH
PP3300_EDP_DX_R
PP3300_EDP_DX
PP3300_S3
AU_MICBIAS0
PP3300_CTP
EDP DISP. CONN.
EN_PP3300_EDP_DX
AU_MICBIAS0
AU_MICBIAS0_R
DMIC CONNECTOR
VIO18_MT6358
PP1800_SENSOR
IMU/GYRO (BMI160)
PP1800_S3
COMPASS (BMM150)
LID ACCEL (SX9321IULTRT)
PP1800_WLAN
PROXIMITY (SX9321IULTRT)
PP5000_ALW
AMP_L_POWER
SPK AMP. (MAX98357A)
AMP_R_POWER
SPK AMP. (MAX98357A)
PP3300_ALW
TS3A227E_POWER
HP JACK DET. (TS3A227EYFFR)
PP1800_ALW
PP3300_ALW
HP AMP* (DA7219)
NOTE: EXTERNAL HP AMP IS RECOMMENDED
Quanta Computer Inc.
PROJECT : ZDS
04_Power Tree



Schematic design notice of "BB_POWER_PDN" page.

Note 10-1: Differential pair of DVDD_GPU remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

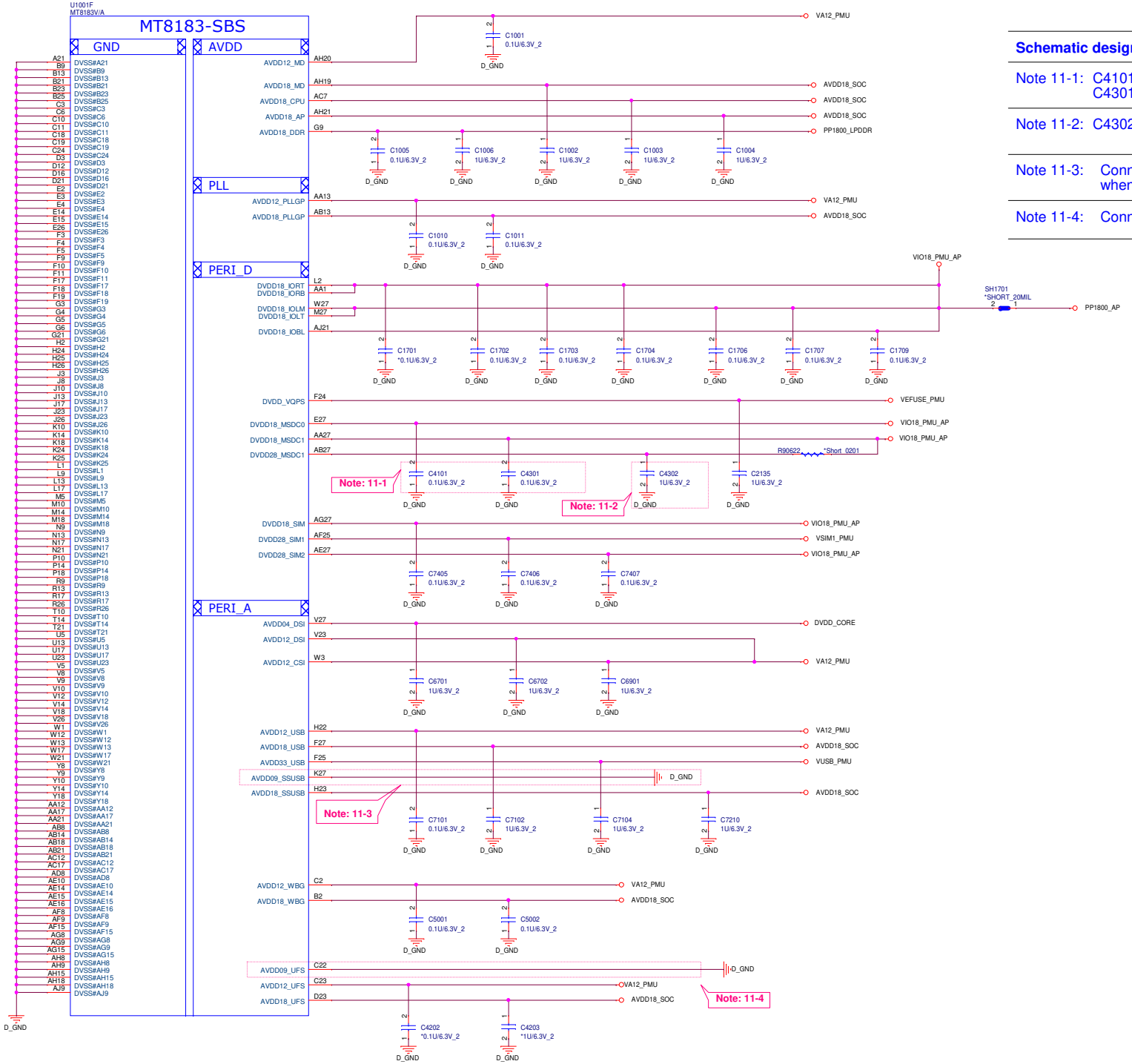
Note 10-2: Differential pair of DVDD_PROC remote sense must be close to BB's ball
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-3: Differential pair of DVDD_MODEM remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Note 10-4: Differential pair of DVDD_CORE remote sense must be close to BB's ball.
Remote sense trace with GND shielding to PMIC (Differential)

Quanta Computer Inc.
PROJECT : ZDE

Size	Document Number	Rev
	05_BB_ POWER_PDN	1A
Date: Wednesday, May 06, 2020	Sheet 5 of 39	



Schematic design notice of "BB_POWER_IO" page.

Note 11-1: C4101 closed DVDD18_MSDC0 150mil
C4301 closed DVDD18_MSDC1 150mil

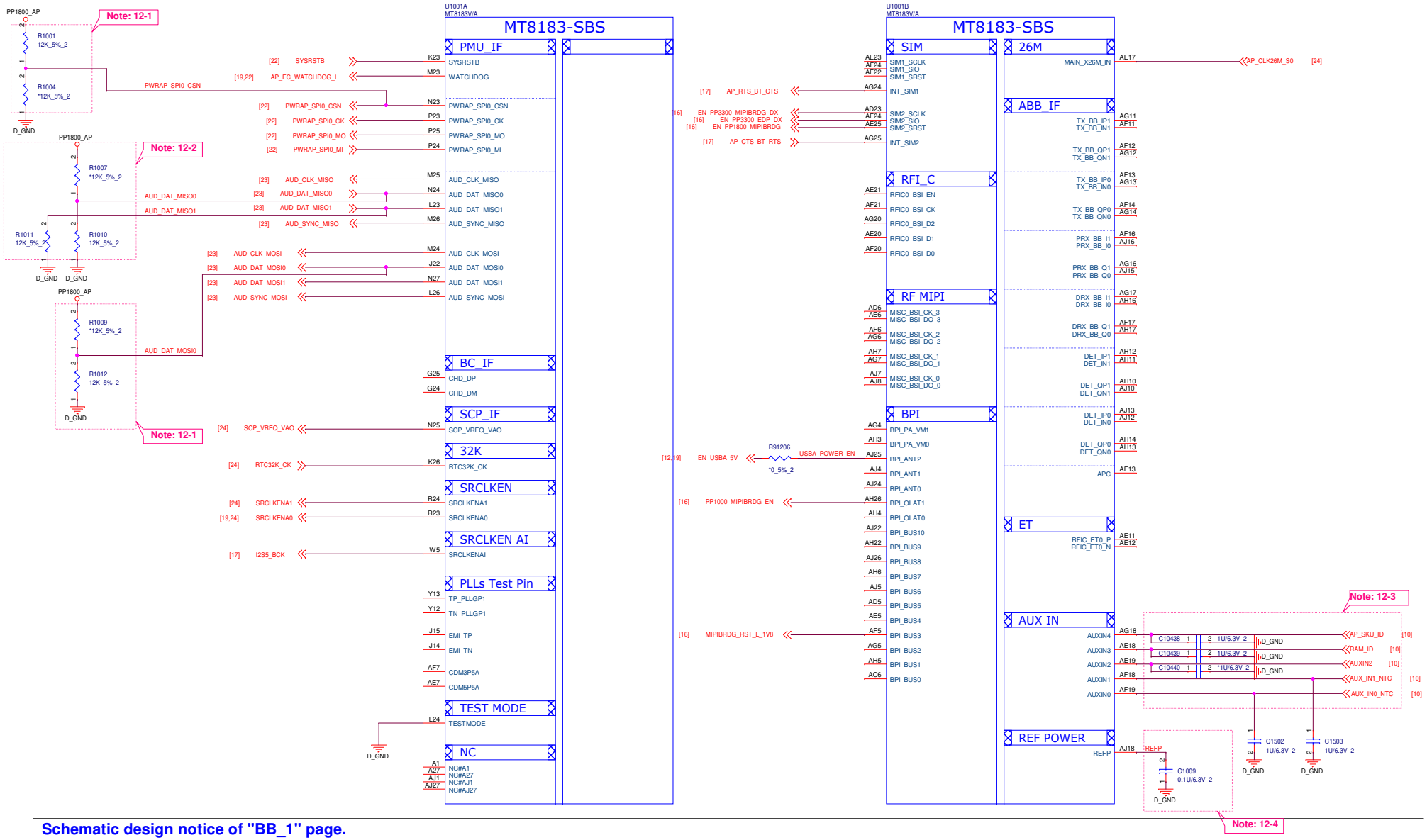
Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: Connects "AVDD09_SSUSB" to GND when USB3.0 is not used.

Note 11-4: Connects "AVDD09_UFS" to GND when UFS is not used.

Quanta Computer Inc.
PROJECT : ZDE

Size	Document Number	Rev
	06_BB_ POWER_PDN	1A
Date: Wednesday, May 06, 2020	Sheet 6 of 39	



Schematic design notice of "BB_1" page.

Note 12-1: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	N/A
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC/DPI_DE/ DPI_CK/DPI_D8/DPI_D9
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

AUD_DAT_MISO1	Booting device
LO	eMMC
HI	UFS

Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

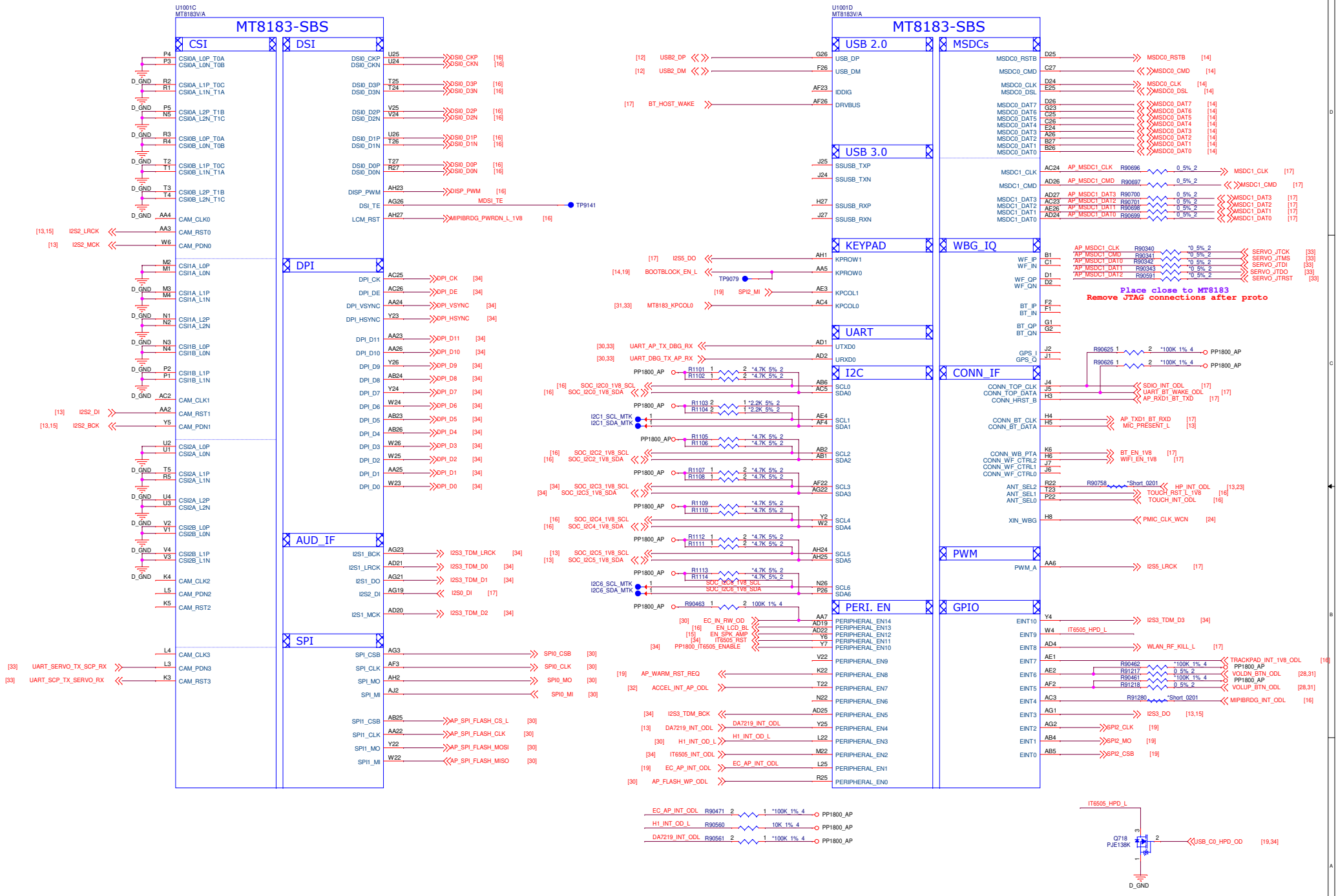
Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

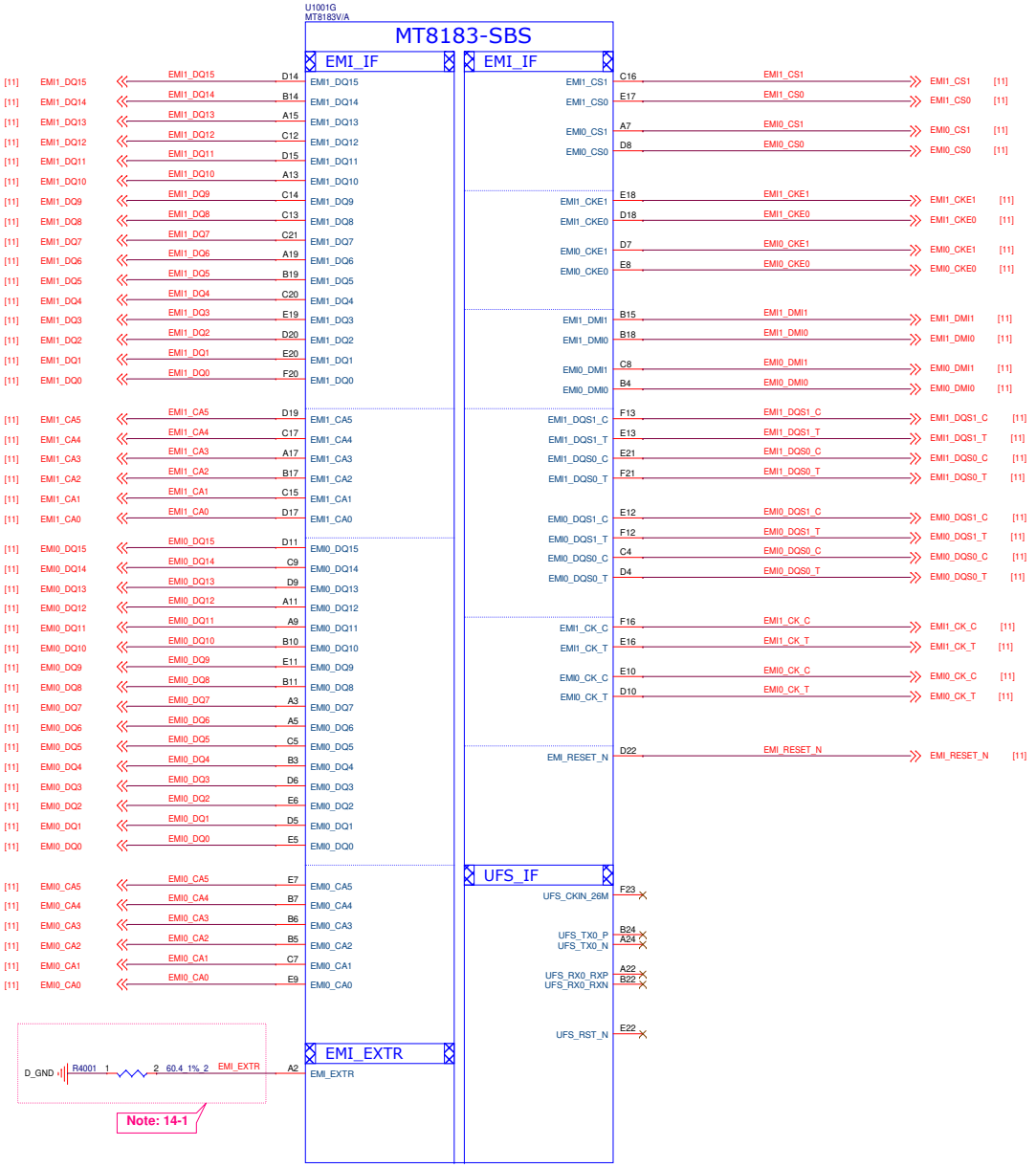
Note 12-5: AUD_SYNC_MISO and AUD_CLK_MISO are DDR type feature in bootstrap

AUD_SYNC_MISO	AUD_CLK_MISO	DDR
LO	LO	LPDDR4X
LO	HI	LPDDR4X(Ext x 2 EN)
HI	LO	LPDDR3
HI	HI	LPDDR4X(Ext x 1 EN)

Quanta Computer Inc.
PROJECT : ZDE

Size	Document Number	Rev
	07_BB_1	1A
Date: Wednesday, May 06, 2020	Sheet 7 of 39	

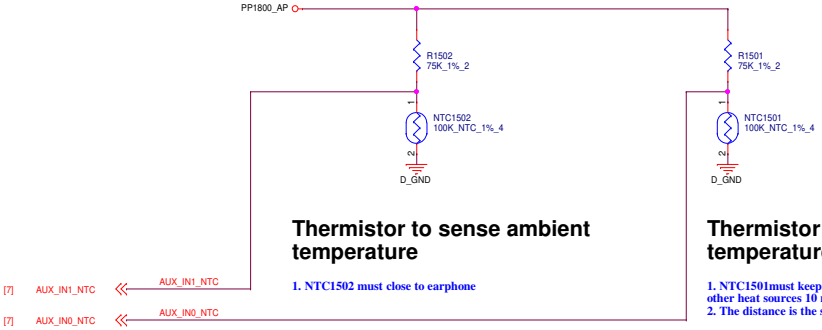

U1001C
MT8183V/A
MT8183-SBS
CSI
DSI
DPI
AUD_IF
SPI
U1001D
MT8183V/A
MT8183-SBS
USB 2.0
USB 3.0
KEYPAD
UART
I2C
PERI. EN
MSDCs
WBG_IQ
CONN_IF
PWM
GPIO
Place close to MT8183
Remove JTAG connections after proto
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
08_BB_2
Rev
1A
Date: Friday, May 08, 2020
Sheet 8 of 39



Schematic design notice of "BB_3" page.

Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R4001, please select 60.4 ohm 1% resistor

Quanta Computer Inc.		
PROJECT : ZDE		
Size	Document Number: 09_BB_3	Rev: 1A
Date: Wednesday, May 06, 2020	Sheet 9 of 39	



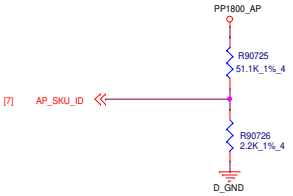
Thermistor to sense ambient temperature

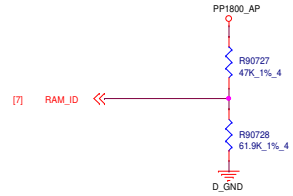
1. NTC1502 must close to earphone

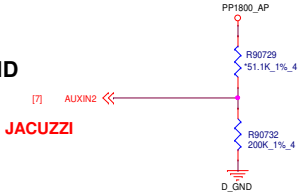
Thermistor to sense AP temperature

1. NTC1501must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

SKU ID (AP AUXIN4)					
NUMERIC ID	RP (KOHM)	RD (KOHM)	VOLTAGE (V)	SKU	VIO (V)
0	51.1	2.2	0.074	0	1.8
1	51.1	6.81	0.212		
2	51.1	11	0.319		
3	57.6	18	0.429		
4	51.1	22	0.542		
5	51.1	30	0.666		
6	51.1	39.2	0.781		
7	56	56	0.900		
8	47	61.9	1.023		
9	47	80.6	1.137		
10	56	124	1.240		
11	51.1	150	1.343		







LCM_ID

NOT USED IN JACUZZI

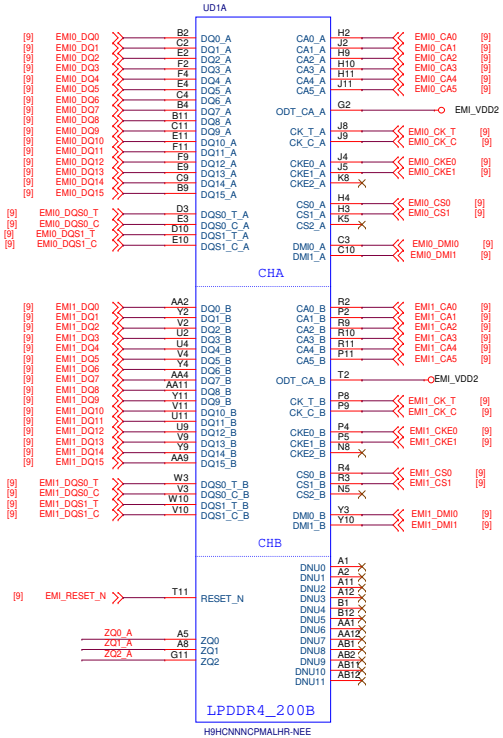
RAM ID (AP AUXIN3)						
NUMERIC ID	RP (KOHM)	RD (KOHM)	VOLTAGE (V)	VIO (V)	VENDOR	MPN
0	51.1	2.2	0.074	1.8	SAMSUNG 4GB LP4X	K4UBE3D4AM-MGCJ
1	51.1	6.81	0.212		HYNIX 4GB QDP LP4X	H9HCNNNCPMALHR-NEE
2	51.1	11	0.319		MICRON 4GB LP4X	MT53E1G32D4NQ-053 WT:E MT53E1G32D4NQ-046 WT:E
3	57.6	18	0.429		SAMSUNG eMCP: 4GB LP4x + 64GB eMMC v5.1 (MLC)	KMDH6001DA-B422
4	51.1	22	0.542		SAMSUNG eMCP: 4GB LP4x + 64GB eMMC v5.1 (TLC)	KMDP6001DA-B425
5	51.1	30	0.666		MICRON eMCP: 4GB LP4x + 64GB eMMC v5.1	MT29VZZZAD8DQKSL-046 W.9K8
6	51.1	39.2	0.781		SAMSUNG eMCP: 4GB LP4x + 128GB eMMC v5.1 (TLC)	KMDV6001DA-B620
7	56	56	0.900		Sandisk eMCP: 4GB LP4x + 128GB eMMC v5.1	SDADA4CR-128G
8	47	61.9	1.023		SAMSUNG 4GB LP4X	K4UBE3D4AA-MGCL
9	47	80.6	1.137		MICRON 8GB LP4X	MT53E2G32D4NQ-046 WT:A
10	56	124	1.240			
11	51.1	150	1.343			

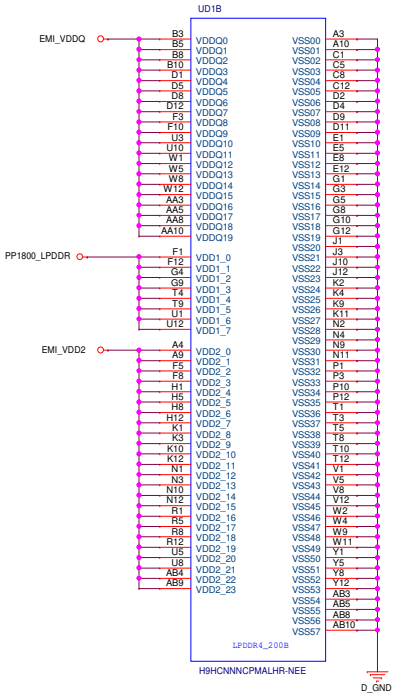
Quanta Computer Inc.
PROJECT : ZDE

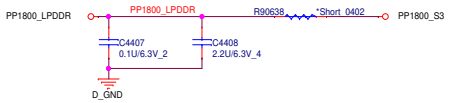
Size	Document Number	Rev
	10_AUXADC_Thermal_RAM/Board_ID	1A

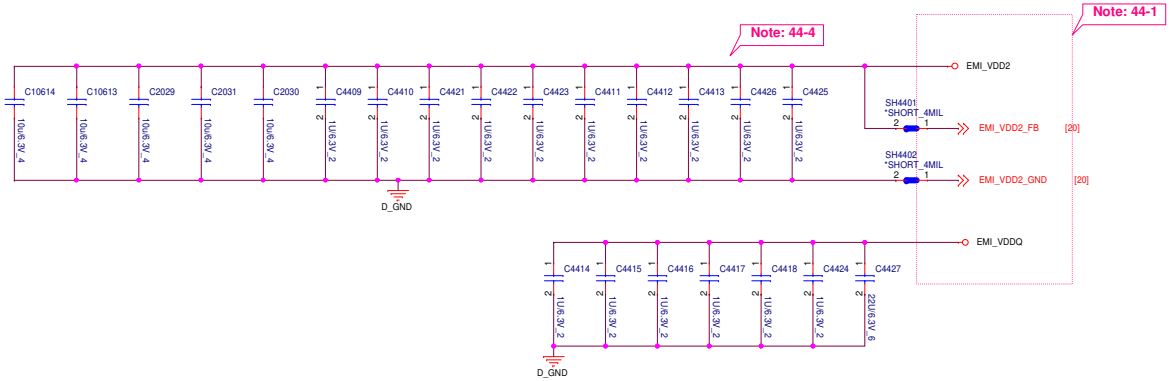
Date: Wednesday, May 06, 2020 Sheet 10 of 39

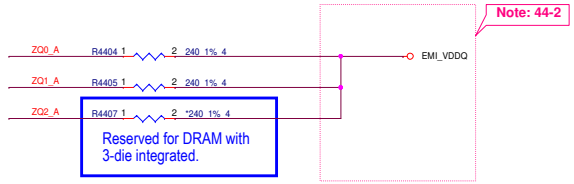
Ext. EMI_VDD1 for LPDDR4x VDD1











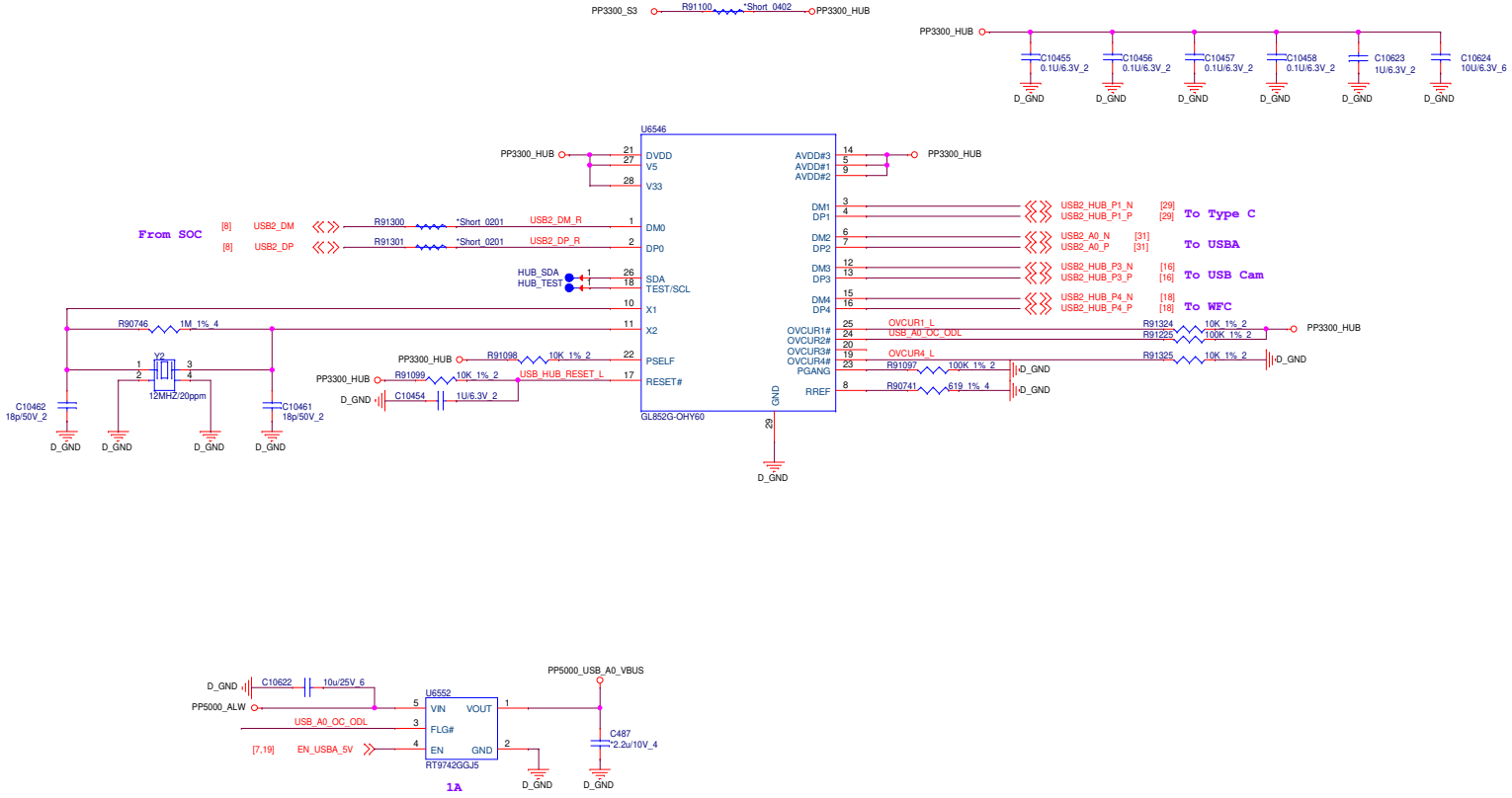
Schematic design notice of "Memory_LPDDR4"

Note 44-1: Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

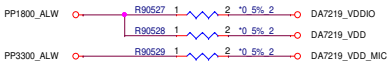
Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

Quanta Computer Inc.		
PROJECT : ZDE		
Size	Document Number: 11_Memory_LPDDR4x	Rev: 1A
Date: Wednesday, May 06, 2020	Sheet 11 of 39	

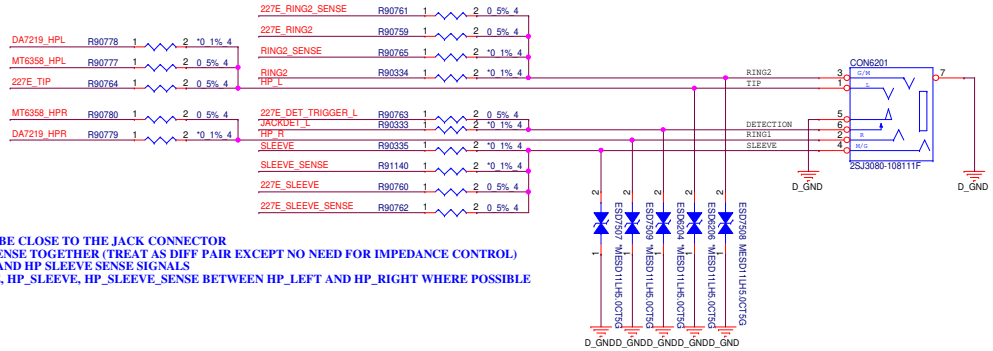


Quanta Computer Inc.		
PROJECT : ZDE		
Size	Document Number: 12_HUB/USBA	Rev: 1A
Date: Wednesday, May 06, 2020	Sheet 12 of 39	

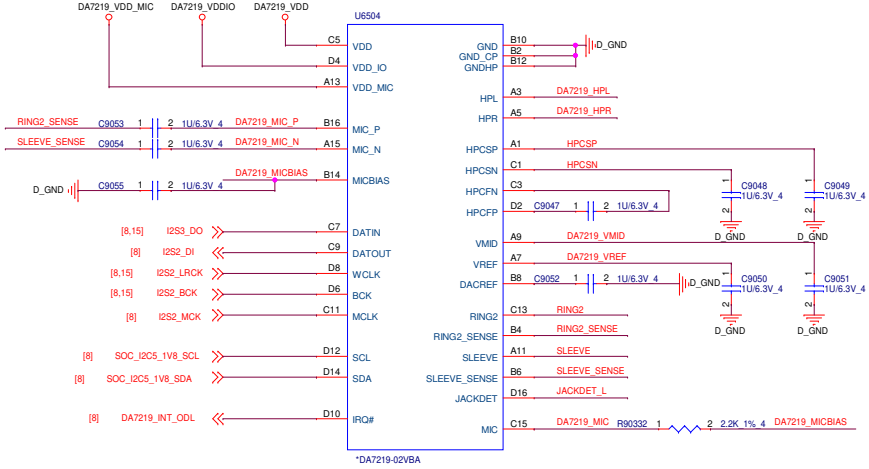
Earphone Audio

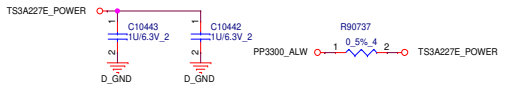


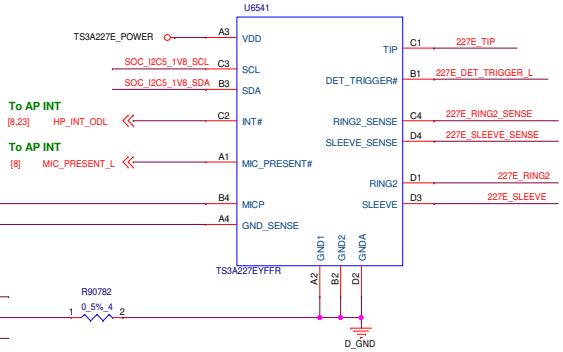
VDD 1.7V~2.5V
VDD_IO 1.5V~3.6V
VDD_MIC 1.8V~3.6V

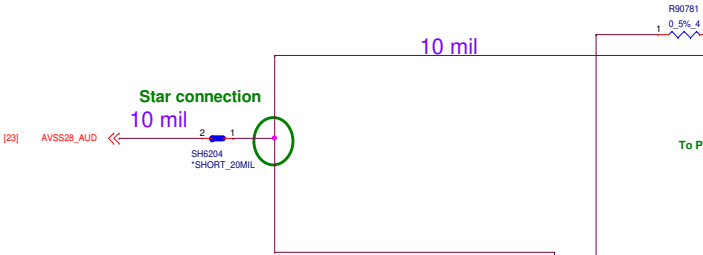


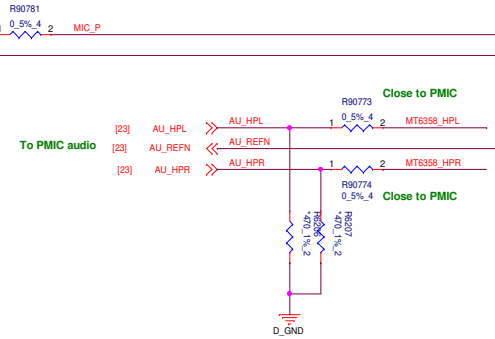
THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR
ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL)
THE SAME APPLIES TO HP SLEEVE AND HP SLEEVE SENSE SIGNALS
ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE



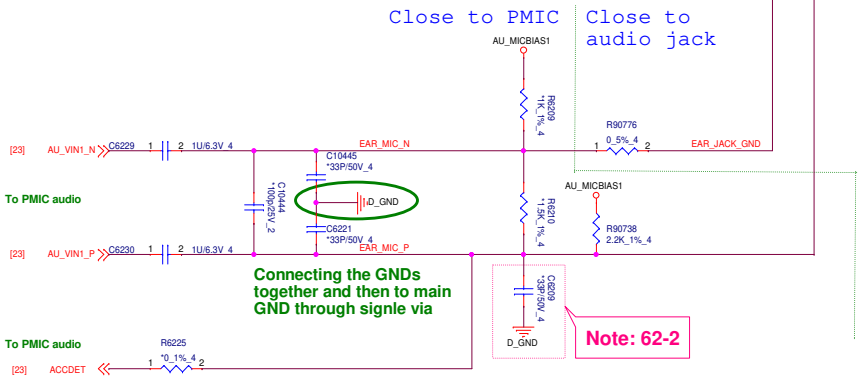








Earphone Microphone

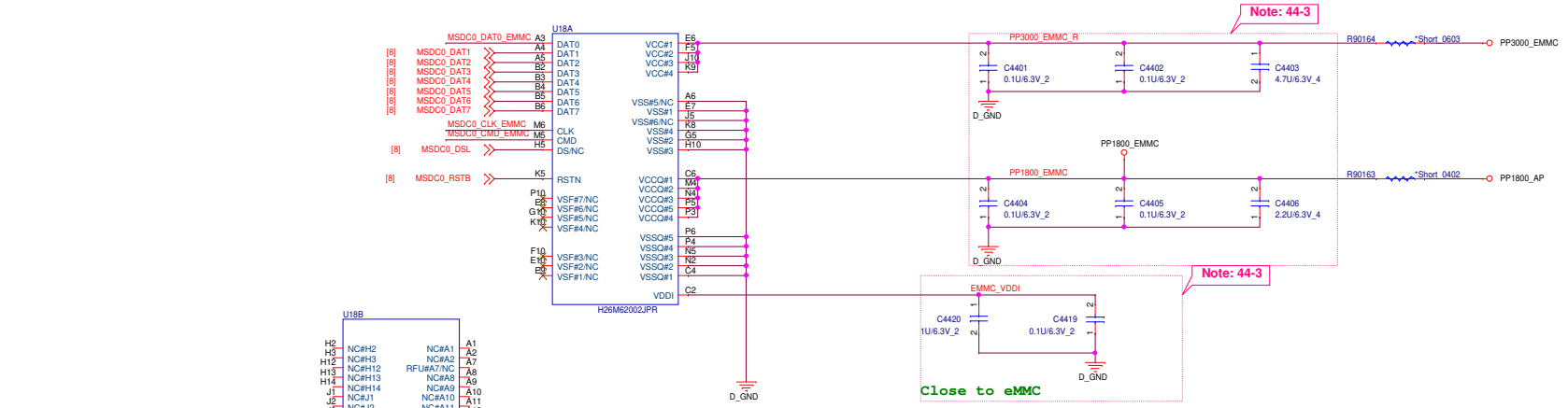


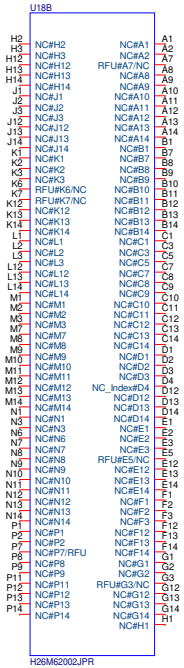
Schematic design notice of "62_PERI_AUDIO_IO" page.

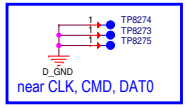
Note 62-2: Reserved Cap for CS/RS test, please double check multi-key function when used

Quanta Computer Inc.
PROJECT : ZDE

Size	Document Number	Rev
	13_PERI_AUDIO_DA7219	1A
Date: Wednesday, May 06, 2020	Sheet 13 of 39	







Layout: trace extension to compensate mux propagation delay ~68ps for DAT1-7 and DS

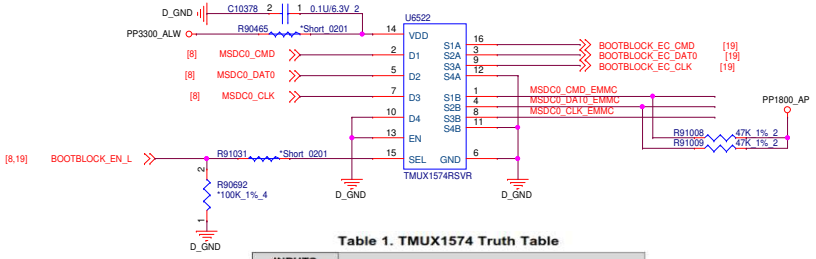


Table 1. TMUX1574 Truth Table

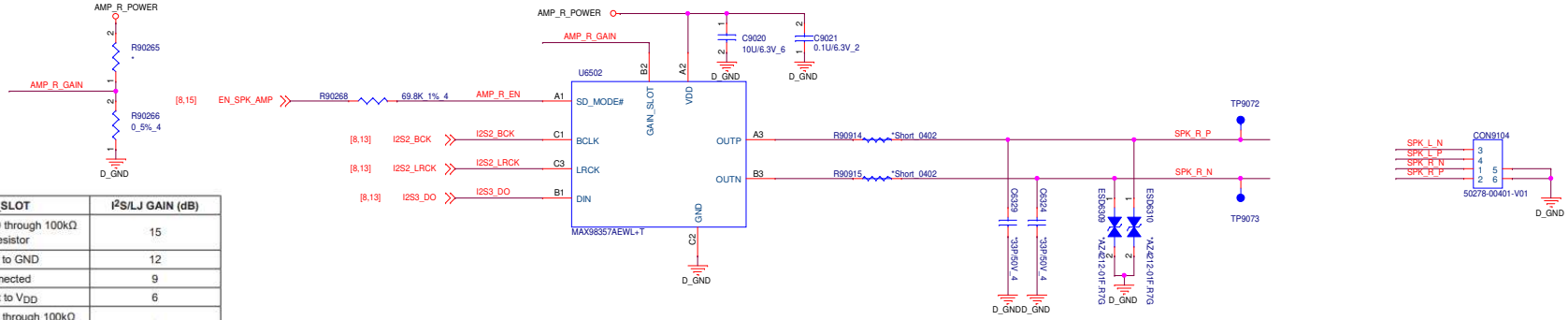
INPUTS		Selected Source Pins Connected To Drain Pins (Dx)
EN	SEL	
0	0	SxA connected to Dx
0	1	SxB connected to Dx
1	X	Hi-Z (OFF)

Schematic design notice of "Memory_eMMC"

Note 44-3: Please refer to vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Speaker Amplifier

5/22 maybe 100K or 0 ohm, depned on gain(DB) now just set to NC



GAIN_SLOT	I²S/LJ GAIN (dB)
Connect to GND through 100kΩ ±5% resistor	15
Connect to GND	12
Unconnected	9
Connect to V_{DD}	6
Connect to V_{DD} through 100kΩ ±5% resistor	3

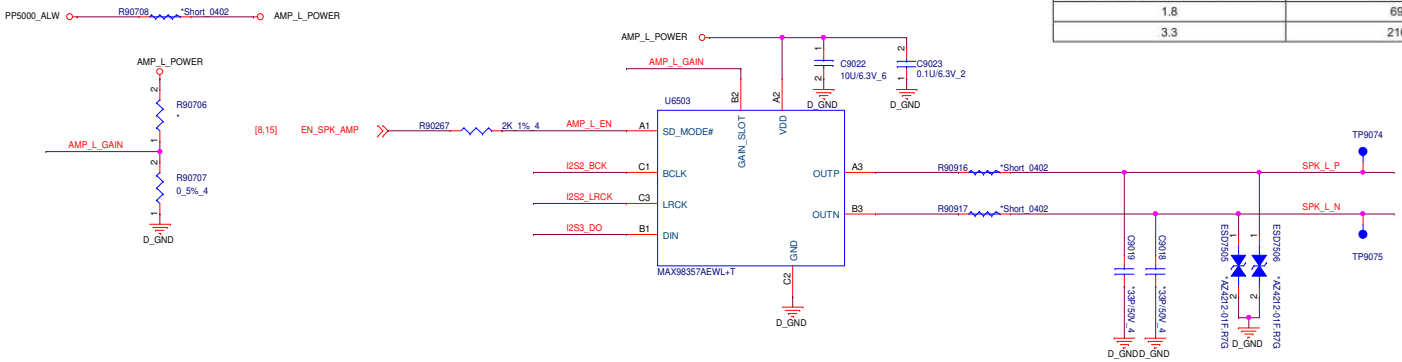
SD_MODE COMPARATOR TRIP POINTS						
B0		See SD_MODE and shutdown operation for details	0.08	0.16	0.355	V
B1			0.65	0.77	0.825	
B2			1.245	1.4	1.5	
SD_MODE Pulldown Resistor	R_{PD}		92	100	108	kΩ

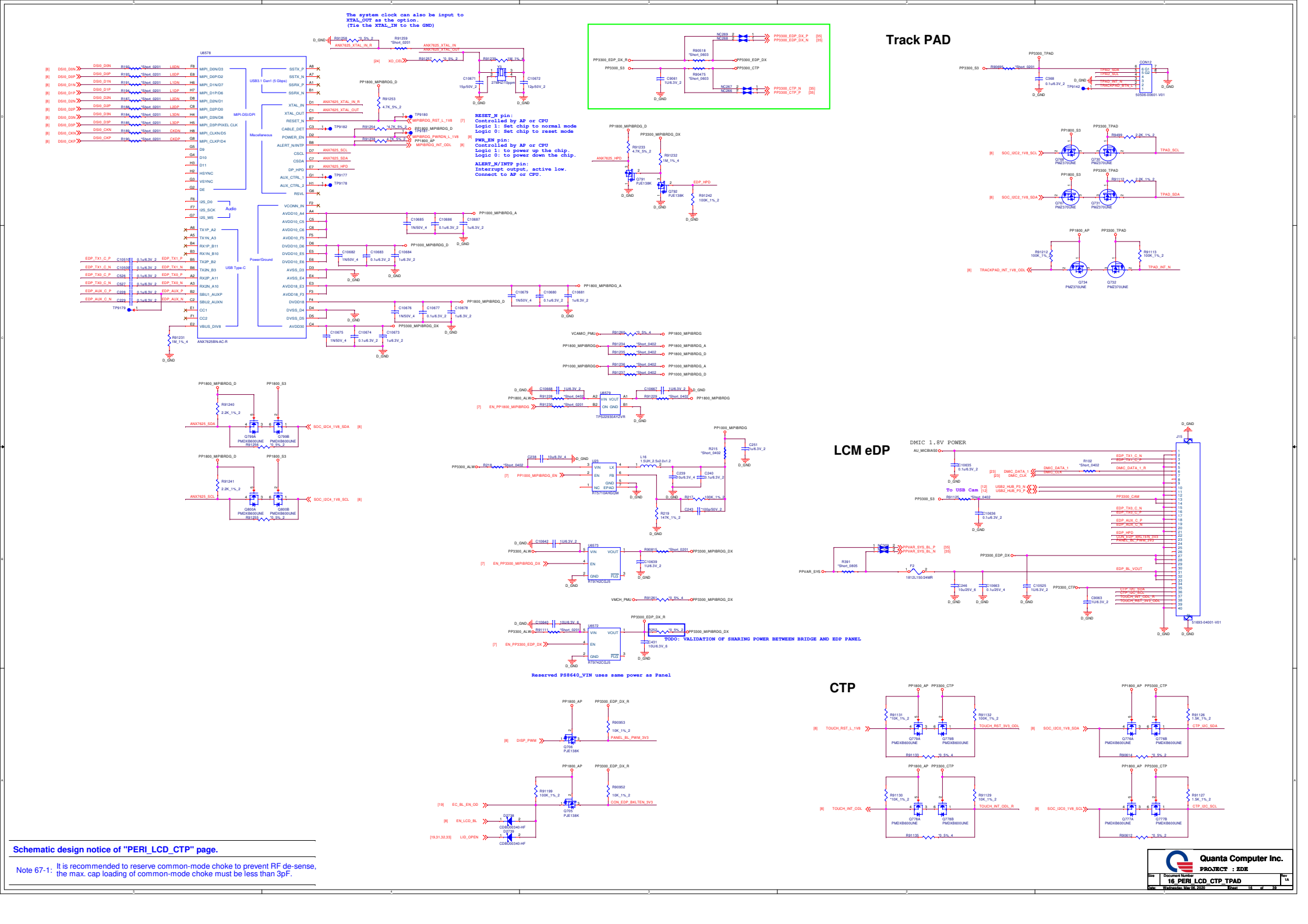
Table 5. SD_MODE Control

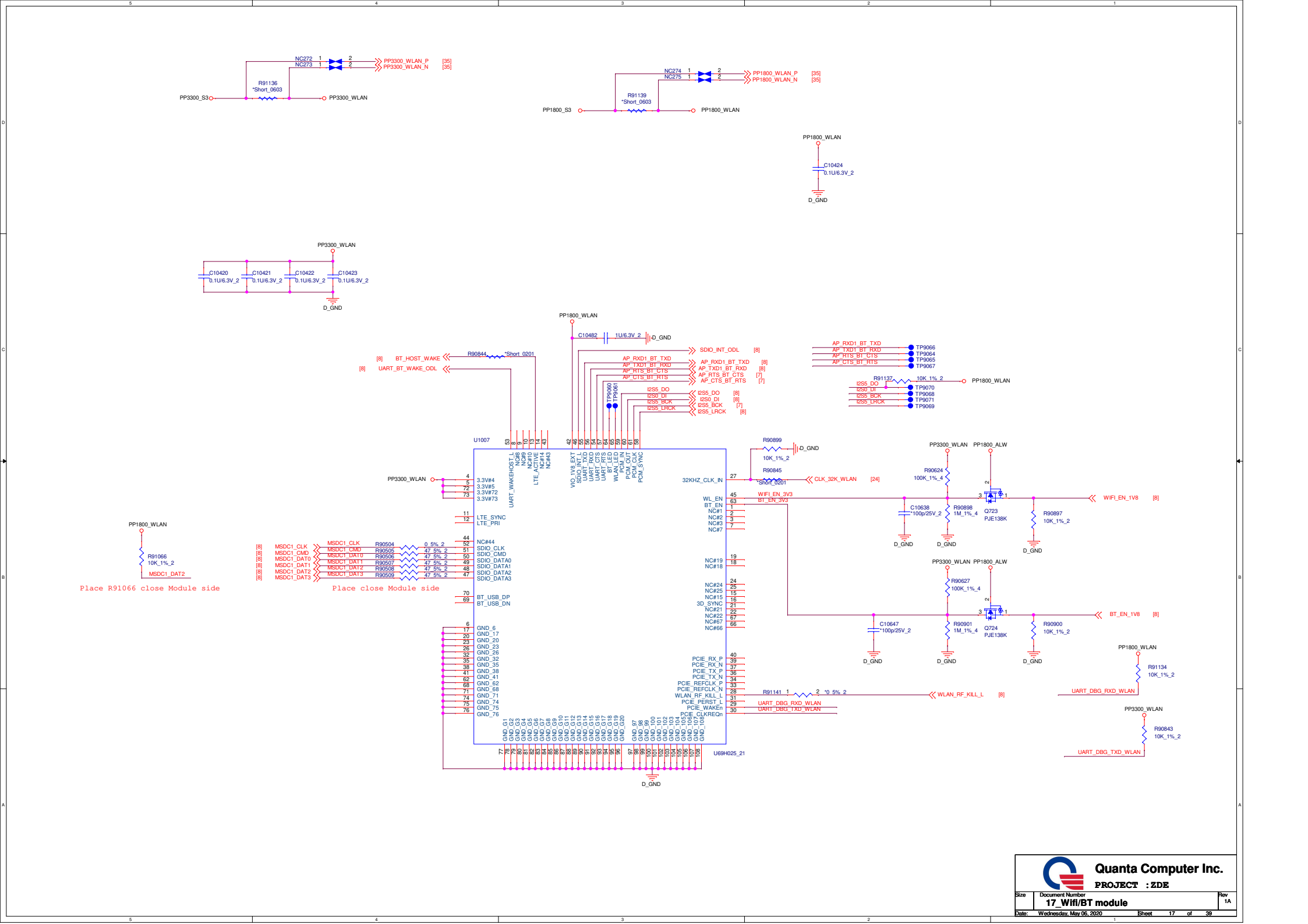
SD_MODE STATUS		SELECTED CHANNEL
High	V_{SD_MODE} > B2 trip point	Left
Pullup through R_{SMALL}	B2 trip point > V_{SD_MODE} > B1 trip point	Right
Pullup through R_{LARGE}	B1 trip point > V_{SD_MODE} > B0 trip point	(Left/2 + right/2)
Low	B0 trip point > V_{SD_MODE}	Shutdown

Table 6. Examples of SD_MODE Pullup Resistor Values

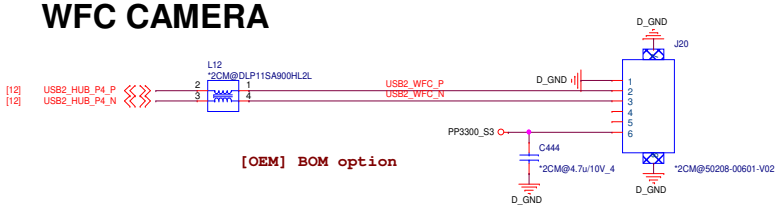
LOGIC VOLTAGE LEVEL (V_{DDIO}) (V)	R_{SMALL} (kΩ)	R_{LARGE} (kΩ)
1.8	69.8	300
3.3	210.2	634




The system clock can also be input to XTAL_OUT as the option. (Tie the XTAL_IN to the GND)
RESET_N pin: Controlled by AP or CPU Logic 1: Set chip to normal mode Logic 0: Set chip to reset mode
PWR_EN pin: Controlled by AP or CPU Logic 1: to power up the chip. Logic 0: to power down the chip.
ALERT_N/INTP pin: Interrupt output, active low. Connect to AP or CPU.
Track PAD
LCM eDP
DMIC 1.8V POWER
To USB Cam
CTP
TODO: VALIDATION OF SHARING POWER BETWEEN BRIDGE AND EDP PANEL
Reserved PS8640_VIN uses same power as Panel
Schematic design notice of "PERI_LCD_CTP" page.
Note 67-1: It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.
Quanta Computer Inc.
PROJECT : ZDE
Document Number 16_PERI_LCD_CTP_TPAD
Rev 1A
Date: Wednesday, May 06, 2020
Sheet 16 of 39


NC272 1 2 PP3300_WLAN_P [35]
NC273 1 2 PP3300_WLAN_N [35]
R91136 *Short_0603
PP3300_S3
PP3300_WLAN
NC274 1 2 PP1800_WLAN_P [35]
NC275 1 2 PP1800_WLAN_N [35]
R91139 *Short_0603
PP1800_S3
PP1800_WLAN
PP1800_WLAN
C10424 0.1U/6.3V_2
D_GND
PP3300_WLAN
C10420 0.1U/6.3V_2
C10421 0.1U/6.3V_2
C10422 0.1U/6.3V_2
C10423 0.1U/6.3V_2
D_GND
PP1800_WLAN
C10482 1U/6.3V_2
D_GND
[8] BT_HOST_WAKE
[8] UART_BT_WAKE_ODL
R90844 *Short_0201
SDIO_INT_ODL [8]
AP_RXD1_BT_TXD
AP_TXD1_BT_RXD
AP_RTS_BT_CTS
AP_CTS_BT_RTS
I2S5_DO
I2S0_DI
I2S5_BCK
I2S5_LRCK
TP9060
TP9061
AP_RXD1_BT_TXD
AP_TXD1_BT_RXD
AP_RTS_BT_CTS
AP_CTS_BT_RTS
TP9066
TP9064
TP9065
TP9067
R91137 10K_1%_2
PP1800_WLAN
I2S5_DO
I2S0_DI
I2S5_BCK
I2S5_LRCK
TP9070
TP9068
TP9071
TP9069
U1007
UART_WAKEHOST_L
NC#8
NC#9
NC#10
NC#13
LTE_ACTIVE
NC#14
NC#43
VIO_1V8_EXT
SDIO_INT_L
UART_TXD
UART_RXD
UART_CTS
UART_RTS
BT_LED
WLAN_LED
PCM_IN
PCM_OUT
PCM_CLK
PCM_SYNC
R90899 10K_1%_2
D_GND
R90845 *Short_0201
CLK_32K_WLAN [24]
32KHZ_CLK_IN
PP3300_WLAN
3.3V#4
3.3V#5
3.3V#72
3.3V#73
LTE_SYNC
LTE_PRI
NC#44
SDIO_CLK
SDIO_CMD
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
BT_USB_DP
BT_USB_DN
GND_6
GND_17
GND_20
GND_23
GND_26
GND_32
GND_35
GND_38
GND_41
GND_62
GND_68
GND_71
GND_74
GND_75
GND_76
GND_G1
GND_G2
GND_G3
GND_G4
GND_G5
GND_G6
GND_G7
GND_G8
GND_G9
GND_G10
GND_G11
GND_G12
GND_G13
GND_G14
GND_G15
GND_G16
GND_G17
GND_G18
GND_G19
GND_G20
GND_97
GND_98
GND_99
GND_100
GND_101
GND_102
GND_103
GND_104
GND_105
GND_106
GND_107
GND_108
U69H025_21
WL_EN
BT_EN
NC#1
NC#2
NC#3
NC#7
NC#19
NC#18
NC#24
NC#25
NC#15
3D_SYNC
NC#21
NC#22
NC#67
NC#66
PCIE_RX_P
PCIE_RX_N
PCIE_TX_P
PCIE_TX_N
PCIE_REFCLK_P
PCIE_REFCLK_N
WLAN_RF_KILL_L
PCIE_PERST_L
PCIE_WAKEn
PCIE_CLKREQn
WIFI_EN_3V3
BT_EN_3V3
PP3300_WLAN
PP1800_ALW
R90624 100K_1%_4
R90898 1M_1%_4
Q723 PJE138K
C10638 *100p/25V_2
R90897 10K_1%_2
WIFI_EN_1V8 [8]
D_GND
PP3300_WLAN
PP1800_ALW
R90627 100K_1%_4
R90901 1M_1%_4
Q724 PJE138K
C10647 *100p/25V_2
R90900 10K_1%_2
BT_EN_1V8 [8]
D_GND
PP1800_WLAN
R91066 10K_1%_2
MSDC1_DAT2
Place R91066 close Module side
[8] MSDC1_CLK
[8] MSDC1_CMD
[8] MSDC1_DAT0
[8] MSDC1_DAT1
[8] MSDC1_DAT2
[8] MSDC1_DAT3
R90504 0_5%_2
R90505 47_5%_2
R90506 47_5%_2
R90507 47_5%_2
R90508 47_5%_2
R90509 47_5%_2
Place close Module side
R91141 1 2 *0_5%_2
WLAN_RF_KILL_L [8]
UART_DBG_RXD_WLAN
UART_DBG_TXD_WLAN
PP1800_WLAN
R91134 10K_1%_2
UART_DBG_RXD_WLAN
PP3300_WLAN
R90843 10K_1%_2
UART_DBG_TXD_WLAN
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
17_Wifi/BT module
Rev 1A
Date: Wednesday, May 06, 2020
Sheet 17 of 39

WFC CAMERA

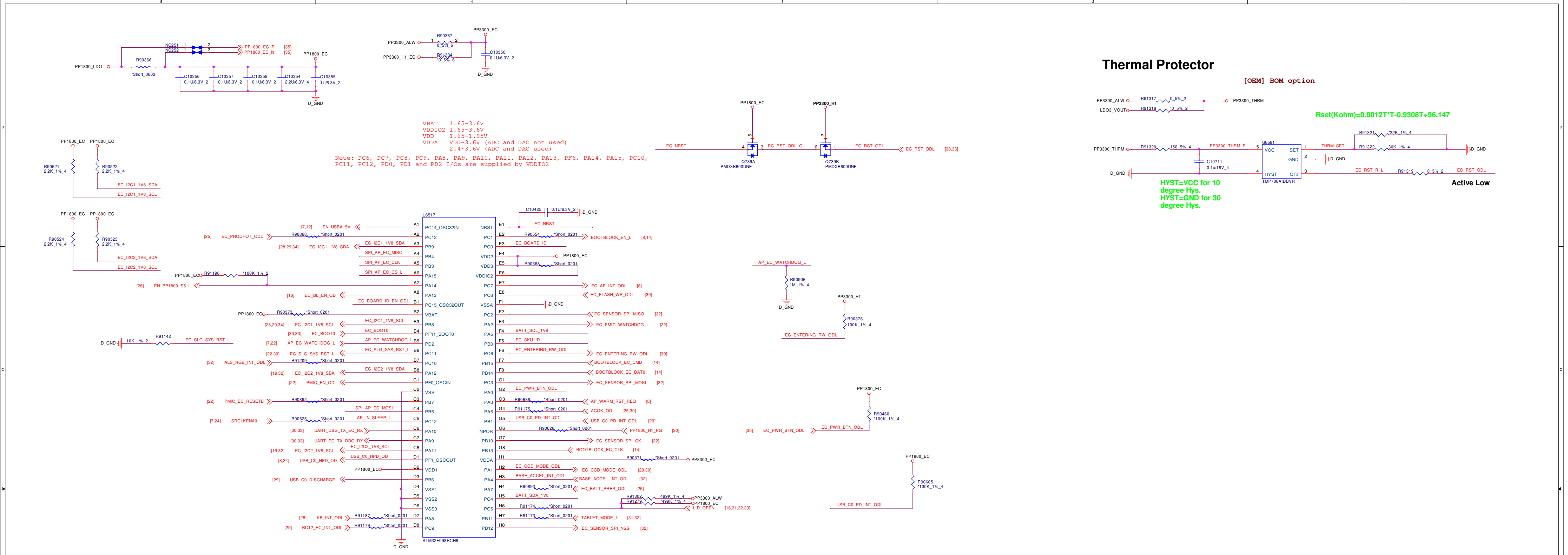


[OEM] BOM option

Quanta Computer Inc.

PROJECT : ZDE

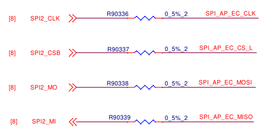
Size	Document Number	Rev
	18_PERI_CAMERA	1A
Date: Wednesday, May 06, 2020	Sheet 18 of 39	

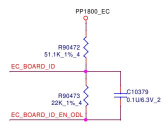


VBAT 1.65~3.6V
VDDIO2 1.65~3.6V
VDD 1.65~1.95V
VDDA VDD~3.6V (ADC and DAC not used)
2.4~3.6V (ADC and DAC used)

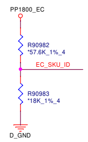
Note: PC6, PC7, PC8, PC9, PA8, PA9, PA10, PA11, PA12, PA13, PF6, PA14, PA15, PC10, PC11, PC12, PD0, PD1 and PD2 I/Os are supplied by VDDIO2

R90336, R90337, R90338 place close to AP, R90339 place close to EC



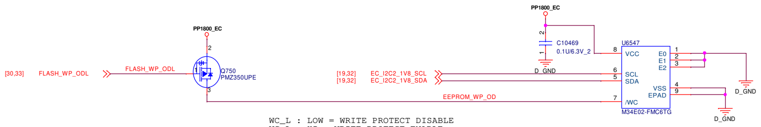


BOARD REV ID (EC ADC_IN10)					
NUMERIC ID	RP (KOHM)	RD (KOHM)	VOLTAGE (V)	BUILD	VIO (V)
0	51.1	2.2	0.074	Jacuzzi Proto	1.8
1	51.1	6.81	0.212	Juniper Proto	
2	51.1	11	0.319	Juniper EVT	
3	57.6	18	0.429	Juniper DVT	
4	51.1	22	0.542	Juniper PVT	
5	51.1	30	0.666		
6	51.1	39.2	0.781		
7	56	56	0.900		
8	47	61.9	1.023		
9	47	80.6	1.137		
10	56	124	1.240		
11	51.1	150	1.343		
12	47	200	1.457		
13	47	330	1.576		
14	47	680	1.684		
15	56	DNS/NC	1.800		

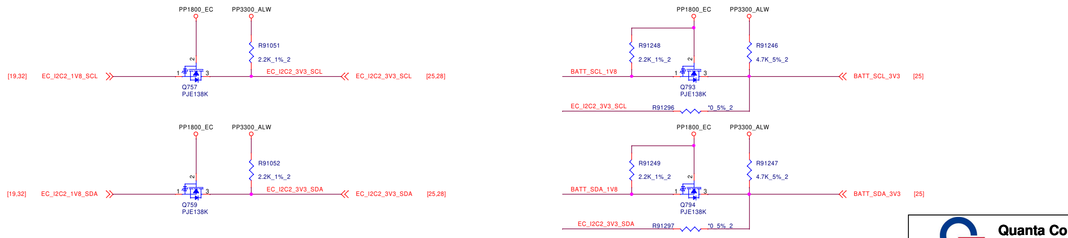


SKU ID (EC ADC_IN8, RSVD ONLY)					
NUMERIC ID	RP (KOHM)	RD (KOHM)	VOLTAGE (V)	SKU	VIO (V)
0	51.1	2.2	0.074		1.8
1	51.1	6.81	0.212		
2	51.1	11	0.319		
3	57.6	18	0.429		
4	51.1	22	0.542		
5	51.1	30	0.666		
6	51.1	39.2	0.781		
7	56	56	0.900		
8	47	61.9	1.023		
9	47	80.6	1.137		
10	56	124	1.240		
11	51.1	150	1.343		
12	47	200	1.457		
13	47	330	1.576		
14	47	680	1.684		
15	56	DNS/NC	1.800		

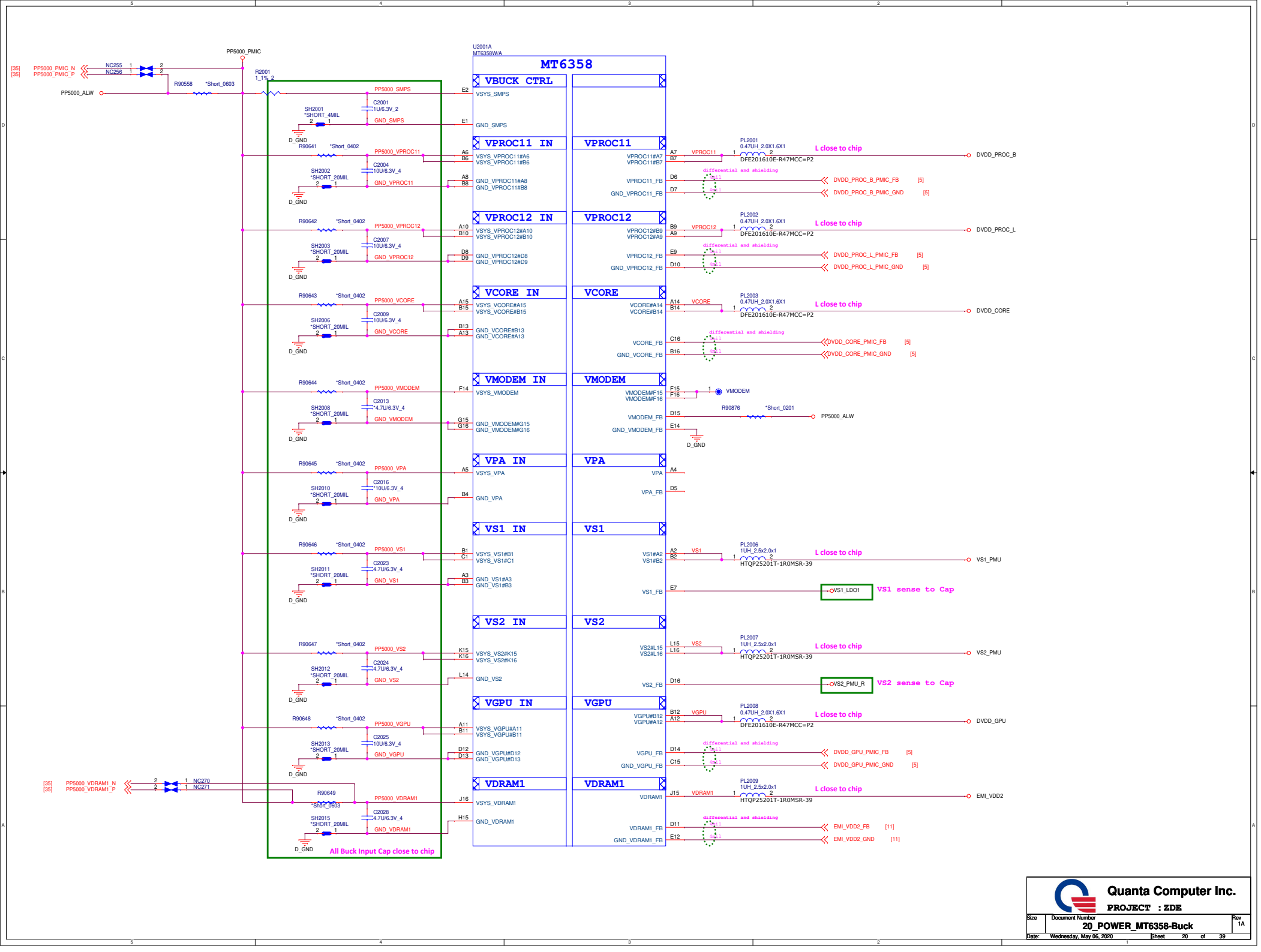
EEPROM

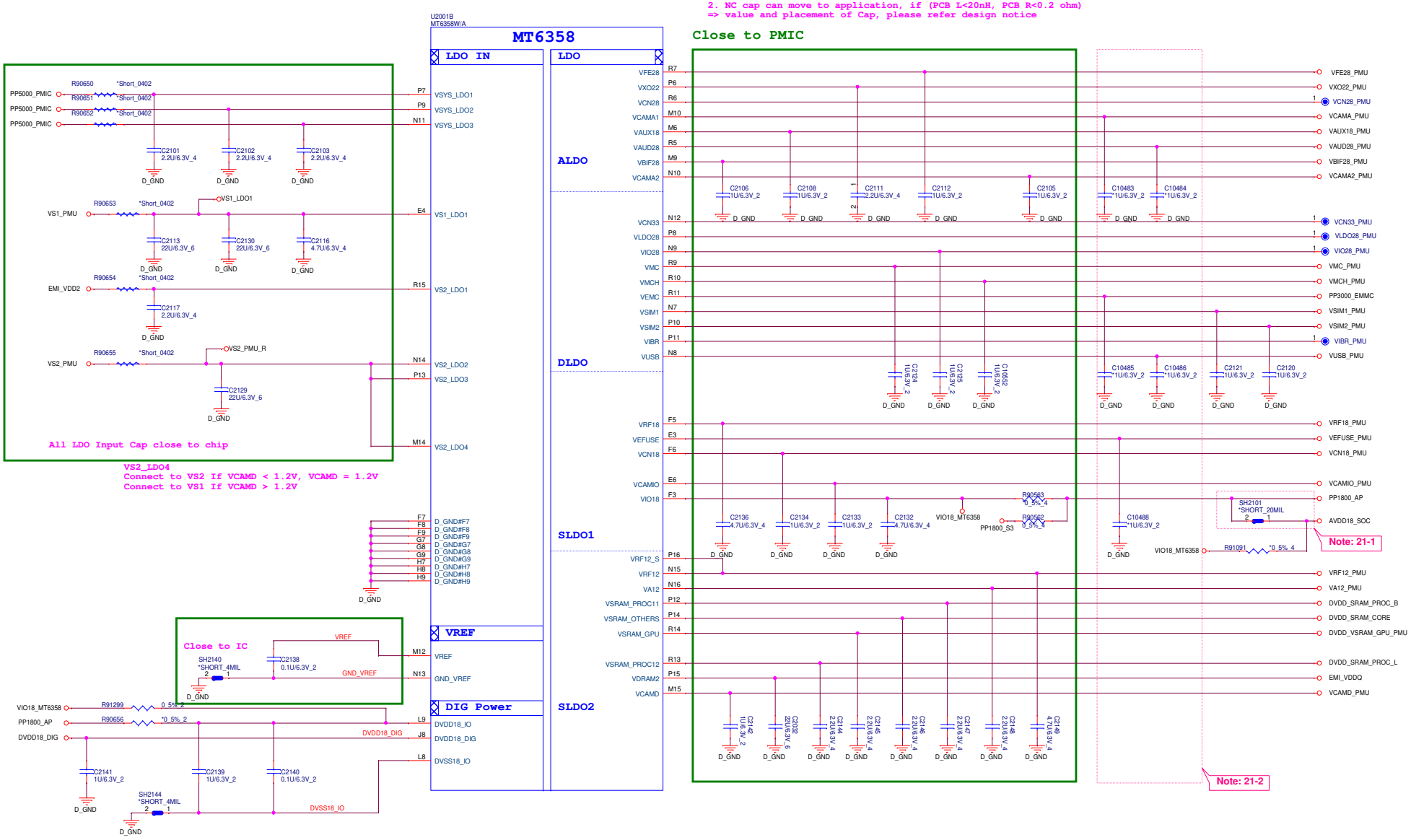


WC_L : LOW = WRITE PROTECT DISABLE
WC_L : HI = WRITE PROTECT ENABLE



Quanta Computer Inc.
PROJECT : ZDE
Document Number: 19_EC_STM32F098RCH6
Rev 1A
Date: Wednesday, May 06, 2020 Sheet 19 of 39


PP5000_PMIC
U2001A
MT6358W/A
MT6358
VBUCK CTRL
VPROC11 IN
VPROC12 IN
VCORE IN
VMODEM IN
VPA IN
VS1 IN
VS2 IN
VGPU IN
VDRAM1
VPROC11
VPROC12
VCORE
VMODEM
VPA
VS1
VS2
VGPU
VDRAM1
PP5000_PMIC_N
PP5000_PMIC_P
PP5000_ALW
NC255
NC256
R90558 *Short_0603
R2001 1_1%_2
PP5000_SMPS
C2001 1U/6.3V_2
SH2001 *SHORT_4MIL
GND_SMPS
D_GND
R90641 *Short_0402
PP5000_VPROC11
C2004 10U/6.3V_4
SH2002 *SHORT_20MIL
GND_VPROC11
R90642 *Short_0402
PP5000_VPROC12
C2007 10U/6.3V_4
SH2003 *SHORT_20MIL
GND_VPROC12
R90643 *Short_0402
PP5000_VCORE
C2009 10U/6.3V_4
SH2006 *SHORT_20MIL
GND_VCORE
R90644 *Short_0402
PP5000_VMODEM
C2013 *4.7U/6.3V_4
SH2008 *SHORT_20MIL
GND_VMODEM
R90645 *Short_0402
PP5000_VPA
C2016 *10U/6.3V_4
SH2010 *SHORT_20MIL
GND_VPA
R90646 *Short_0402
PP5000_VS1
C2023 4.7U/6.3V_4
SH2011 *SHORT_20MIL
GND_VS1
R90647 *Short_0402
PP5000_VS2
C2024 4.7U/6.3V_4
SH2012 *SHORT_20MIL
GND_VS2
R90648 *Short_0402
PP5000_VGPU
C2025 10U/6.3V_4
SH2013 *SHORT_20MIL
GND_VGPU
[35] PP5000_VDRAM1_N
[35] PP5000_VDRAM1_P
NC270
NC271
R90649 *Short_0603
PP5000_VDRAM1
C2028 4.7U/6.3V_4
SH2015 *SHORT_20MIL
GND_VDRAM1
All Buck Input Cap close to chip
PL2001 0.47UH_2.0X1.6X1
DFE201610E-R47MCC=P2
L close to chip
DVDD_PROC_B
differential and shielding
DVDD_PROC_B_PMIC_FB [5]
DVDD_PROC_B_PMIC_GND [5]
PL2002 0.47UH_2.0X1.6X1
DFE201610E-R47MCC=P2
L close to chip
DVDD_PROC_L
DVDD_PROC_L_PMIC_FB [5]
DVDD_PROC_L_PMIC_GND [5]
PL2003 0.47UH_2.0X1.6X1
DFE201610E-R47MCC=P2
L close to chip
DVDD_CORE
DVDD_CORE_PMIC_FB [5]
DVDD_CORE_PMIC_GND [5]
VMODEM
R90876 *Short_0201
PP5000_ALW
PL2006 1UH_2.5x2.0x1
HTQP25201T-1R0MSR-39
L close to chip
VS1_PMU
VS1_LDO1
VS1 sense to Cap
PL2007 1UH_2.5x2.0x1
HTQP25201T-1R0MSR-39
L close to chip
VS2_PMU
VS2_PMU_R
VS2 sense to Cap
PL2008 0.47UH_2.0X1.6X1
DFE201610E-R47MCC=P2
L close to chip
DVDD_GPU
DVDD_GPU_PMIC_FB [5]
DVDD_GPU_PMIC_GND [5]
PL2009 1UH_2.5x2.0x1
HTQP25201T-1R0MSR-39
L close to chip
EMI_VDD2
EMI_VDD2_FB [11]
EMI_VDD2_GND [11]
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
20_POWER_MT6358-Buck
Rev 1A
Date: Wednesday, May 06, 2020
Sheet 20 of 39



Schematic design notice of "POWER_MT6358-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information

Note 21-2: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
Please refer to MT6358 design notice.

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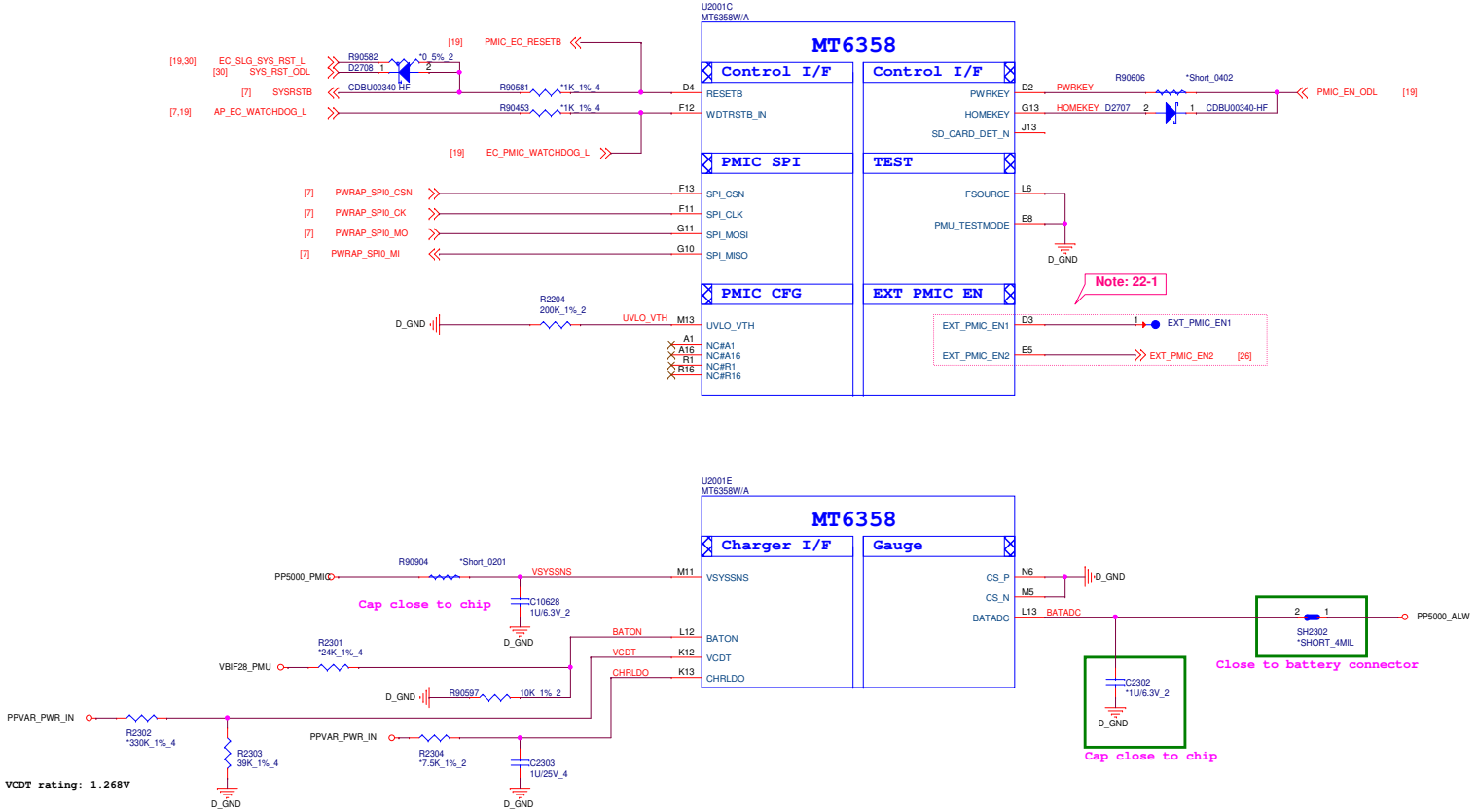
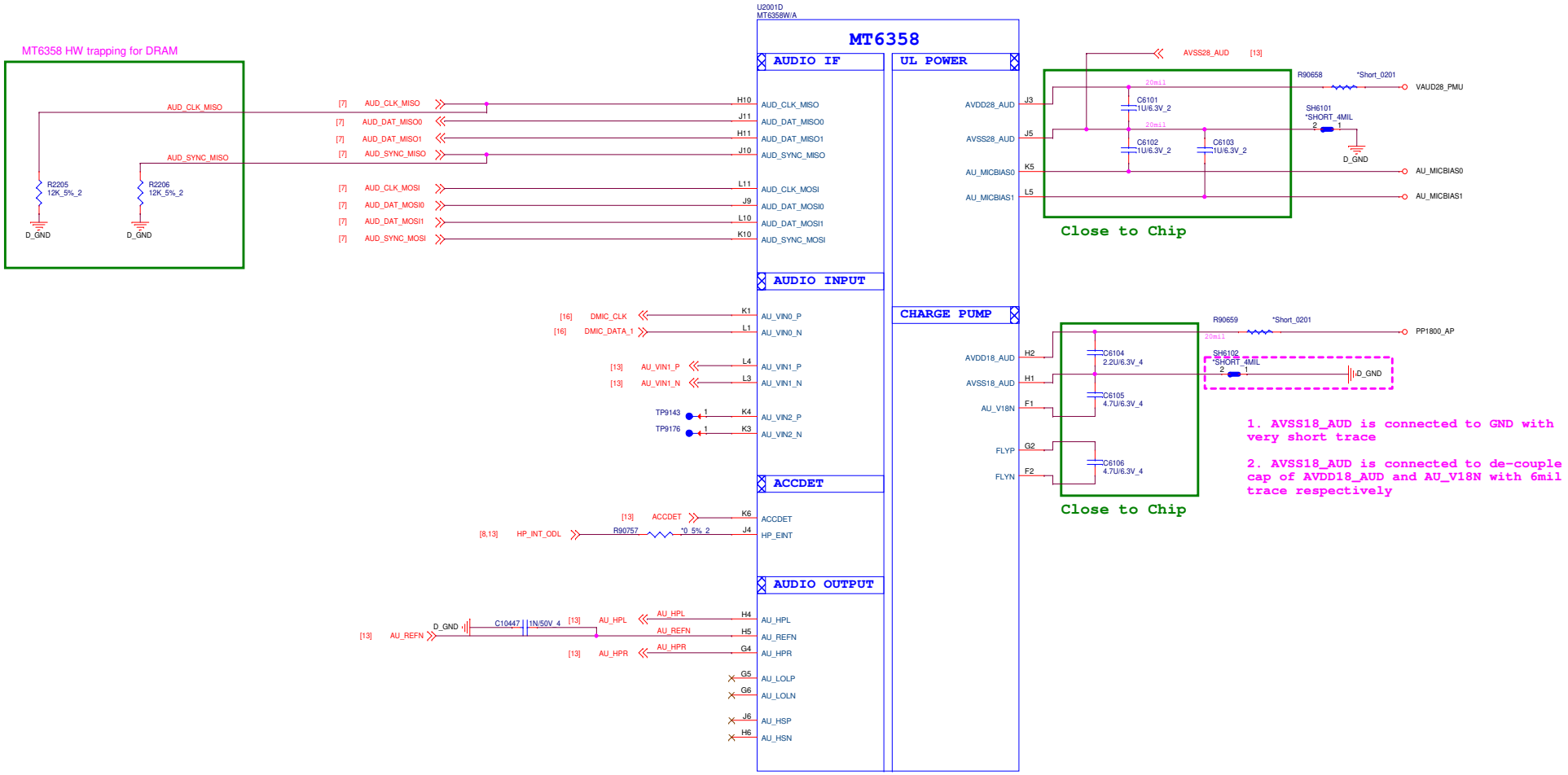
PROJECT : ZDE		
Size	Document Number: 21_POWER_MT6358-LDO	Rev: 1A
Date: Wednesday, May 06, 2020	Sheet 21 of 39	



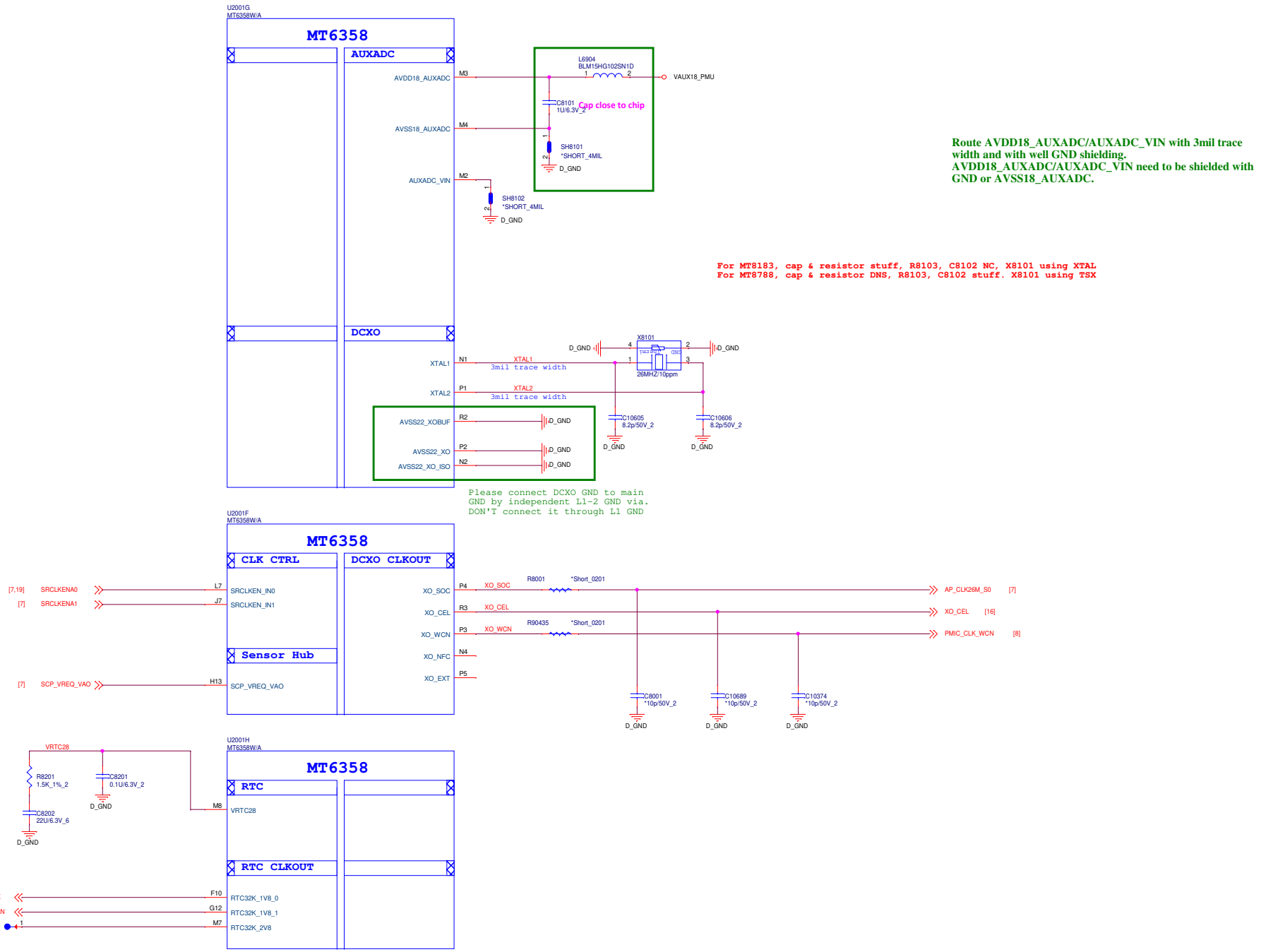
Quanta Computer Inc.			
PROJECT : ZDE			
Size	Document Number		Rev
	22_POWER_MT6358-IF		1A
Date: Wednesday, May 06, 2020	Sheet 22 of 39		



Schematic design notice of "POWER_MT6358-Audio"

Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2_LDO1_ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1



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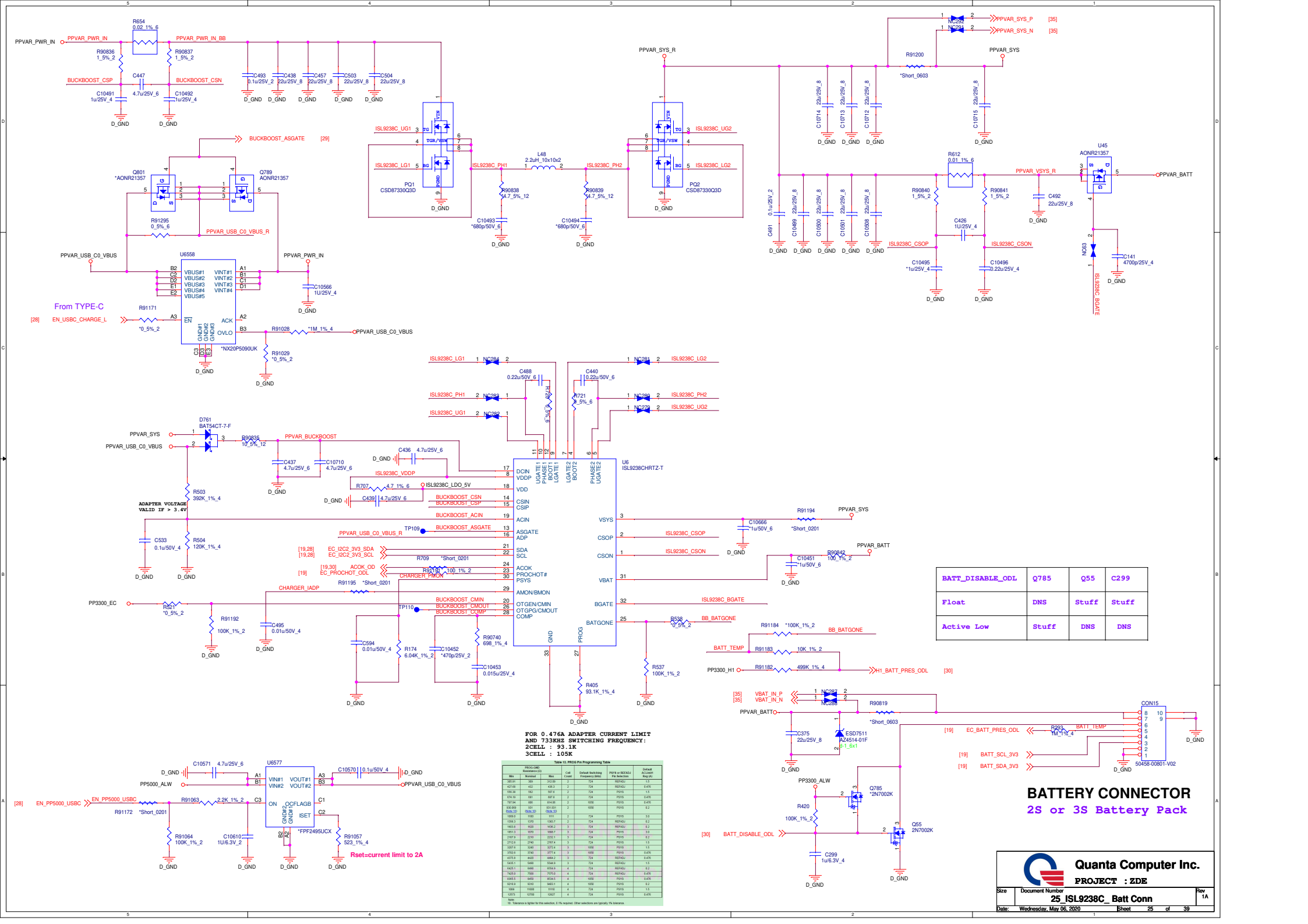
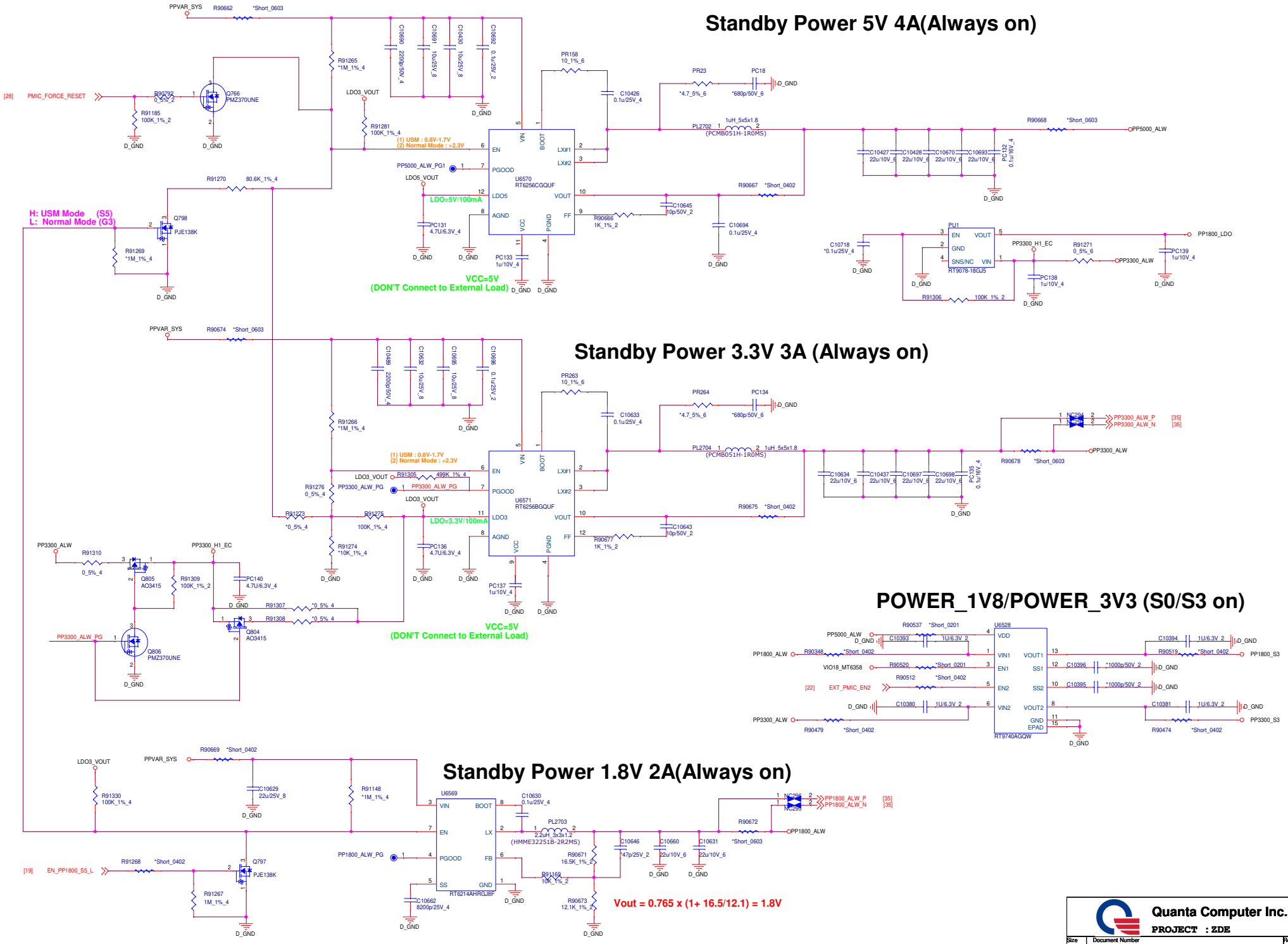
PROJECT : ZDE

Size	Document Number	Rev
	24_POWER_MT6358_Clock	1A

Date: Wednesday, May 06, 2020 Sheet 24 of 39


PPVAR_PWR_IN
PPVAR_PWR_IN_BB
BUCKBOOST_CSP
BUCKBOOST_CSN
BUCKBOOST_ASGATE [29]
PPVAR_USB_C0_VBUS_R
PPVAR_USB_C0_VBUS
From TYPE-C
[28] EN_USBC_CHARGE_L
*NX20P5090UK
PPVAR_SYS_R
ISL9238C_UG1
ISL9238C_LG1
ISL9238C_PH1
ISL9238C_UG2
ISL9238C_LG2
ISL9238C_PH2
PQ1 CSD87330Q3D
PQ2 CSD87330Q3D
L48 2.2uH_10x10x2
PPVAR_SYS
PPVAR_SYS_P [35]
PPVAR_SYS_N [35]
PPVAR_VSYS_R
PPVAR_BATT
ISL9238C_CSOP
ISL9238C_CSON
ISL9238C_BGATE
PPVAR_BUCKBOOST
ADAPTER VOLTAGE VALID IF > 3.4V
ISL9238C_VDDP
ISL9238C_LDO_5V
BUCKBOOST_CSN
BUCKBOOST_CSP
BUCKBOOST_ACIN
BUCKBOOST_ASGATE
PPVAR_USB_C0_VBUS_R
[19,28] EC_I2C2_3V3_SDA
[19,28] EC_I2C2_3V3_SCL
[19,30] ACOK_OD
[19] EC_PROCHOT_ODL
CHARGER_PMON
CHARGER_IADP
PP3300_EC
BUCKBOOST_CMIN
BUCKBOOST_CMOUT
BUCKBOOST_COMP
U6 ISL9238CHRTZ-T
DCIN VDDP UGATE1 PHASE1 BOOT1 LGATE1 LGATE2 BOOT2 PHASE2 UGATE2
VDD CSIN CSIP ACIN ASGATE ADP SDA SCL ACOK PROCHOT# PSYS AMON/BMON OTGEN/CMIN OTGPG/CMOUT COMP GND PROG
VSYS CSOP CSON VBAT BGATE
BB_BATGONE
BATT_TEMP
PP3300_H1
H1_BATT_PRES_ODL [30]
[35] VBAT_IN_P
[35] VBAT_IN_N
[19] EC_BATT_PRES_ODL
[19] BATT_SCL_3V3
[19] BATT_SDA_3V3
CON15
50458-00801-V02
PP5000_ALW
[28] EN_PP5000_USBC
*FPF2495UCX
Rset=current limit to 2A
PP3300_ALW
[30] BATT_DISABLE_ODL
Q785 *2N7002K
Q55 2N7002K
FOR 0.476A ADAPTER CURRENT LIMIT AND 733KHZ SWITCHING FREQUENCY:
2CELL : 93.1K
3CELL : 105K
Table 15. PROG Pin Programming Table
BATT_DISABLE_ODL | Q785 | Q55 | C299
Float | DNS | Stuff | Stuff
Active Low | Stuff | DNS | DNS
BATTERY CONNECTOR
2S or 3S Battery Pack
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
25_ISL9238C_ Batt Conn
Rev 1A
Date: Wednesday, May 06, 2020
Sheet 25 of 39


Standby Power 5V 4A(Always on)
PPVAR_SYS
R90662 *Short_0603
C10690 2200p/50V_4
C10691 10u/25V_8
C10430 10u/25V_8
C10692 0.1u/25V_2
R91265 *1M_1%_4
[28] PMIC_FORCE_RESET
R90792 0_5%_2
Q766 PMZ370UNE
R91185 100K_1%_2
D_GND
LDO3_VOUT
R91281 100K_1%_4
(1) USM : 0.8V-1.7V
(2) Normal Mode : >2.3V
PR158 10_1%_6
C10426 0.1u/25V_4
PR23 *4.7_5%_6
PC18 *680p/50V_6
PL2702 1uH_5x5x1.8 (PCMB051H-1R0MS)
R90668 *Short_0603
PP5000_ALW
C10427 22u/10V_6
C10428 22u/10V_6
C10670 22u/10V_6
C10693 22u/10V_6
PC132 0.1u/16V_4
PP5000_ALW_PG1
LDO5_VOUT
LDO=5V/100mA
U6570 RT6256CGQUF
EN PGOOD LDO5 AGND VIN BOOT LX#1 LX#2 VOUT FF VCC PGND
R91270 80.6K_1%_4
R90667 *Short_0402
C10645 10p/50V_2
R90666 1K_1%_2
C10694 0.1u/25V_4
PC131 4.7U/6.3V_4
PC133 1u/10V_4
VCC=5V
(DON'T Connect to External Load)
H: USM Mode (S5)
L: Normal Mode (G3)
Q798 PJE138K
R91269 *1M_1%_4
PU1 RT9078-18GJ5
EN VOUT GND SNS/NC VIN
C10718 *0.1u/25V_4
PP3300_H1_EC
R91271 0_5%_6
PP3300_ALW
PP1800_LDO
PC139 1u/10V_4
PC138 1u/10V_4
R91306 100K_1%_2
Standby Power 3.3V 3A (Always on)
PPVAR_SYS
R90674 *Short_0603
C10489 2200p/50V_4
C10632 10u/25V_8
C10695 10u/25V_8
C10696 0.1u/25V_2
R91266 *1M_1%_4
PR263 10_1%_6
C10633 0.1u/25V_4
PR264 *4.7_5%_6
PC134 *680p/50V_6
PL2704 1uH_5x5x1.8 (PCMB051H-1R0MS)
NC294 NC295
PP3300_ALW_P [35]
PP3300_ALW_N [35]
R90678 *Short_0603
PP3300_ALW
C10634 22u/10V_6
C10437 22u/10V_6
C10697 22u/10V_6
C10698 22u/10V_6
PC135 0.1u/16V_4
(1) USM : 0.8V-1.7V
(2) Normal Mode : >2.3V
R91305 499K_1%_4
LDO3_VOUT
R91276 0_5%_4
PP3300_ALW_PG
LDO=3.3V/100mA
U6571 RT6256BGQUF
EN PGOOD LDO3 AGND VIN BOOT LX#1 LX#2 VOUT FF VCC PGND
R91273 *0_5%_4
R91275 100K_1%_4
R90675 *Short_0402
C10643 10p/50V_2
R90677 1K_1%_2
R91274 *10K_1%_4
PC136 4.7U/6.3V_4
PC137 1u/10V_4
VCC=5V
(DON'T Connect to External Load)
PP3300_ALW
R91310 0_5%_4
Q805 AO3415
PP3300_H1_EC
R91309 100K_1%_2
PC140 4.7U/6.3V_4
R91307 *0_5%_4
R91308 *0_5%_4
Q804 AO3415
PP3300_ALW_PG
Q806 PMZ370UNE
POWER_1V8/POWER_3V3 (S0/S3 on)
U6528 RT9740AGQW
PP5000_ALW
R90537 *Short_0201
C10393 1U/6.3V_2
VDD
PP1800_ALW
R90348 *Short_0402
VIN1
VIO18_MT6358
R90520 *Short_0201
EN1
[22] EXT_PMIC_EN2
R90512 *Short_0402
EN2
PP3300_ALW
R90479 *Short_0402
VIN2
VOUT1
VOUT2
SS1
SS2
GND EPAD
C10396 *1000p/50V_2
C10395 *1000p/50V_2
C10380 1U/6.3V_2
C10394 1U/6.3V_2
R90519 *Short_0402
PP1800_S3
C10381 1U/6.3V_2
R90474 *Short_0402
PP3300_S3
Standby Power 1.8V 2A(Always on)
LDO3_VOUT
R91330 100K_1%_4
PPVAR_SYS
R90669 *Short_0402
C10629 22u/25V_8
R91148 *1M_1%_4
U6569 RT6214AHRGJ8F
VIN BOOT EN LX PGOOD FB SS GND
C10630 0.1u/25V_4
PL2703 2.2uH_3x3x1.2 (HMME32251B-2R2MS)
R90672 *Short_0603
NC296 NC297
PP1800_ALW_P [35]
PP1800_ALW_N [35]
PP1800_ALW
PP1800_ALW_PG
C10646 *47p/25V_2
C10660 22u/10V_6
C10631 22u/10V_6
R90671 16.5K_1%_2
R91169 10K_1%_2
C10662 8200p/25V_4
R90673 12.1K_1%_2
[19] EN_PP1800_S5_L
R91268 *Short_0402
Q797 PJE138K
R91267 1M_1%_4
Vout = 0.765 x (1+ 16.5/12.1) = 1.8V
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
26_ThirdParty_Powers
Rev 1A
Date: Wednesday, May 06, 2020
Sheet 26 of 39

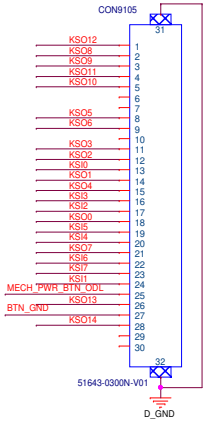
Quanta Computer Inc.

PROJECT : ZDE

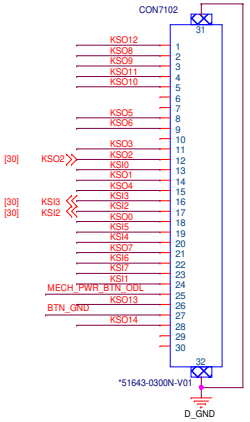
Size	Document Number	Rev
	27_POWER_ThirdParty_Powers	1A

Date: Wednesday, May 06, 2020 Sheet 27 of 39

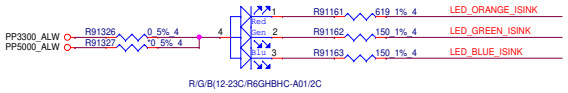
For 11"

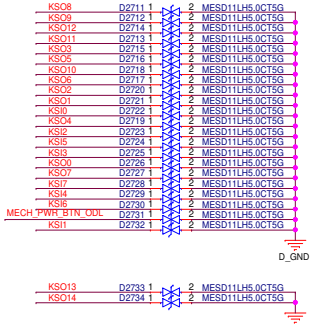


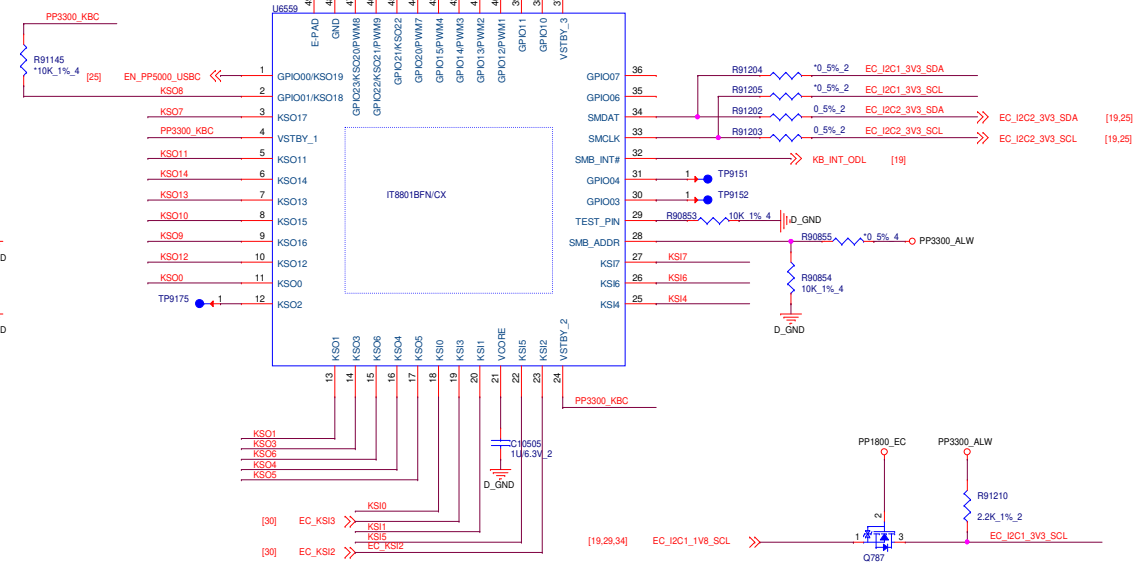
For 15"

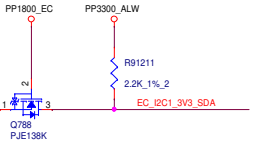


CHARGE/BATTERY LED

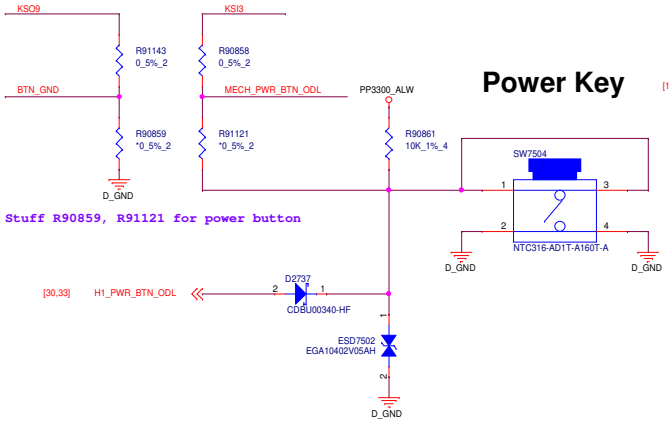








Stuff R91143, R90858 for lock button



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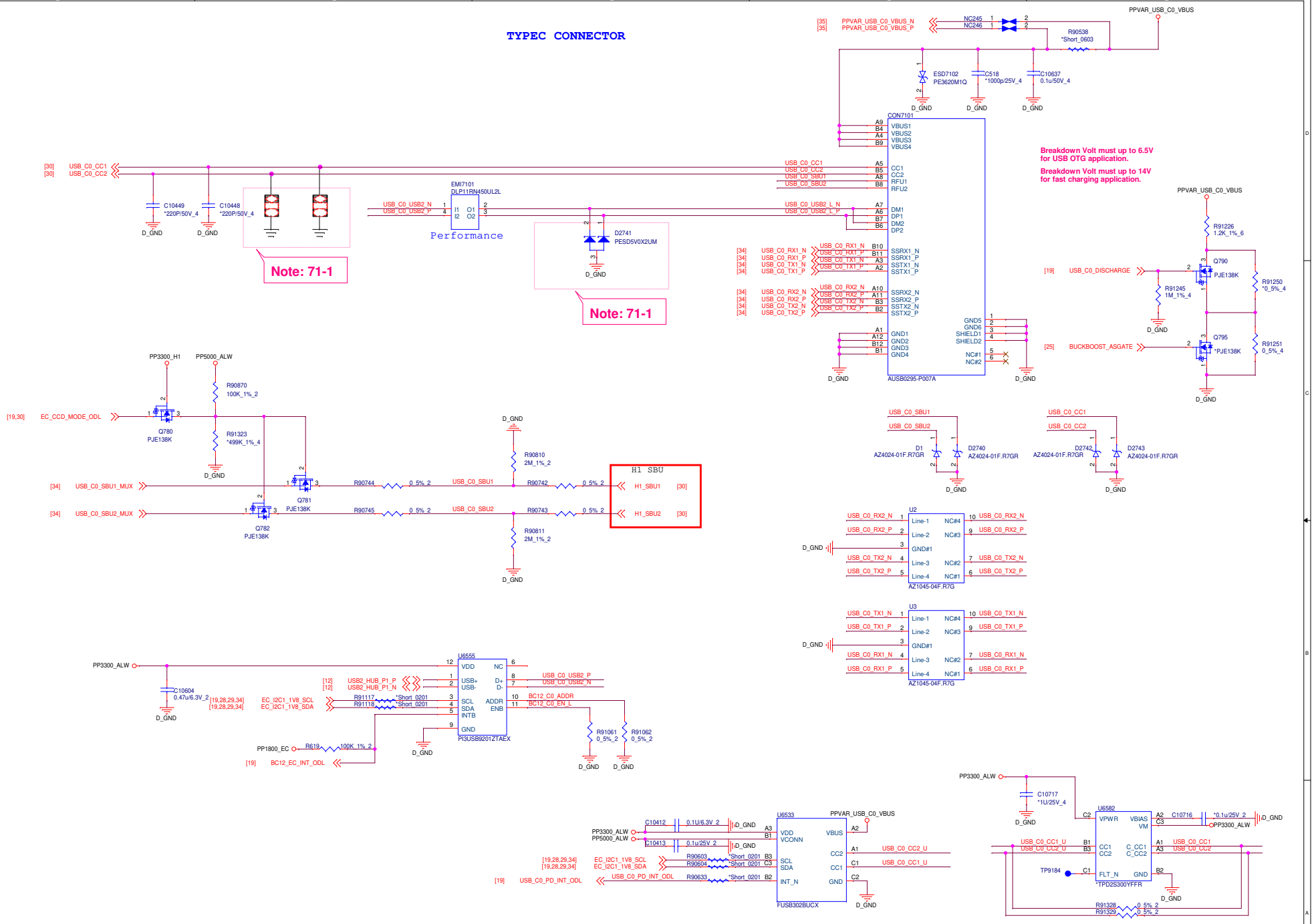
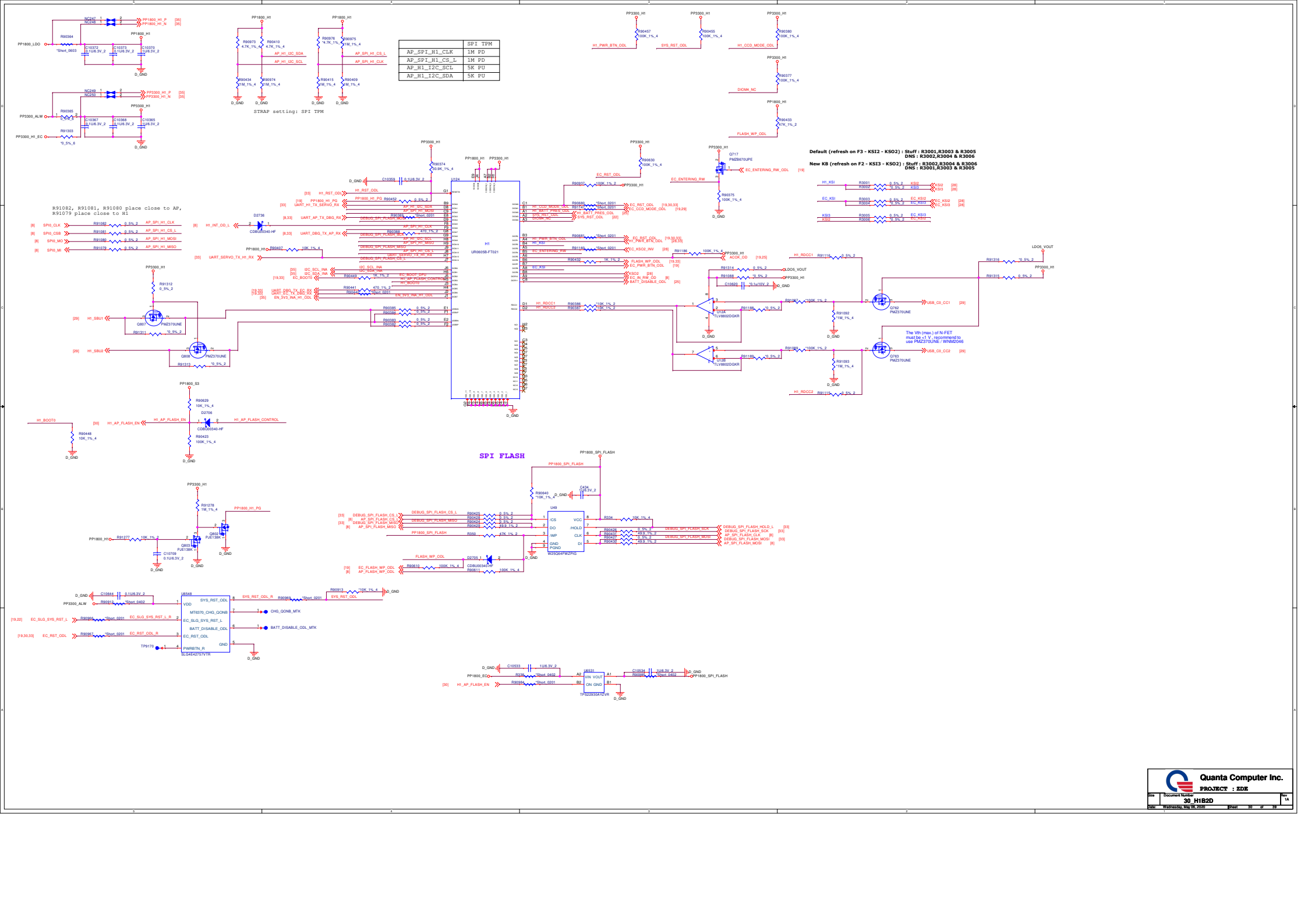
PROJECT : ZDE
Size: Document Number: 28_KEYBOARD_LED Rev: 1A
Date: Wednesday, May 06, 2020 Sheet 28 of 39



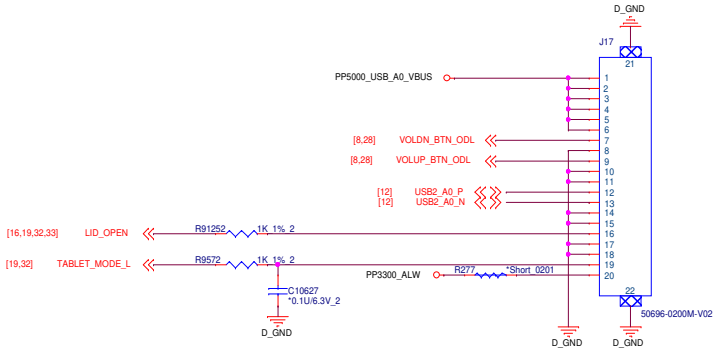
Schematic design notice of "PERI_USB 2.0" page.

Note 71-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

Quanta Computer Inc.		
PROJECT : ZDE		
Size	Document Number: 29_PERI_TypeC	Rev: 1A
Date: Wednesday, May 06, 2020	Sheet 29 of 39	


PP1800_LDO
R90364
*Short_0603
PP1800_H1
PP1800_H1_P
PP1800_H1_N
PP3300_ALW
R90365
PP3300_H1_EC
R91303
*0_5%_6
PP3300_H1
PP3300_H1_P
PP3300_H1_N
AP_H1_I2C_SDA
AP_H1_I2C_SCL
AP_SPI_H1_CS_L
AP_SPI_H1_CLK
STRAP setting: SPI TPM
SPI TPM
AP_SPI_H1_CLK 1M PD
AP_SPI_H1_CS_L 1M PD
AP_H1_I2C_SCL 5K PU
AP_H1_I2C_SDA 5K PU
R91082, R91081, R91080 place close to AP,
R91079 place close to H1
SPI0_CLK
SPI0_CSB
SPI0_MO
SPI0_MI
AP_SPI_H1_CLK
AP_SPI_H1_CS_L
AP_SPI_H1_MOSI
AP_SPI_H1_MISO
H1_INT_OD_L
UART_AP_TX_DBG_RX
UART_DBG_TX_AP_RX
UART_SERVO_TX_H1_RX
I2C_SCL_INA
I2C_SDA_INA
EC_BOOT0
UART_DBG_TX_EC_RX
UART_EC_TX_DBG_RX
EN_3V3_INA_H1_ODL
H1_SBU1
H1_SBU2
H1_BOOT0
H1_AP_FLASH_EN
H1_AP_FLASH_CONTROL
H1_RST_ODL
PP1800_H1_PG
UART_H1_TX_SERVO_RX
H1_CCD_MODE_ODL
H1_BATT_PRES_ODL
SYS_RST_ODL
H1_PWR_BTN_ODL
EC_KSI
EC_ENTERING_RW
FLASH_WP_ODL
EC_IN_RW_OD
EC_KSO2_INV
BATT_DISABLE_ODL
H1_RDCC1
H1_RDCC2
ACOK_OD
LDOS_VOUT
USB_C0_CC1
USB_C0_CC2
The Vth (max.) of N-FET
must be <1 V , recommend to
use PMZ370UNE / WNM2046
SPI FLASH
PP1800_SPI_FLASH
DEBUG_SPI_FLASH_CS_L
DEBUG_SPI_FLASH_MISO
DEBUG_SPI_FLASH_SCK
DEBUG_SPI_FLASH_MOSI
DEBUG_SPI_FLASH_HOLD_L
AP_SPI_FLASH_CLK
AP_SPI_FLASH_MOSI
W25Q64FWZPIG
SYS_RST_ODL_R
CHG_QONB_MTK
BATT_DISABLE_ODL_MTK
EC_SLG_SYS_RST_L
EC_RST_ODL
PWRBTN_R
SLG4E42757VTR
TPS22930AYZVR
Default (refresh on F3 - KSI2 - KSO2) : Stuff : R3001,R3003 & R3005
DNS : R3002,R3004 & R3006
New KB (refresh on F2 - KSI3 - KSO2) : Stuff : R3002,R3004 & R3006
DNS : R3001,R3003 & R3005
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
30_H1B2D
Rev
1A
Date: Wednesday, May 06, 2020
Sheet 30 of 39

To SUB Board Connector



Force Download key

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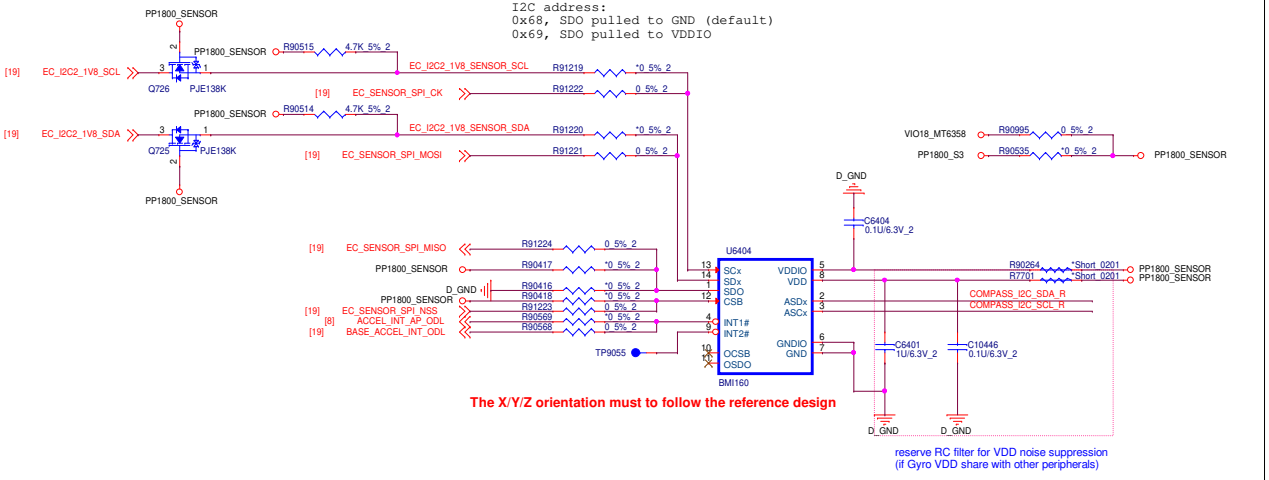
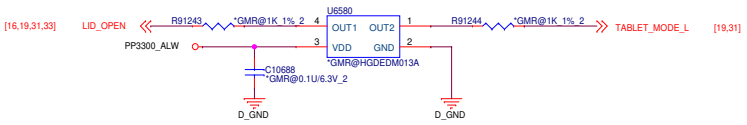
PROJECT : ZDE		
Size	Document Number: 31_CONNECTOR TO SUB BOARD	Rev: 1A
Date: Wednesday, May 06, 2020	Sheet 31 of 39	

Accerometer + Gyro Sensor



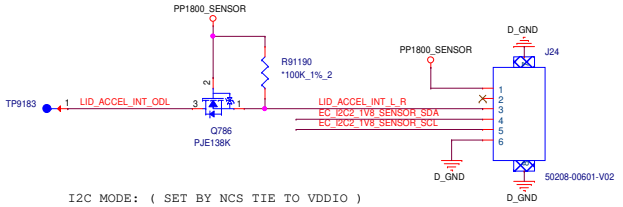
GMR Sensor

DNS IF GMR IS ON SUB-BOARD



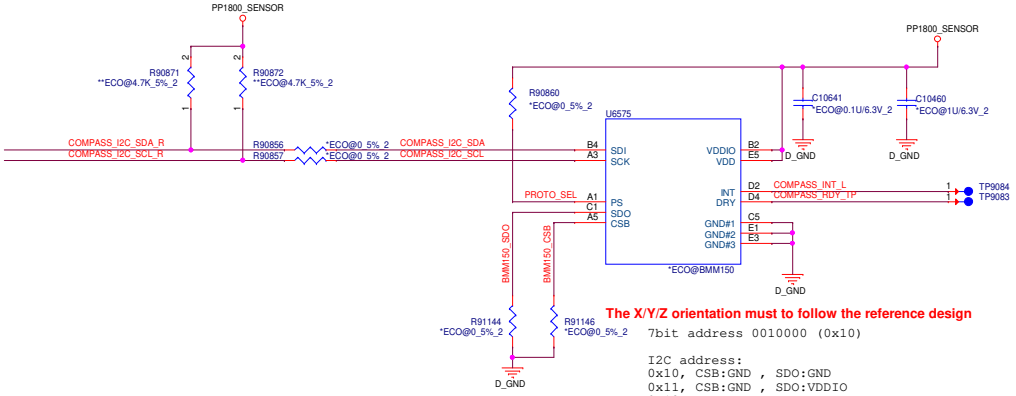
[OEM] BOM option

LID ACCEL



I2C MODE: (SET BY NCS TIE TO VDDIO)
I2C 8bit ADDRESS: 0X3E (SDO_ADDR = VDDIO)
I2C MAX SPEED = 3.4MHZ

COMPASS

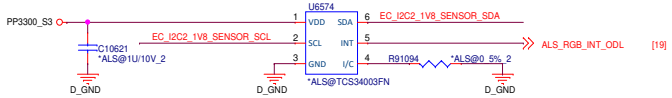


The X/Y/Z orientation must to follow the reference design

7bit address 0010000 (0x10)

I2C address:
0x10, CSB:GND , SDO:GND
0x11, CSB:GND , SDO:VDDIO
0x12, CSB:VDDIO ,SDO:GND
0x13, CSB:VDDIO, SDO:VDDIO

Ambient Light Sensor



[OEM] BOM option

Schematic design notice of "PERI_SENSORS_MEMs_ALS/PS" page.

Note 77-1: [Compass] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail

Note 77-2: [A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide

Note 77-3: [A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C**

Note 77-4: [A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.

Note 77-5: [Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)

Note 77-6: DO NOT share Sensor hub i2C to other non-SCP device

Note 77-7: Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]

HOLE

HOLE7 *h-o118x157d118x157n
HOLE8 *H-C276D118P2
HOLE15 *H-C276D110P2
HOLE19 *SPAD-RE394X118NP
HOLE20 *SPAD-RE197X787NP
HOLE9 *H-C315D118P2
HOLE10 *H-C315D177P2
HOLE11 *h-zde-1p2
HOLE12 *H-C315D177P2
HOLE13 *H-C315D118P2
HOLE14 *H-C276D110P2
HOLE16 *spad-re295x472np
HOLE17 *2D-BARCODE-8X8-S
HOLE18 *2D-BARCODE-8X8-S

Clip

CLIP19 *FBFG200601
CLIP17 *FBFG200601
CLIP21 *FBFG200601
CLIP9 *FBFG200601
CLIP10 *FBFG200601
CLIP11 *FBFG200601
CLIP12 *FBFG200601
CLIP20 *FBFG200601

D_GND

P1V8_H1 for H1 UART
PP1800_AP for AP JTAG

PP1800_H1
PP1800_AP
R323 0_5%_2
R90587 *0_5%_2
PP3300_ALW
Q727 PJE138K

CON16
AXK750147G

[8] SERVO_JTRST
[30] DEBUG_SPI_FLASH_CS_L
[30] DEBUG_SPI_FLASH_MISO
[30] DEBUG_SPI_FLASH_HOLD_L
DEBUG_SPI_FLASH_SCK [30]
DEBUG_SPI_FLASH_MOSI [30]
PP1800_SPI_FLASH
TP9158 TP9159 TP9160 TP9157
TP9168 TP9169 TP9165 TP9166 TP9167 TP9163 TP9162 TP9161 TP9154 TP9155

[8,30] UART_AP_TX_DBG_RX R332 *Short_0402
[8] UART_SERVO_TX_SCP_RX R90962 *0_5%_4
[8] SERVO_JTCK
[30] UART_SERVO_TX_H1_RX R313 0_5%_4
[8] SERVO_JTMS
[30] UART_H1_TX_SERVO_RX R314 0_5%_4
[8] SERVO_JTDO
[8] UART_SCP_TX_SERVO_RX R90963 *0_5%_4
SERVO_JTRST
H1_UART_VREF
[19,30] UART_EC_TX_DBG_RX R90438 *Short_0402 R476 *Short_0402
PP3300_SERVO_INA
[35] I2C_SDA_INA_SERVO
[19,30,33] EC_RST_ODL R90683 *0_5%_2
SERVO_SYS_RST_ODL
SERVO_EC_BOOT0_ODL
[8,31] MT8183_KPCOL0
[30] H1_RST_ODL R90874 *Short_0402

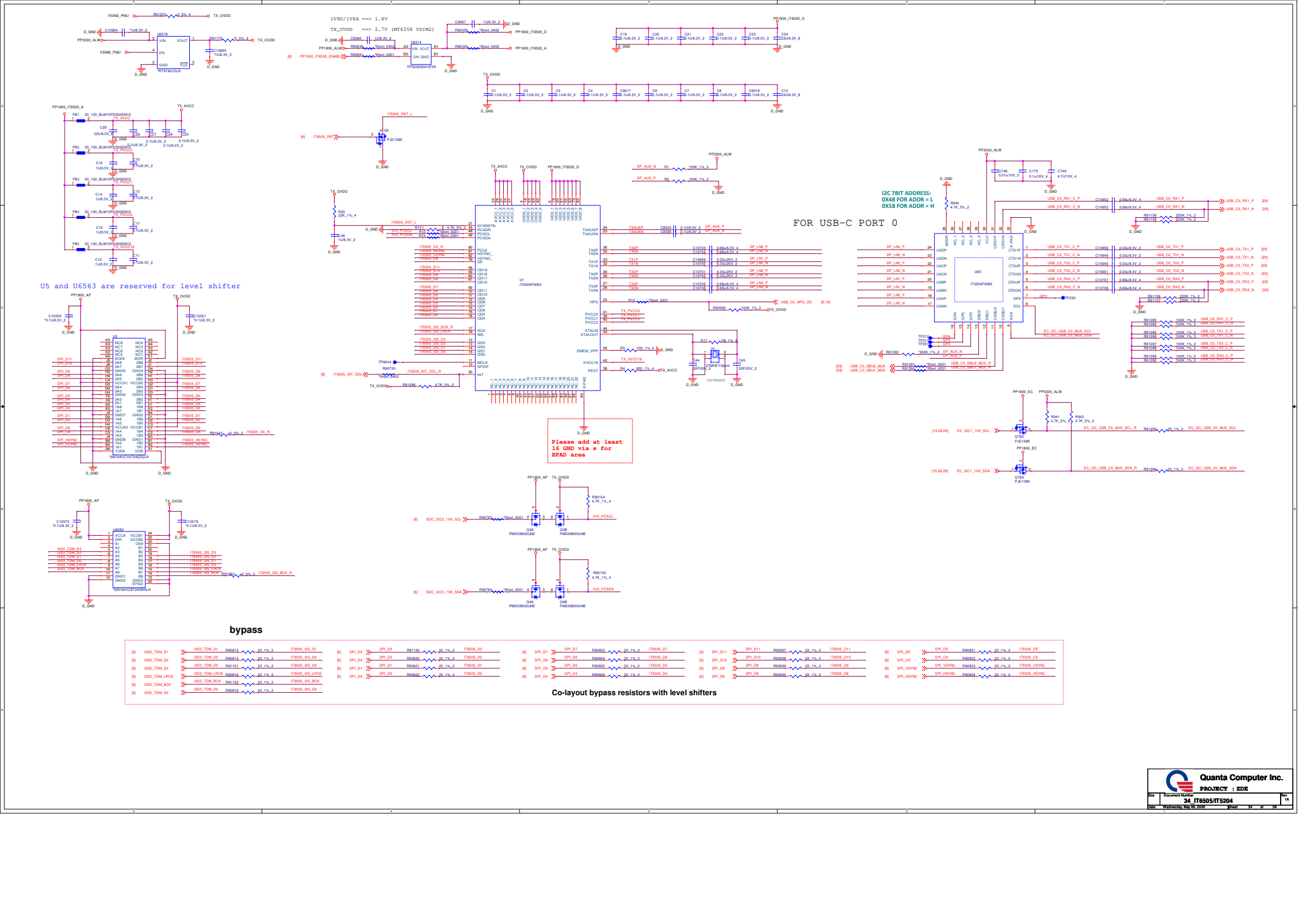
AP_UART_VREF R90682 R331 R330 *Short_0402
EC_RST_ODL [19,30,33]
UART_DBG_TX_AP_RX [8,30]
PP1800_AP
SERVO_JTDI [8]
H1_PWR_BTN_ODL [28,30]
EC_UART_VREF R90439 R90440 *Short_0402
UART_DBG_TX_EC_RX [19,30]
PP1800_EC
R512 *Short_0402
I2C_SCL_INA_SERVO [35]
FLASH_WP_ODL [19,30]
R91181 *Short_0402
LID_OPEN [16,19,31,32]

PP1800_EC
R90451 1M_1%_4
Q8 PMZB670UPE
SERVO_EC_BOOT0_ODL
EC_BOOT0
EC_BOOT0 [19,30]
R90450 10K_1%_4

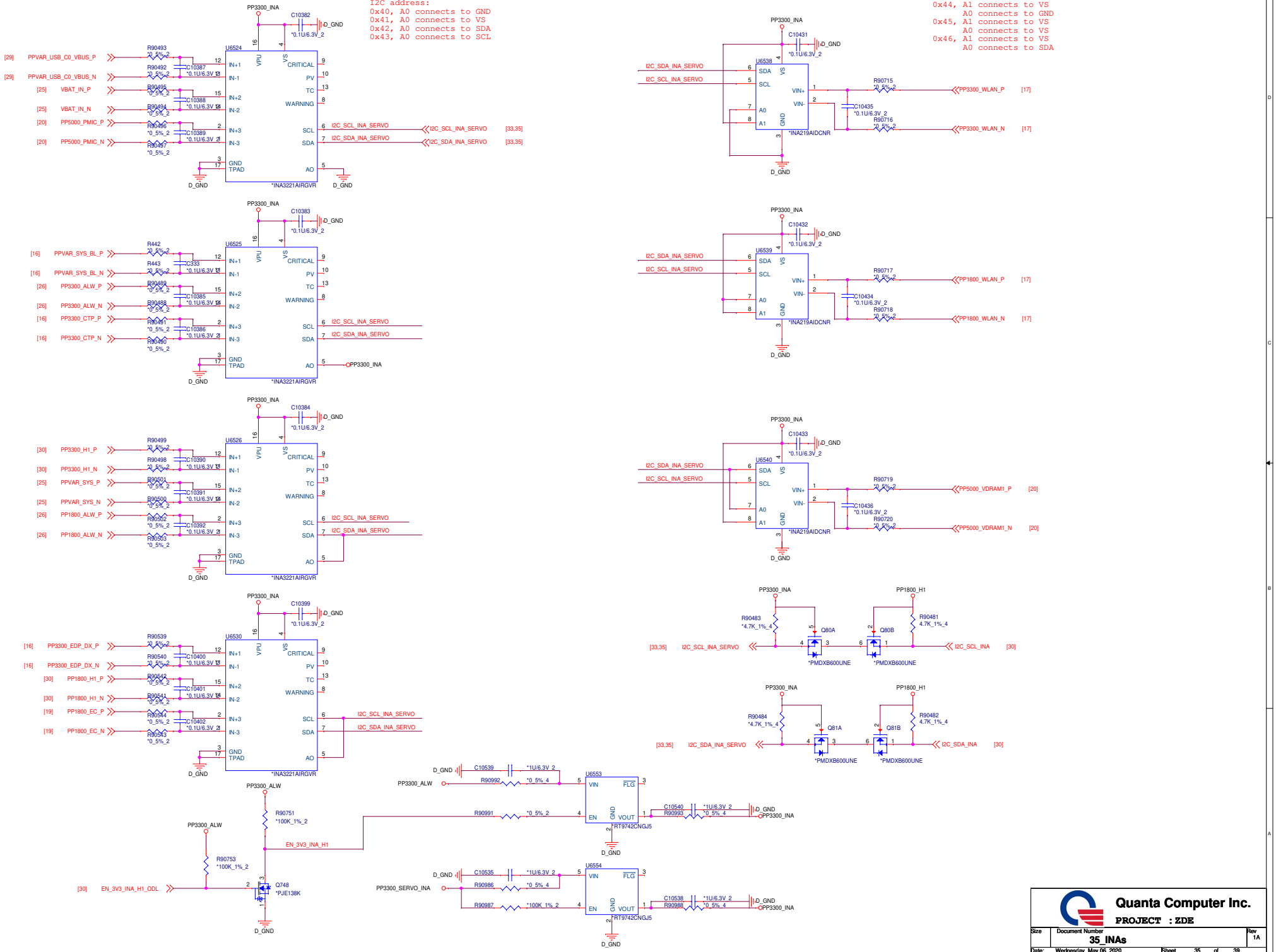
NC once there's no need for servo header

H1_UART_VREF
C412 *0.1U/6.3V_2
EC_UART_VREF
C414 *0.1U/6.3V_2
AP_UART_VREF
C415 *0.1U/6.3V_2

Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number 33_DEBUG_IO/CLIP/HOLE
Rev 1A
Date: Wednesday, May 06, 2020
Sheet 33 of 39



Quanta Computer Inc.	
PROJECT : ZDE	
Size	Document Number: 34_IT6505/IT5204
Rev: 1A	
Date: Wednesday, May 06, 2020	Sheet 34 of 39


I2C address:
0x40, A0 connects to GND
0x41, A0 connects to VS
0x42, A0 connects to SDA
0x43, A0 connects to SCL
I2C address:
0x44, A1 connects to VS
A0 connects to GND
0x45, A1 connects to VS
A0 connects to VS
0x46, A1 connects to VS
A0 connects to SDA
PP3300_INA
U6524
U6525
U6526
U6530
U6538
U6539
U6540
*INA3221AIRGVR
*INA219AIDCNR
D_GND
I2C_SCL_INA_SERVO
I2C_SDA_INA_SERVO
PP3300_WLAN_P
PP3300_WLAN_N
PP1800_WLAN_P
PP1800_WLAN_N
PP5000_VDRAM1_P
PP5000_VDRAM1_N
PP1800_H1
Q80A
Q80B
Q81A
Q81B
*PMDXB600UNE
I2C_SCL_INA
I2C_SDA_INA
PP3300_ALW
U6553
U6554
*RT9742CNGJ5
PP3300_SERVO_INA
EN_3V3_INA_H1
EN_3V3_INA_H1_ODL
Q748
*PJE138K
Quanta Computer Inc.
PROJECT : ZDE
Size
Document Number
35_INAs
Rev
1A
Date: Wednesday, May 06, 2020
Sheet 35 of 39

Data	Page	Item
5/27	16	change CON6801 & J19 to Bobba360 eDP panel connector J15(include DMIC connection too)
5/27	25	remove R90739, ISL9241_BYPSG, ISL9241_NGATE test point, add circuit as note pic
5/27	25,30	Add inveter circuit for BATT_DISABLE_ODL net (PU 100K to PP3300_ALW) that connects to Battery Conn.
5/27	25	Add a power symbol ISL9241_5V for ISL9241 VDD (pin18)
5/28	30	U124 B4 pin connects to KSI2, A5 pin connect to EC_KSO2_INV, A8 pin connects to EC_KSI2, B8 pin connects to KSO2
6/3	7	AE24 pin net name PANEL_3V3_ENABLE, AE25 net name LCD_POWER_EN connect to page 16, AJ25 pin net name USBA_POWER_EN connects to page 12
6/3	16	change R91125 connects to PP3300_S3
6/3	16	remove U6549 circuit
6/3	16	change R90695 connect to PP3300_S3
6/3	12	change U6552 to 0.5A PN
6/3	16	VSYS_BL_P/VSYS_BL_N connect to R391. Maybe move R391 to VSYS/R259 location is more better
6/3	19,32	change GAUGE_INT_ODL to RGB_INT_ODL connects to page U6574 pin 5 . R90865 remove
6/3	34	add DPI/I2S level shift circuit & 3.3V power back as backup for PCB size
6/4	1	Update block diagram
6/4	17	consider to remove U6534, U6535 circuit.
6/10	16	Please change U260 from LDO(RT9018) back buck converter(RT5710)
6/10	25	Please connect replace PPVAR_PWR_IN with PPVAR_USB_C0_VBUS.
6/11	25	AONP36336 and AONR36336 seem to have better power efficiency than SISA14DN. Please double confirm if there are other concerns like cost and thermal to replace SISA14DN with AONP36336x2 or AONR36336 x 4.
6/11	29	Change U6533 pin A2 from VBUS to PPVAR_USB_C0_VBUS
6/14	28	- add 0 ohm between LED_1_L and GPIO12/PWM1 of IT8801.- add 0 ohm between LED_2_L and GPIO13/PWM2 of IT8801. - add one more power led and LED_3_L to GPIO14/PWM3 of IT8801. (b/135086465)
6/14	25	A bi-directional power switch is required between USB-C connector and charger input: please add AOZ1375DI
6/14	28	RGB_INT_ODL to U6559.38 (IT8801), and add TP to all unused pins of IT8801
6/14	30	Add 0 ohm between EC_KSO2_INV and H1
6/14	34	Add USB-C MUX (IT5205) in order to resolve USB3.0 detection issue
6/18	25	Reserve a 0 ohm to bypass U6562
6/18	26	Change U6569 to RT6214AHRGJ8F, PG is needed for PP1800_ALW_PG
6/18	1	Update the block diagram
6/18	12	Add WFC using DM4 and DP4 of U6546
6/18	16	Replace LCD_POWER_EN circuit with a fuse, and add another 1uF on EDP_BL_VOUT
6/18	28	DNS R90875 since there's internal pull up, and change net name from KB_VSTBY to PP3300_KBC
6/18	28	Assign LID_ACCEL_INT_L to U6559.39 (GPIO11)
6/18	34	For I/O power of IT6505 (TX_OVDD), please add a power switch and use VSIM2_PMU as enable pin. PS. For proto build, please pick 3V3 as default route
6/18	34	(a) AC caps on SSTX lines should be 0.1uF; while AC caps on SSRX lines are 0.33uF (b) From loss perspective, please use 0201 size for caps and resistors on SSTX/SSRX lines (and void pads in layout)
6/18	34	[Netname fix] DDI0_TX*_P -> DP_LN*_P; DDI0_TX*_N -> DP_LN*_N; DDI0_AUX_P -> DP_AUX_P; DDI0_AUX_N -> DP_AUX_N; AUX+ -> USB_C0_SBU1_MUX; AUX- -> USB_C0_SBU2_MUX
6/18	29	FSUSB42UMX is not required, please follow h1 ref.
6/18	34	Connect IT5205 to EC_I2C1_1V8_* with level shifts, and mount R941/R942
6/18	25	Remove AOZ1375DI since it does not support dead battery mode. Please follow kukui using U6561(FPF2495UCX) and U6558 (NX20P5090UK), EN_USBC_CHARGE_L and EN_PP5000_USBC.
6/18	19	Update EC GPIO pin assign
6/20	30	DNS/NC R90640
6/20	30	Add netname onto U124.J5: EC_BOOT_DFU
6/20	33	Please reserve testpoints onto servo header NC pins
6/20	33	[Netname for nit] DEBUG_UART_POWER -> AP_UART_VREF ; DEBUG_EC_UART_POWER -> EC_UART_VREF ; H1_DEBUG_POWER -> H1_UART_VREF ; LID_OPEN_L -> LID_OPEN
6/20	33	Connect LID_OPEN to servo header pin44 via a 0ohm
6/20	28	Remove EC_WAKE and the interrupt OR circuit
6/20	19	KB_INT_ODL to EC's PA8 with a 0 ohm
6/20	30	Remove PWRBTN, PWRBTN_R and add TP on U6548.4
6/20	28	The note in p28 about R90857, should be R91143
6/20	30	Reserve 0 ohm bypassing U12A.3->1 and U12B.5->7
6/20	32	Add a mosfet onto LID_ACCEL_INT_L as level shift
6/20	12	Reserve a 0-ohm resistor array (can be replaced by EMI choke) for DP/DM near USB-A connector
6/20	12	[For nit] 2. USBA_POWER -> PP5000_USB_A0_VBUS 3. USB_HUB2_DM -> USB2_A0_N 4. USB_HUB2_DP -> USB2_A0_P 5. TYPEC0_USB_DM -> USB_C0_USB2_N 6. TYPEC0_USB_DP -> USB_C0_USB2_P 7. USB_HUB1_DM -> USB2_HUB_P1_N 8. USB_HUB1_DP -> USB2_HUB_P1_P 9. USB_HUB3_DM -> USB2_HUB_P3_N 10. USB_HUB3_DP -> USB2_HUB_P3_P 11. HUB_USB4_DM -> USB2_HUB_P4_N 12. HUB_USB4_DP -> USB2_HUB_P4_P 13. USB_WFC_N -> USB2_WFC_N 14. USB_WFC_P -> USB2_WFC_P 15. VSYS_PMIC -> PP5000_PMIC 16. VSYS_PMIC_P -> PP5000_PMIC_P 17. VSYS_PMIC_N -> PP5000_PMIC_N 18. PMIC_FORCE_RESET_OD -> EN_PP5000_ALW_L
6/20	1	Update block diagram
6/20	19	Change netname from OTG_EN to EN_OTG
6/20	29,30	Remove R90585/Q719/R90586, re-connect AC_PRESENT to ACOK_OD and add a 100kOhm pull-up to PP3300_H1
6/20	19	EN_USBC_CHARGE_L to EC's PC7, EN_PP5000_USBC to PD2
6/20	25	Remove J927 and related components, change H1_CHASSIS_OPEN to H1_BATT_PRES_ODL with 499K pull up to PP3300_H1
6/20	26	Add a test point on PP3300_ALW_PG
6/20	25	Remove R58 and CD5, add 100k serie resistor from EC_BATT_PRES_ODL to R293
6/20	25	Battery I2C interface should be connected to EC_I2C2_3V3
6/20	25	Change ISL9241 I2C interface to EC_I2C2_3V3
6/20	25	PPVAR_CHG_VIN should be replaced by PPVAR_PWR_IN.

Data	Page	Item
6/20	25	1. Add netname to CON15.5 "BATT_TEMP" 2. Change R293 to 100kOhm 3. Connect BATT_TEMP to H1_BATT_PRES_ODL via a 0ohm 4. Connect BATT_TMEP to BB_BATGONE via a DNS'd 100kohm
6/20	25	Change BATT_TEMP circuit
6/21	32	Remove note "IMU sensor has to be placed as close (<4cm) to WF CAM"
6/21	19,32	ACCEL_INT_ODL -> BASE_ACCEL_INT_ODL
6/21	25	Change charger IC to ISL9238
6/21	34	Change C10649,C10650,C10651,C10656 to 0.22uF
6/21	19	Reserve an external pull resistor on EC PA14. (1k ohm to PP1800_EC)
6/21	19	- Reserve an external pull resistor on EC PC13. (100k ohm to PP1800_EC) - R91178 can be DNS
6/21	16	Change the backlight control
6/24	14	Remove R90723
6/24	19	Add testpoints on EC's unused pins
6/24	28	Reserve stuffing options for IT8801 on EC_I2C1
6/24	10	DNS R90729 since LCM_ID will not be used for Jacuzzi
6/24	12	Add a note near CON481 "Change to USB2 connector from EVT"
6/24	12	Add capacitor(s) on PP5000_USB_A0_VBUS near USB-A connector, the total capacitance should be >120uF by spec.
6/24	16,19,25,26	[Netname] 1. EN_PP5000_ALW_L -> PMIC_FORCE_RESET 2. VSYS -> PPVAR_SYS
6/24	12,19	1. Change USBA_POWER_EN to EN_USBA_5V 2. Connect EN_USBA_5V to EC's PC14 3. Reserve connection to USBA_POWER_EN via a DNS's 0Ohm
6/24	-	[Netname] 1. ISL9241_5V to ISL9241_LDO_5V 2. RGB_INT_ODL to ALS_RGB_INT_ODL 3. LID_ACCEL_INT_L to LID_ACCEL_INT_ODL
6/24	30	Change R91116 / R91115 from Q762.3/Q763.3 to Q762.2/Q763.2
6/24	30	Change Q762.1/Q763.1 from PP3300_H1 to ISL9241_LDO_5V
6/24	28	1. LID_ACCEL_INT_ODL to EC's PA14, no external pull high 2. ALS_RGB_INT_ODL to EC's PC4, no external pull high 3. Reserve TP on IT8801 side
6/24	34	Having a 0 ohm from VSIM2_PMU to TX_OVDD, DNS U6576
6/24	22	PPVAR_CHG_VIN is signal net, should change to PPVAR_PWR_IN
6/24	25	Check battery spec to determine stuffing option of Q785/Q55/R420/C299.
6/24	25	Adding 20m ohm between PQ2.1 and VSYS, connect to VSYS_P / VSYS_N instead of R612
6/24	25	Reserve ASGATE control with PFET from PPVAR_USB_C0_VBUS to PPVAR_PWR_IN
6/24	10,19	Please complete HWID tables in schematic
6/24	16	1. Rename TP_INT_1V8 to TRACKPAD_INT_1V8_ODL, with an external 100kOhm pull-up 2. Remove Q733 and R91114 3. Change Q732 & Q734 design similar as in column K 4. Please use 100kOhm for external pull-up on interrupt
6/25	19,32	1. Use SPI as default interface from EC to BMI160, and reserve I2C 2. EC pins need to be moved around, please see link in column K
6/25	8	1. Connect EC_VOLUP_BTN_ODL to AP's EINT5 via a 0ohm 2. Connect EC_VOLDN_BTN_ODL to AP's EINT6 via a 0ohm
6/25	25,30	[Netname] *9241 to *9238C
6/25	30	[BOM] 1. DNS U12, R91088, R90386, R90387, R91188, R91189, C10620 2. STUFF R91115, R91116
6/26	19	[BOM] Stuff U6547/ Q750 / R90880 / C10469
6/27	19	[BOM change] For Jacuzzi, we decided to reset EC_BOARD_ID. Please change R90473 to 2.2kOhm and modify the table accordingly
6/27	30	Kukui post_p2 #28 didn't get introduced: 1. Update reset map to v2.3 2. Change R90973 & R90410 to 4.7kOhm (and modify the strap table)
6/27	8	Note near R90591: "Remove JTAG connections after proto"
6/27	10	Note near LCM_ID: "NOT USED IN JACUZZI"
6/27	25	[BOM change] 1. Mount Q789 2. DNS U6558 and U6577
7/19	25	ISL9238C ds suggests C437 to be at 50V rating, to have effective capacitance higher than 0.4µF at 20V
7/19	30	DNS R91087, R91089, R91092, and R91093
7/19	1,2	Please update block diagram and I2C table accordingly
7/19	16	DNS R218 as RT5710AHGQW cannot stand PPVAR_SYS as input power
7/19		LCM_RST_L_1V8 -> MIPIBRDG_PWRDN_L_1V8 ; EC_VOLUP_BTN_ODL -> VOLUP_BTN_ODL ; EC_VOLDN_BTN_ODL -> VOLDN_BTN_ODL ; PS8640_1V2 -> PP1200_MIPIBRDG PS8640_VIN -> PP3300_MIPIBRDG_DX ; PP3300_LCM -> PP3300_EDP_DX ; PP3300_PANEL -> PP3300_EDP_DX_R ; PP3300_LCM_P -> PP3300_EDP_DX_P PP3300_LCM_N -> PP3300_EDP_DX_N ; PANEL_3V3_ENABLE -> EN_PP3300_EDP_DX
7/19	12	Connect U6552 FLG pin to U6546 OVCUR2# pin, with a 100kOhm external pull-up and netname USB_A0_OC_ODL
7/19	29	Fix typo: Brealdown to Breakdown
7/19	4	Add power tree into schematics
7/25	19	Remove the following connections to EC: - CHARGER_PMON (R91177) - EN_OTG (R91193/R91180) - CHARGER_IADP (R91176)
7/25	29	Need to have discharge path on PPVAR_USB_C0_VBUS. Adding a NFET which is controled by U6517.PB6 with 1.2K (0603) discharging resistor. The net name is USB_C0_DISCHARGE.
7/25	25	[Net name] 1. VBAT to PPVAR_BATT 2. VSYS_BL_* to PPVAR_SYS_BL_* 3. VSYS_P to PPVAR_SYS_P, VSYS_N to PPVAR_SYS_N 4. VSYS_SMPS to PP5000_SMPS 5. VSYS_V* to PP5000_V*
7/25	19	Remove note "reserved to enable PP1800_EMMC for developing only"
7/25	2	Please update the i2c table for jacuzzi and add ec i2c block diagram
7/25	25	Swap polarity of VBAT_IN_N/VBAT_IN_P on R90819
7/25	19	DNS R91208, since driver is not using LID_ACCEL_INT_ODL
7/25	26	Change R90668 to 0603 package
7/30	7,16	VDDIO_MIPIBRDG_EN -> EN_PP3300_MIPIBRDG_DX
7/30	34	Change USB-C MUX from IT5205 to IT5204 for cost benefit
7/30	19	Change R90880 to 100kOhm to save power when write protection is off
8/8	28	Reconnect EC_KSO2_INV to IT8801 pin KSO20 via a 0ohm
8/8	13	Add note for DA7219: THE TWO SENSE SIGNALS NEED TO BE CLOSE TO THE JACK CONNECTOR ROUTE HP_RING2 AND HP_RING2_SENSE TOGETHER (TREAT AS DIFF PAIR EXCEPT NO NEED FOR IMPEDANCE CONTROL) THE SAME APPLIES TO HP SLEEVE AND HP SLEEVE SENSE SIGNALS ROUTE HP_RING2, HP_RING2_SENSE, HP_SLEEVE, HP_SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

Data	Page	Item
8/13	4	Update power tree
8/13	28	[OEM] Add keyboard backlight circuit
8/13	28	[OEM] Reserve CON9105 Keyboard connector for 15"
8/13	31	[OEM] Change to sub board connector to 20pin
8/13	12,31	[OEM] Move USBA connector to sub board
8/13	16	[OEM] Remove 2nd DMIC
8/13	7,16	[OEM] Change PS8640QFN56GTR2-A0 to ANX7625BN-AC-R ; Rename PP1200_MIPIBRDG_EN to PP1000_MIPIBRDG_EN ; R219 change to 147Kohm ; Add U6579 for ANX7625 1.8V
8/15	33	Change R91181 from 0 ohm to 1k ohm.
8/15	29	[OEM] Change ESD protect for cost benefit : Change U2,U3 from RCLAMP0524PATCT to AZ1045-04F.R7G ; Change D1 from RCLAMP0502BATCT to AZ4024-01F.R7GR Change ESD7105,ESD7106 from ESD73031N-2/TR to PESD5V0X2UM ; Change ESD7102 from AZ4520-01F.R7G to PE3620M1Q
8/15	32	[OEM] Reserve GMR circuit
8/20	19	Connect EC_PROCHOT_ODL to EC pin PC13, not PC14
8/20	2	Update block diagram and I2C table accordingly
8/20	29	Add a 1MOhm pull-down on USB_C0_DISCHARGE, to avoid being floating
8/20	19,25	Separate battery's SCL/SDA from EC_I2C2 bus:(a) BATT_SDA to EC pin PC4 (b) BATT_SCL to EC pin PA5 (c) 4.7kOhm pull-up resistors are required
8/20	25	Move R91200 to make sure PPVAR_SYS power consumption is readable via INA, in battery-only condition
8/20	19	Change R90880 back to 2.2k ohm. (refer to the comment of #14)
8/20	25,29	About PPVAR_USB_C0_VBUS, please reserve the following circuitry for experiment.
8/20	31	Add a 1kOhm series res from J17.16 to LID_OPEN
8/22	16	Add 0 ohm NC connects Q708 pin 1 to Q709 pin1. Add 0 ohm NC connects to Q707 pin1 to Q710 pin1
8/22	16, 24	Reserve U2001 XO_CEL pin 0 ohm NC connects to ANX7625 XTAL_OUT(C1 pin)
8/22	16	Add a 0ohm on ANX7625_XTAL_IN in case XTAL drive level needs to be tuned
8/22	16	ANX7625_INT_L -> MIPIBRDG_INT_ODL
8/22	8	Connect MIPIBRDG_INT_ODL to AP pin AC3
8/22	16	Pull-up R91238 to PP1800_AP instead of PP1800_MIPIBRDG_D
8/22	16	[Netname] (a) J15.13: PP3300_CAM (b) PP1800_MIPIBRDG_EN -> EN_PP1800_MIPIBRDG
8/22	7,16	Connect EN_PP1800_MIPIBRDG_DX to AP pin AE25 (GPIO36)
8/22	16	Reserve 0ohms bypassing Q708/Q709 and Q707/Q710
8/22	16	Reserve a testpoint on ANX7625 CABLE_DET for debug usage
8/22	16,21	Reserve power path from VCAMIO_PMU to PP1800_MIPIBRDG
8/22	16	Move C10525 to PP3300_EDP_DX, close to eDP connector
8/22	16	Fix note of R252: "TODO: VALIDATION OF SHARING POWER BETWEEN BRIDGE AND EDP PANEL"
8/22	16,21	Reserve power path from VMCH_PMU to PP3300_MIPIBRDG_DX
8/27	32	Add note to GMR sensor: "DNS IF GMR IS ON SUB-BOARD"
8/27	4,26	Change U6570 to RT6256C and U6571 to RT6256B to improve power consumptoin. Update power tree
8/27	28	[OEM] Remove keyboard backlight circuit
8/27	34	Change ac coupling capacitors to follow it6505fn_v35_20190722.pdf (need to verifiy on proto board)
8/29	19,26,30,32 35	[For G3 power consumption] (a) Add LDO for powering PP1800_EC and PP1800_H1, input from PP3300_ALW. Netname PP1800_LDO (c) Change R90987 to 100kOhm, and reconnect U6554 EN pin to PP3300_SERVO_INA with R90987 (d) Change R91148 to 1MOhm (e) Reconnect PP1800_ALW_PG to PP1800_H1_PG (f) Modify H1_RST_ODL circuit as shown in note (g) Change R91196 to 100kOhm, still DNS'd (h) Add control circuit from EC PA14 via a 0ohm to U6569 EN, a mosfet inverter is needed as EC cannot take PPVAR_SYS voltage. Netname EN_PP1800_S5_L
8/29	25	Add a PMOS back-to-back with Q789 to avoid negative power source going into ISL9238C ADP pin, whose AMR minimux is -0.3V
8/29	26	Add a 0 ohm between EC PA14 and EN_PP1800_S5_L. Populate this resistor by default.
8/29	26	Reserve 1M ohm (DNS by default) between LDO3_VOUT and the EN pin of RT6256CGQUF.
8/29	19	Add a 499k ohm between LID_OPEN and PP1800_EC. (To allow system bootup without GMR)
8/29	8	Please reserve a serial 0Ohm on MIPIBRDG_INT_ODL.
8/29	34	[ITE suggestion] (a) DP_AUX_N reserve P/D 300K ohm (b) Change C10652,C10653 to 0.68uF (c) Add 100K P/D between IT5204 CTX/CRX and AC caps (d) Add serial 0ohm on USB_C0_SBU1_MUX/USB_C0_SBU2_MUX (e) Add serial 22ohm on EC_I2C_USB_C0_MUX_SCL/SDA
8/30	19,29,30	Some PP1800_ALW should be changed to PP1800_LDO or PP1800_EC - Q739A.5 (PP1800_EC) - R619 (PP1800_EC) - R338 (PP1800_EC)
8/30	8	Nit: remove note for MDSI_TE "NEAR CON9102"
8/30	29	For better ESD protectoin and filtering, move ESD7102, C518, and C10637 to be closet to USB-C connector.
9/2	19	Stuff R90868
9/10	19	Change BOARD REV ID from 0 to 1
11/4	25	Having 0 ohm to bypass Q801 for cost saving, since it's for reverse plugging protection
11/4	19	It's better to add and populate 0 ohm by default between. - EC_I2C2_3V3_SCL and BATT_SCL_3V3, - EC_I2C2_3V3_SDA and BATT_SDA_3V3
11/4	34	Please refer to it6505fn_v36_20190903.pdf (Add R91298)
11/4	21	Add a 0 ohm (populate by default) between DVDD18_IO (U2001.L9) and VIO18_MT6358 and de-populate R90656.
11/4	33	Change R91181 (LID_OPEN) back to 0 ohm
11/4	12	Please add resistor of 0 ohm on USB2_DM and USB2_DP. (For USB SI measurement)
11/4	12	Change R90741 from 680 ohm to 619 ohm for USB2.0 S/I
11/4	2	Update EC I2C MAP for bigbang
11/4	29	Netname nit: BC12_POGO_ADDR -> BC12_C0_ADDR, BC12_POGO_EN_L -> BC12_C0_EN_L
11/7	19,25	Change ISL9238CHRTZ-T's I2C to EC_I2C2_3V3_SDA from BATT_SDA_3V3 ; to EC_I2C2_3V3_SCL from BATT_SCL_3V3

Data	Page	Item
11/19	19	Reserve a pull-up resistor (499k ohm) to PP3300_ALW on LID_OPEN
11/19	19	Change R90880 from 2.2k ohm to 10k ohm. (Double confirm EEPROM_WP_OD sitll works well)
11/20	19	Change EC Board_ID to "2"
11/21	25	PQ1 and PQ2 need to change the part with higher Vgs support. (CSD87330Q3D)
11/21	19	Change Q750 from nFET to pFET.
11/21	19,26,30	To ensure EC, H1 and hardware battery-off workable when U6571 is latched off due to OCP or OVP
11/21	19	deppop R91279 and populate R91302. (for LID_OPEN)
11/26	25	Change R293 to 1M ohm (from 100k ohm) and R91183 to 10k ohm (from 0 ohm)
11/27	28	R91161,R91162,R91163 should not be 0 ohm. Please change their value according to their brightness.
11/27	13	Delete R90775, move MIC_P net name to R90781 pin2. Make the routing, MIC_P/EAR_JACK_GND as differential pair. EAR_MIC_P/EAR_MIC_N as differential pair. AU_VIN1_P/AU_VIN1_N as differential pair.
11/27	16	Change R9499 and R91112 to 2.2K ohm for I2C rising time
11/28	25	Change R405 to 93.1K ohm for 2CELL battery
12/9	26	Please depop R91265 and R91266 and populate - R91281 (100k ohm) and R91270 (80.6 kohm) for 5V - R91276 (0 ohm) and R91275 (100 kohm) for 3V.
12/9	28	DNS R90859 & R91121, stuff R91143 & R90858 for keyboard lock button
1/15	4	Update Jacuzzi power tree - 20191216
1/15	1	Update Jacuzzi block diagram - 20191216
1/15	30	Reserve a NFET to protect H1 USB interface
1/15	30	Change some of ISL9238C_LDO_5V to LDO5_VOUT according to charger vendor's recommendation.
1/15	17	Reserve a 100pF shut capacitor (C10647) on BT_EN_3V3 according to U69H025.21 datasheet
1/22	19	Add HW thermal protect circuit.
2/7	25	PPVAR_SYS_R reserve 3*22uF/25V/0805 MLCC, PPVAR_SYS reserve 22uF/25V/0805 MLCC
2/7	29	Add TVS AZ4024-01F.R7GR on USB_C0_CC1/USB_C0_CC2
2/7	19	Change BOARD REV ID from 2 (evt) to 3 for (dvt)
2/7	30	Stuff Q807 and Q808. DNS R91311 and R91313
3/6	28	DNS R91145 (To improve power consumption in G3 state about 1mW)
3/6	16,24	Change C10671,C10605,C10606 to 15pF, C10672 to 12pF for X'tal vendor measured result.
4/8	28,30	Reserve the path from H1's DIOR2 to KSI3 and H1's DIRO8 to EC_KSI3 to support the keyboard with refresh button on F2 location.
4/8	25	Change the power to U6577's VIN from PPVAR_PWR_IN to PP5000_ALW.
4/8	16	Change R91132(TOUCH_RST_3V3_ODL) from 10k ohm to 100k ohm to improve 1mW in S3 mode
4/8	30	1. Change the power rail to nnn from ISL9238C_LDO_5V to PP3300_H1 2. DNS R91316 and populate R91315 3. Change the power rail to R91312 from PP5000_ALW to PP3300_H1 4. Change R91312 from 100k ohm to 0 ohm
4/8	29	Reserve a 499 kohm (DNS) pull-down resistor on Q782.G/Q781.G for volate division on EC_CCD_MODE_ODL to protect IT5204 and keep normal operation.
4/8	12	Check the OVCUR1#~4# setting right. 1. add a pull-up resistor on OVCUR1# because type-C port is removable. 2. reserve a pull-down resistor on OVCUR4# because it might be no used for non-WFC sku.
4/8	35	DNS INA component
4/8	28	Reserve PP5000_ALW for LED
4/15	29	Add another path of TPD2S300 between FUSB302BUCX and Type-C Connector to protect TPD2S300 cc pins when VBUS short to cc pins unexpectedly.
4/15	26	Add a 100k ohm from LDO3_VOUT to U6569.EN and DNS R91148. (The AMR of EN pin is 6V)
4/15	30	Change power rail of R91088 from ISL9238C_LDO_5V to PP3300_H1
4/24	19	Change BOARD REV ID from 3 (dvt) to 4 for (pvt)
4/24	26	Reserve a 0.1uF capacitor on PU1.EN in case soft-start is required.
4/24	12	Change U6552 form RT9742QGJ5 (0.5A) to RT9742GGJ5 (1A) for meet OEM USB 1 port min. 1A requirement
4/30	24	Follow Xtal measured result to change C10605,C10606 to 8.2pF
5/6	13	U6504 DA7219-02VBA DNS
5/6	28	LED limit resistor change: Blue (Green) to 150ohm, Amber to 619ohm
5/6	25	Follow vendor suggestion to add CAP. Mount C10712 ,C10713, C10714, C10715 22uF. Mount C10496 0.22U. Change C10453 from 0.022uF to 0.015uF
5/8	8	Mount H1_INT_OD_L external PU resistor R90560, change 10K ohm.

Quanta Computer Inc.

PROJECT : ZDE

Size	Document Number	Rev
	39_Change_Notice	1A

Date: Friday, May 08, 2020 Sheet 39 of 39