0RC

TABLE OF CONTENTS

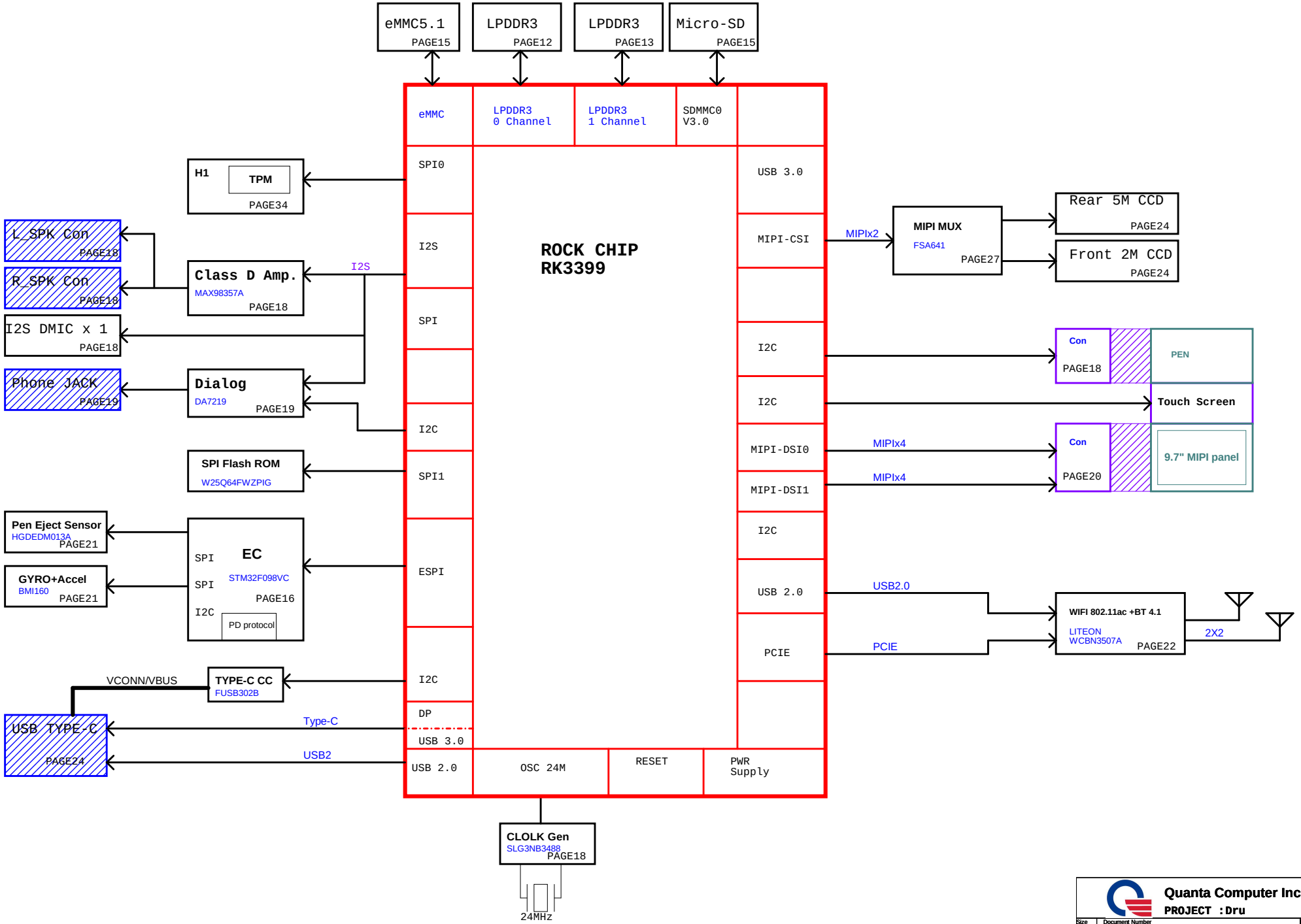
SHEET NO.	SHEET NAME
1	TABLE OF CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER TREE
4	RESET MAP
5	I2C MAP
6	SOC MEMORY
7	SOC HIGH SPEED BUSES
8	SOC GPIO 1
9	SOC GPIO 2
10	SOC CORE POWER
11	SOC MISC POWER
12	SOC GND
13	LPDDR
14	LPDDR DECOUPLING
15	eMMC / SD
16	EC-STM32
17	H1
18	SERVO
19	SPI ROM / BUTTONS / LEDS
20	AUDIO
21	PANEL / ALS / CAMERAS
22	CLOCK / SENSORS / EXPANSION
23	WIFI / BT
24	USB-C
25	POWER - BATTERY CHARGER
26	POWER - SYSTEM RAILS
27	POWER - CORE RAILS
28	POWER - SWITCHES AND LDOS

MODIFY HISTORY

20170823
First Release.

20170926
EVT schematic final.

SYSTEM BLOCK DIAGRAM



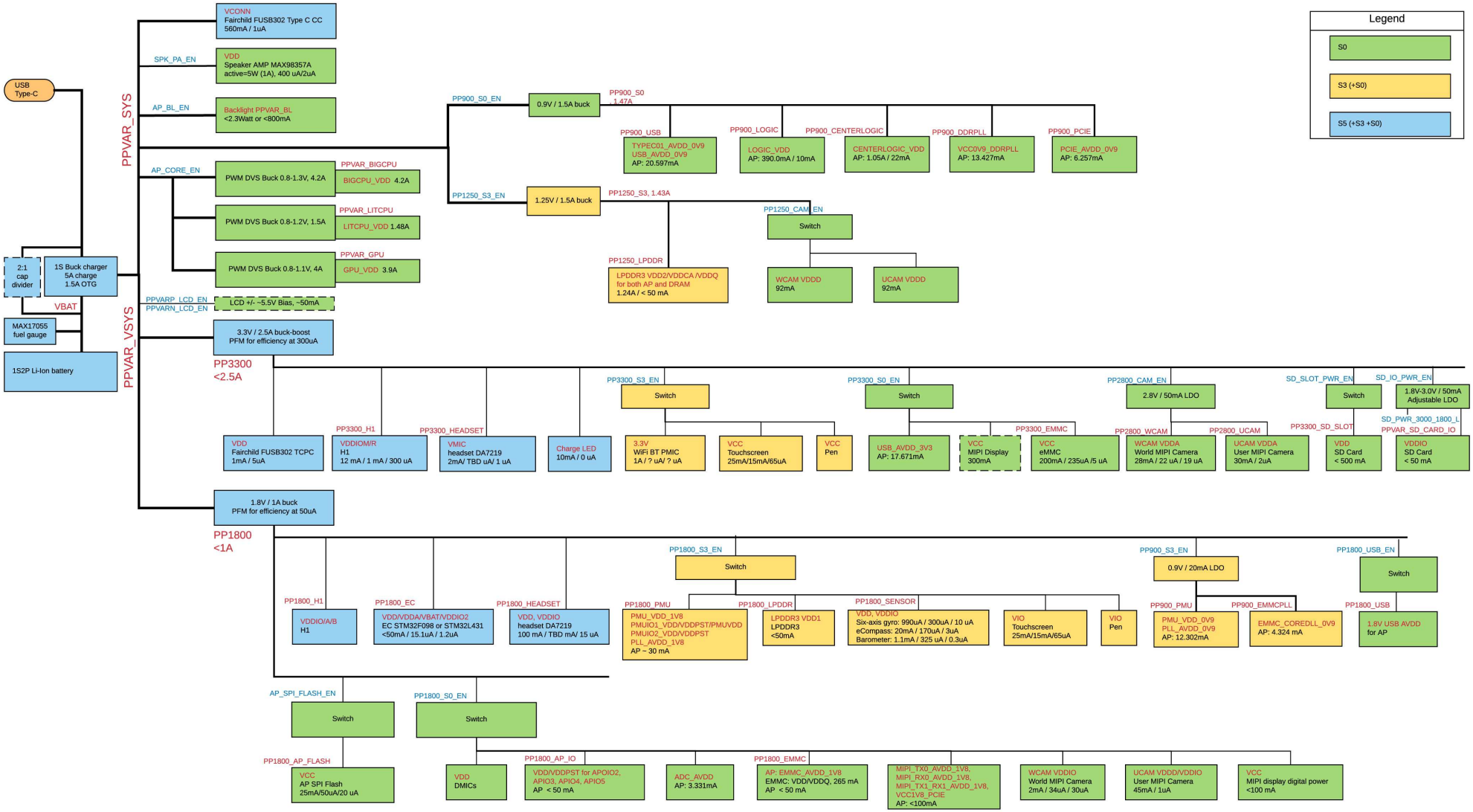
Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	SYSTEM BLOCK DIAGRAM	1A

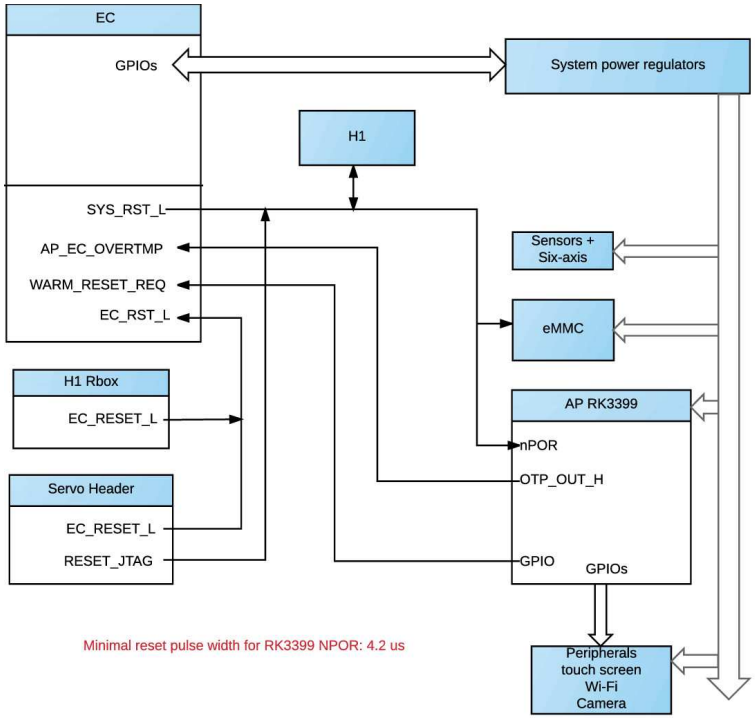
Date: Tuesday, February 06, 2018 Sheet 2 of 28

POWER TREE

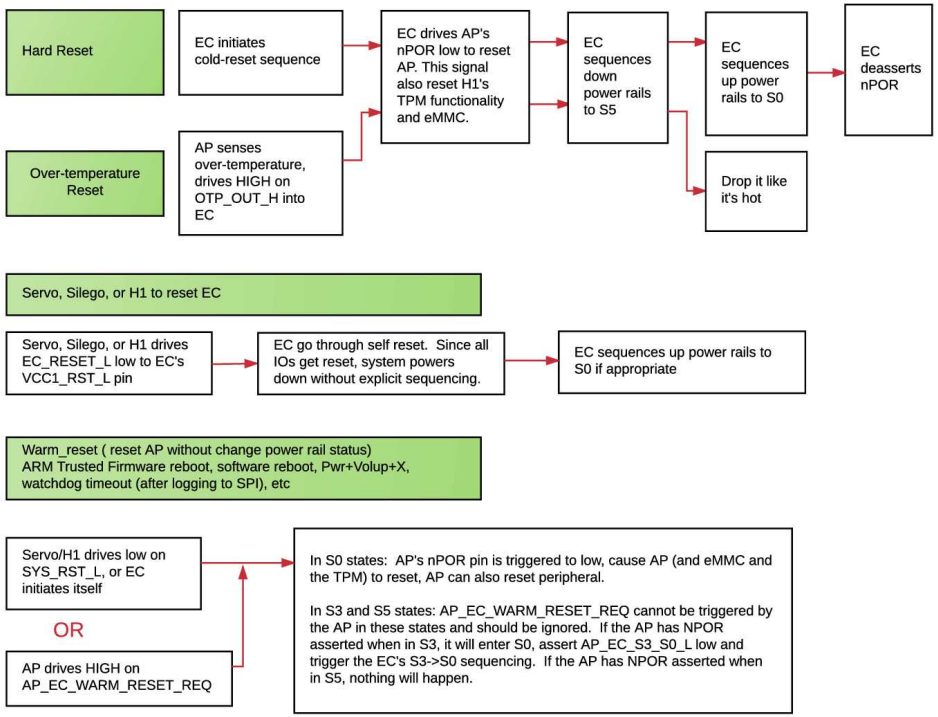


Quanta Computer Inc.
PROJECT : Dru
POWER TREE

RESET MAP



Minimal reset pulse width for RK3399 NPOR: 4.2 us

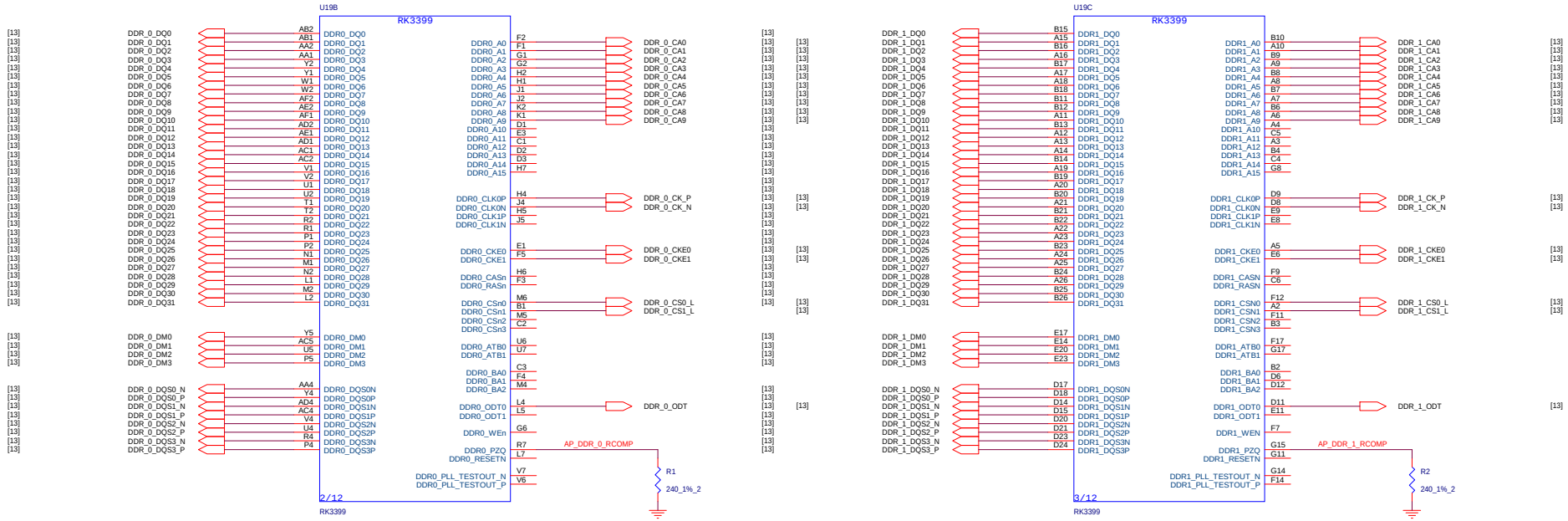


I2C MAP

Master	Port	Doc reference(Pin name)	Voltage Domain	Bus Name	Bus Speed	Slave Device	8-bit Addr	Note
AP-RK3399	I2c1	GPIO4_A2/I2C1_SCL,GPIO4_A1/I2C1_SDA	VCCA18_CODEC	AP_I2C_EXPANSION	400KHz	(TBD)		Expansion port
	I2c2	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL, GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA	VCC18_IO	AP_I2C_PEN	400KHz	V9013	0x12	Pen
	I2c3	GPIO4_C1/I2C3_SCL/UART2B_TX, GPIO4_C0/I2C3_SDA/UART2B_RX	VCC18_IO	AP_I2C_TS(Touch screen)	400KHz	eKTH3900	0x20	Touch Panel
	I2c7	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL, GPIO2_A7/VOP_D7_CIF_D7/I2C7_SDA	VCC18_IO	AP_I2C_CAM	400KHz	(TBD)	R:0x6C W:0x6D	User Camera
						(TBD)	R:0x78 W:0x79	World Camera
	I2c8	GPIO1_C5/I2C8_SCL,GPIO01_C4/I2C8_SDA	VCC18_PMU	AP_I2C_AUDIO	400KHz	Dialog DA7219	0x34	Audio Jack

Master	Port	Doc reference(Pin name)	Voltage Domain	Bus Name	Bus Speed	Slave Device	8-bit Addr	Note
STM32F098VCH6	I2c2	PB10, PB11	PP1800_EC	EC_I2C_USB_CO_PD_1V8	1MHZ	FUSB302B	0x44	USB-C TCPC
	I2c1	PB6, PB7	TBD	EC_I2C_EXPANSION_1V8	400KHz	(TBD)		Expansion port
	I2c1	PB8, PB9	PP1800_EC	EC_I2C_CHARGER_BATTERY_1V8	400KHz	MAX17055	0x6C	Fuel Gauge
						RT9467	0xB6	Buck Charger

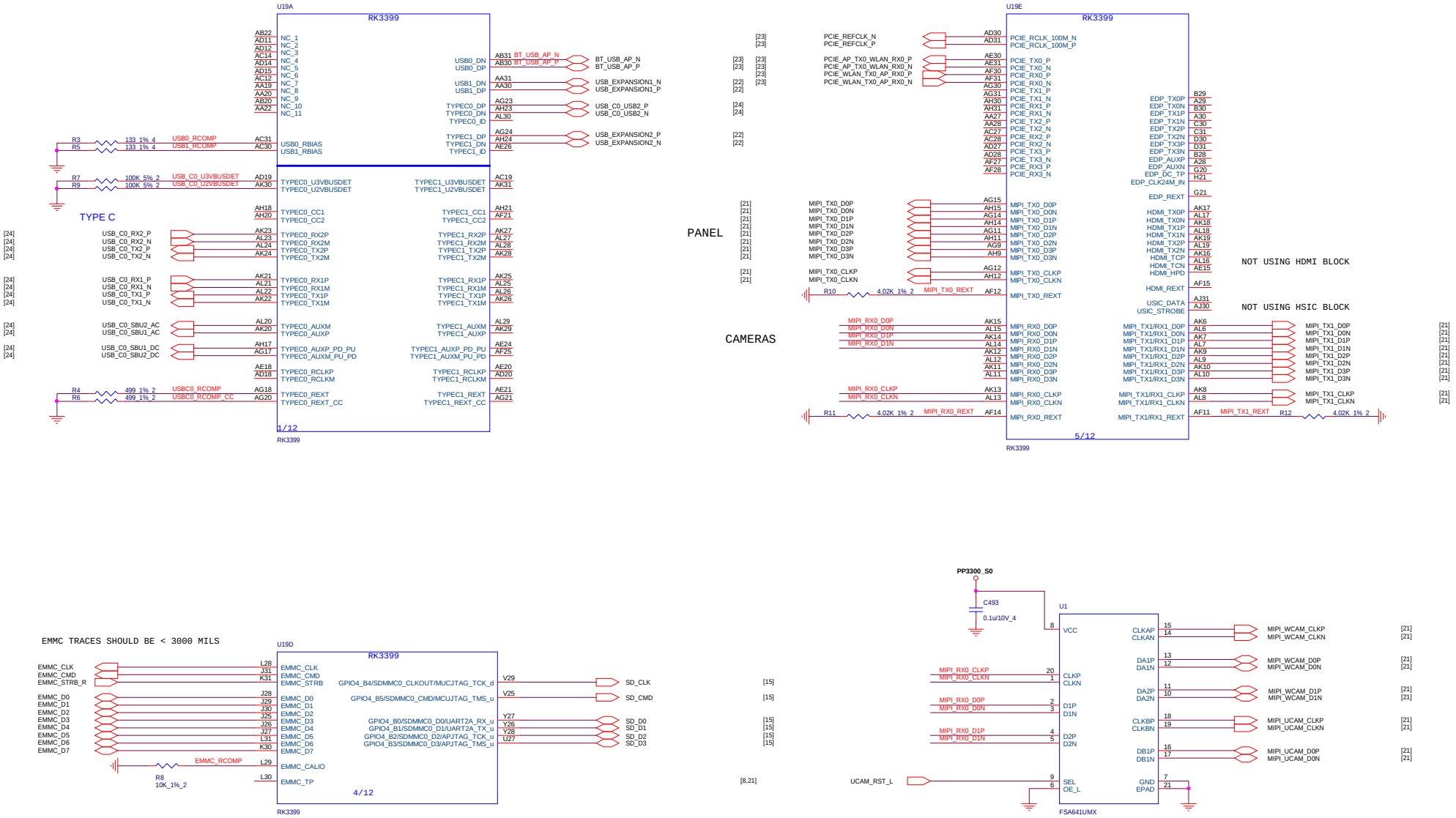
LAYOUT NOTE:
CAN'T SWAP BYTE OR CLUSTER
BITS WITHIN THE BYTE CAN BE SWAPPED



Quanta Computer Inc.
PROJECT : Dru

Size	Document Number	Rev
	SOC MEMORY	1A

Date: Tuesday, February 06, 2018 Sheet 6 of 28

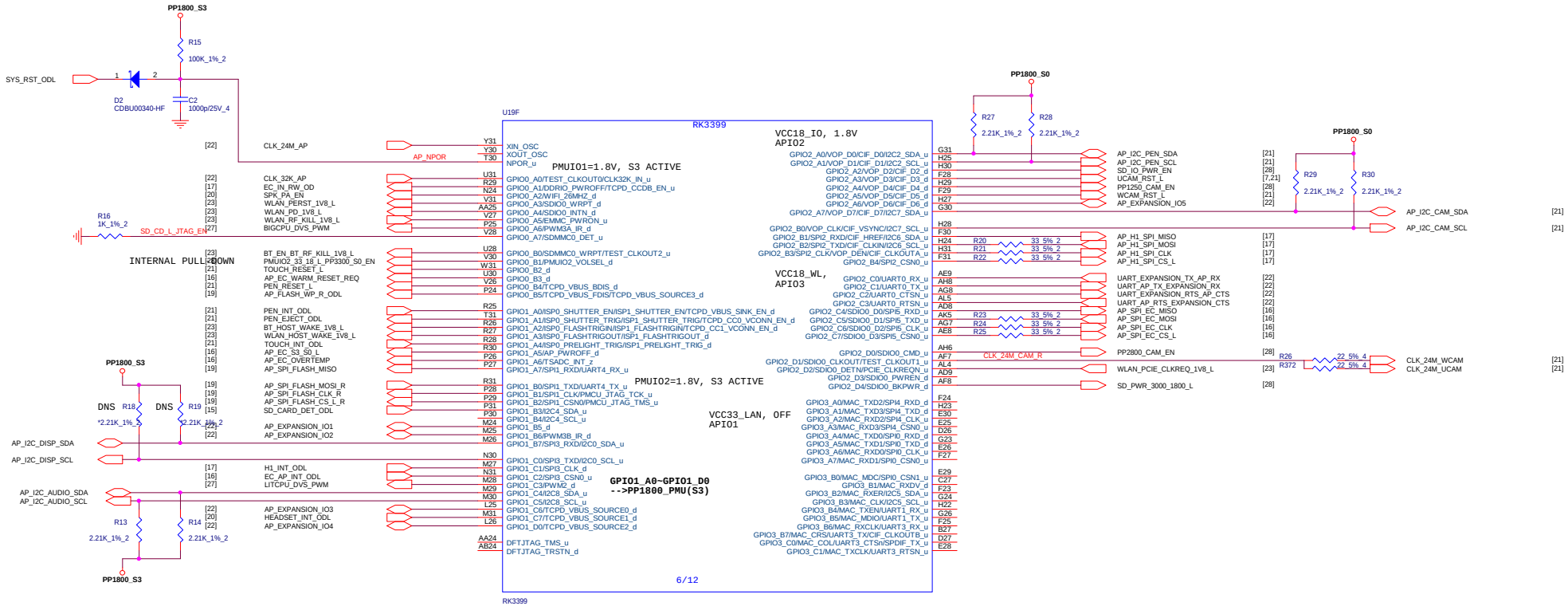


Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	SOC HIGH SPEED BUSES	1A

Date: Tuesday, February 06, 2018 Sheet 7 of 28

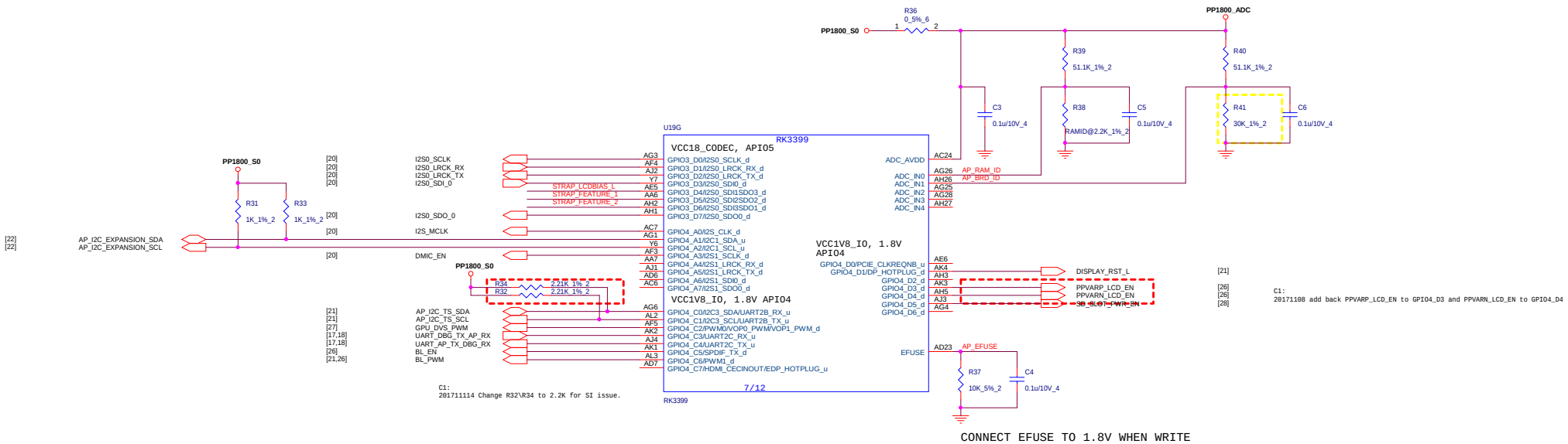


Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	SOC GPIO 1	1A

Date: Tuesday, February 06, 2018 Sheet 8 of 28

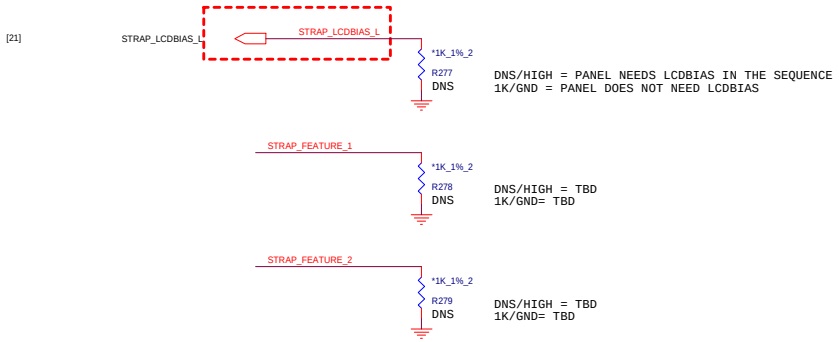


CONNECT EFUSE TO 1.8V WHEN WRITE

R277 notice:

inx: need to deal with strapping resistor R277. In order of preference:
A) If PPVARP_LCD and PPVARN_LCD are connected to
pins that are NC on K&D, just no-stuff R277 because it's
safe to apply the voltage with either panel connected
B) If PPVARP_LCD/PPVARN_LCD cannot be safely
enabled when attached to K&D, take a pin that is NC on
the K&D pinout and make it GND on the INX pinout;
connect that to STRAP_LCDBIAS_L (and keep R277
stuffed)
C) No-stuff R277, and we'll have to make sure that the
resistor matches the currently attached panel

c1 20171116 For INX flex to GND pin.



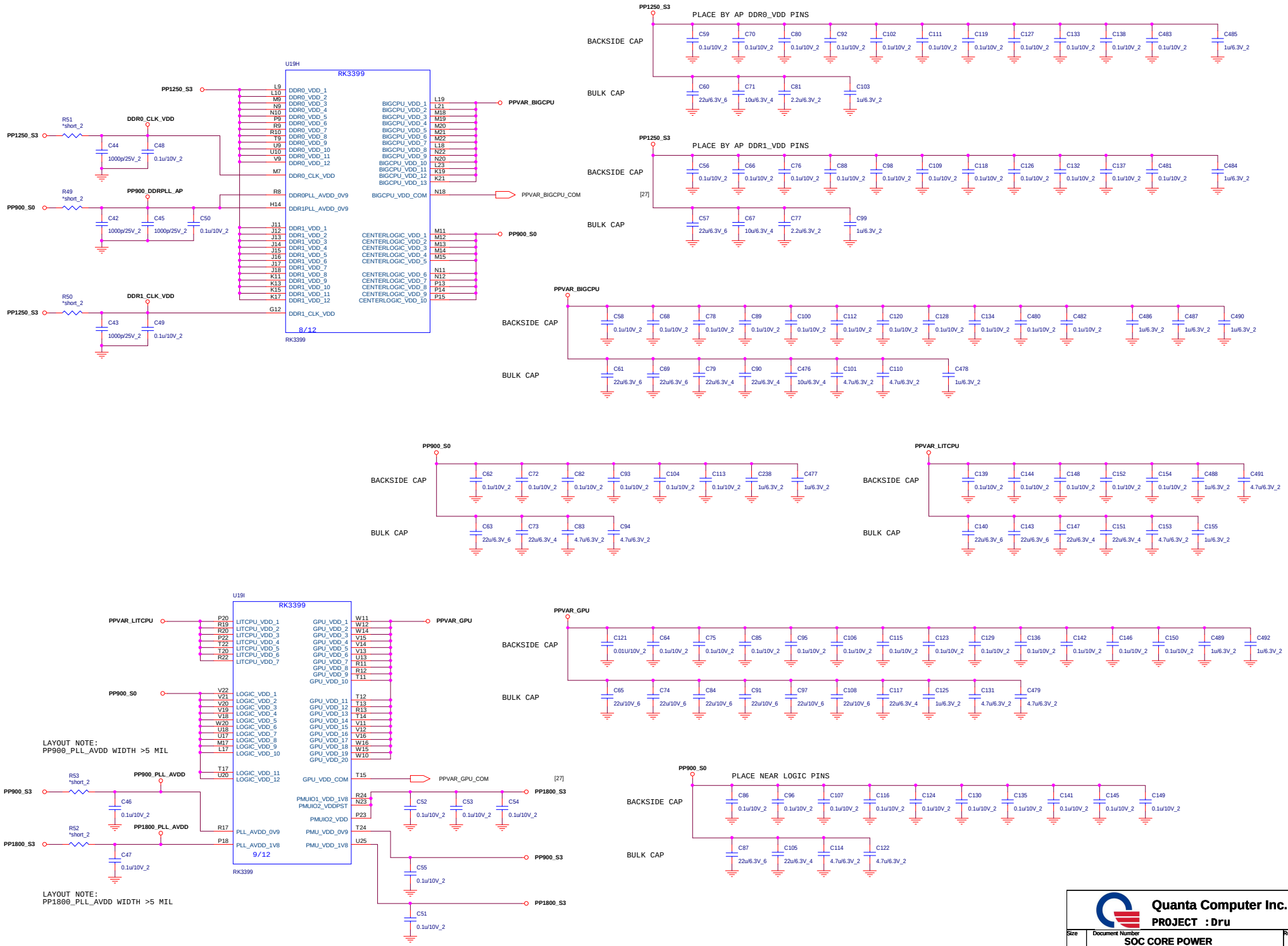
R40	VALUE	R41	VALUE	VOLTAGE	BUILD
51.1	KOHM	2.2	KOHM	0.074V	PROTO1
51.1	KOHM	6.8	KOHM	0.211V	PROTO2
51.1	KOHM	11	KOHM	0.319V	EVT
57.6	KOHM	**18**	KOHM	0.427V	**EVT2**
51.1	KOHM	22	KOHM	0.542V	**DVT**
51.1	KOHM	30	KOHM	0.666V	**DVT3**
51.1	KOHM	39.2	KOHM	0.78V	BUILD7
56	KOHM	56	KOHM	0.9V	BUILD8
47	KOHM	61.9	KOHM	1.023V	BUILD9
47	KOHM	80.6	KOHM	1.137V	BUILD10
56	KOHM	124	KOHM	1.240V	BUILD11
51.1	KOHM	150	KOHM	13.43	BUILD12
47	KOHM	200	KOHM	1.457V	BUILD13
47	KOHM	330	KOHM	1.576V	BUILD14
47	KOHM	680	KOHM	1.684V	BUILD15
56	KOHM	NC	KOHM	1.8V	BUILD16

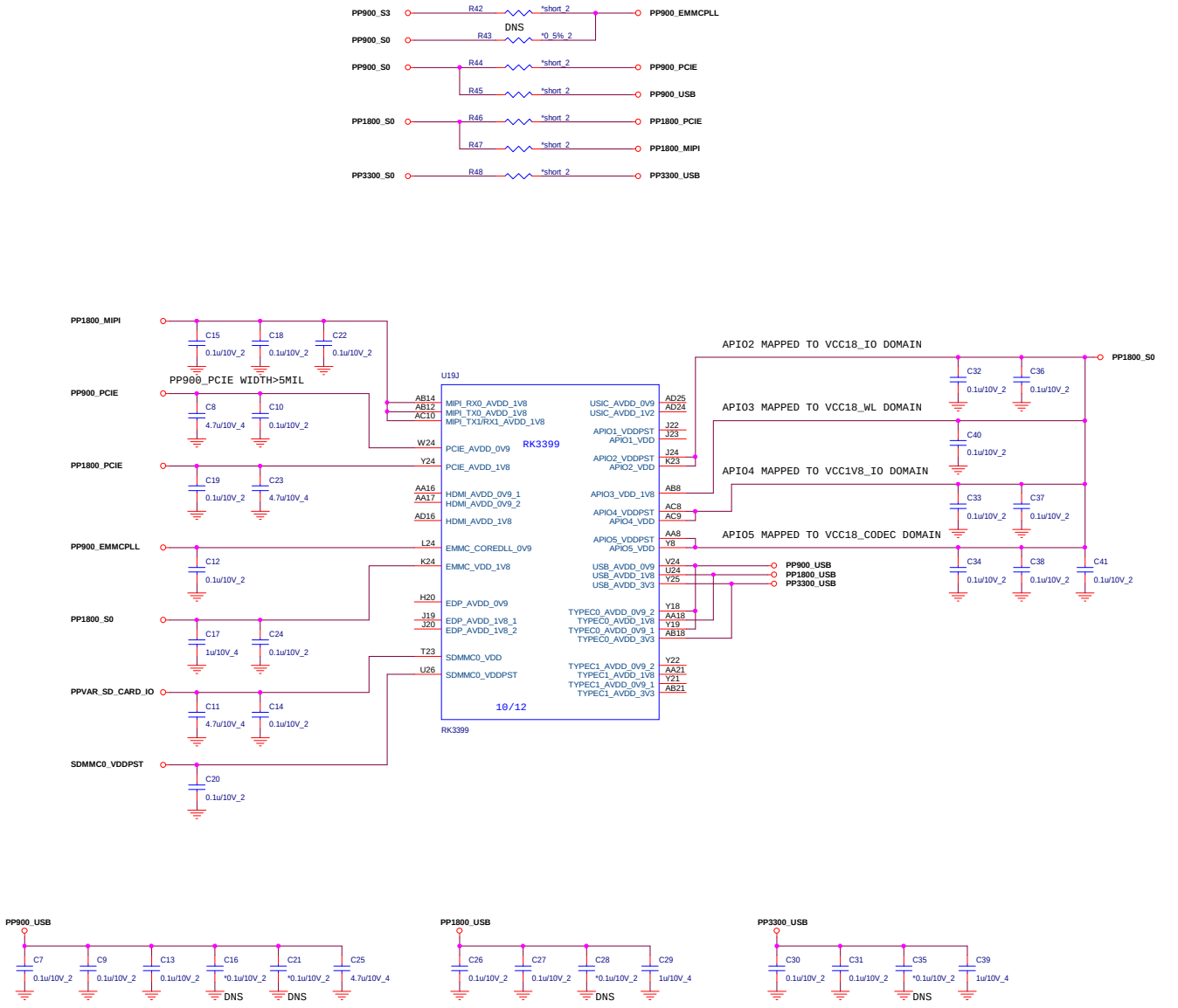
R38	VALUE	VOLTAGE	RAM
2.2	KOHM	0.074V	Samsung 2GB DDP LPDDR3
6.8	KOHM	0.211V	Hynix 2GB DDP LPDDR3
39.2	KOHM	0.78V	Micron 2GB DDP LPDDR3

Quanta Computer Inc.
PROJECT : Dru

Size	Document Number	Rev
	SOC GPIO 2	1A

Date: Tuesday, February 06, 2018 Sheet 9 of 28


U19H
RK3399
PP1250_S3
DDR0_CLK_VDD
DDR0PLL_AVDD_0V9
DDR1PLL_AVDD_0V9
DDR1_CLK_VDD
BIGCPU_VDD_COM
CENTERLOGIC_VDD_1
CENTERLOGIC_VDD_2
CENTERLOGIC_VDD_3
CENTERLOGIC_VDD_4
CENTERLOGIC_VDD_5
CENTERLOGIC_VDD_6
CENTERLOGIC_VDD_7
CENTERLOGIC_VDD_8
CENTERLOGIC_VDD_9
CENTERLOGIC_VDD_10
PPVAR_BIGCPU
PPVAR_BIGCPU_COM
PP900_S0
8/12
R51 *short_2
R49 *short_2
R50 *short_2
PP900_DDRPLL_AP
C44 1000p/25V_2
C48 0.1u/10V_2
C42 1000p/25V_2
C45 1000p/25V_2
C50 0.1u/10V_2
C43 1000p/25V_2
C49 0.1u/10V_2
PP1250_S3
PLACE BY AP DDR0_VDD PINS
BACKSIDE CAP
BULK CAP
C59 0.1u/10V_2
C70 0.1u/10V_2
C80 0.1u/10V_2
C92 0.1u/10V_2
C102 0.1u/10V_2
C111 0.1u/10V_2
C119 0.1u/10V_2
C127 0.1u/10V_2
C133 0.1u/10V_2
C138 0.1u/10V_2
C483 0.1u/10V_2
C485 1u/6.3V_2
C60 22u/6.3V_6
C71 10u/6.3V_4
C81 2.2u/6.3V_2
C103 1u/6.3V_2
PLACE BY AP DDR1_VDD PINS
[27]
C56 0.1u/10V_2
C66 0.1u/10V_2
C76 0.1u/10V_2
C88 0.1u/10V_2
C98 0.1u/10V_2
C109 0.1u/10V_2
C118 0.1u/10V_2
C126 0.1u/10V_2
C132 0.1u/10V_2
C137 0.1u/10V_2
C481 0.1u/10V_2
C484 1u/6.3V_2
C57 22u/6.3V_6
C67 10u/6.3V_4
C77 2.2u/6.3V_2
C99 1u/6.3V_2
PPVAR_BIGCPU
C58 0.1u/10V_2
C68 0.1u/10V_2
C78 0.1u/10V_2
C89 0.1u/10V_2
C100 0.1u/10V_2
C112 0.1u/10V_2
C120 0.1u/10V_2
C128 0.1u/10V_2
C134 0.1u/10V_2
C480 0.1u/10V_2
C482 0.1u/10V_2
C486 1u/6.3V_2
C487 1u/6.3V_2
C490 1u/6.3V_2
C61 22u/6.3V_6
C69 22u/6.3V_6
C79 22u/6.3V_4
C90 22u/6.3V_4
C476 10u/6.3V_4
C101 4.7u/6.3V_2
C110 4.7u/6.3V_2
C478 1u/6.3V_2
PP900_S0
C62 0.1u/10V_2
C72 0.1u/10V_2
C82 0.1u/10V_2
C93 0.1u/10V_2
C104 0.1u/10V_2
C113 0.1u/10V_2
C238 1u/6.3V_2
C477 1u/6.3V_2
C63 22u/6.3V_6
C73 22u/6.3V_4
C83 4.7u/6.3V_2
C94 4.7u/6.3V_2
PPVAR_LITCPU
C139 0.1u/10V_2
C144 0.1u/10V_2
C148 0.1u/10V_2
C152 0.1u/10V_2
C154 0.1u/10V_2
C488 1u/6.3V_2
C491 4.7u/6.3V_2
C140 22u/6.3V_6
C143 22u/6.3V_6
C147 22u/6.3V_4
C151 22u/6.3V_4
C153 4.7u/6.3V_2
C155 1u/6.3V_2
U19I
RK3399
PPVAR_LITCPU
PPVAR_GPU
PP900_S0
LITCPU_VDD_1
LITCPU_VDD_2
LITCPU_VDD_3
LITCPU_VDD_4
LITCPU_VDD_5
LITCPU_VDD_6
LITCPU_VDD_7
LOGIC_VDD_1
LOGIC_VDD_2
LOGIC_VDD_3
LOGIC_VDD_4
LOGIC_VDD_5
LOGIC_VDD_6
LOGIC_VDD_7
LOGIC_VDD_8
LOGIC_VDD_9
LOGIC_VDD_10
LOGIC_VDD_11
LOGIC_VDD_12
GPU_VDD_COM
PMUIO1_VDD_1V8
PMUIO2_VDDPST
PMUIO2_VDD
PMU_VDD_0V9
PMU_VDD_1V8
PLL_AVDD_0V9
PLL_AVDD_1V8
PPVAR_GPU_COM
PP1800_S3
PP900_S3
9/12
LAYOUT NOTE:
PP900_PLL_AVDD WIDTH >5 MIL
LAYOUT NOTE:
PP1800_PLL_AVDD WIDTH >5 MIL
R53 *short_2
R52 *short_2
PP900_PLL_AVDD
PP1800_PLL_AVDD
C46 0.1u/10V_2
C47 0.1u/10V_2
C52 0.1u/10V_2
C53 0.1u/10V_2
C54 0.1u/10V_2
C55 0.1u/10V_2
C51 0.1u/10V_2
PPVAR_GPU
C121 0.01U/10V_2
C64 0.1u/10V_2
C75 0.1u/10V_2
C85 0.1u/10V_2
C95 0.1u/10V_2
C106 0.1u/10V_2
C115 0.1u/10V_2
C123 0.1u/10V_2
C129 0.1u/10V_2
C136 0.1u/10V_2
C142 0.1u/10V_2
C146 0.1u/10V_2
C150 0.1u/10V_2
C489 1u/6.3V_2
C492 1u/6.3V_2
C65 22u/10V_6
C74 22u/10V_6
C84 22u/10V_6
C91 22u/10V_6
C97 22u/10V_6
C108 22u/10V_6
C117 22u/6.3V_4
C125 1u/6.3V_2
C131 4.7u/6.3V_2
C479 4.7u/6.3V_2
PLACE NEAR LOGIC PINS
C86 0.1u/10V_2
C96 0.1u/10V_2
C107 0.1u/10V_2
C116 0.1u/10V_2
C124 0.1u/10V_2
C130 0.1u/10V_2
C135 0.1u/10V_2
C141 0.1u/10V_2
C145 0.1u/10V_2
C149 0.1u/10V_2
C87 22u/6.3V_6
C105 22u/6.3V_4
C114 4.7u/6.3V_2
C122 4.7u/6.3V_2
Quanta Computer Inc.
PROJECT : Dru
Size
Document Number
SOC CORE POWER
Rev
1A
Date: Tuesday, February 06, 2018
Sheet 10 of 24



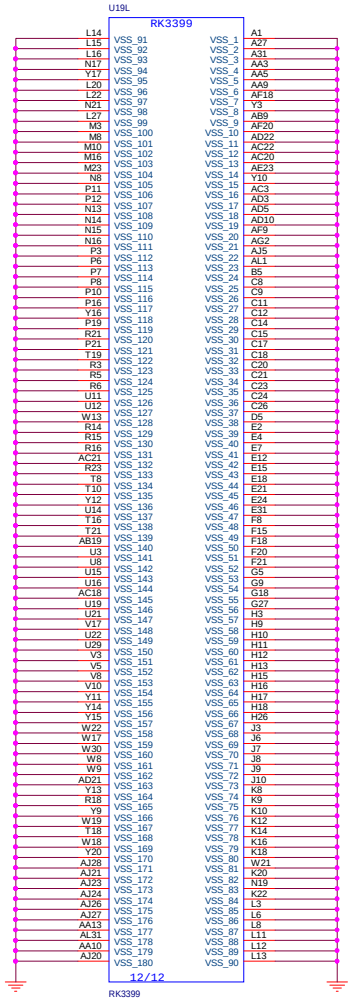
Quanta Computer Inc.

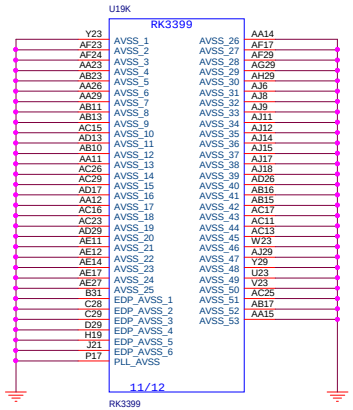
PROJECT : Dru

Size	Document Number	Rev
	SOC MISC POWER	1A

Date: Tuesday, February 06, 2018 Sheet 11 of 24

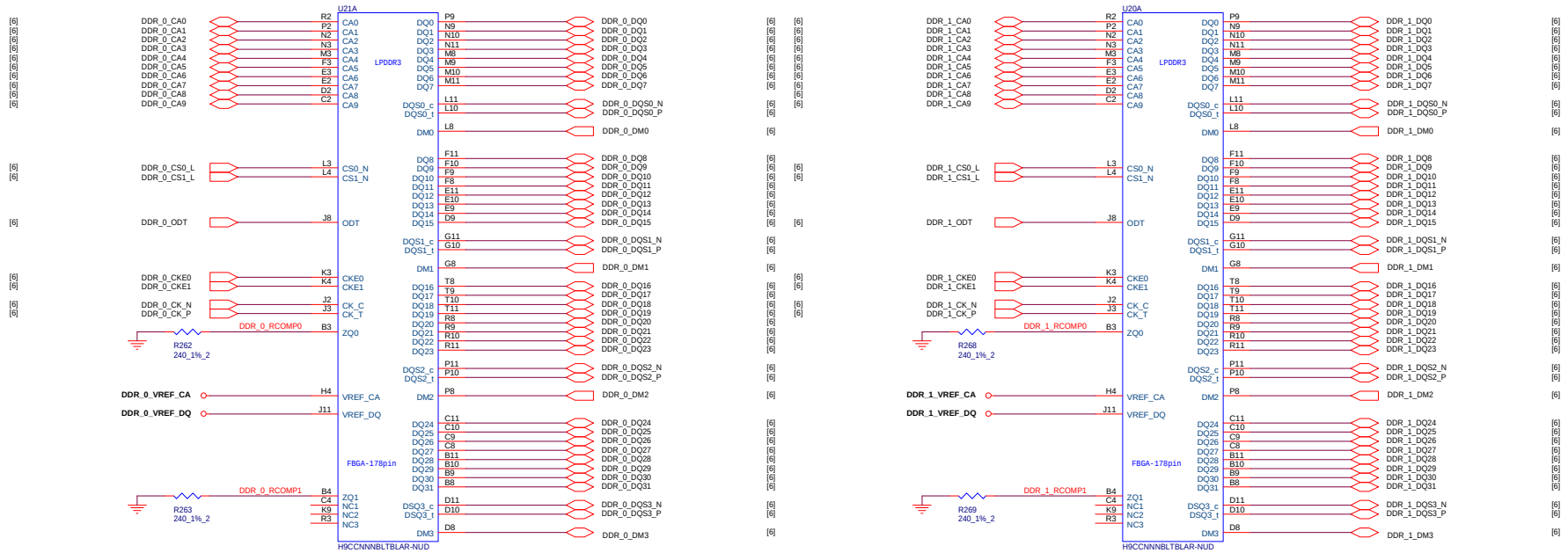
LAYOUT NOTE: CONNECT AVSS48 /PIN Y29 TO THE GND SIDE OF C1 ASSOCIATED WITH AP_XOUT.

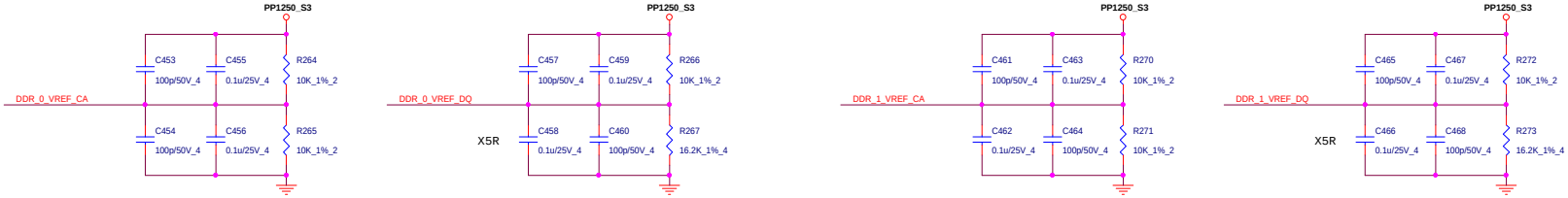




Quanta Computer Inc.		
PROJECT : Dru		
Size	Document Number: SOC GND	Rev: 1A
Date: Tuesday, February 06, 2018	Sheet 12 of 28	

NOTES:
BITS WITHIN THE BYTE CAN BE SWAPPED
CAN'T SWAP BYTE OR CLUSTER

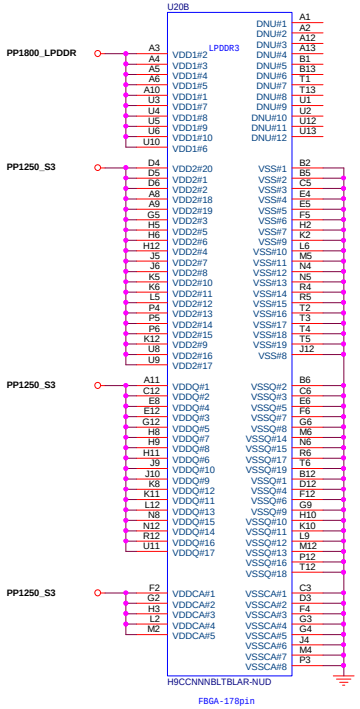


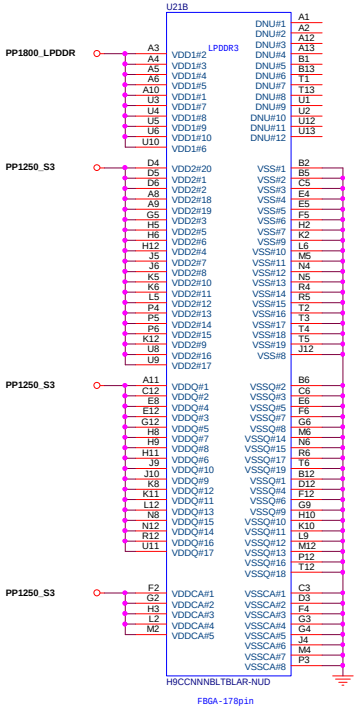


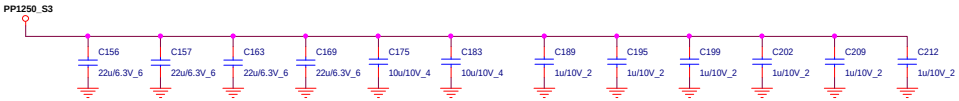
DEFAULT: VREF CA= 50% OF DDR IO VOLTAGE
VREF DQ IS SET AT 0.77V

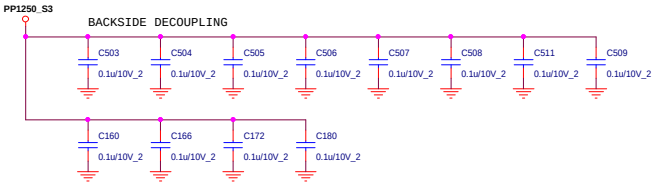
Quanta Computer Inc.		
PROJECT : Dru		
Size	Document Number: LPDDR	Rev 1A
Date: Tuesday, February 06, 2018	Sheet 13 of 28	

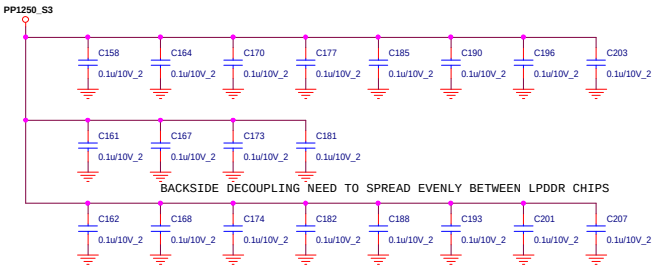
LPDDR IS SET AT 1.25V FOR DRAM PERFORMANCE

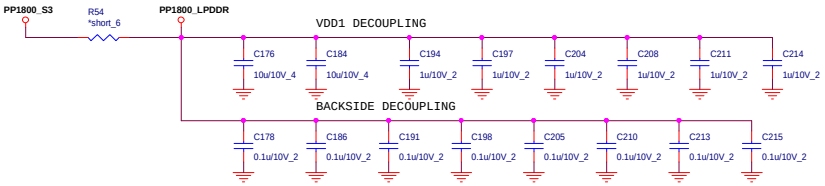












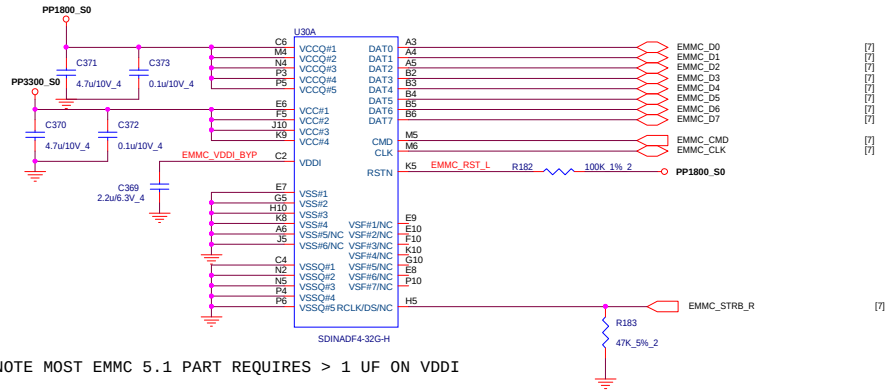
Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	LPDDR DECOUPLING	1A

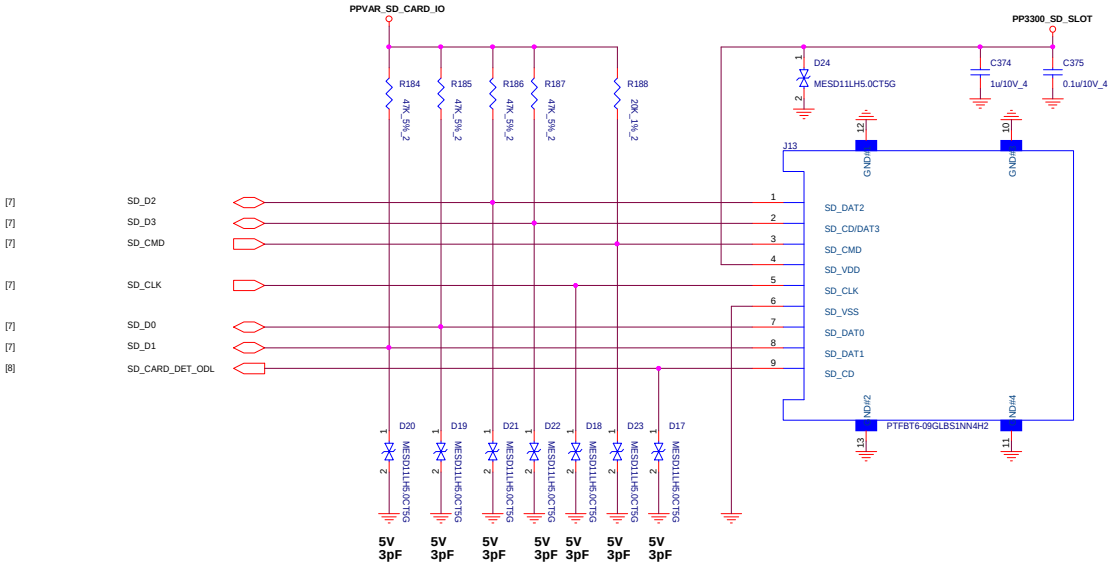
Date: Tuesday, February 06, 2018 Sheet 14 of 28

32 GB EMMC STORAGE

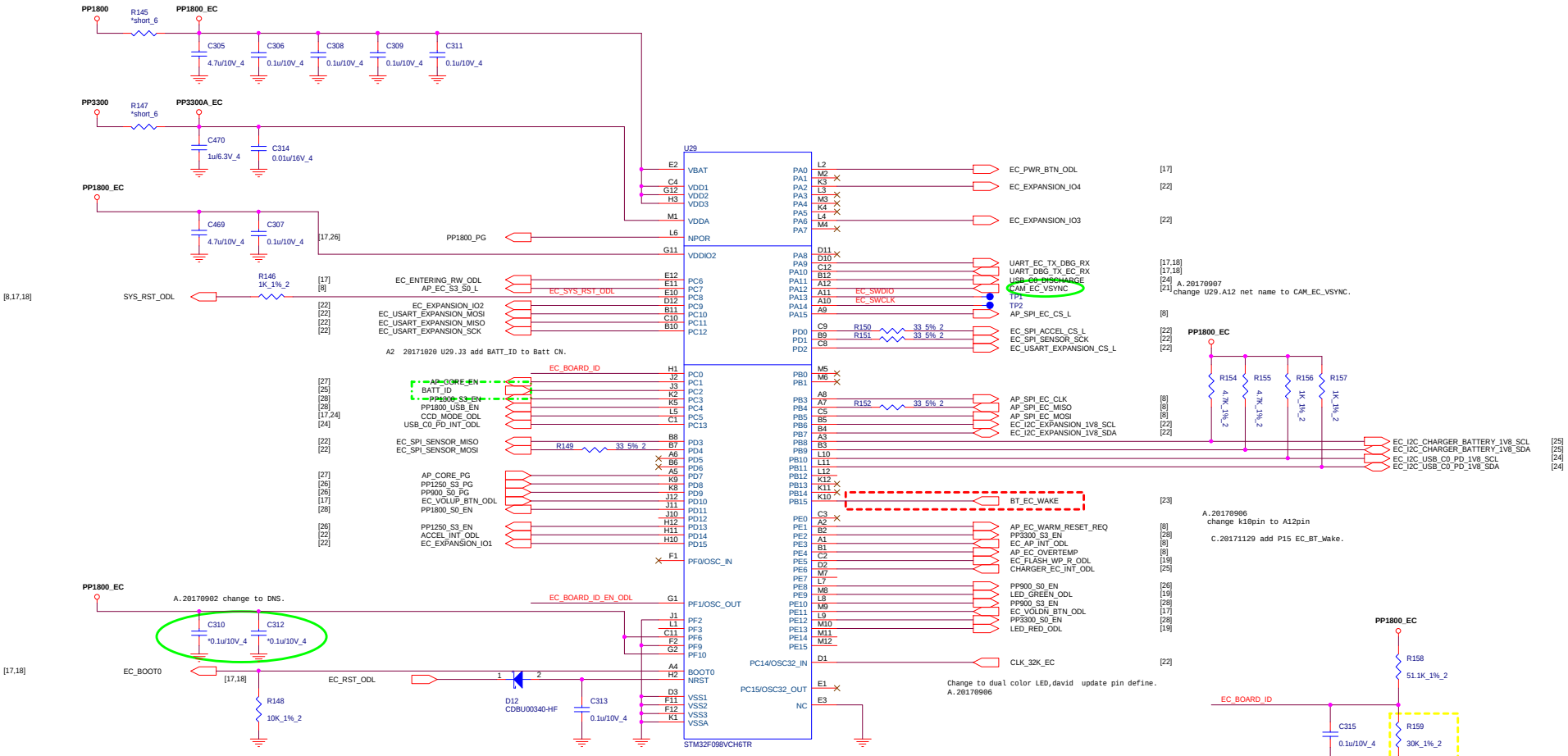


NOTE MOST EMMC 5.1 PART REQUIRES > 1 UF ON VDDI

0.5A MAX



Different w/SEL's ESD part.

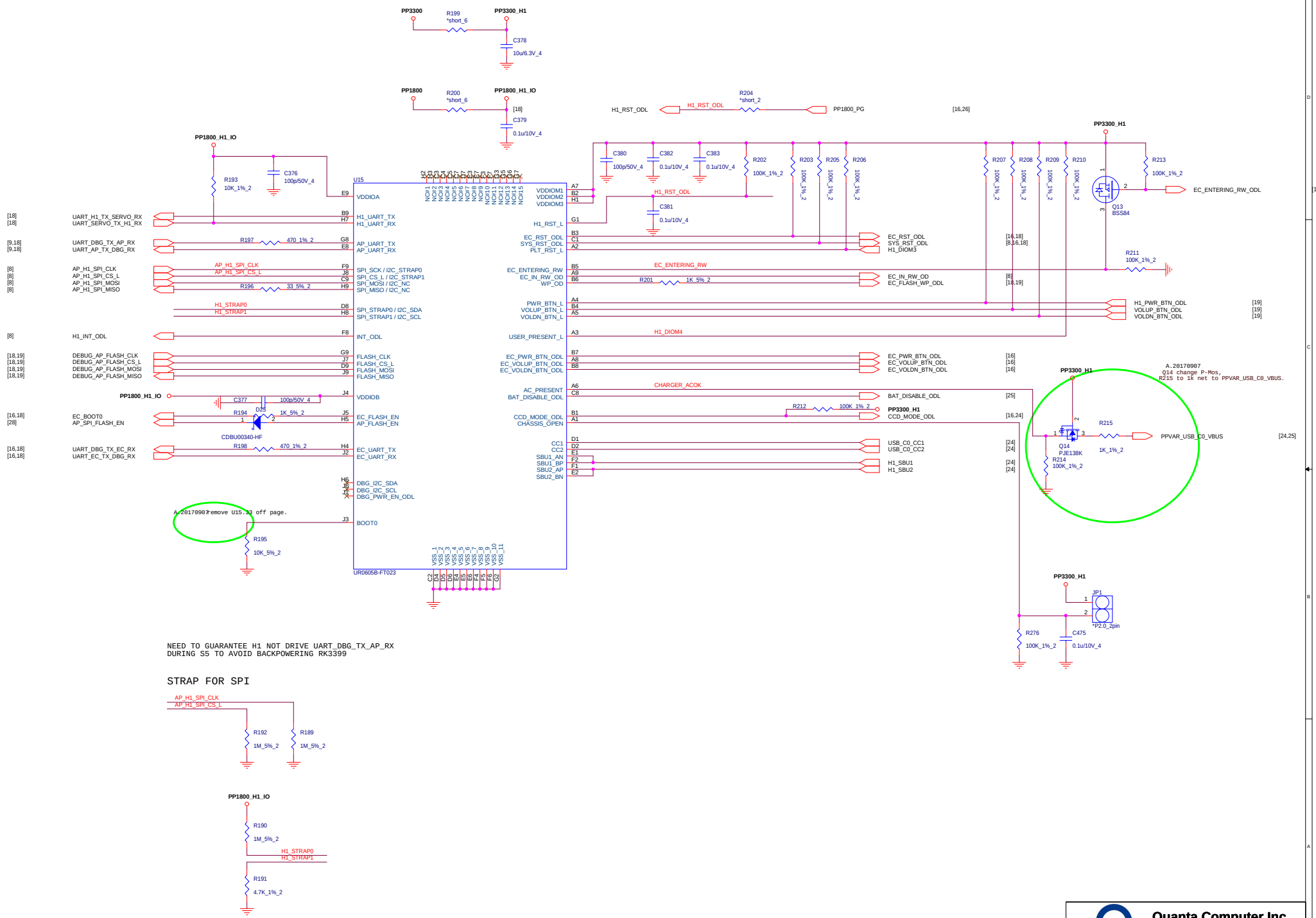


A.20170907 Change U29 footpring for type-3.

PIN-COMPATIBLE WITH STM32L431VC

PLEASE SEE ID TABLE ON PAGE 9
MATCH EC_BOARD_ID RESISTORS TO AP_BRD_ID

Quanta Computer Inc.		
PROJECT : Dru		
Size	Document Number: EC-STM32	Rev 1A
Date: Tuesday, February 06, 2018	Sheet 16 of 28	



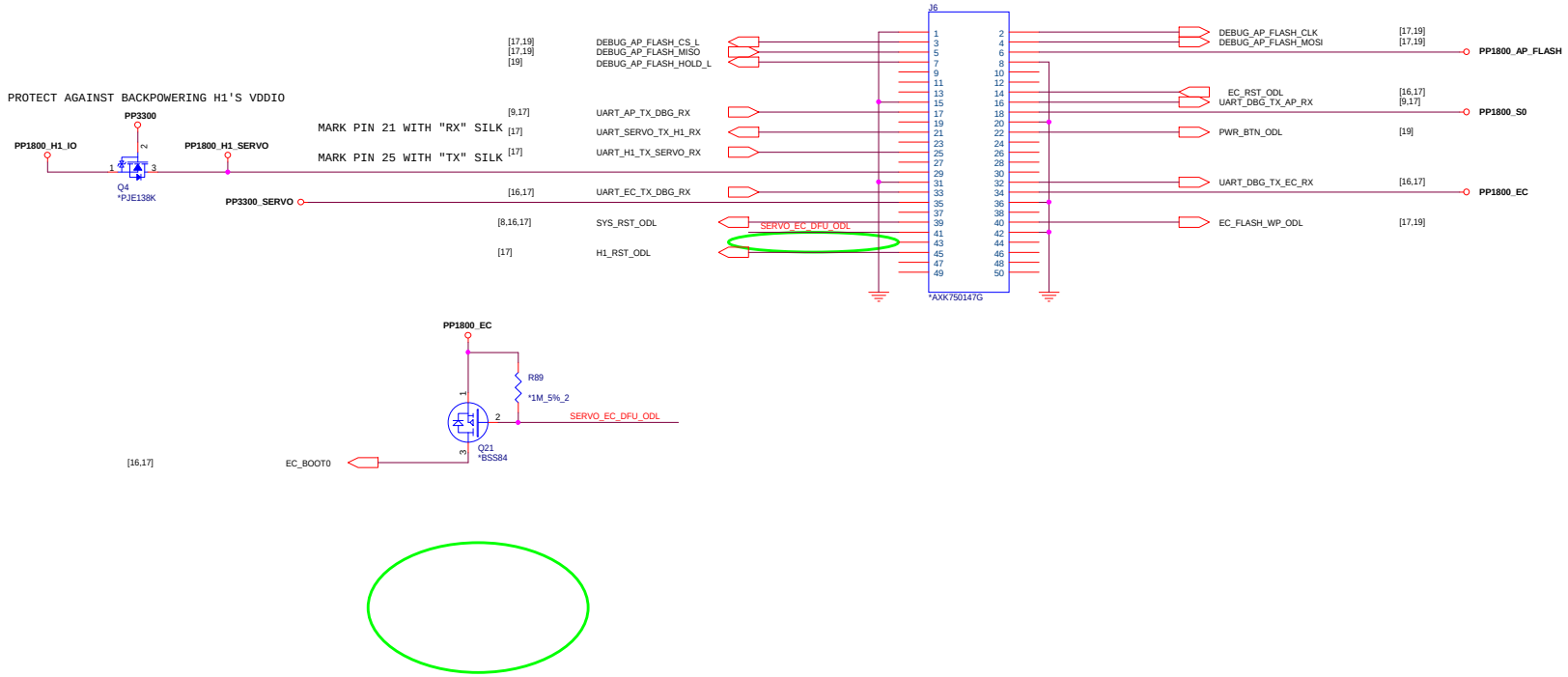
Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	H1	1A

Date: Tuesday, February 06, 2018 Sheet 17 of 28

DNS ENTIRE PAGE IN PVT



A.20170907 Remove net H1_Boot0 and Q22\R90 and net SERVO_H1_DFU_ODL.

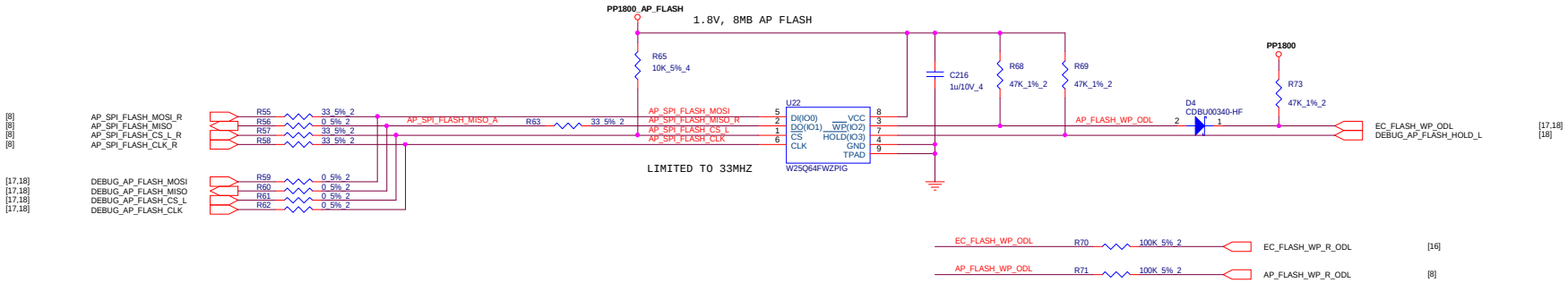
Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	SERVO	1A

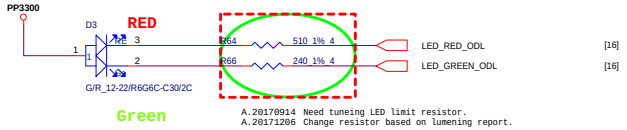
Date: Tuesday, February 06, 2018 Sheet 18 of 28

AP 1.8V SPI FLASH

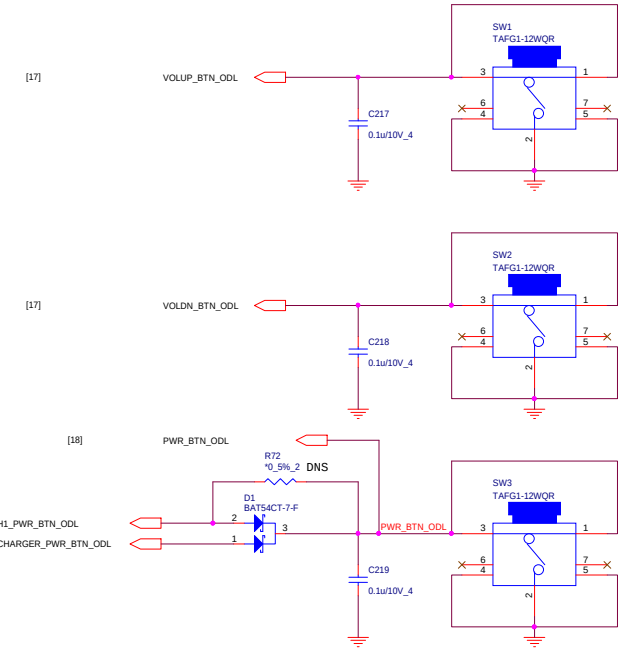


FIXME: ADJUST LED BRIGHTNESS

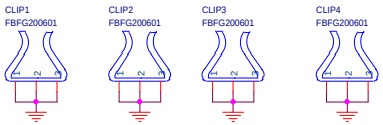
A.20170906
Change to dual color LED,david update pin define.



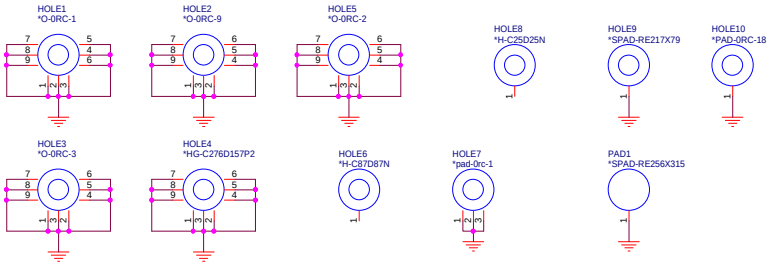
A.20170914 Need tuneing LED limit resistor.
A.20171206 Change resistor based on lumening report.



CLIP



HOLE



Quanta Computer Inc.
PROJECT : Dru

Size	Document Number	Rev
	SPI ROM / BUTTONS / LEDS	1A

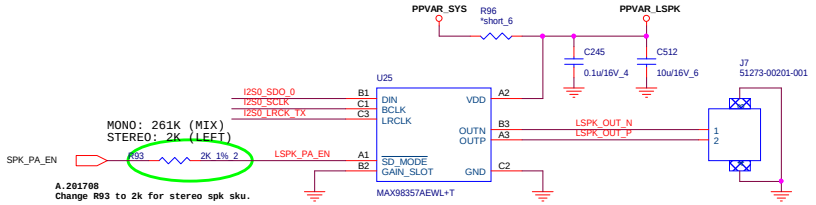
Date: Tuesday, February 06, 2018 Sheet 19 of 28

GAIN TABLE

100K TO GND: GAIN =15 DB
SHORT TO GND: GAIN =12 DB
FLOATING: GAIN = 9 DB
SHORT TO VDD: GAIN = 6 DB
100K TO VDD: GAIN = 3 DB

SPK_PA_EN V	R	STATE
0.000 -- 0.080	X	SHUTDOWN
0.355 -- 0.650	261.0K	MONO MIX
0.825 -- 1.245	69.8K	RIGHT
1.500 -- VDD	2.0K	LEFT

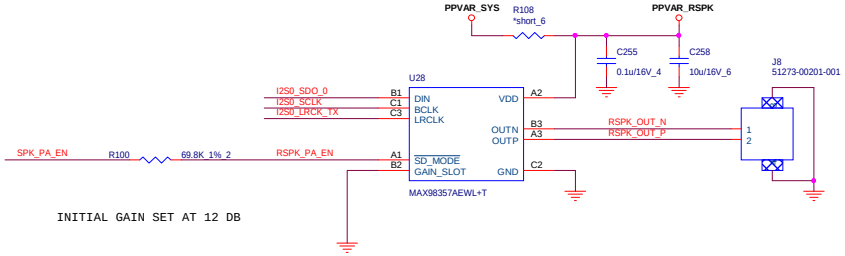
LEFT CHANNEL



GAIN SET AT 12 DB
ENABLES TYPE-3 ESCAPING

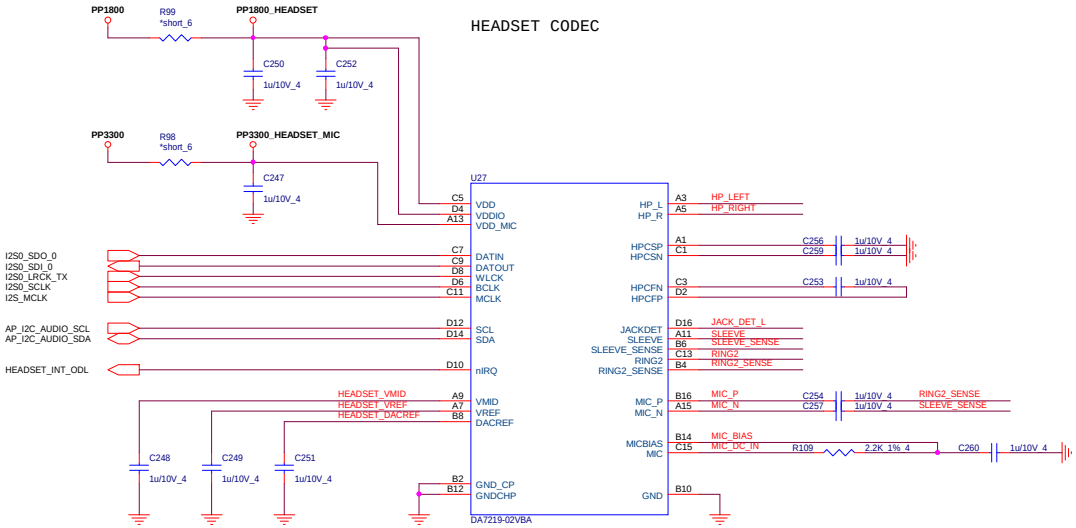
RIGHT SPEAKER STEREO SKUS

RIGHT CHANNEL

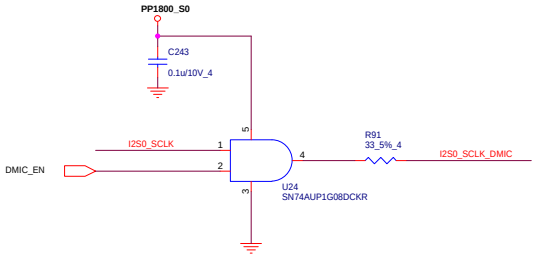


INITIAL GAIN SET AT 12 DB

HEADSET CODEC

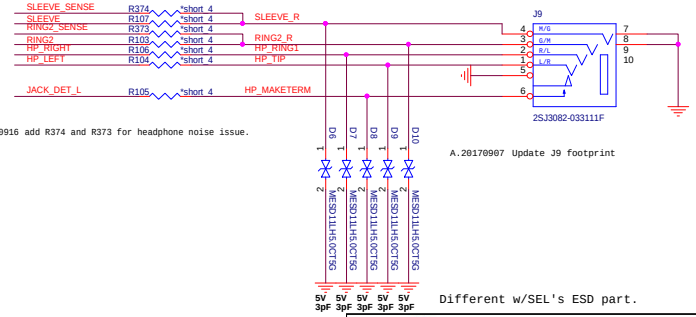


FIXME: SWITCH TO REALTEK HYBRID CODEC



HEADSET JACK

THE TWO SENSE SIGNALS NEED TO BE CLOSE TO JACK CONNECTOR
ROUTE RING2 AND RING2_SENSE TOGETHER (DIFF PAIR WITHOUT IMPEDANCE CONTROL)
THE SAME APPLIES TO SLEEVE AND SLEEVE_SENSE SIGNALS.
ROUTE RING2, RING2_SENSE, SLEEVE, SLEEVE_SENSE BETWEEN HP_LEFT AND HP_RIGHT WHERE POSSIBLE

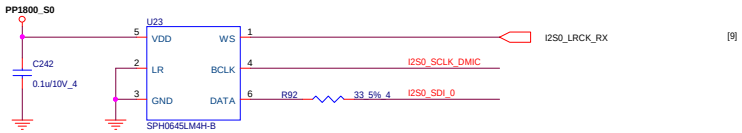


A20170916 add R374 and R373 for headphone noise issue.

A.20170907 Update J9 footprint

Different w/SEL's ESD part.

I2S DMICS
FIXME: PICK SOMETHING CHEAP



Quanta Computer Inc.
PROJECT : Dru

Size	Document Number	Rev
	AUDIO	1A

Date: Tuesday, February 06, 2018 Sheet 20 of 28

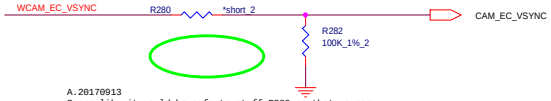
FIXME: CONNECTOR PARTS AND PINOUTS ARE MOST LIKELY WRONG

AMBIENT LIGHT SENSOR / PROX

CHOOSE PART AND STUFF ON HIGH-END SKUS

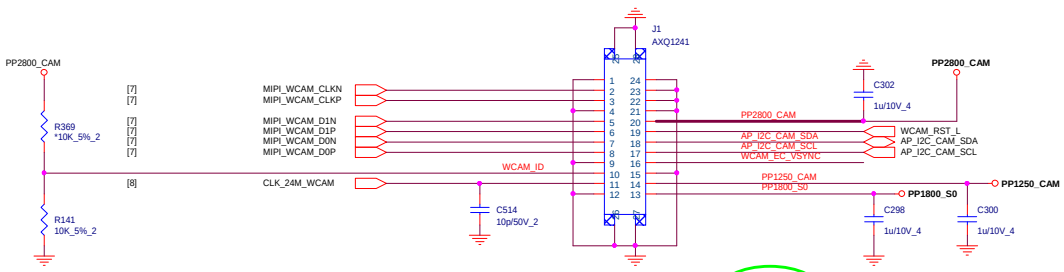
EVT1 Camera Pin 21 is GND, EVT2 for new camera become VSYNC siganl.

Near the J1



A.20170913
Seems like it would be safe to stuff R280 so that we can swap in the new modules when we get them
A.20170907
Remove R281, no need storbe pin of UCAM.
Change R282 to 100k pull down.

World CAMERA

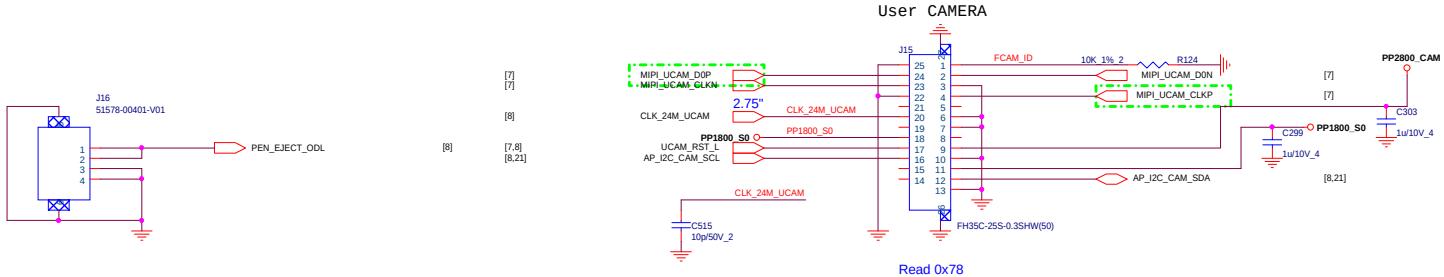


20170829 remove ALS

Read 0x6C
Write 0x6D
1.8V 92mA
1.2V 2mA
2.8V 28mA

A.20170915 Remove R364 Agnd change to GND.

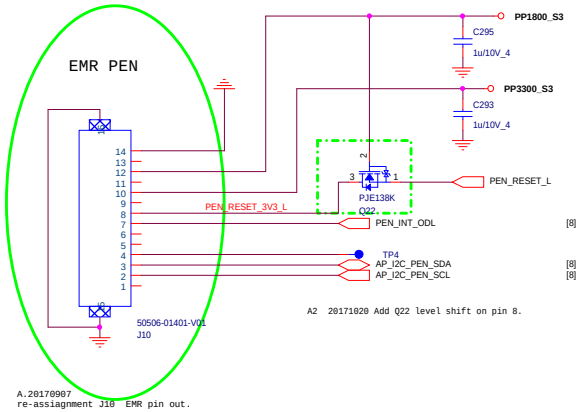
User CAMERA



Read 0x78
Write 0x79
1.8V 45mA
2.8V 30mA

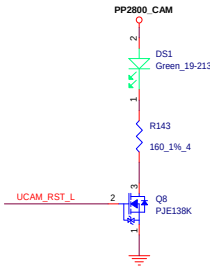
A2 20170020 swap PIN24 and PIN2.

EMR PEN

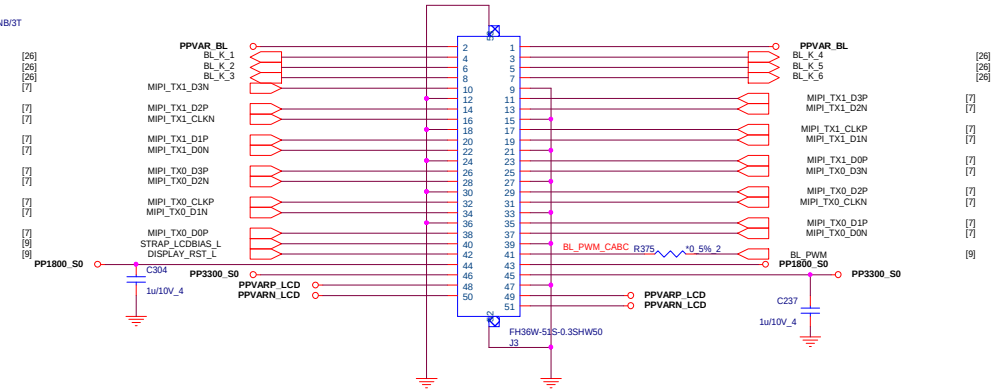


A2 20171020 Add Q22 level shift on pin 8.

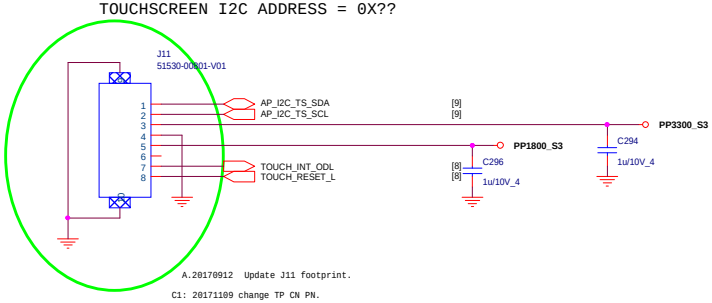
A.20170907
re-assiagnment J10 EMR pin out.



C1: 20171108 add INX panel and select K&D NC pin to add extra INX pin.
C1: 20171109 change LVDS CN PN.



TOUCHSCREEN I2C ADDRESS = 0X??



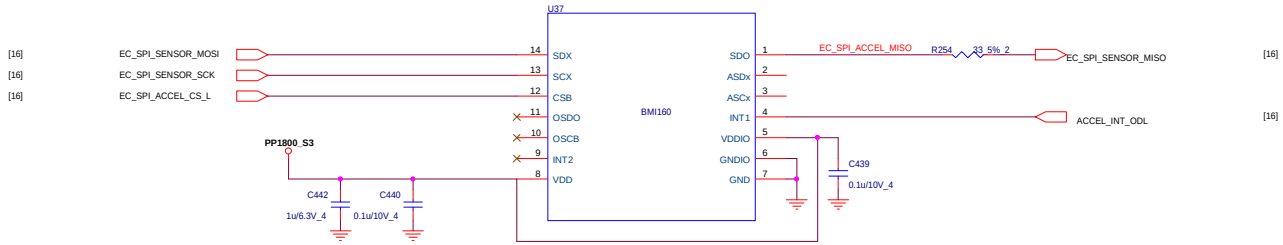
A.20170912 Update J11 footprint.

C1: 20171109 change TP CN PN.

Quanta Computer Inc.		
PROJECT : Dru		
Size	Document Number: PANEL / ALS / CAMERAS	Rev 1A
Date: Tuesday, February 06, 2018	Sheet 21 of 28	

FIXME: STUFFING OPTION FOR ACCEL ONLY?

SIXAXIS

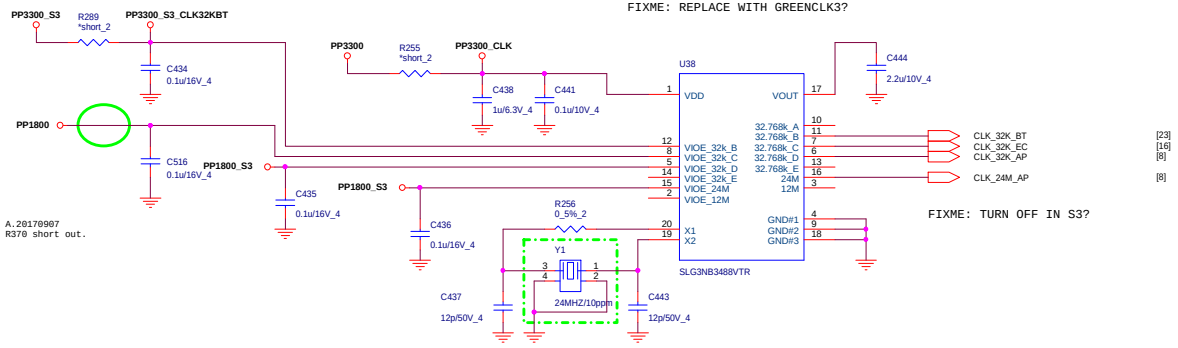


PLACE AS CLOSE TO WCAM AS POSSIBLE

CLOCK

PLACE CLOSE TO RK3399

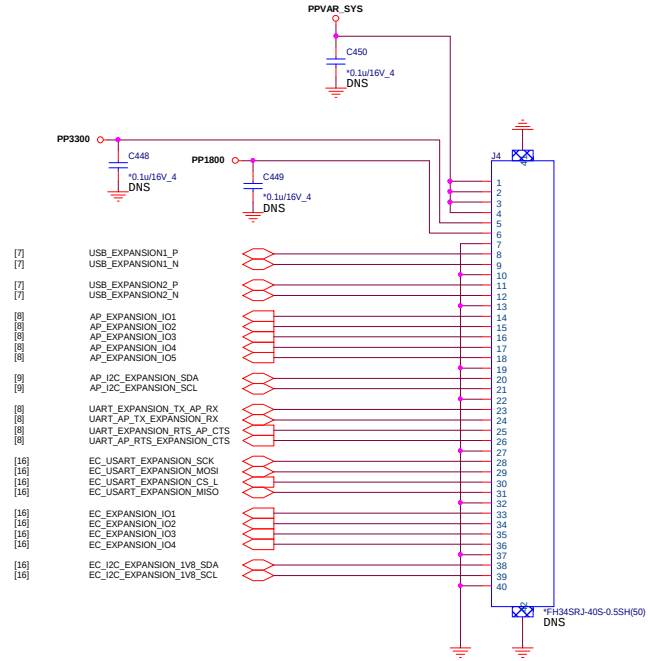
FIXME: REPLACE WITH GREENCLK3?



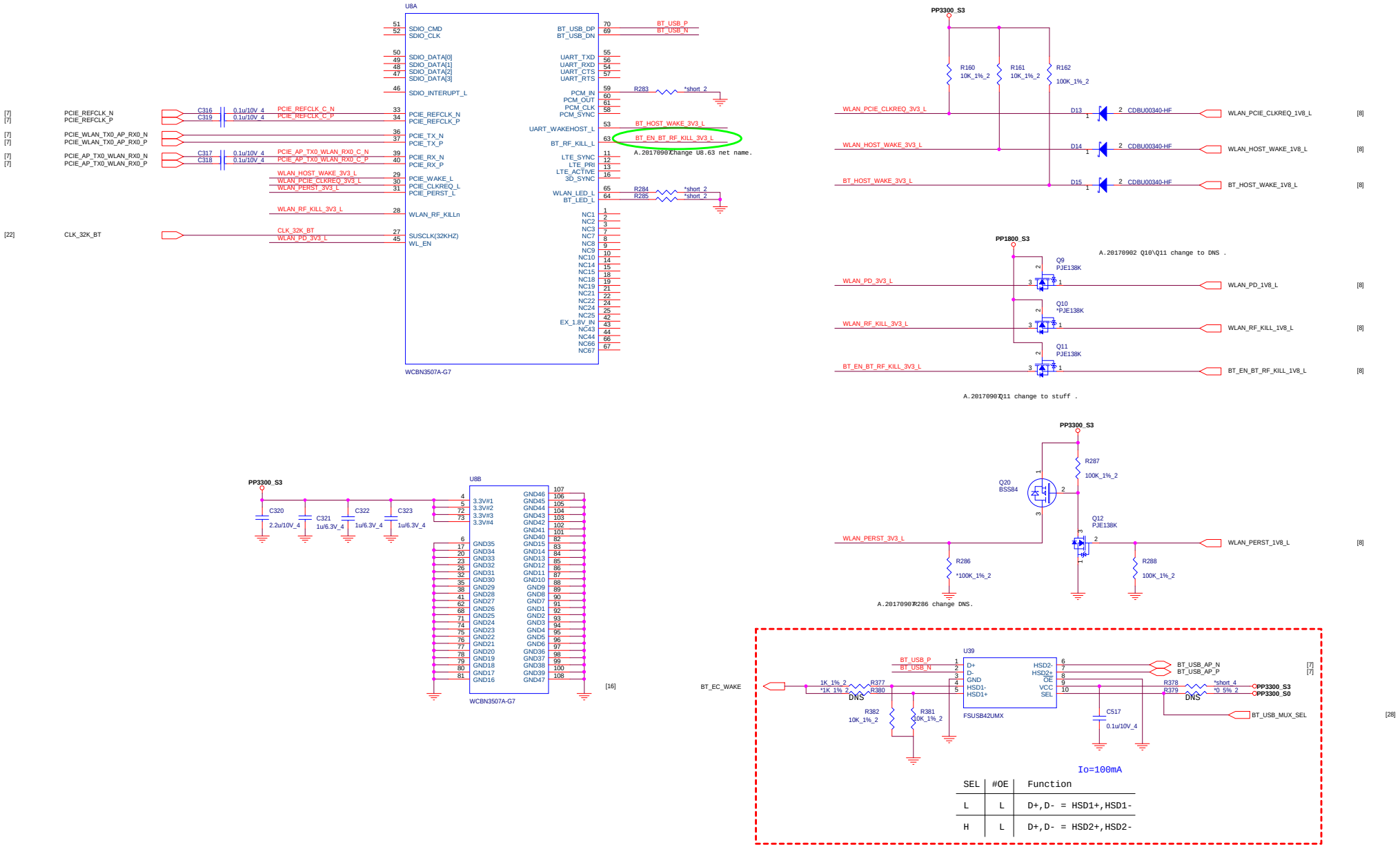
A.20170907
R370 short out.

FIXME: TURN OFF IN S3?

A2 20171018 correct footprint.



Quanta Computer Inc.		
PROJECT : Dru		
Size	Document Number: CLOCK / SENSORS / EXPANSION	Rev 1A
Date: Tuesday, February 06, 2018	Sheet 22 of 28	

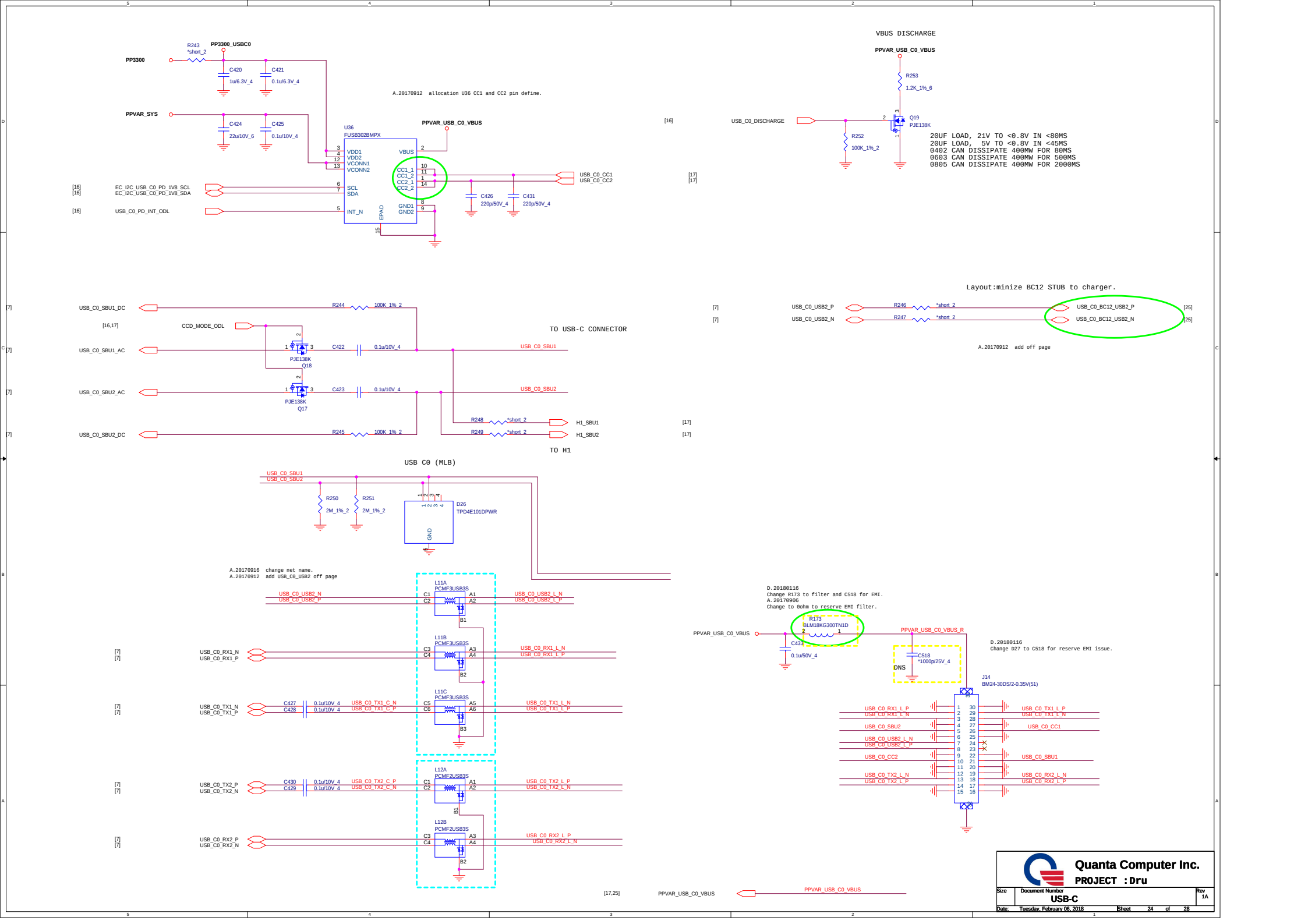


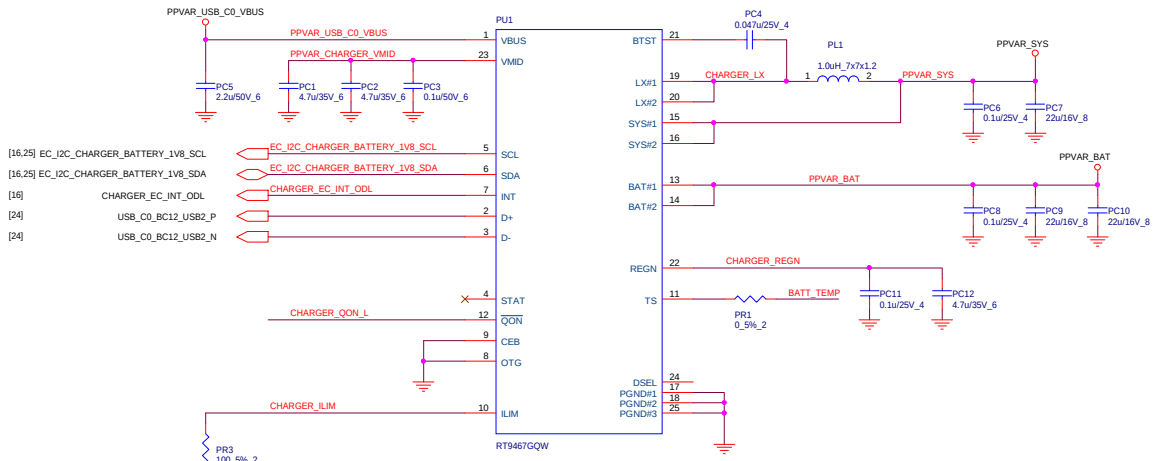
Quanta Computer Inc.

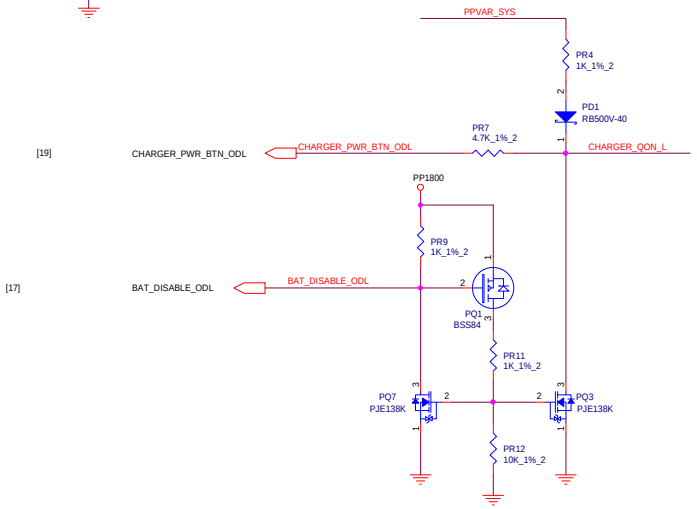
PROJECT : Dru

Size	Document Number	Rev
	WIFI / BT	1A

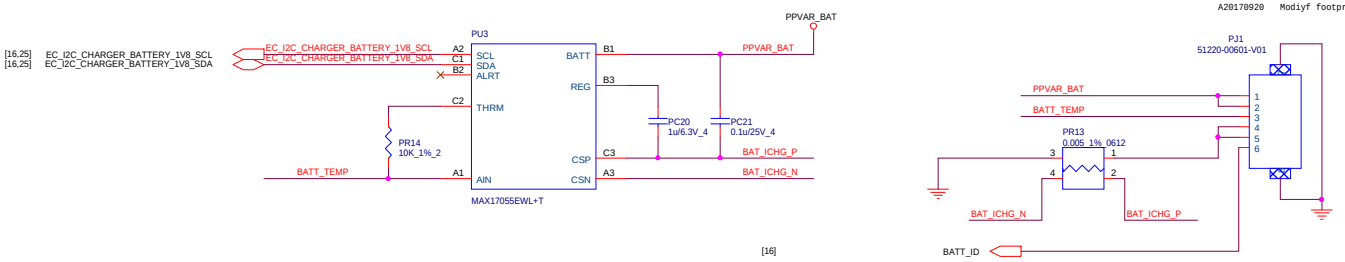
Date: Tuesday, February 06, 2018 Sheet 23 of 28


PP3300
R243
*short_2
PP3300_USBC0
C420
1u/6.3V_4
C421
0.1u/6.3V_4
PPVAR_SYS
C424
22u/10V_6
C425
0.1u/10V_4
A.20170912 allocation U36 CC1 and CC2 pin define.
U36
FUSB302BMPX
PPVAR_USB_C0_VBUS
VDD1
VDD2
VCONN1
VCONN2
VBUS
CC1_1
CC1_2
CC2_1
CC2_2
SCL
SDA
INT_N
GND1
GND2
EPAD
[16] EC_I2C_USB_C0_PD_1V8_SCL
[16] EC_I2C_USB_C0_PD_1V8_SDA
[16] USB_C0_PD_INT_ODL
USB_C0_CC1
USB_C0_CC2
[17]
[17]
C426
220p/50V_4
C431
220p/50V_4
VBUS DISCHARGE
PPVAR_USB_C0_VBUS
R253
1.2K_1%_6
[16] USB_C0_DISCHARGE
R252
100K_1%_2
Q19
PJE138K
20UF LOAD, 21V TO <0.8V IN <80MS
20UF LOAD, 5V TO <0.8V IN <45MS
0402 CAN DISSIPATE 400MW FOR 80MS
0603 CAN DISSIPATE 400MW FOR 500MS
0805 CAN DISSIPATE 400MW FOR 2000MS
[7] USB_C0_SBU1_DC
R244
100K_1%_2
[16,17] CCD_MODE_ODL
[7] USB_C0_SBU1_AC
C422
0.1u/10V_4
PJE138K
Q18
[7] USB_C0_SBU2_AC
C423
0.1u/10V_4
PJE138K
Q17
[7] USB_C0_SBU2_DC
R245
100K_1%_2
TO USB-C CONNECTOR
USB_C0_SBU1
USB_C0_SBU2
R248
*short_2
R249
*short_2
H1_SBU1
H1_SBU2
[17]
[17]
TO H1
Layout:minize BC12 STUB to charger.
[7] USB_C0_USB2_P
[7] USB_C0_USB2_N
R246
R247
*short_2
*short_2
USB_C0_BC12_USB2_P
USB_C0_BC12_USB2_N
[25]
[25]
A.20170912 add off page
USB C0 (MLB)
USB_C0_SBU1
USB_C0_SBU2
R250
2M_1%_2
R251
2M_1%_2
D26
TPD4E101DPWR
GND
A.20170916 change net name.
A.20170912 add USB_C0_USB2 off page
L11A
PCMF3USB3S
USB_C0_USB2_N
USB_C0_USB2_P
USB_C0_USB2_L_N
USB_C0_USB2_L_P
L11B
PCMF3USB3S
[7] USB_C0_RX1_N
[7] USB_C0_RX1_P
USB_C0_RX1_L_N
USB_C0_RX1_L_P
L11C
PCMF3USB3S
[7] USB_C0_TX1_N
[7] USB_C0_TX1_P
C427
0.1u/10V_4
C428
0.1u/10V_4
USB_C0_TX1_C_N
USB_C0_TX1_C_P
USB_C0_TX1_L_N
USB_C0_TX1_L_P
L12A
PCMF2USB3S
[7] USB_C0_TX2_P
[7] USB_C0_TX2_N
C430
0.1u/10V_4
C429
0.1u/10V_4
USB_C0_TX2_C_P
USB_C0_TX2_C_N
USB_C0_TX2_L_P
USB_C0_TX2_L_N
L12B
PCMF2USB3S
[7] USB_C0_RX2_P
[7] USB_C0_RX2_N
USB_C0_RX2_L_P
USB_C0_RX2_L_N
D.20180116
Change R173 to filter and C518 for EMI.
A.20170906
Change to 0ohm to reserve EMI filter.
PPVAR_USB_C0_VBUS
R173
BLM18KG300TN1D
C433
0.1u/50V_4
PPVAR_USB_C0_VBUS_R
C518
*1000p/25V_4
DNS
D.20180116
Change D27 to C518 for reserve EMI issue.
J14
BM24-30DS/2-0.35V(51)
USB_C0_RX1_L_P
USB_C0_RX1_L_N
USB_C0_SBU2
USB_C0_USB2_L_N
USB_C0_USB2_L_P
USB_C0_CC2
USB_C0_TX2_L_N
USB_C0_TX2_L_P
USB_C0_TX1_L_P
USB_C0_TX1_L_N
USB_C0_CC1
USB_C0_SBU1
USB_C0_RX2_L_N
USB_C0_RX2_L_P
[17,25] PPVAR_USB_C0_VBUS
PPVAR_USB_C0_VBUS
Quanta Computer Inc.
PROJECT : Dru
Size
Document Number
USB-C
Rev
1A
Date: Tuesday, February 06, 2018
Sheet 24 of 28





A20170920 Modiyf footprint becaue CN update.

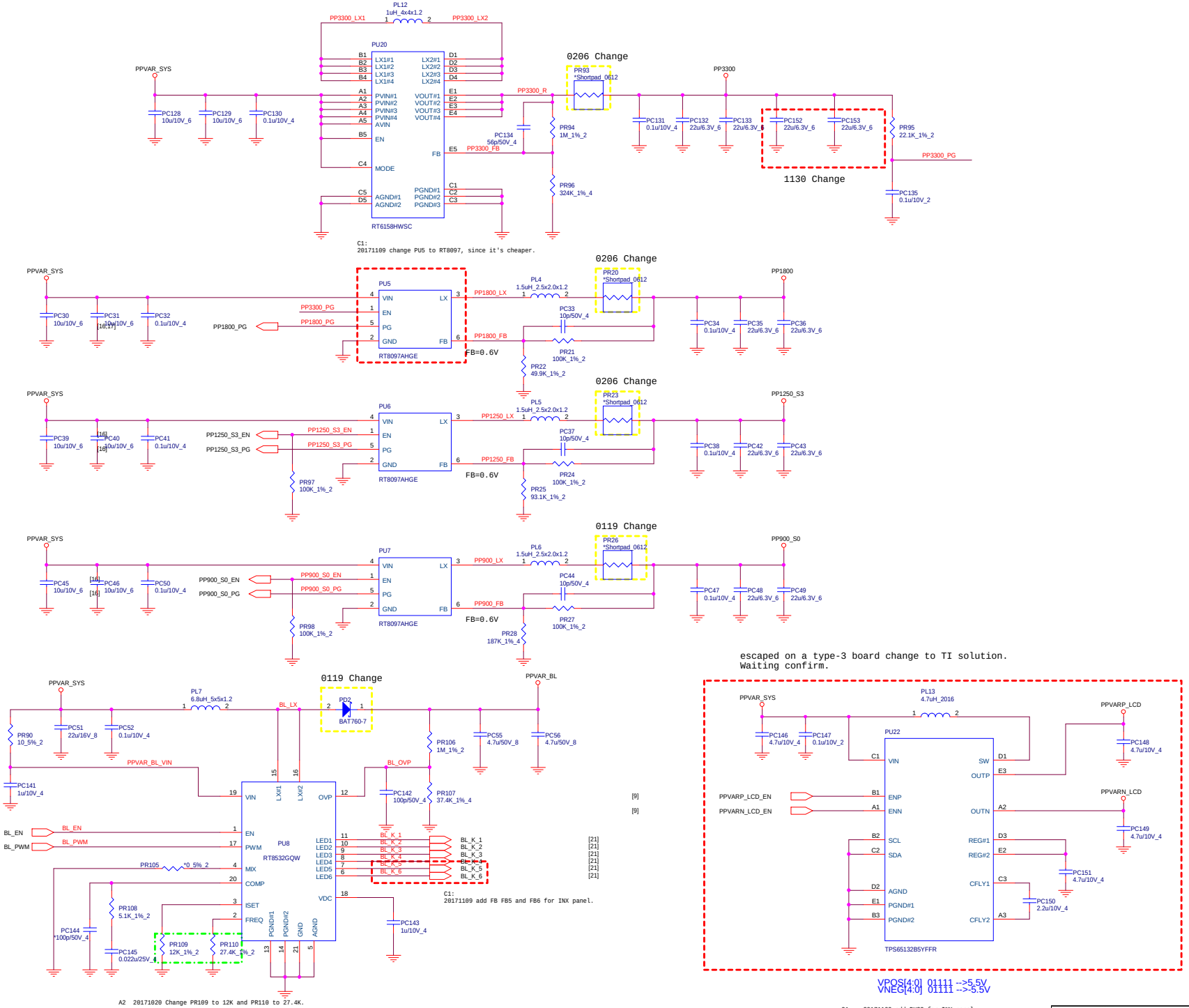


Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	Power Charger	1A

Date: Tuesday, February 06, 2018 Sheet 25 of 28

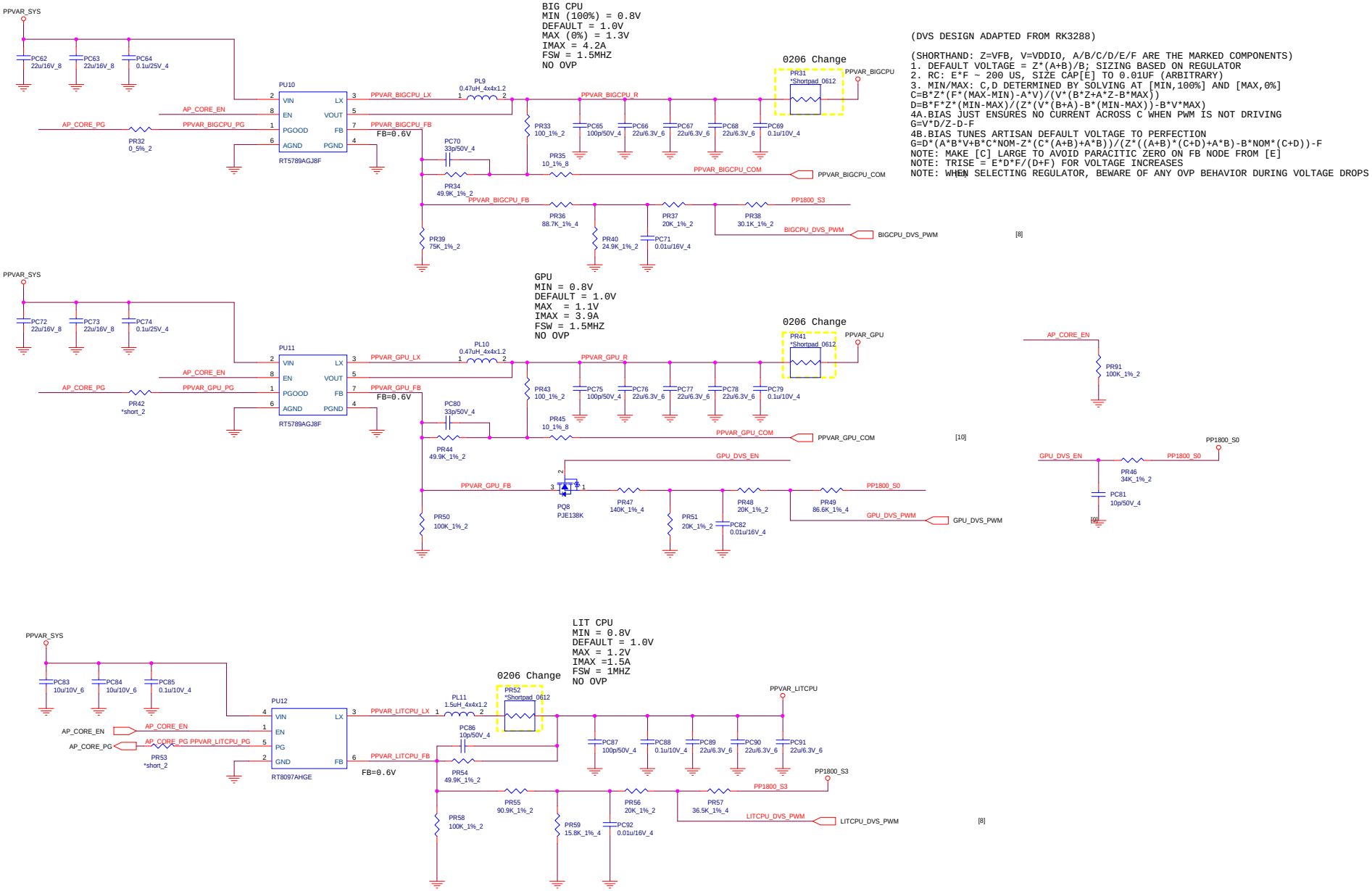


Quanta Computer Inc.

PROJECT : Dru

Size	Document Number	Rev
	Power 3.3V/1.8V/0.9V/LCD	1A

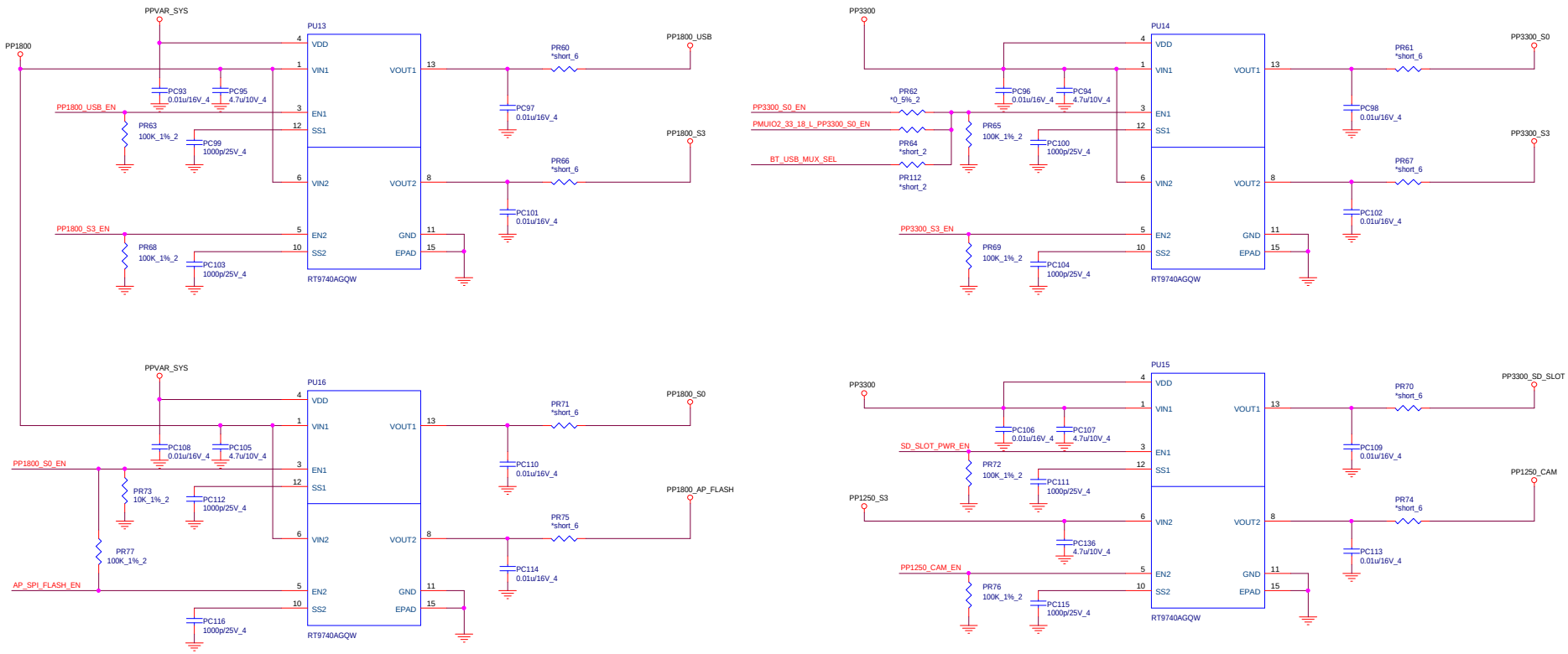
Date: Tuesday, February 06, 2018 Sheet 26 of 28



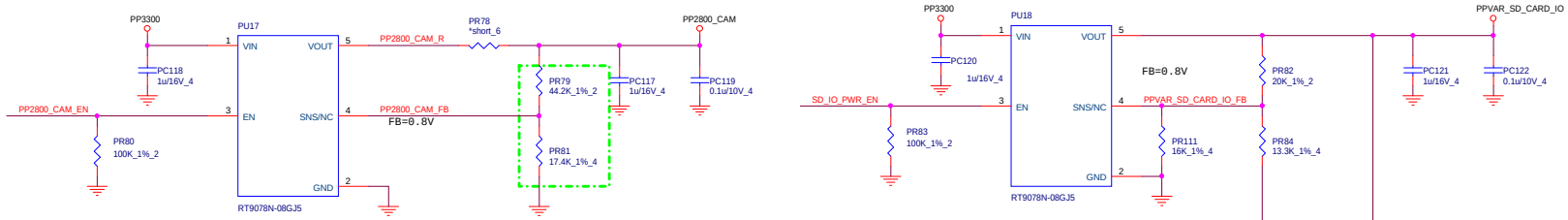
(DVS DESIGN ADAPTED FROM RK3288)

(SHORTHAND: Z=VFB, V=VDDIO, A/B/C/D/E/F ARE THE MARKED COMPONENTS)
1. DEFAULT VOLTAGE = Z*(A+B)/B; SIZING BASED ON REGULATOR
2. RC: E*F ~ 200 US, SIZE CAP[E] TO 0.01UF (ARBITRARY)
3. MIN/MAX: C,D DETERMINED BY SOLVING AT [MIN,100%] AND [MAX,0%]
C=B*Z*(F*(MAX-MIN)-A*V)/(V*(B*Z+A*Z-B*MAX))
D=B*F*Z*(MIN-MAX)/(Z*(V*(B+A)-B*(MIN-MAX))-B*V*MAX)
4A.BIAS JUST ENSURES NO CURRENT ACROSS C WHEN PWM IS NOT DRIVING
G=V*D/Z-D-F
4B.BIAS TUNES ARTISAN DEFAULT VOLTAGE TO PERFECTION
G=D*(A*B*V+B*C*NOM-Z*(C*(A+B)+A*B))/(Z*((A+B)*(C+D)+A*B)-B*NOM*(C+D))-F
NOTE: MAKE [C] LARGE TO AVOID PARACITIC ZERO ON FB NODE FROM [E]
NOTE: TRISE = E*D*F/(D+F) FOR VOLTAGE INCREASES
NOTE: WHEN SELECTING REGULATOR, BEWARE OF ANY OVP BEHAVIOR DURING VOLTAGE DROPS

Quanta Computer Inc.		
PROJECT : Dru		
Size	Document Number: Power 3.3V/1.8V/0.9V/LCD	Rev 1A
Date: Tuesday, February 06, 2018	Sheet 27 of 28	

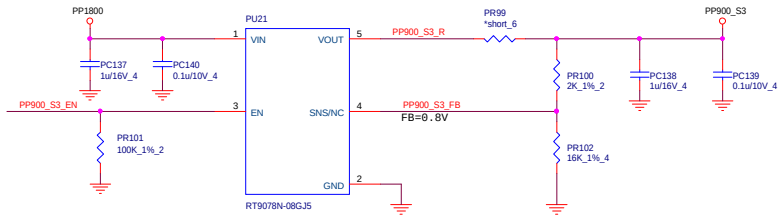


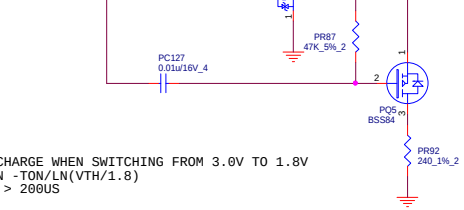
2.8V FOR CAMERA AVDD
IMAX=60MA



A2 20171024 change PR79 44.2K and PR81 change to 17.4K.

0.9V S3
IMAX=20MA





DISCHARGE WHEN SWITCHING FROM 3.0V TO 1.8V
RC=N -TON/LN(VTH/1.8)
TON > 200US

PP1800_USB_EN	PP1800_USB_EN	PP1800_USB_EN
PP1800_S3_EN	PP1800_S3_EN	PP1800_S3_EN
PP1800_S0_EN	PP1800_S0_EN	PP1800_S0_EN
AP_SPI_FLASH_EN	AP_SPI_FLASH_EN	AP_SPI_FLASH_EN
PP2800_CAM_EN	PP2800_CAM_EN	PP2800_CAM_EN
PP900_S3_EN	PP900_S3_EN	PP900_S3_EN

[23]	BT_USB_MUX_SEL	BT_USB_MUX_SEL
[16]	PP3300_S0_EN	PP3300_S0_EN
[8]	PMUIO2_33_18_L_PP3300_S0_EN	PMUIO2_33_18_L_PP3300_S0_EN
[16]	PP3300_S3_EN	PP3300_S3_EN
[9]	SD_SLOT_PWR_EN	SD_SLOT_PWR_EN
[8]	PP1250_CAM_EN	PP1250_CAM_EN
[8]	SD_IO_PWR_EN	SD_IO_PWR_EN
[8]	SD_PWR_3000_1800_L	SD_PWR_3000_1800_L

Quanta Computer Inc.
PROJECT : Dru

Size	Document Number	Rev
	Power 3.3V/1.8V/0.9V/LCD	1A

Date: Tuesday, February 06, 2018 Sheet 28 of 28