

Volteer MLB
SCH: TGL CHROME
ASSY:NA
PCB: NA

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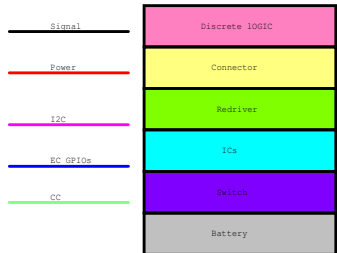
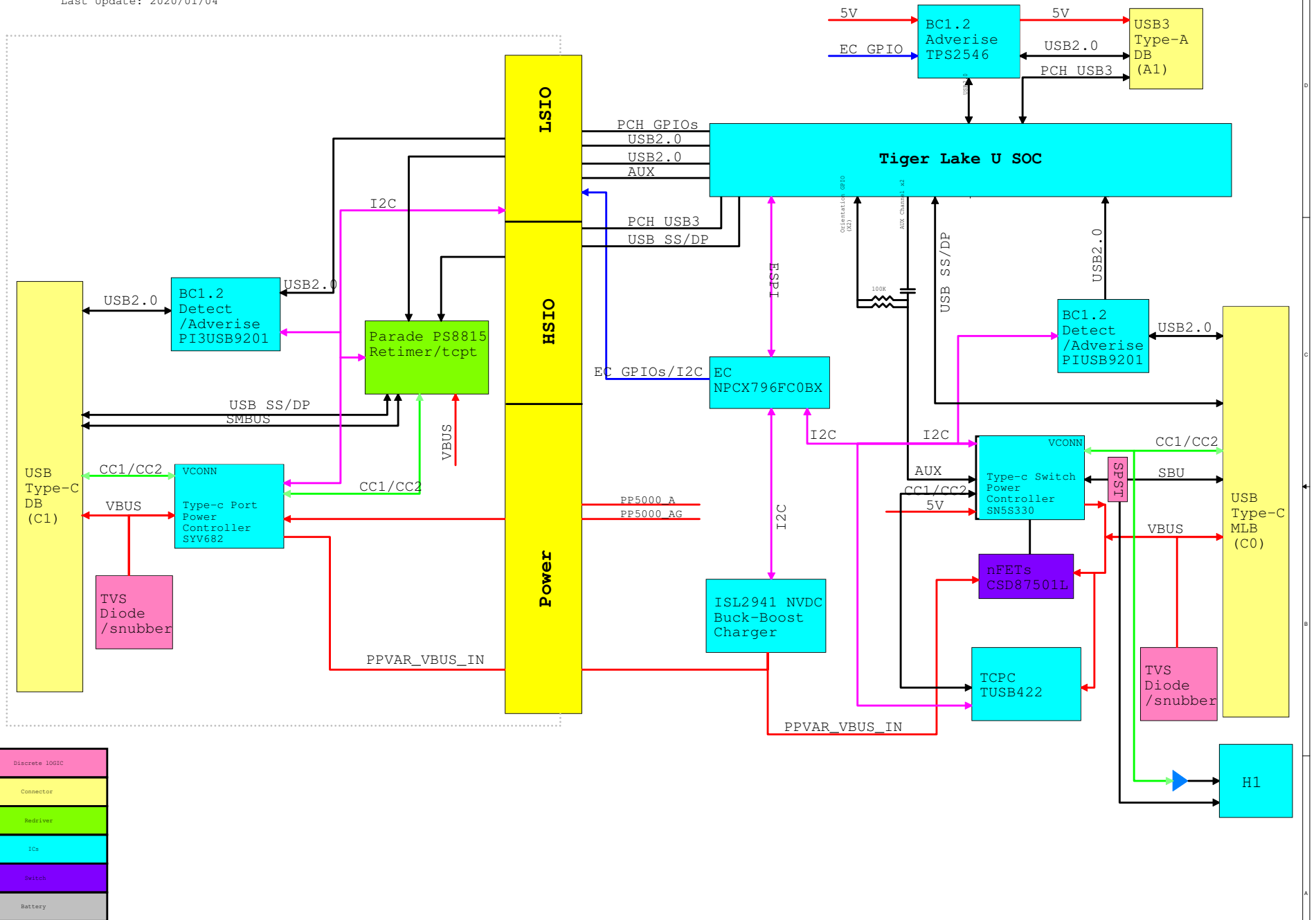
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P54	DB BOARD : TitleBlock0

SHEET NO.	SHEET NAME
P55	RF CAP
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Volteer USB BlockDiagram

Last Update: 2020/01/04

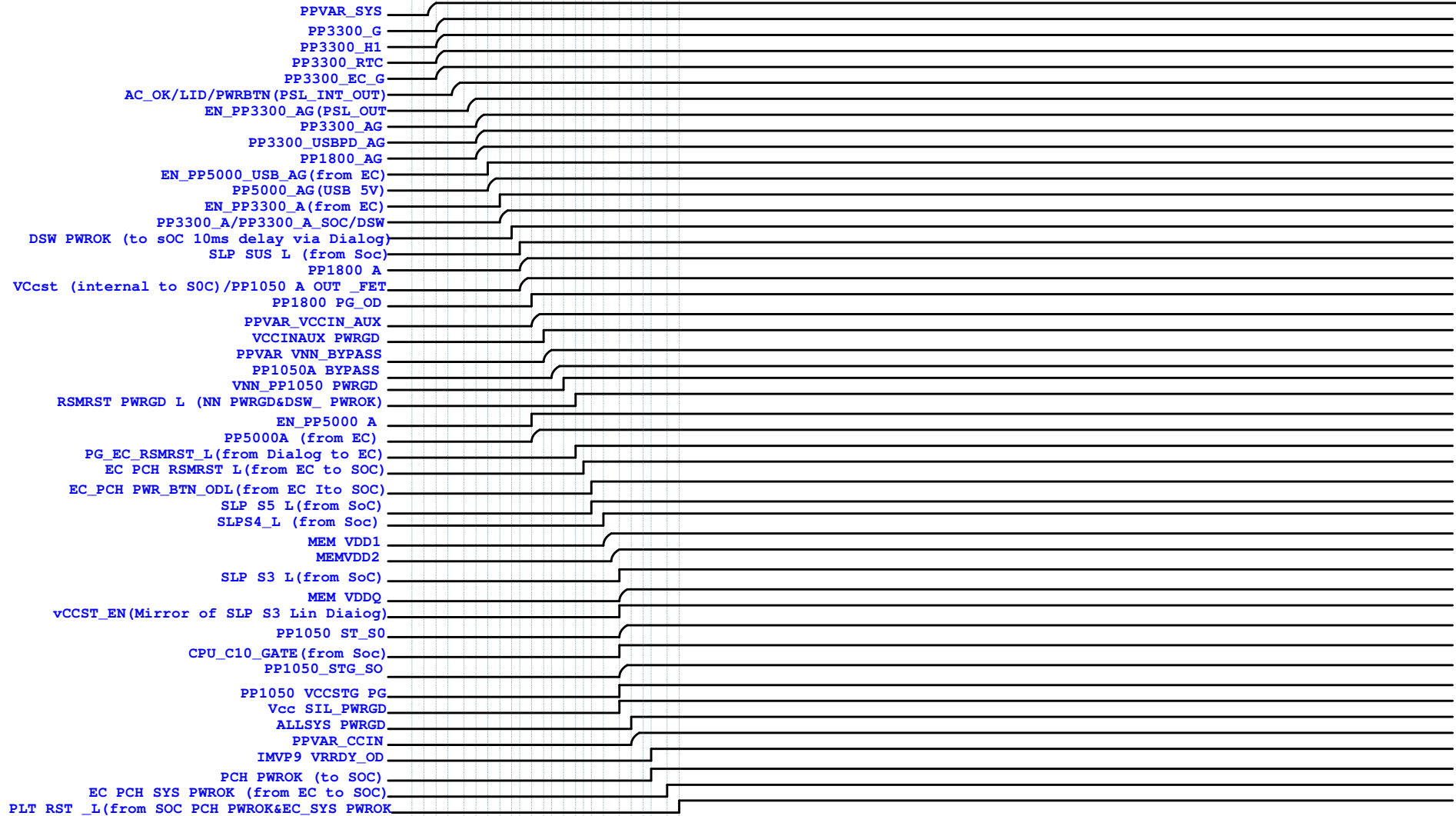


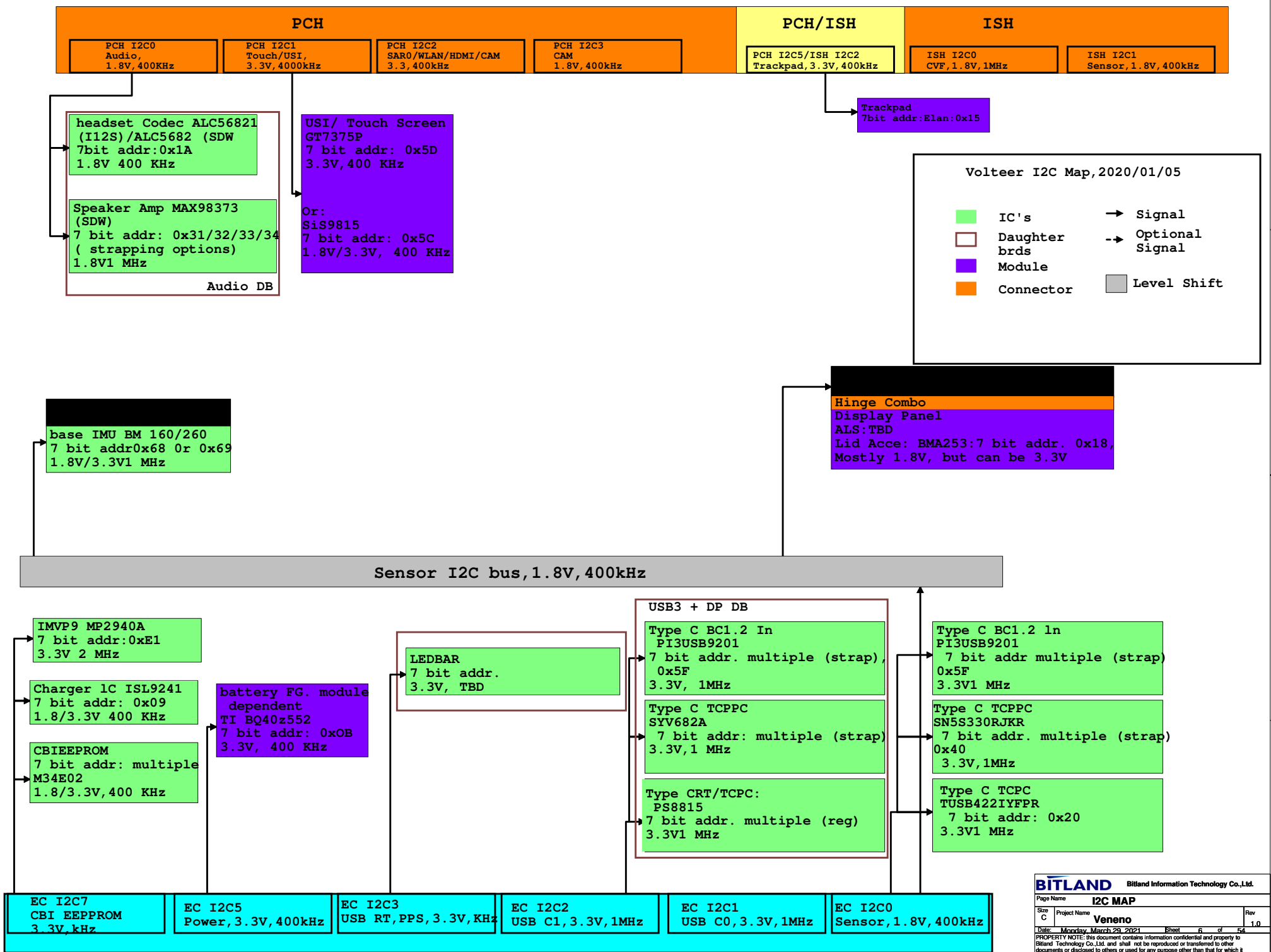
Volteer Proto System power sequence

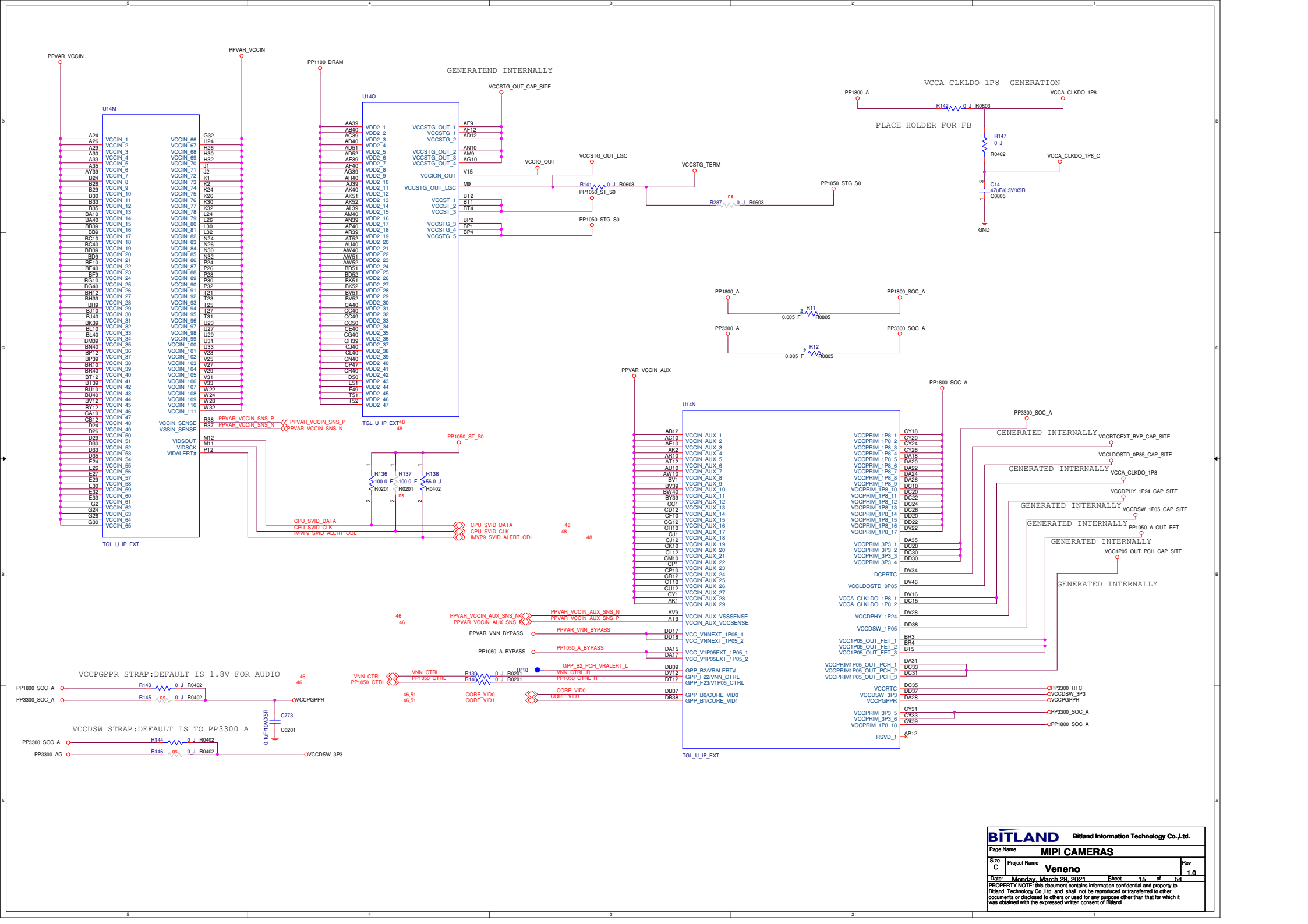
T2 T4 T6 T8 T10 T12 T14 T16 T18 T20 T22 T24
T1 T3 T5 T7 T9 T11 T13 T15 T17 T19 T21 T23

AG state G3 state

S5 TO S0iX state

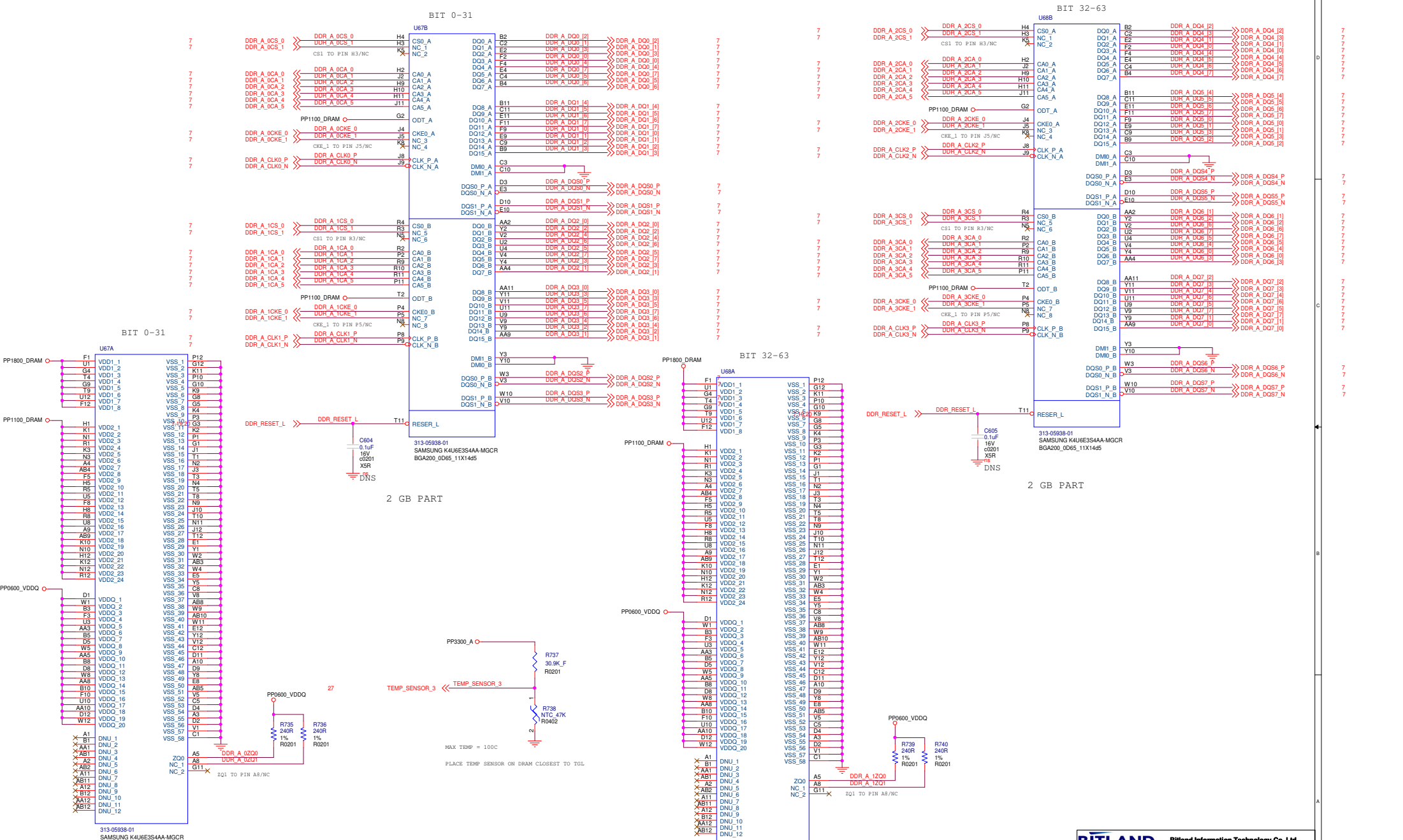






CHA LPDDR4X -4266
BIT SWAPPING IS ALLOWED WITHIN EACH BYTE
BYTE SWAPPING IS ALLOWED WITHIN EACH X 16 SUB-CHANNEL

DDP: 1 RANK PER PKG, QDP AND ODP : 2 RANKS PER PKG



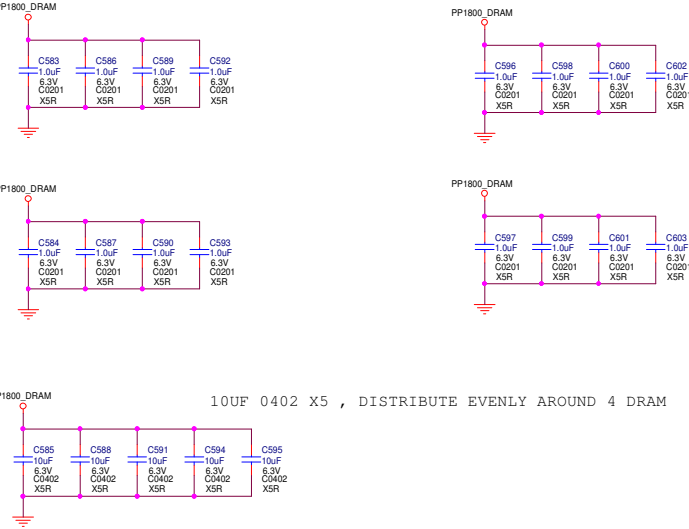
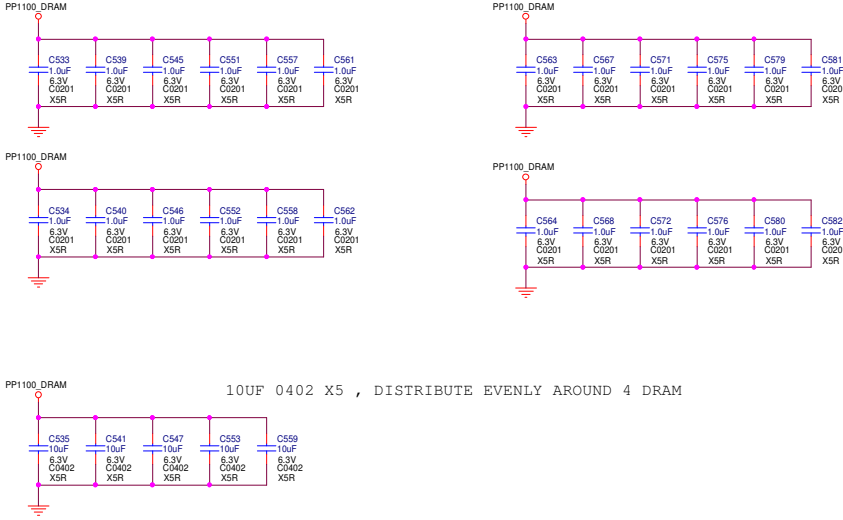
VDD2 DECAP FOR DRAM

TODO: UPDATE PER INTEL PDG AND AFTER INITIAL LAYOUT REVIEW

6 X 1.0UF CAPS PER DRAM 2 PER LONG EDGE 1 PER SHORT EDGE

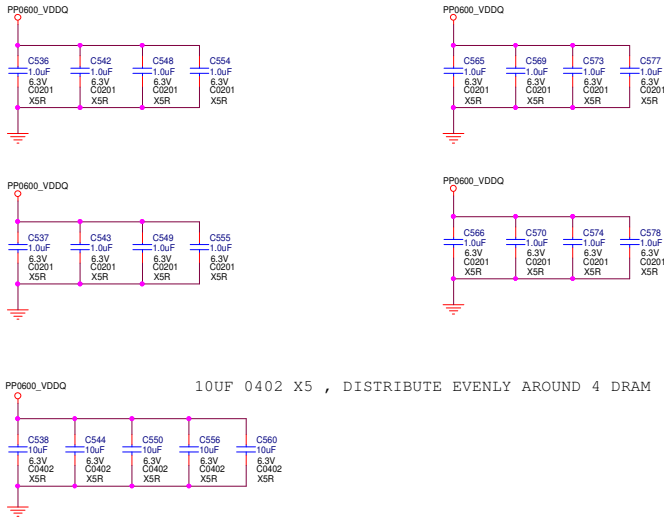
VDD1 DECAP FOR DRAM

4 X 1.0UF CAPS PER DRAM 1 PER EACH CORNER



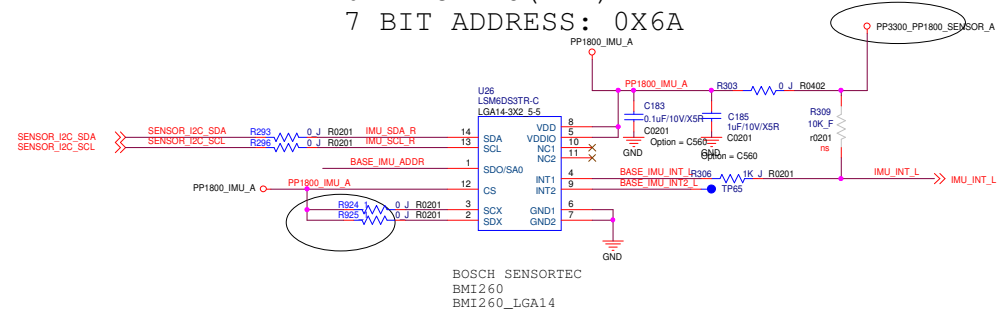
VDDQ DECAP FOR DRAM

4 X 1.0UF CAPS PER DRAM 2 PER EACH SHORT EDGE



IMU AND ACCEL: LSB OF I2C ADDRESS SET BY ADDR NET

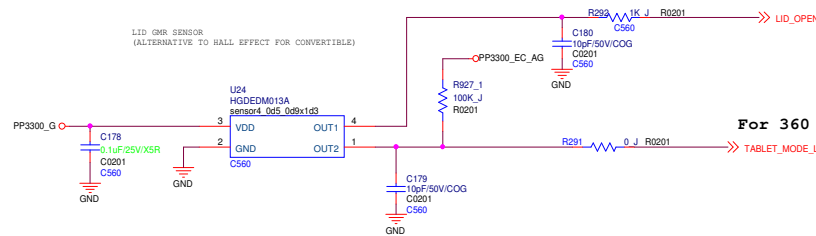
6 AXIS IMU (MLB)
7 BIT ADDRESS: 0X6A



3-AXIS ACCELEROMETER ON LID

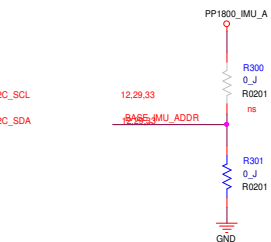
ALS/RGB SENSOR

IMU AND ACCEL: LSB OF I2C ADDRESS SET BY ADDR NET
IF CONFL7I-CBTI,T TACDSD3R4E0S0S7 F0NXM3 9HAS 0X29

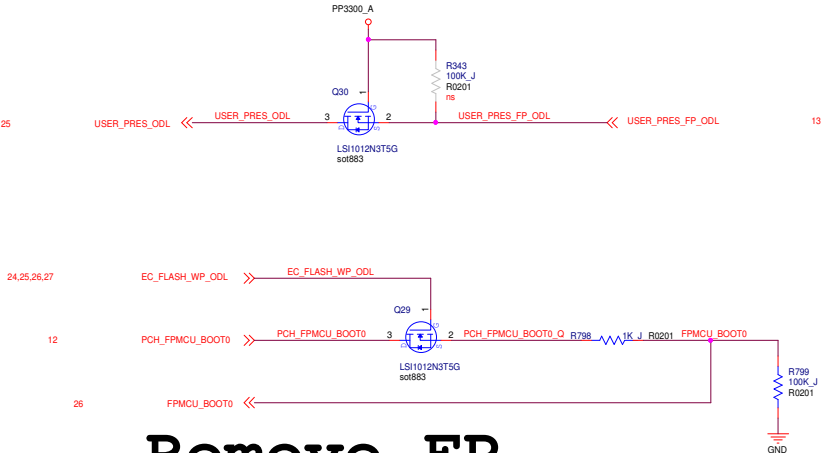


REMOVE ALS

LID SWITCH GMR SENSOR



Remove FP



Remove FP

REMOVE MIPI CAMERA

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Page Name			
MIPI CAMERAS			
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C	Veneno		1.0
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CVF DEV HOOK

Size

C

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Veneno

Rev

1.0

Date

Monday, March 23, 2021

Sheet

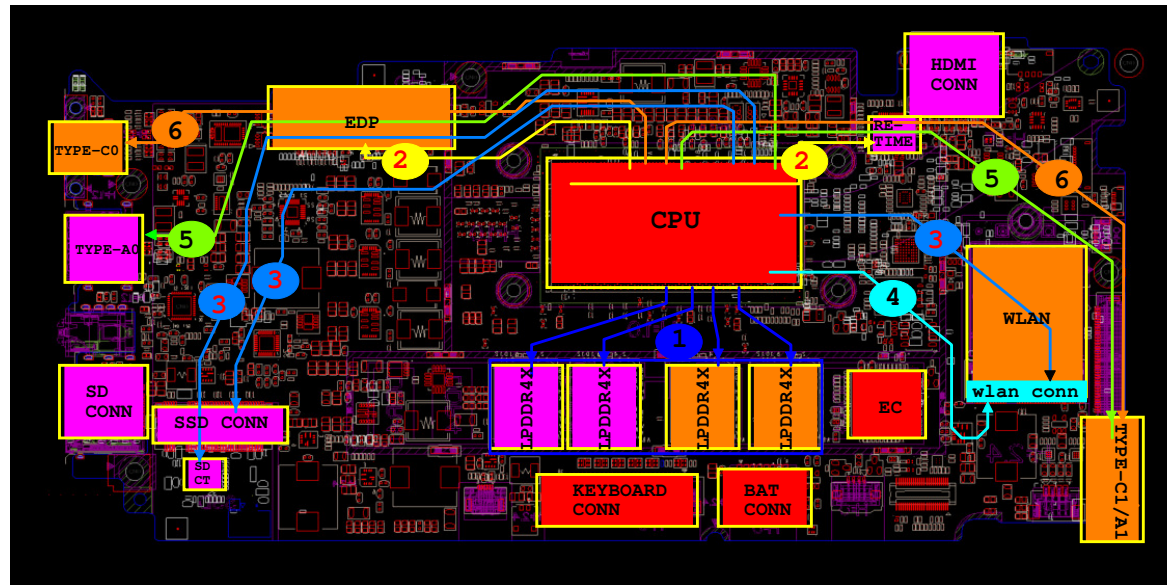
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of

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Botton review



1. LPDDR4X BUS for memory-->BOT/IN3/IN8
2. EDP and HDMI BUS for DP-->BOT/IN3/IN8
3. PCIE BUS for SD Controllor/SSD CONN/WLAN-->BOT/IN8
4. CNVI BUS for WLAN-->BOT/IN8
5. USB BUS for TYPE-A0/A1-->BOT/IN3/IN8
6. TBT BUS for TYPE-C0/C1-->BOT/IN8

IN3
IN8

REMOVE WWAN M.2

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Remove HDMI

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HDMI RETIMER			
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1.0			
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INPUT CAPS: 3X10UF (2S), 4X10UF (3S)

3 10UF CAPS PLACEHOLDERS FOR 22UF
REQUEST FROM INTERSIL

OUTPUT CAPS: 8X22UF PER INTERSIL FEEDBACK

7.3 X 6.8 X 2MM
ISAT = 8.5A
IDC = 8.3A
L@IDC = ~1.7UH

Added 3 x10uF 50V on PPVAR_PWR_IN_BB with note to place on backside
Added 3x 22uF 25V on PPVAR_SYS with note to place on backside
Delete R764 and R765 Add 47uF 35V Tant cap to PPVAR_PWR_IN_BB
Change R490 to 300 ohms Add 100uF 25V empty tant cap site to PPVAR_SYS

PULDOWN SINCE WE
ARE NOT
USING THE OTG
FUNCTIONALITY

VERIFY COMPENSATION VALUES WITH INTERSIL

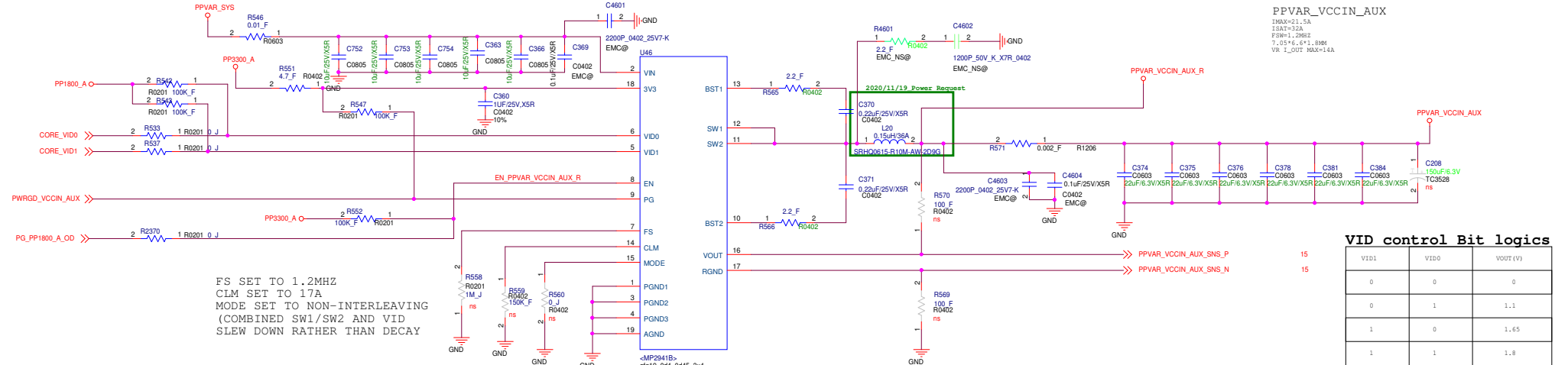
INITIAL PROGRAMMING

3 CELL
724KHZ
1.5A ADAPTER CURRENT LIMIT
PSYS OPERATION

CHANGE TO 562 OHMS FOR 2S (ALL OTHERS EQUAL)
SEE TABLE 13 IN DS FOR MORE DETAILS

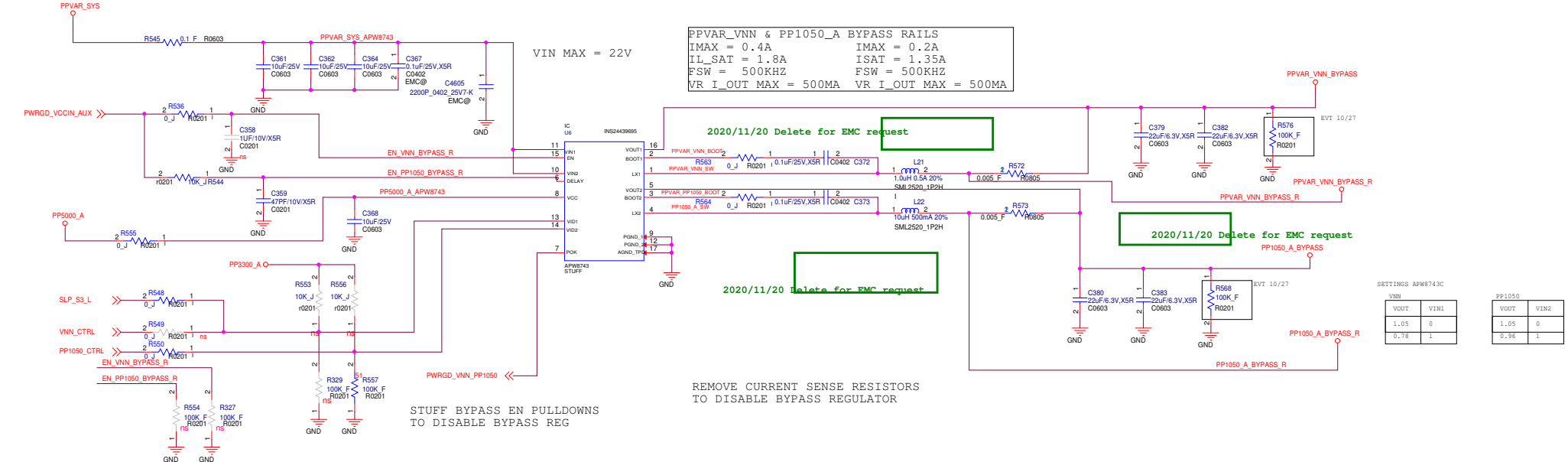
MAX TEMP = 100C
PLACE THERMISTOR NEAR CHARGING INDUCTOR

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VID control Bit logics

VID1	VID0	VOUT (V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

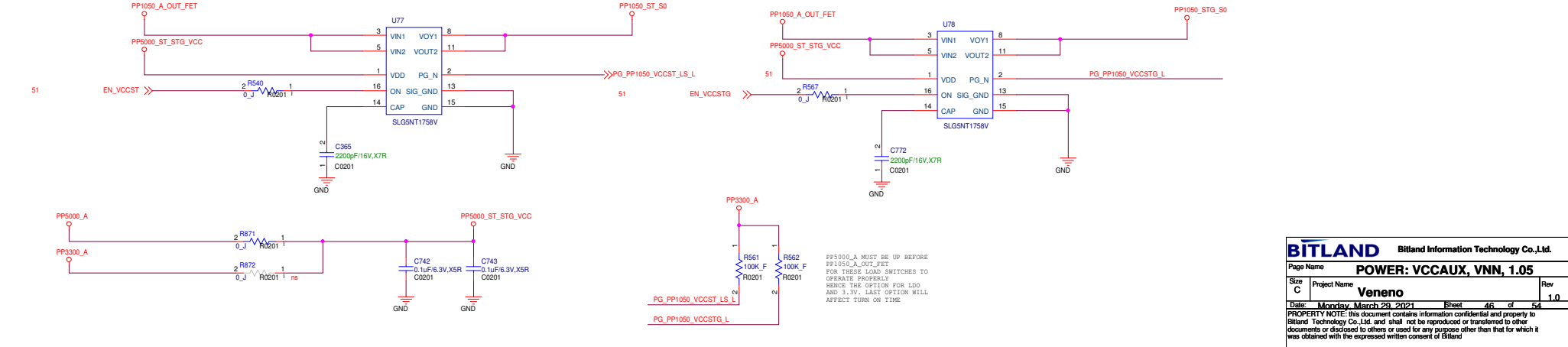


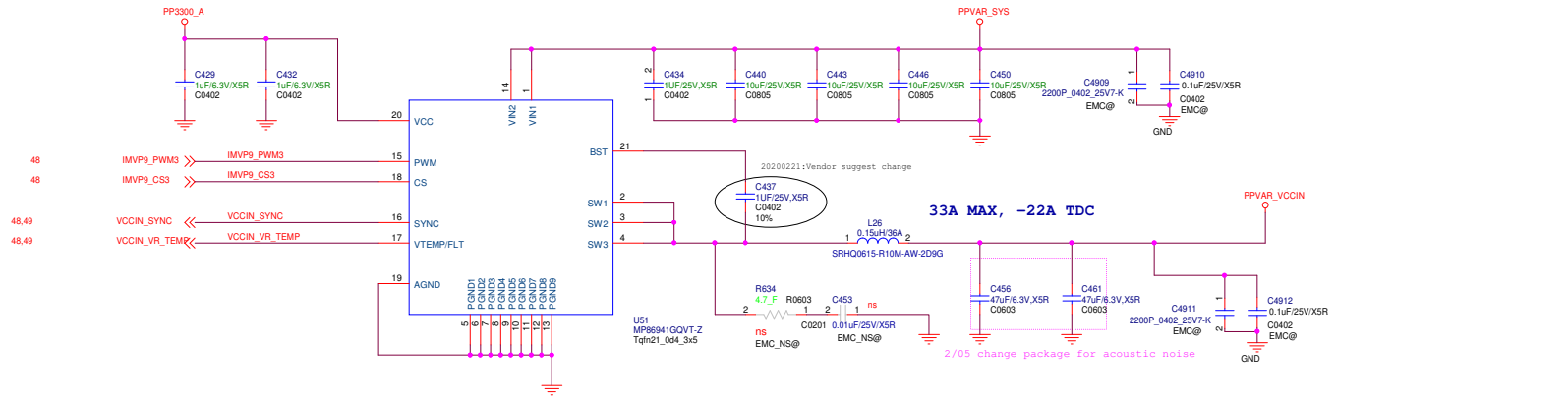
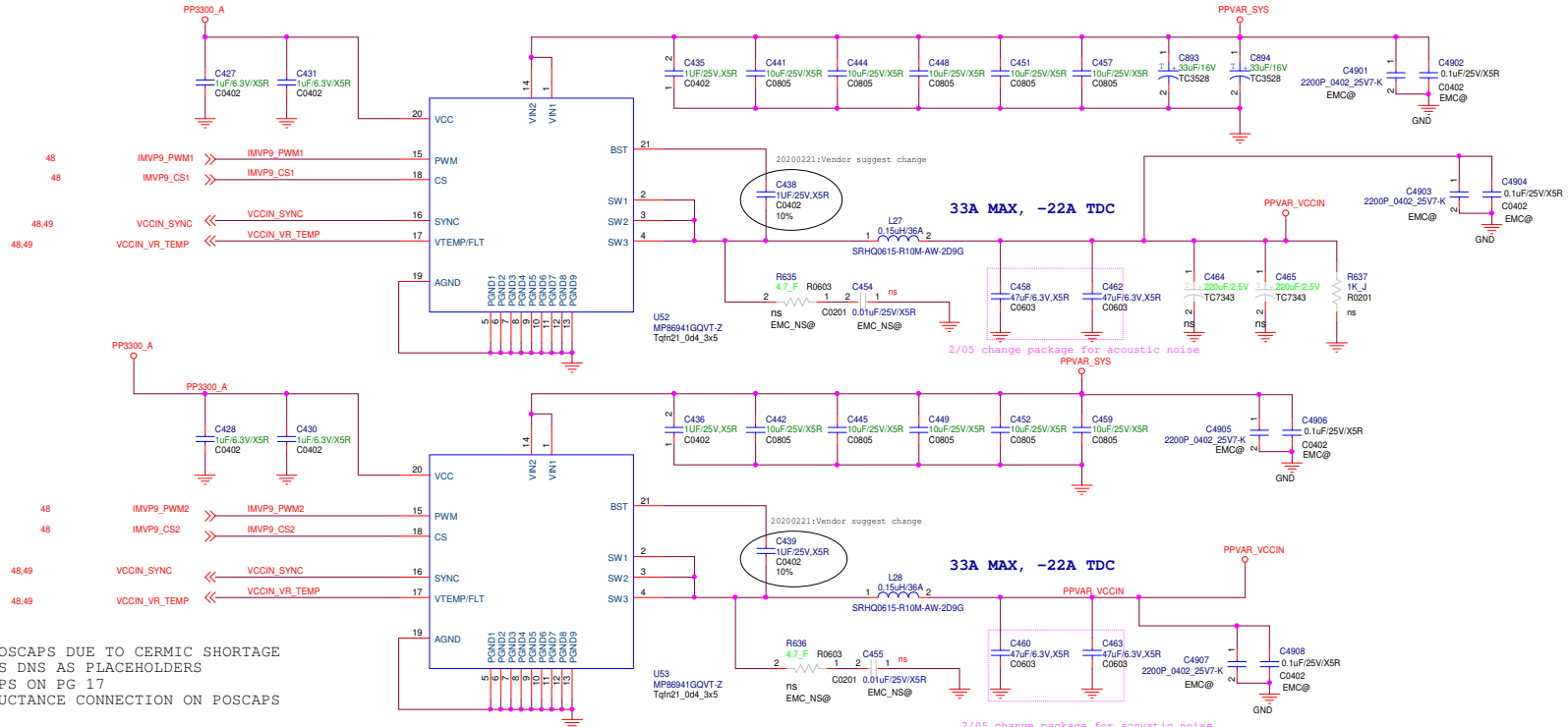
SETTINGS APW8743C

VNN	VOUT	VIN1
1.05	0	0
0.78	1	1

PP1050

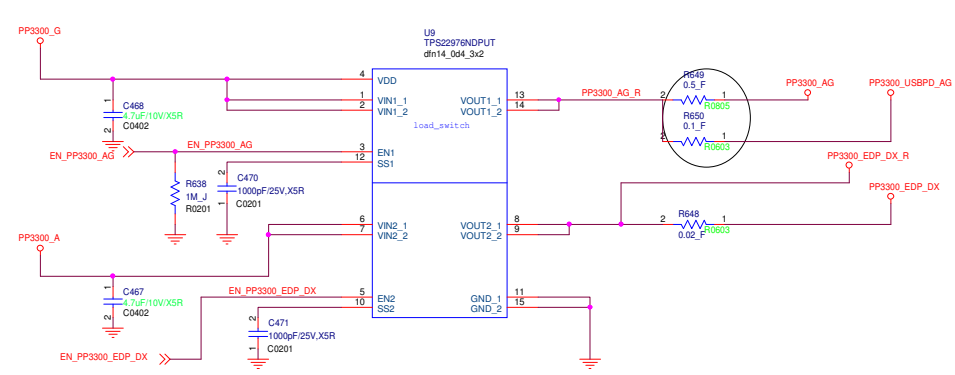
VOUT	VIN2
1.05	0
0.96	1



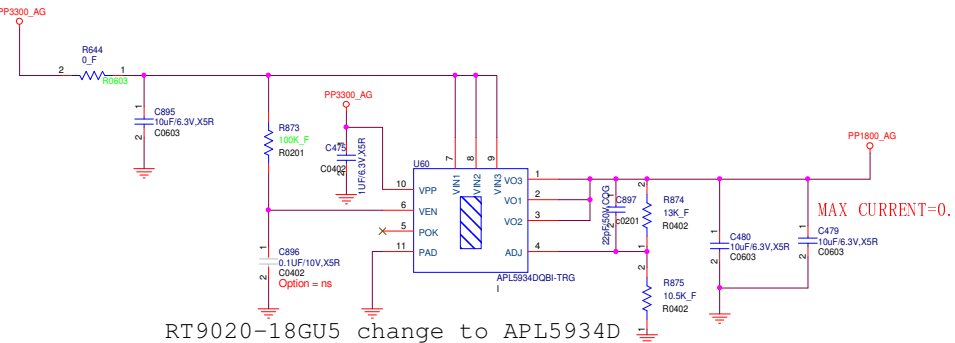


Delete U54/U55

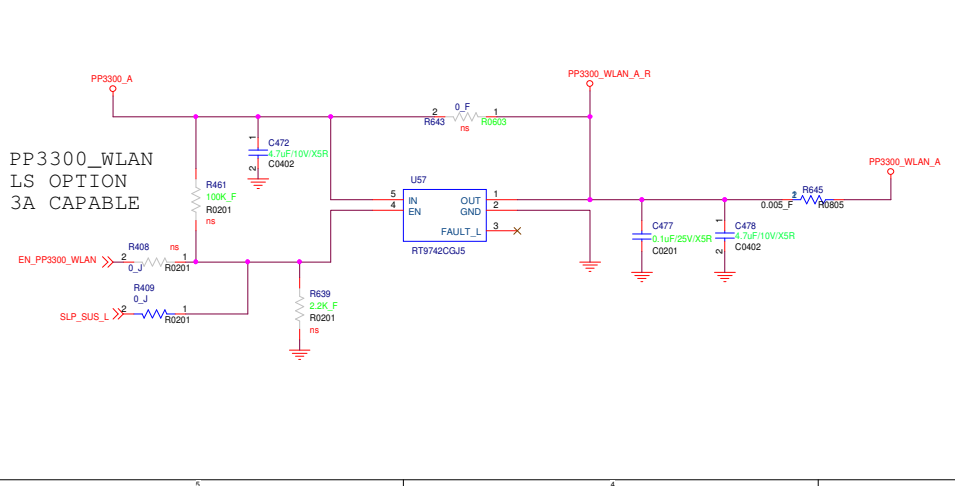
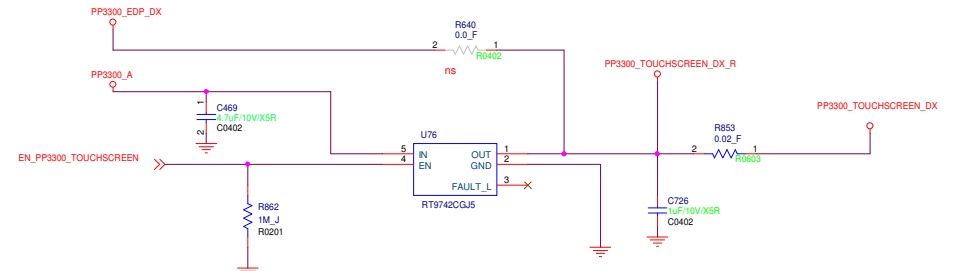
U54, U55 CIRCUITS NEEDED FOR INTEL ES SILICON
 PLAN TO REMOVE FOR PRODUCTION BUT NEED
 INTEL'S APPROVAL. SEE INTEL DOC# 614056



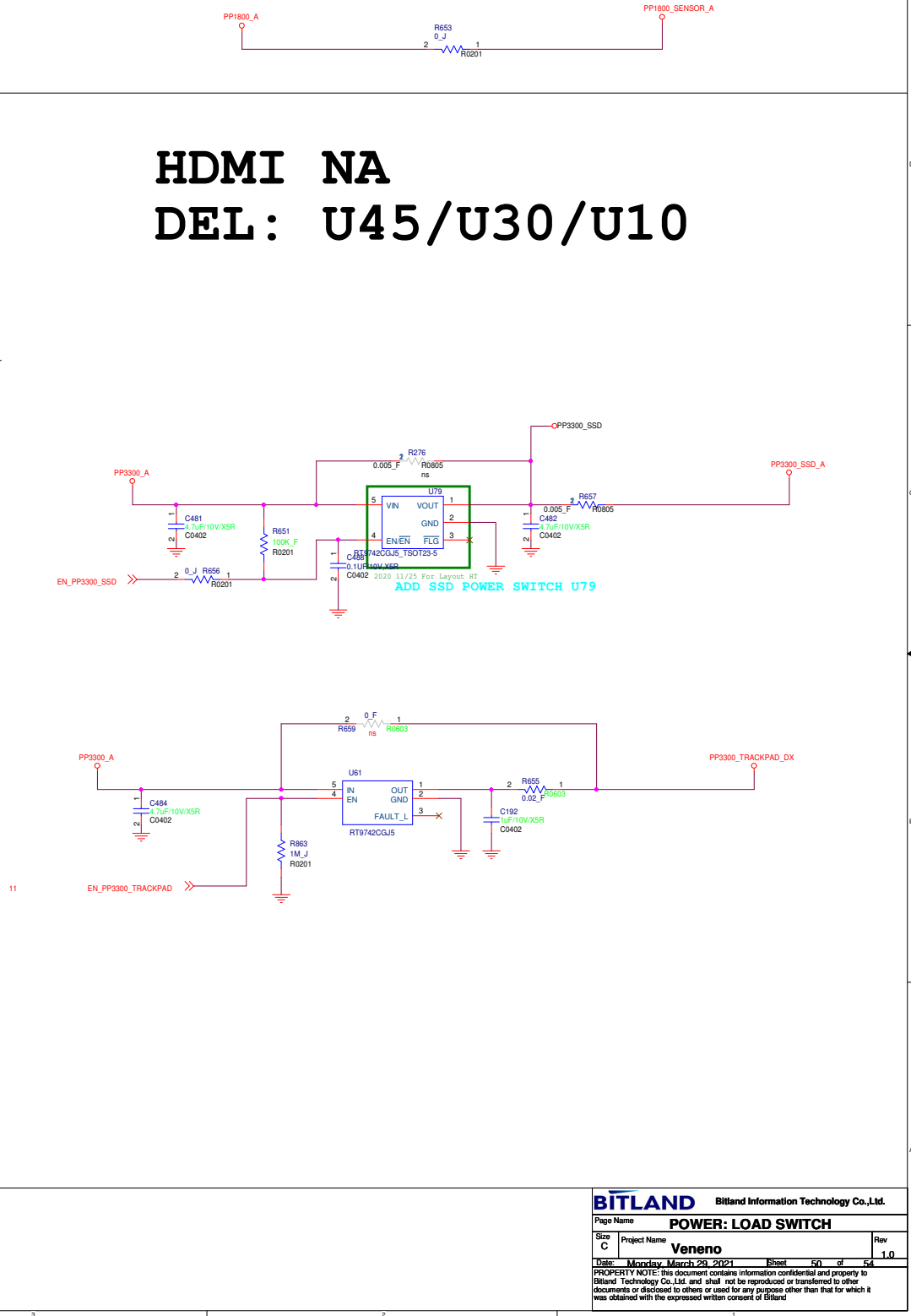
TURN ON: ~1.2MS FOR SS = 1000PF



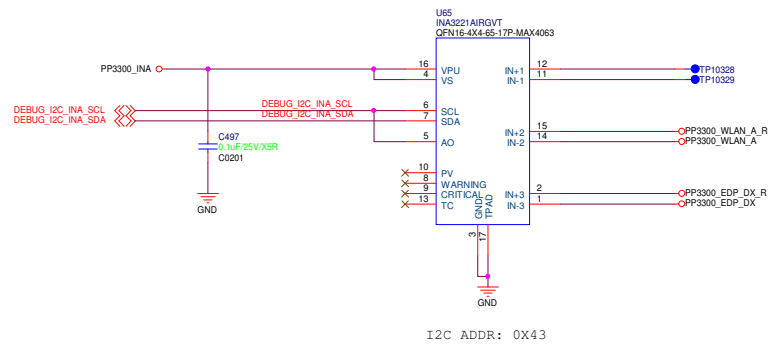
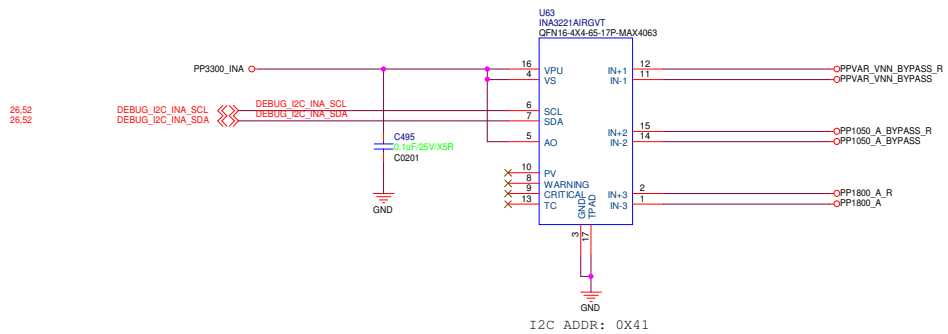
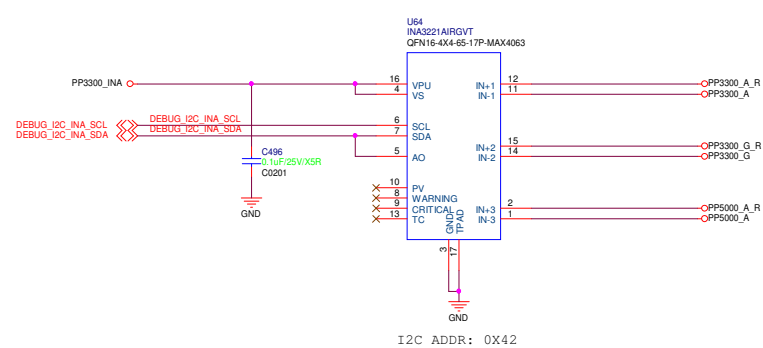
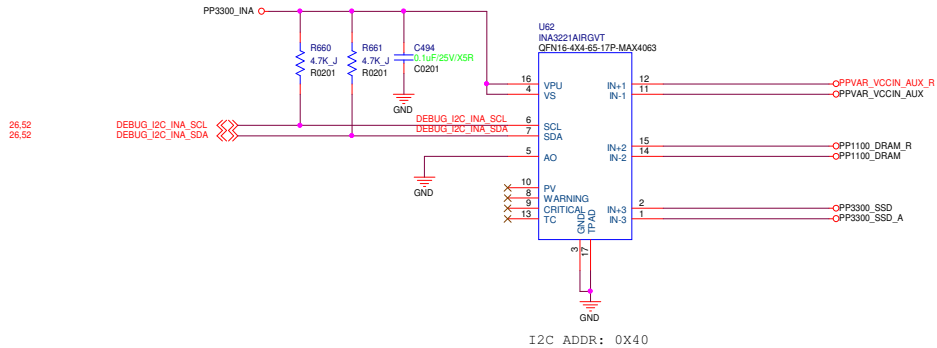
RT9020-18GU5 change to APL5934D



PP3300_WLAN
LS OPTION
3A CAPABLE



HDMI NA
DEL: U45/U30/U10



DB BOARD

3-AXIS ACCEL
7-BIT ADDRESS:0X19

C560 G-sensor
U27
LIS2DE12TR
LGA12 0D5 2x2

C184_2
0.1uF/25V/X5R
C0201
GND_G

C186_1
1uF/10V/X5R
C0201
GND_G

R310_2
10K_F
r0201
ns

DB_SENSOR_I2C_SDA
DB_SENSOR_I2C_SCL

R1_1 NEED CHANGE 49.2K

R2_2
0_J
ns
R0201

GND_G

GND_G

GND_G

Vdd_IO	Resistor value for SDO/SA0 pin	
	Typ. (k0)	
1.7V	54.4	
1.8V	49.2	
2.5V	30.4	
3.6V	20.4	

CON73 connect to PAGE33 J24, PIN41~44

DB_SENSOR_I2C_SDA
DB_SENSOR_I2C_SCL
DB_ACCEL_INT_L

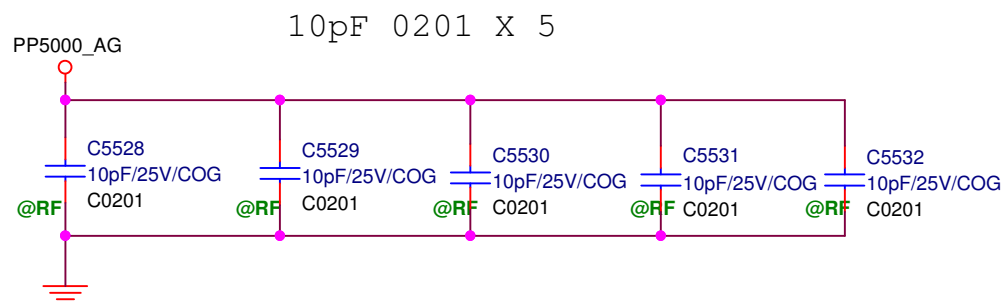
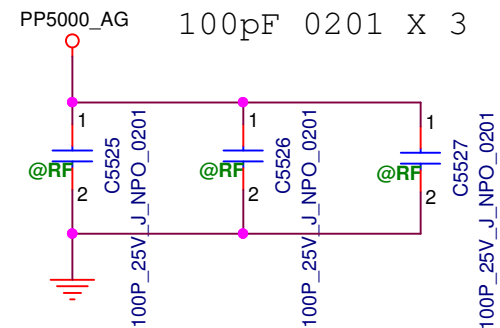
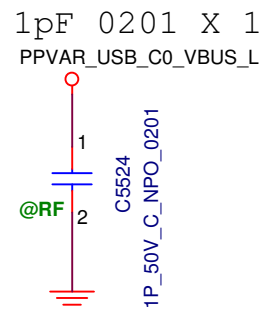
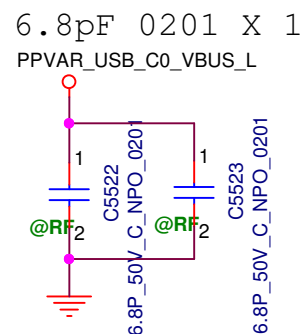
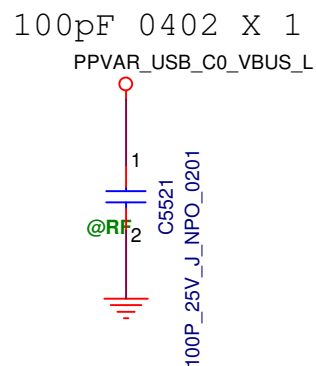
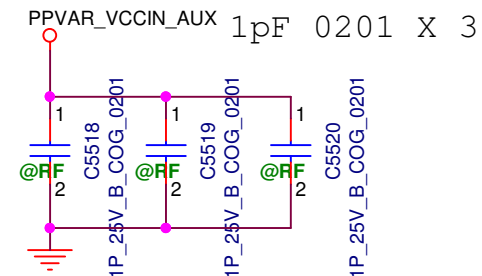
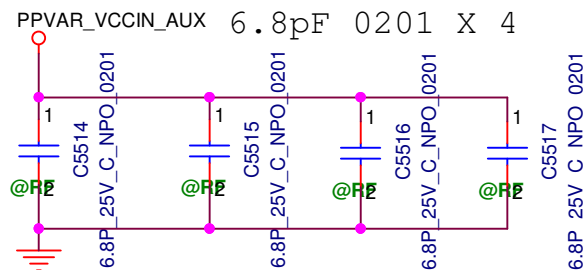
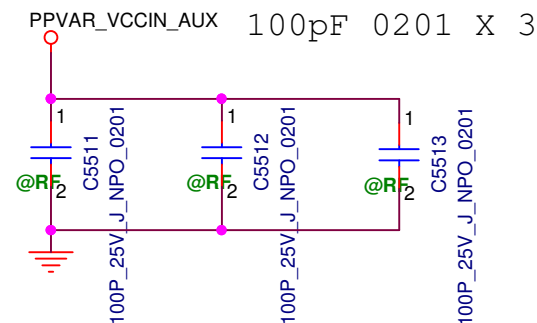
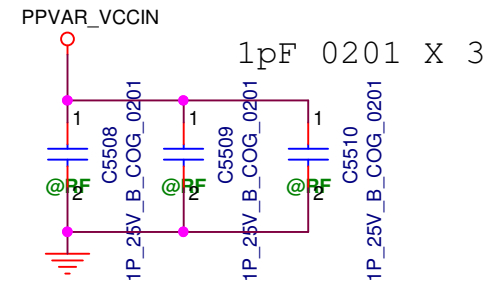
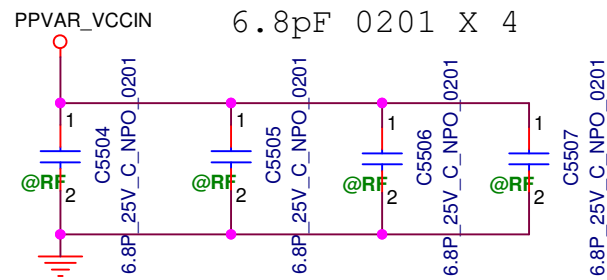
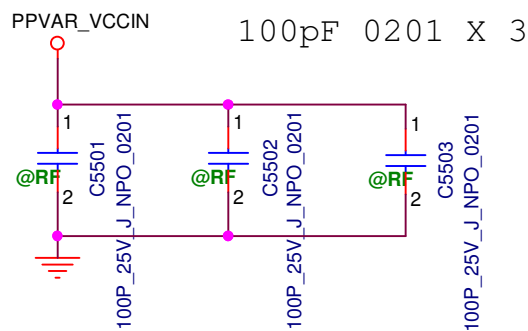
CON73
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cns6_0d6_r_50376

C5401
0.1uF
c0402
25V
X5R
@EMC

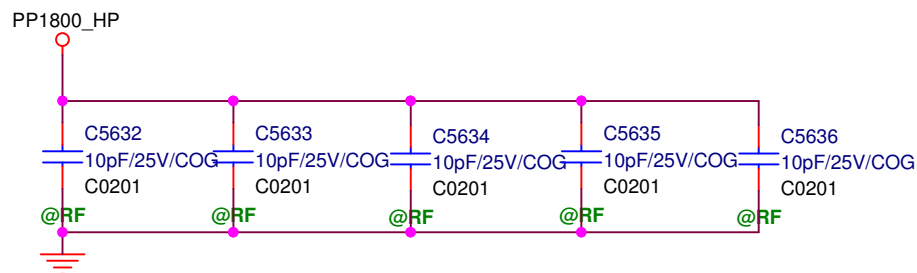
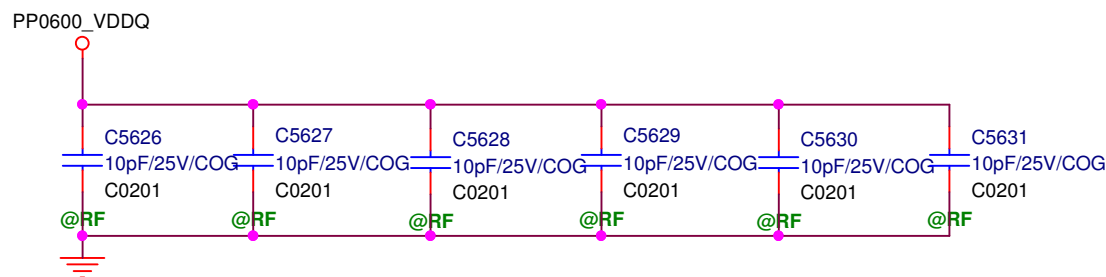
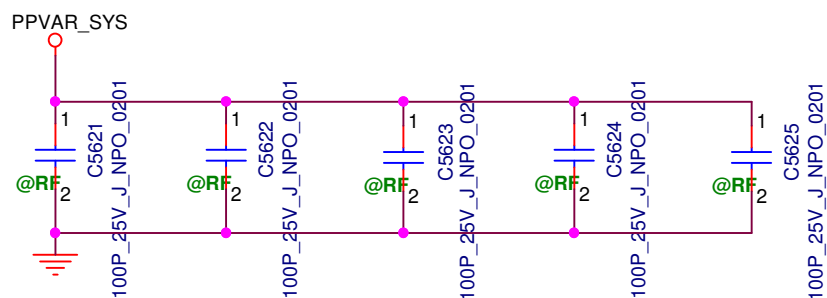
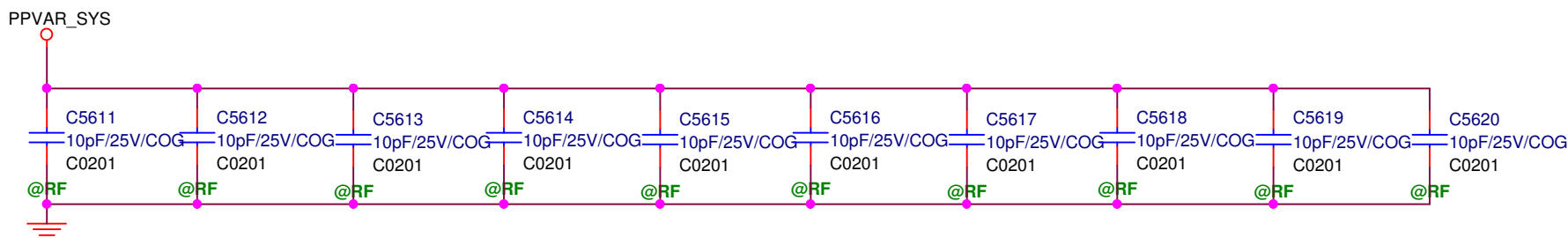
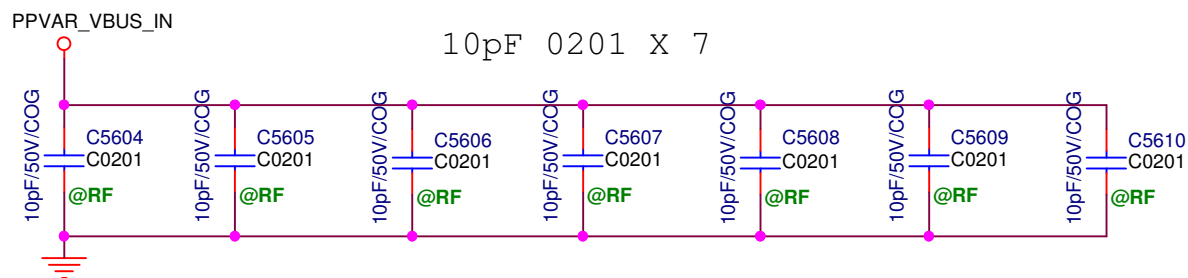
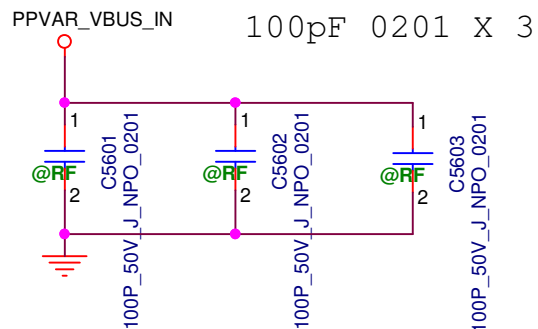
GND_G

EVT 11/3 (EMC@)

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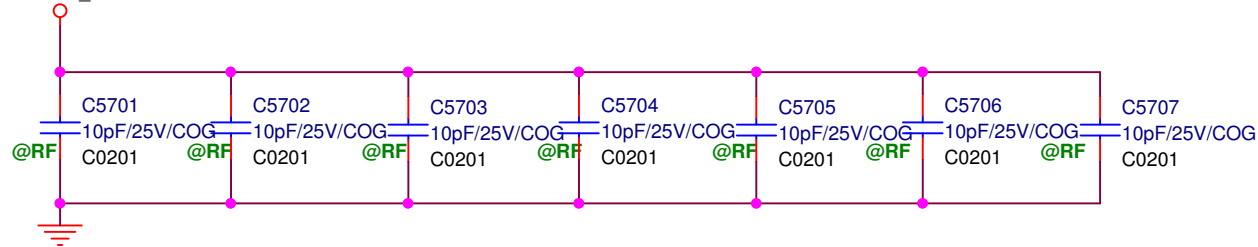


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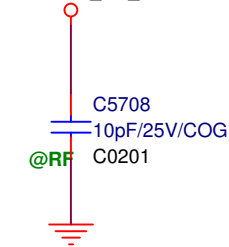


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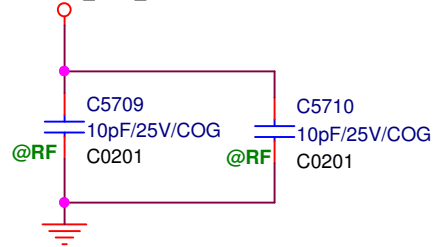
PP1100_DRAM



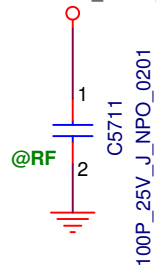
PP3300_SD_DX



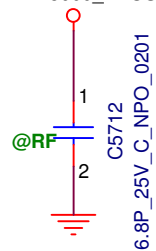
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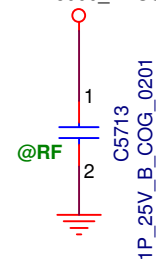
PP5000_VBUS_A0



PP5000_VBUS_A0



PP5000_VBUS_A0



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