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Notes:

Part Value Prefix : "*" means no stuff
Net Value suffix : "*" means Low Active
Part : "*" means NO STUFF

Quanta Computer Inc.
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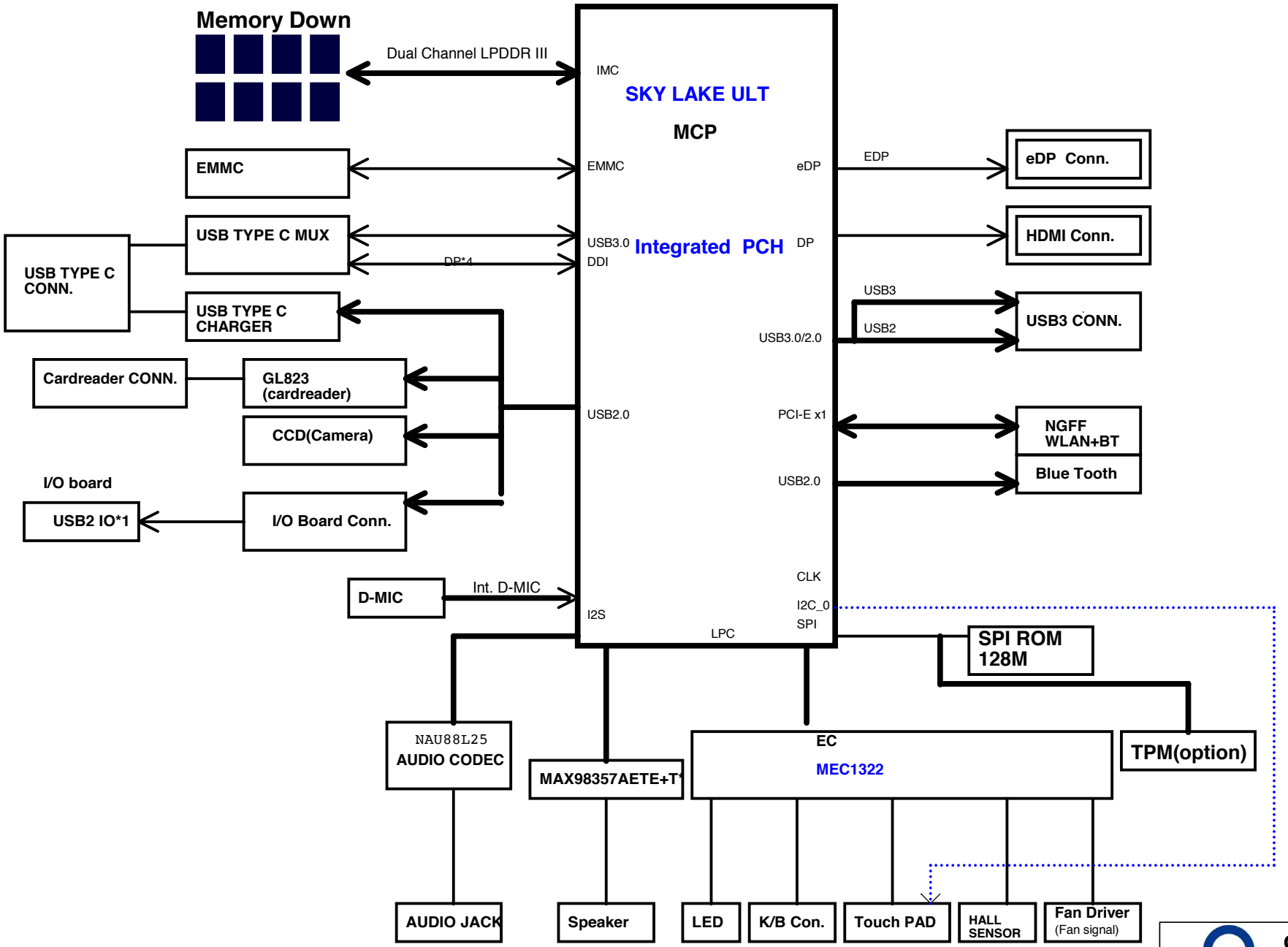
ZDA SKL ULT SYSTEM BLOCK DIAGRAM

02



Quanta Computer Inc.

PROJECT : ZDA

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SKL ULT - SYSTEM CTL

PCIe Clock	ASSIGNMENT
1	WIFI

U80J
SKYLAKE_ULT

CLOCK SIGNALS

+V3P3A
R1113 100K_2

[4,27,30] TRACKPAD_INT*
[26] WIFI_PCIE_CLK_DN
[26] WIFI_PCIE_CLK_DP
[26] WIFI_CLK_REQ*
[9] AUDIO_INT_WAK*

D42 CLKOUT_SRC_N_0
C42 CLKOUT_SRC_P_0
AR10 GPP_B_5_SRCCLKREQB_0
B42 CLKOUT_SRC_N_1
A42 CLKOUT_SRC_P_1
AT7 GPP_B_6_SRCCLKREQB_1
D41 CLKOUT_SRC_N_2
C41 CLKOUT_SRC_P_2
AT8 GPP_B_7_SRCCLKREQB_2
D40 CLKOUT_SRC_N_3
C40 CLKOUT_SRC_P_3
AT10 GPP_B_8_SRCCLKREQB_3
B40 CLKOUT_SRC_N_4
A40 CLKOUT_SRC_P_4
AU8 GPP_B_9_SRCCLKREQB_4
E40 CLKOUT_SRC_N_5
E38 CLKOUT_SRC_P_5
AU7 GPP_B_10_SRCCLKREQB_5

CLKOUT_ITPXDP_N F43
CLKOUT_ITPXDP_P E43
GPD_8_SUSCLK BA17
XTAL_IN E37
XTAL_OUT E35
XCLK_BIASREF E42
RTCX1 AM18
RTCX2 AM20
SRTCRSTB AN18
RTESTB AM16

CLKOUT_XDP_DN* [10]
CLKOUT_XDP_DP [10]
TP120
SUS_CLK [26]
XTAL24_IN
XTAL24_OUT
XCLK_BIASREF
RAP1091 2.7K/F_4
RTC_X1
RTC_X2
SRTCRST*
RTC_RST*

REV = 1
10 OF 20

RAP1089 *SHORT_4 XTAL24_IN_R
RAP1087 1M_4
RAP1090 *SHORT_4 XTAL24_OUT_R
C186 33P/50V_4
X5 24MHz,30ppm
C187 33P/50V_4
+VCCF24NS_1P0

RAP3052 *0_2
SRTCRST* [30]
RTC_RST* [30]

Trace length < 1000 mils
RTC_X1 C291 15P/50V_4
RAP1088 10M_4
X6 32.768KHz,20ppm
RTC_X2 C289 15P/50V_4

+V3P3A_RTC
RAP1072 20K_4
CAP1073 1U/6.3V_4
+V3P3A_RTC
RAP1078 20K_4
CAP1079 1U/6.3V_4

SRTC REST_N
0 - SAVE ME RTC REGISTER WHEN BATTERY IS REMOVED
1 - CLEAR ME RTC REGISTER

RTESTB
1 - SAVE REGISTER BIT IN RTC WELL (DEFAULT)
0 - RESETS THER REGISTER BITS IN THE RTC WELL

+V3P3S +V3P3A
RAP3046 *0_4
RAP3045 0_4
CPM4431 0.1U/16V_4
U135 SN74AHC1G08DCKR
[19,26,30] BUF_PCH_PLT_RST*
RAP3047 *100K_2
RAP3048 *0_4
TP105
TP103
TP104
[10,30] PCH_SYSRST*
[10,30] PCH_RSMRST*
[10,34] ROP_VCCST_PWRGD
[10,34] ROP_SYS_PWROK
[34,38] PCH_PWROK
[34,35] ROP_DSW_PWROK
[26] PCIE_WAKE*
[30] EC_PCH_WAKE*

+V3P3S RAP1003 10K_2
RAP1004 100K_2
+V3P3A_DSW RAP1061 100K_2
RAP1005 10K_2
RAP1011 10K_2
+V1P00S_VCCST+V3P3A RAP1008 100K_2
RAP1062 1K_2
RAP1002 *10K_2

RAP1067 1M_2
R3587 100K_2
CAP14472 *0.1u/10V_2

+V3P3A +V1P8S
RAP3049 10K_2
QPM3390 PJA138K
[16] TPM_PLTRST#
RAP3051 *0_2

PCH_PLT_RST*
PM_CPUPWRGD
VCCST_PWRGD_MCP
RAP1064 TP39 60.4_4
RAP1459 *SHORT_2
PCH_SUSPWRACK*
PCH_SUSACK*
PM_LANPHY_ENABLE
USB_WAKEOUT_INTRUDET*
TP17
TP18

U80K
SKYLAKE_ULT
SYSTEM POWER MANAGEMENT

AN10 GPP_B_13_PLTRSTB
B5 SYS_RESETB
AY17 RSMRSTB
A68 CPUPWRGD
B65 VCCST_PWRGD
B6 SYS_PWROK
BA20 PCH_PWROK
BB20 DSW_PWROK
AR13 GPP_A_13_SUSWARNB_SUSPWRDNACK
AP11 GPP_A_15_SUSACKB
BB15 WAKEB
AM15 GPD_2_LAN_WAKEB
AW17 GPD_11_LANPHYPC
AT15 GPD_7_USB2_WAKEOUTB

11 OF 20
REV = 1

+V3P3A_DSW +V3P3A_RTC
RAP3020 1M_2
RAP1081 *100K_2
RAP1077 10K_2
RAP1075 1M_4

TP100
TP101
TP102
TP75
TP79
TP20
TP78
TP21
TP22

GPP_B_12_SLP_S0B AT11
GPD_4_SLP_S3B AP15
GPD_5_SLP_S4B BA16
GPD_10_SLP_S5B AY16
PCH_SLP_S5*
SLP_SUSB AN15
SLP_LANB AW15
PCH_SLP_LAN*
GPD_9_SLP_WLANB BB17
PCH_SLP_WLAN*
GPD_6_SLP_AB AN16
PCH_SLP_SA*
GPD_3_PWRBTNB BA15
GPD_1_ACPRESENT AY15
GPD_0_BATLOWB AU13
PCH_BATLOW*
GPP_A_11_PMEB AU11
INTRUDERB AP16
EC_HID_INT*
SM_INTRUDER*
GPP_B_11_EXT_PWR_GATEB AM10
GPP_B_2_VRALERTB AM11
MPHY_EXT_PWR_GATE*

PM_SLP_S0* [30,34]
PM_SLP_S3* [30,34,36,37]
PM_SLP_S4* [30,34,35,36]
PCH_EC_SLP_SUS* [30]
RAP1458 *0_2
RAP1457 *SHORT_2
ROP_PCH_PWRBTN* [34]
EC_PCH_PWRBTN* [10,30]
R5150 100K/F_4
EC_PCH_ACPRESENT [30]
HSJ_MIC_DET [28]

Quanta Computer Inc.
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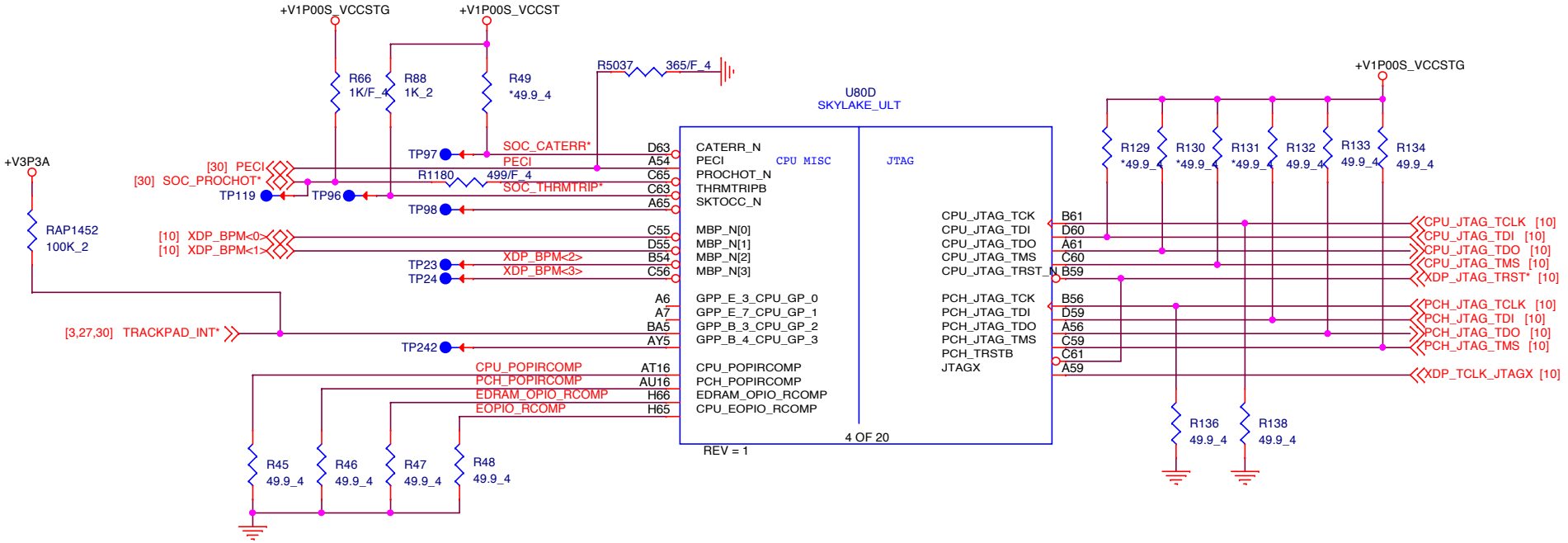
SKL ULT - DEBUG



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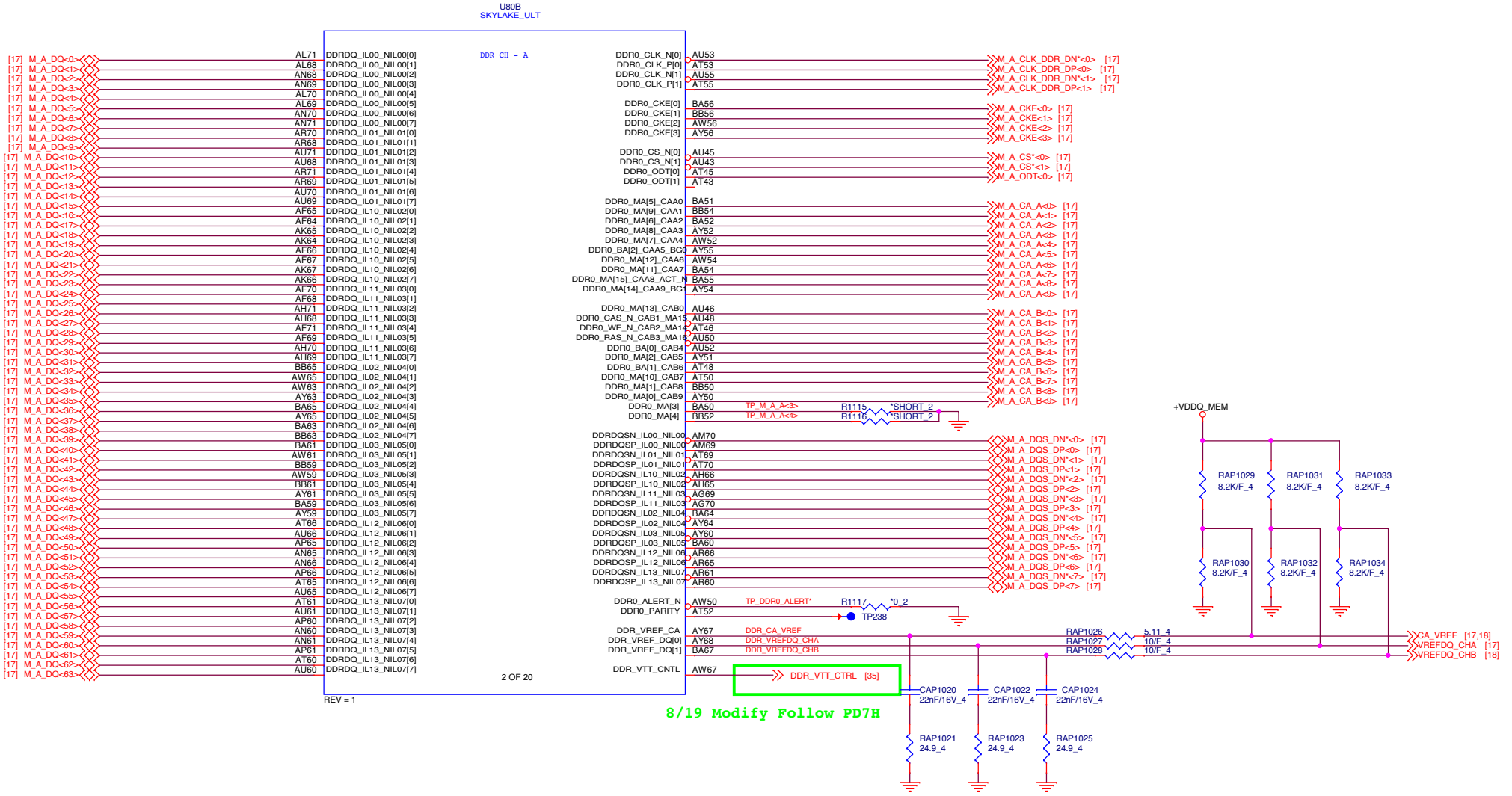
SKL ULT - DDR CHANNEL A



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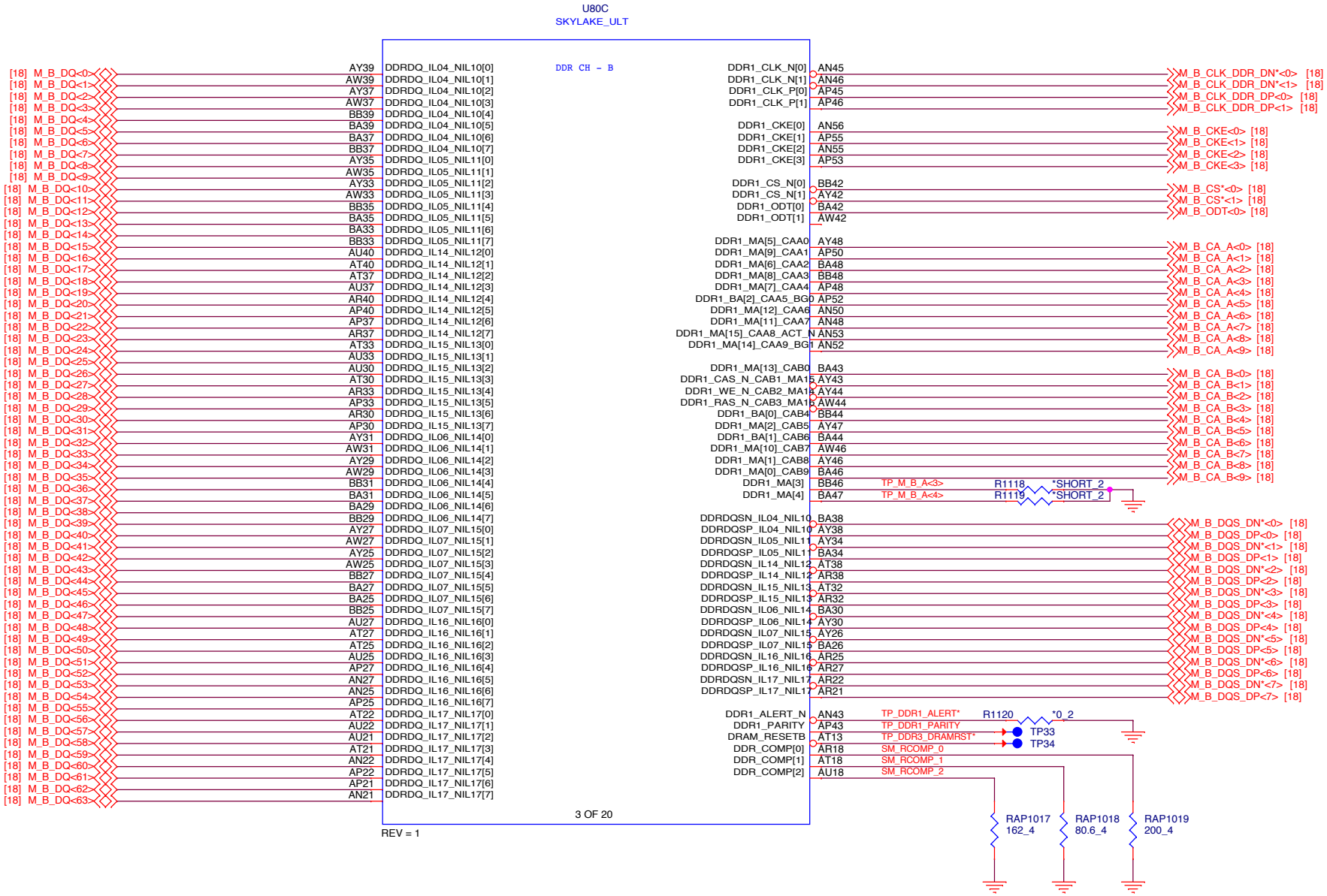
SKL ULT - DDR CHANNEL B



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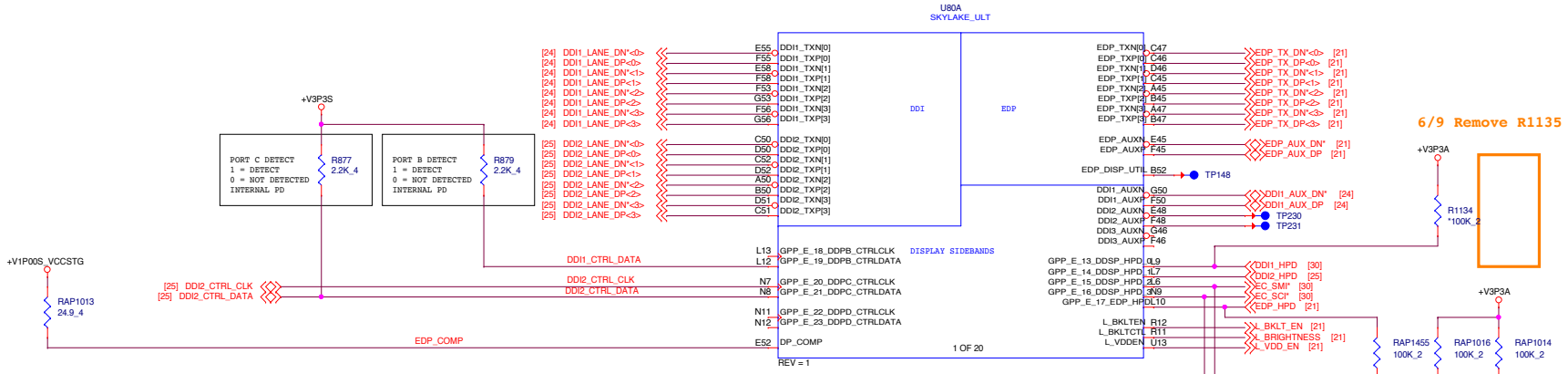
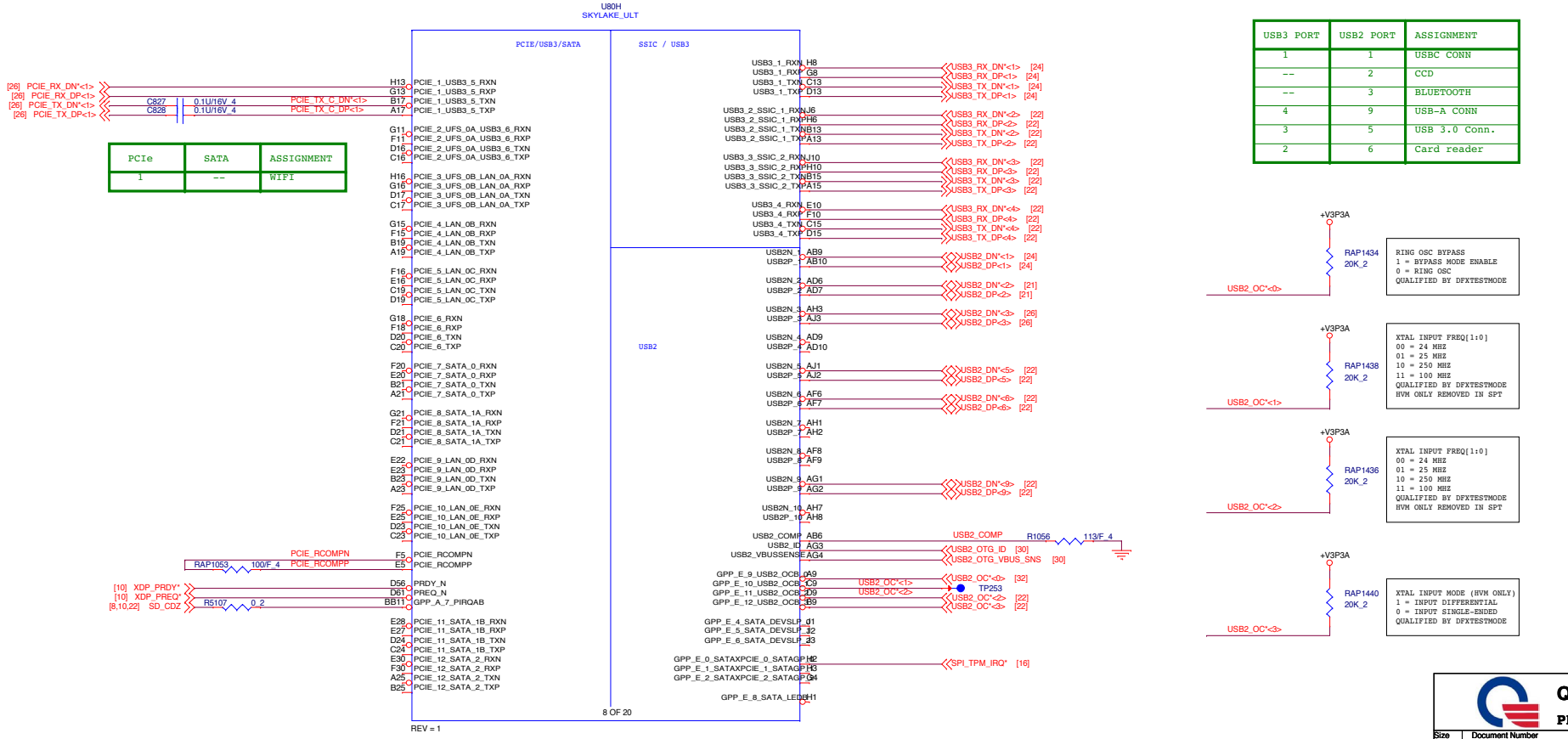
SKL ULT - PCIE/SATA/USB/SSIC/DSI/CSI





PCIe	SATA	ASSIGNMENT
1	--	WIFI

USB3 PORT	USB2 PORT	ASSIGNMENT
1	1	USBC CONN
--	2	CCD
--	3	BLUETOOTH
4	9	USB-A CONN
3	5	USB 3.0 Conn.
2	6	Card reader

Quanta Computer Inc.

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	SKL ULT - PCIE/SATA/USB/DSI	8A

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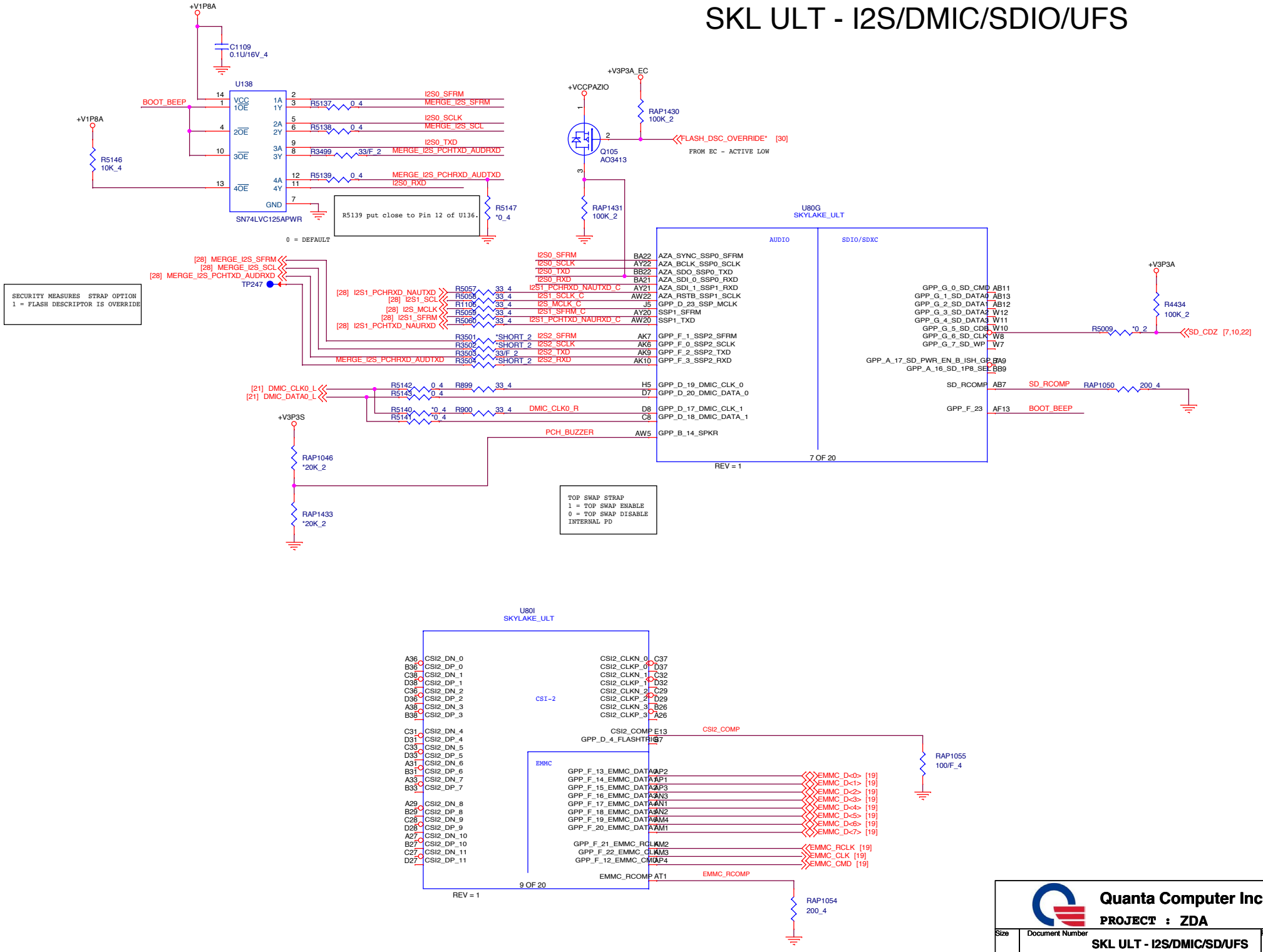
SKL ULT - I2S/DMIC/SDIO/UFS



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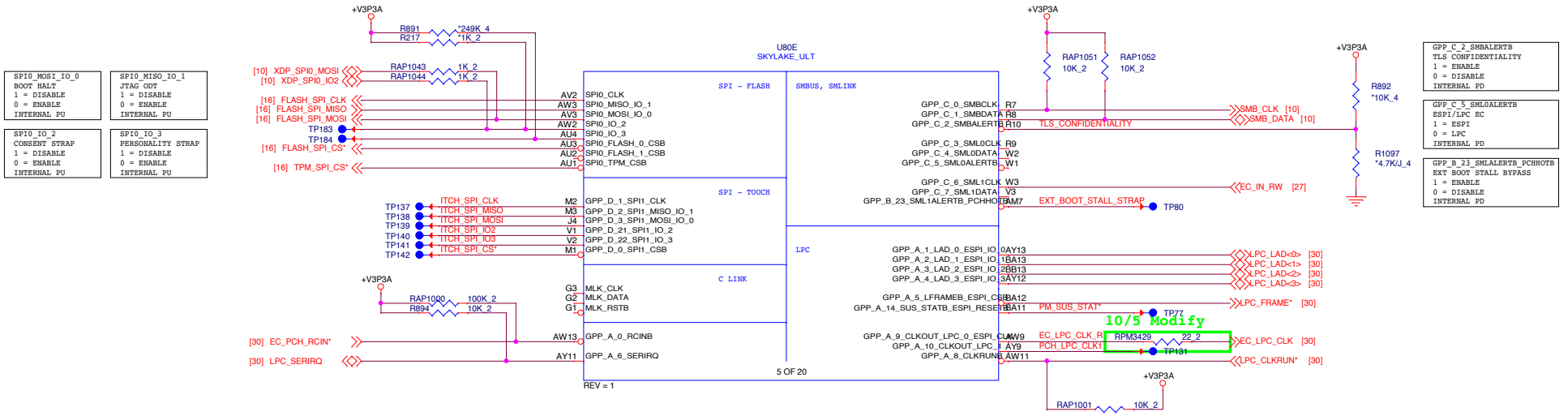
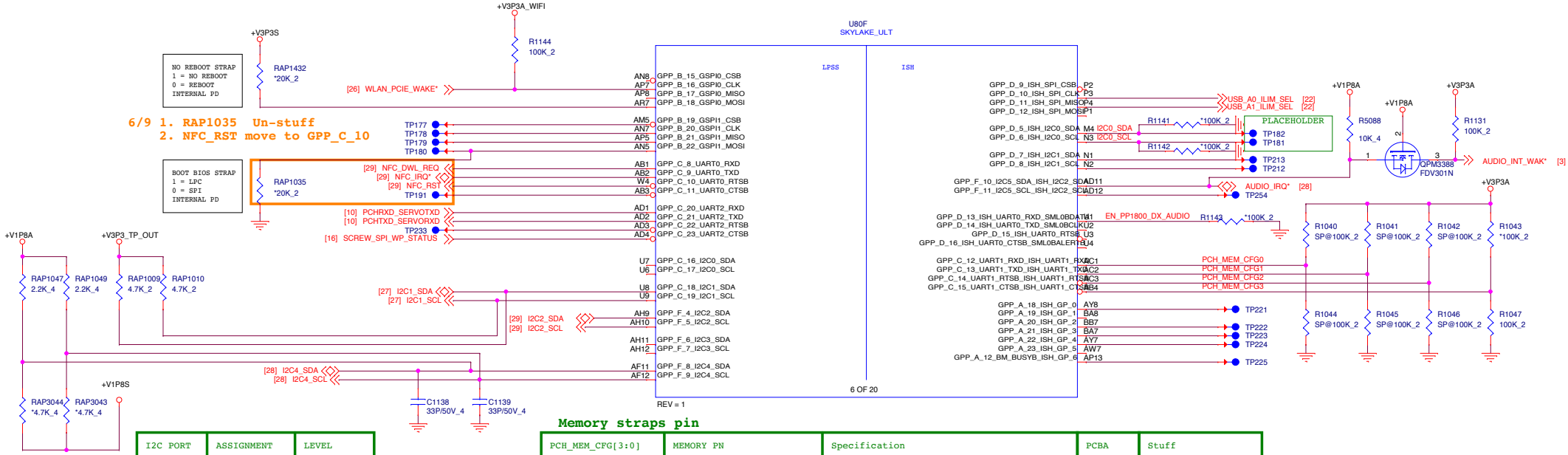
SKL ULT - SPI/LPC/SMB/ISH





Memory straps pin

I2C PORT	ASSIGNMENT	LEVEL
0	RESERVED	+3.3V
1	TRACKPAD	+3.3V
2	NFC	+1.8V
3	RESERVED	+1.8V
4	AUDIO CODEC	+1.8V
ISH 0	ISH	+1.8V

PCH_MEM_CFG[3:0]	MEMORY PN	Specification	PCBA	Stuff
0 0000	H9CCNNN8JTBLAR-NUD	(HYX ,SINGLE CHANNEL (2PCS), 2GB, 1866Mbps)	31x00	R1044,R1045,R1046
1 0001	H9CCNNNBLTBLAR-NUD	(HYX , DUAL CHANNEL (4PCS) ,8GB, 1866Mbps)	31x20	R1040,R1045,R1046
2 0010	K4E8E324EB-EGCF	(SAM , DUAL CHANNEL (4PCS) ,4GB, 1866Mbps)	31x10 , 31x70	R1044,R1041,R1046
3 0011	K4E8E324EB-EGCF	(SAM ,SINGLE CHANNEL (2PCS), 2GB, 1866Mbps)	31x30	R1040,R1041,R1046
4 0100	H9CCNNNBLTBLAR-NUD	(HYX ,SINGLE CHANNEL (2PCS), 4GB, 1866Mbps)	31x40	R1044,R1045,R1042
5 0101	K4E6E304EB-EGCF	(SAM , DUAL CHANNEL (4PCS) ,8GB, 1866Mbps)	31x50	R1040,R1045,R1042
6 0110	H9CCNNN8JTBLAR-NUD	(HYX ,DUAL CHANNEL (4PCS) ,4GB, 1866Mbps)	31x80 , 31x90	R1044,R1041,R1042

K4E6E304EB-EGCF (2GB, 1866Mbps)

EDF8132A3MA-JD-F (1GB, 1866Mbps)

Quanta Computer Inc.

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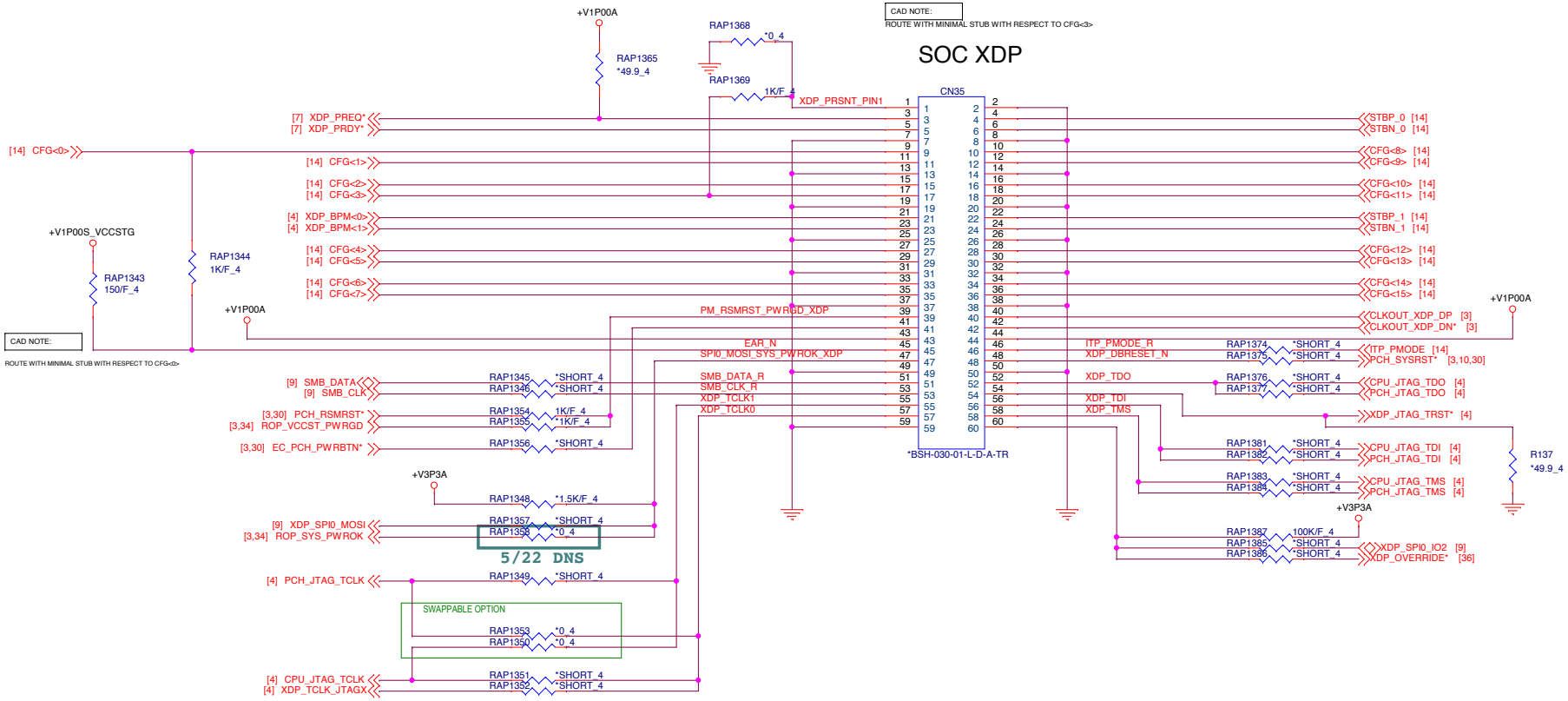
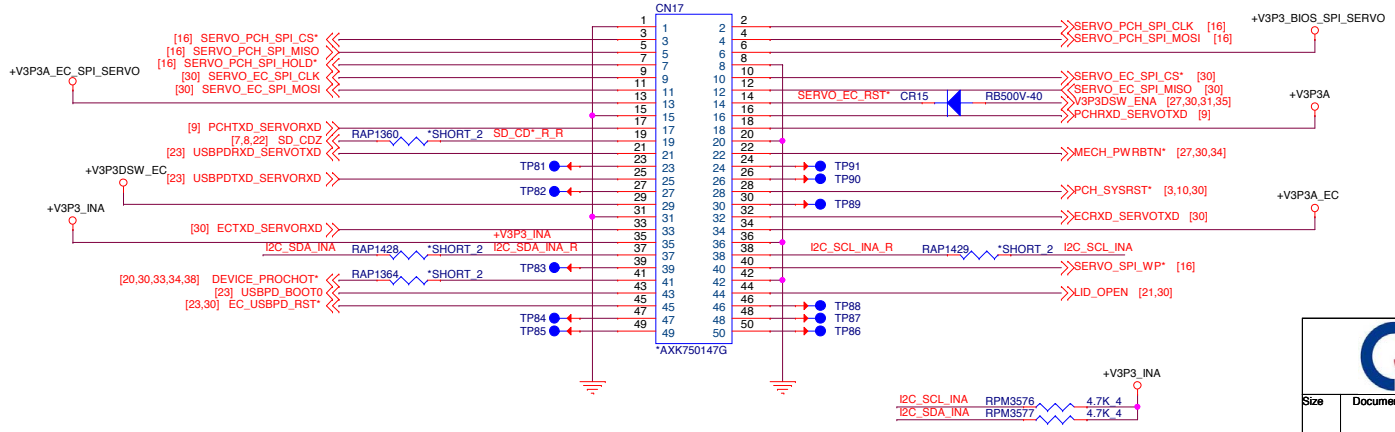
SKL ULT - XDP/CHROME SERVO

For Production systems unstuff ITP header and RAP1348. For ITP to function these 2 components need to be stuffed.

SOC XDP



GOOGLE CHROME SERVO SOCKET CONNECTOR



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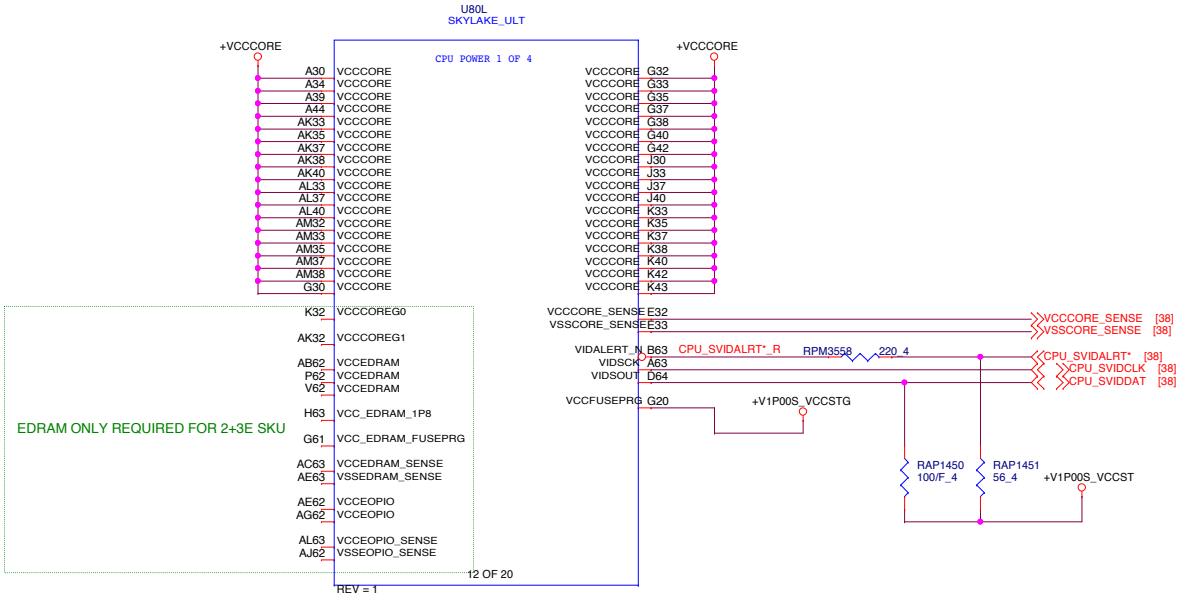
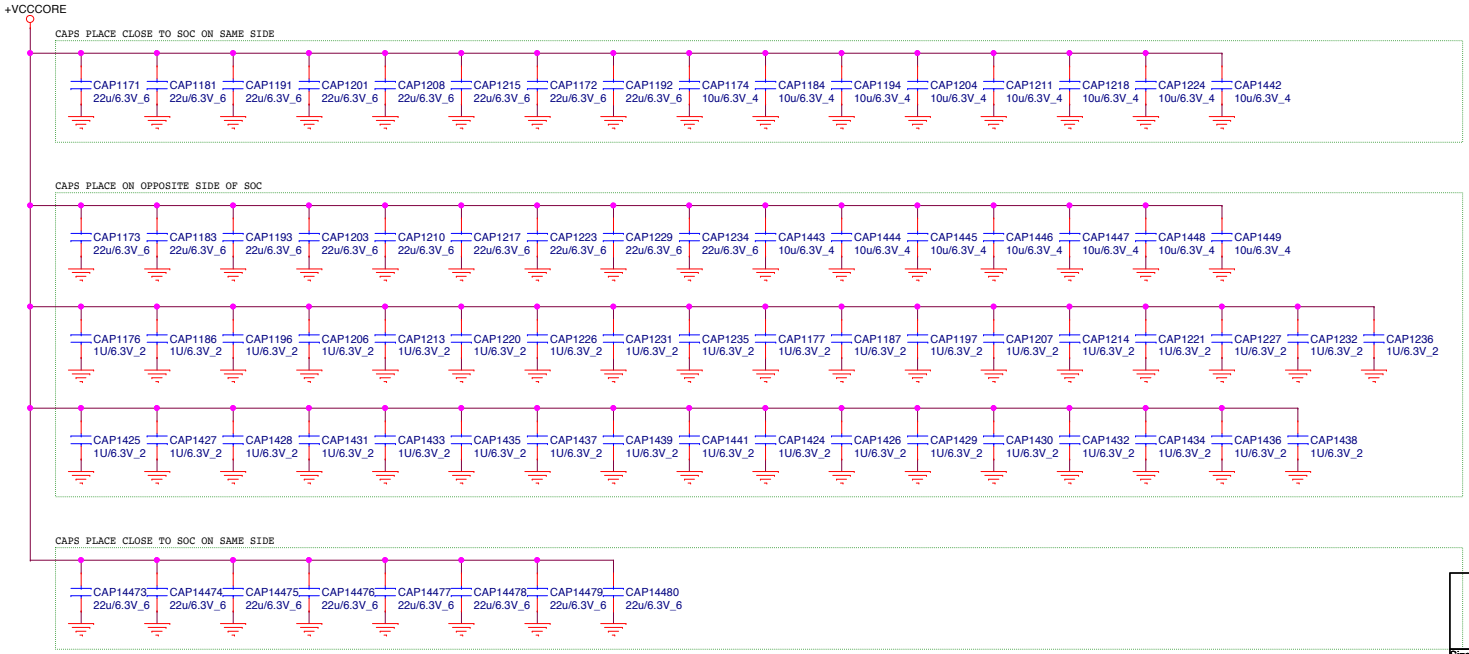
SKL ULT - POWER CORE



CORE



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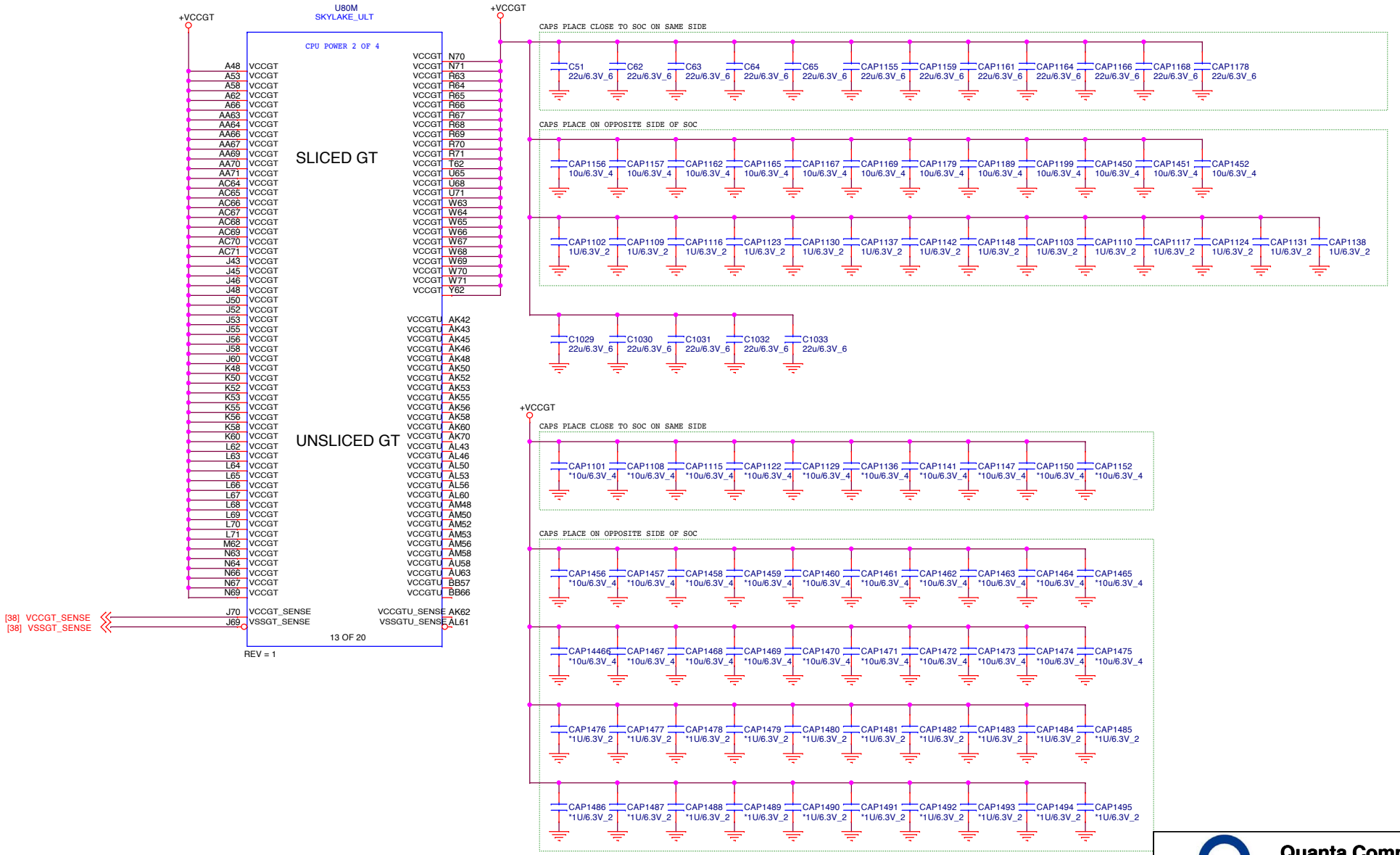
SKL ULT - POWER GRAPHICS



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	SKL ULT - GT POWER	8A

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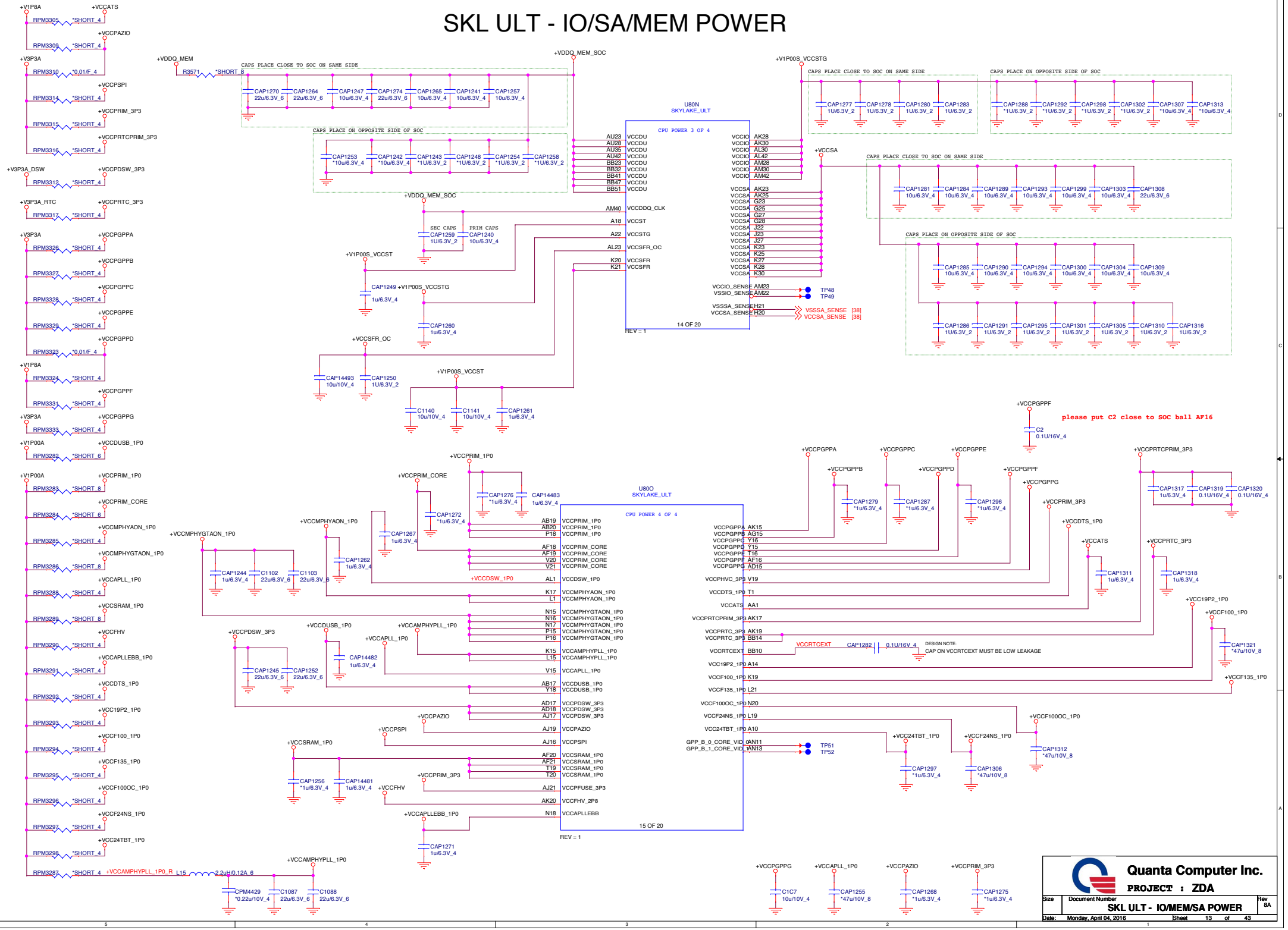
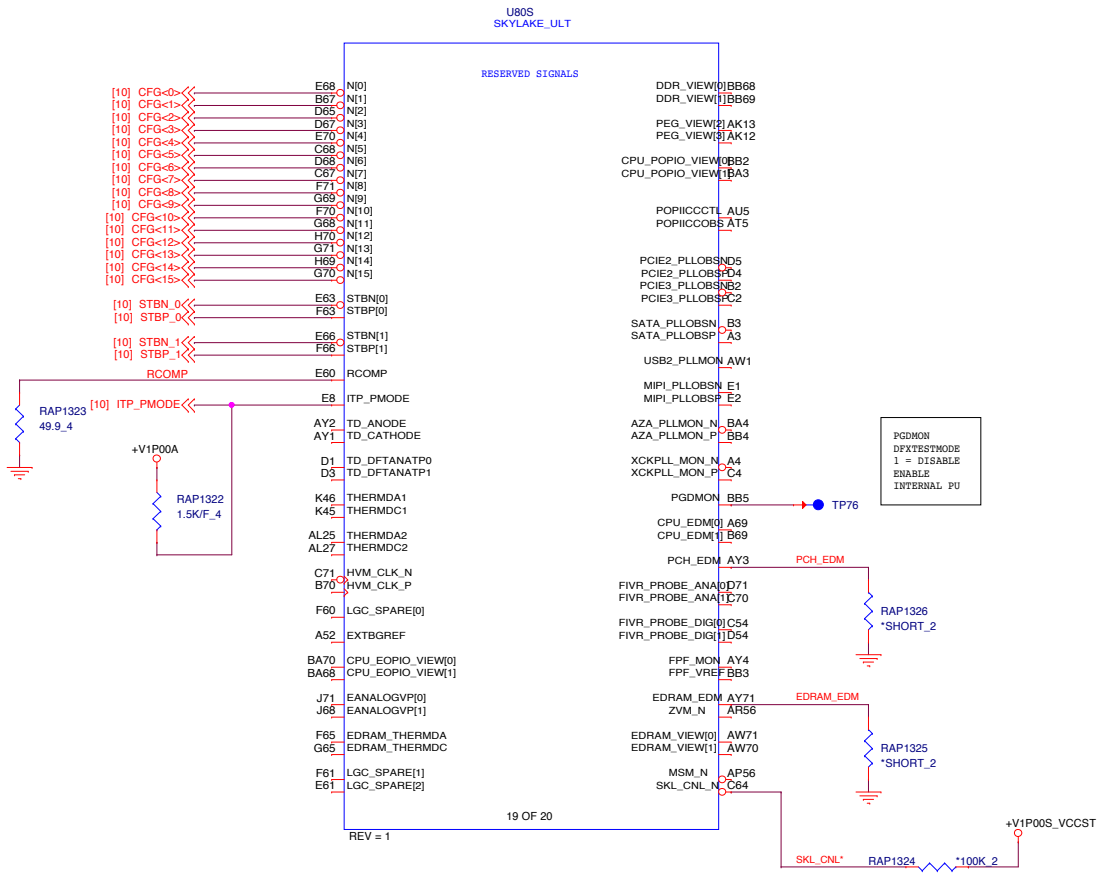
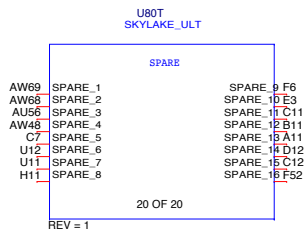
SKL ULT - IO/SA/MEM POWER



SKL ULT - RESERVED





EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	
CFG0	1:(DEFAULT) NORMAL OPERATION; NO STALL 0:STALL

CFG<0>
RAP1328
*1K_2

JUST A PLACEHOLDER - NO PEG FOR ULX/ULT PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: (DEFAULT)NORMAL OPERATION; 0: LANE REVERSAL

CFG<2>
RAP1330
*1K_2

PHYSICAL DEBUG ENABLED (DFX PRIVACY)	
CFG3	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

CFG<3>
RAP1331
*1K_2

DISPLAY PORT PRESENCE STRAP	
CFG4	0: ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1: DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

CFG<4>
RAP1332
1K_2

CFG<5>
JUST A PLACEHOLDER.
NOT NEEDED FOR ULX-ULT
RAP1327
*1K_2

CFG<6>
JUST A PLACEHOLDER.
NOT NEEDED FOR ULX-ULT
RAP1333
*1K_2

PCIE PORT BIFURCATION STRAPS	
CFG[6:5]	11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED 10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED 01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED 00: DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

Reserve	
CFG8	1: DISABLED(DEFAULT) 0: ENABLED; WILL BE

CFG<8>
RAP1335
*1K_2

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1:VRS SUPPORTING SVID PROTOCOL ARE PRESENT 0:NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

CFG<9>
RAP1336
*1K_2

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

CFG<10>
RAP1337
*1K_2

Quanta Computer Inc.
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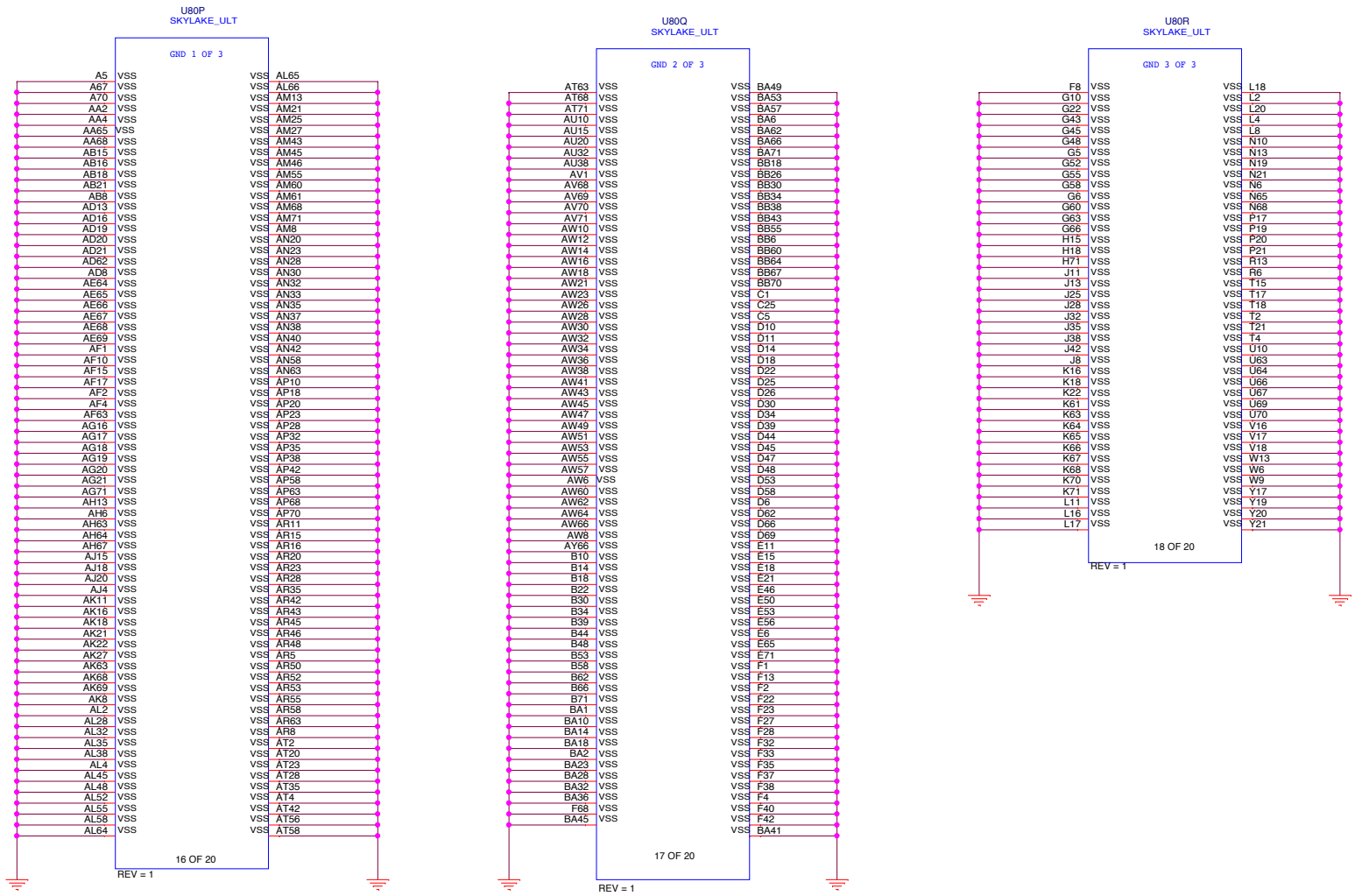
SKL ULT - GND



Quanta Computer Inc.

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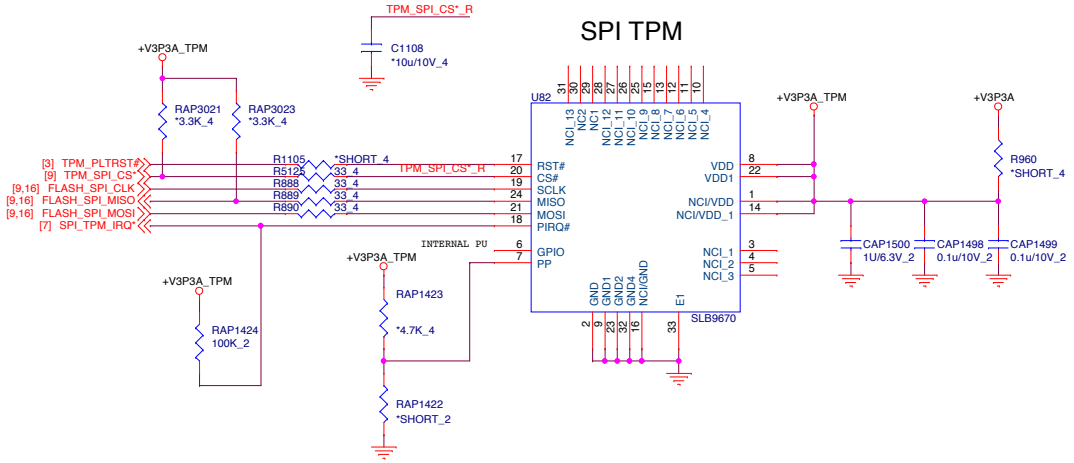
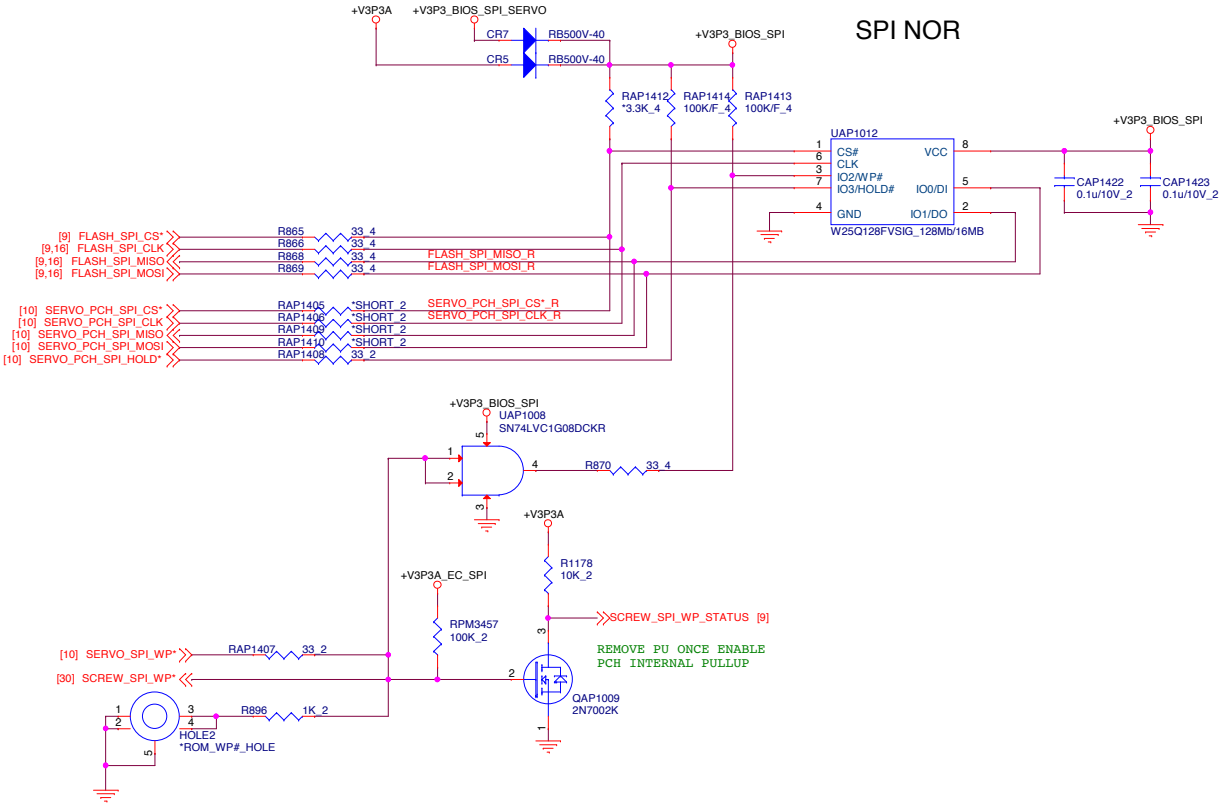
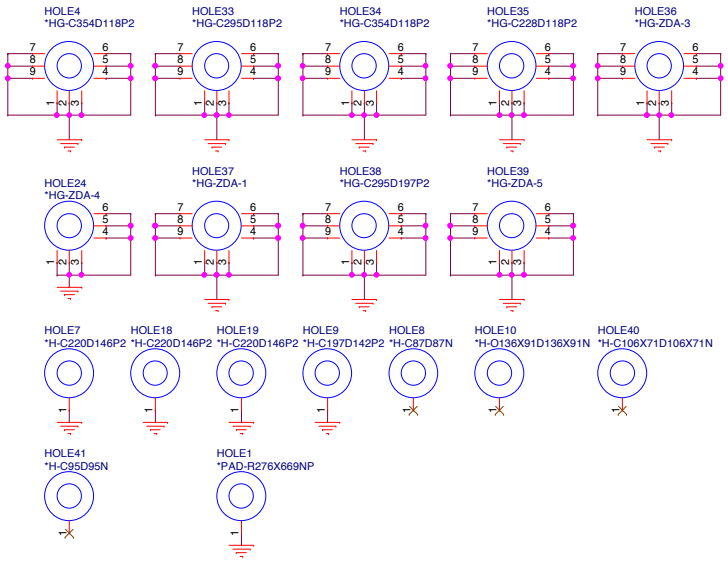
TPM & BOOT ROM

SPI TPM



SPI NOR





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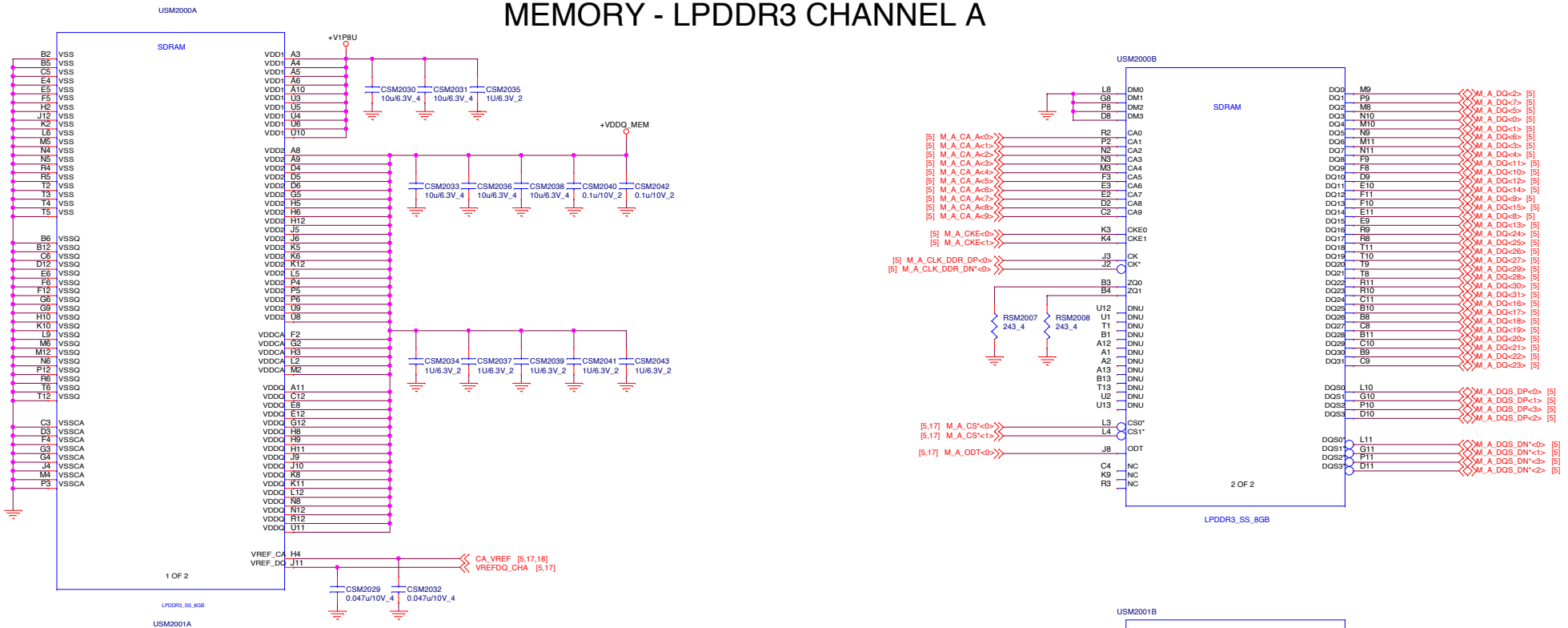
MEMORY - LPDDR3 CHANNEL A



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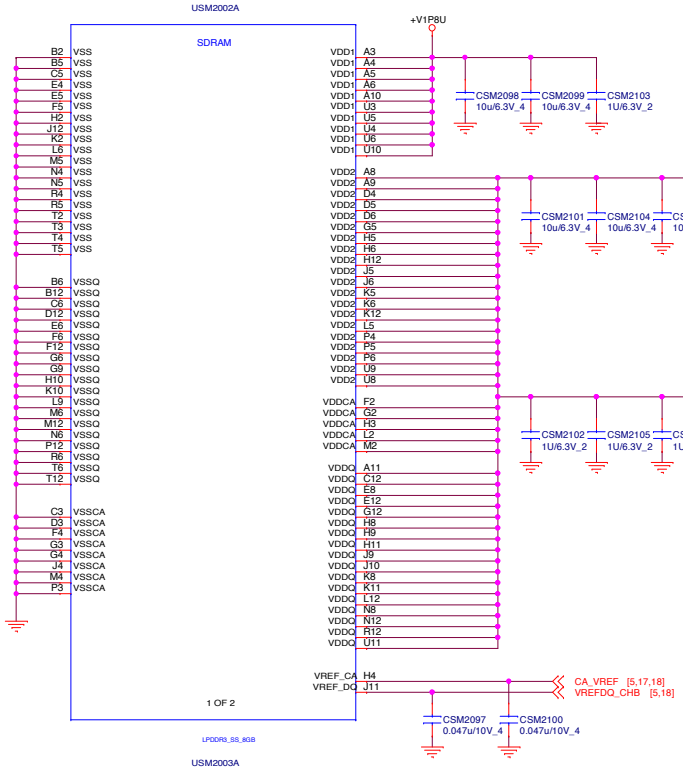
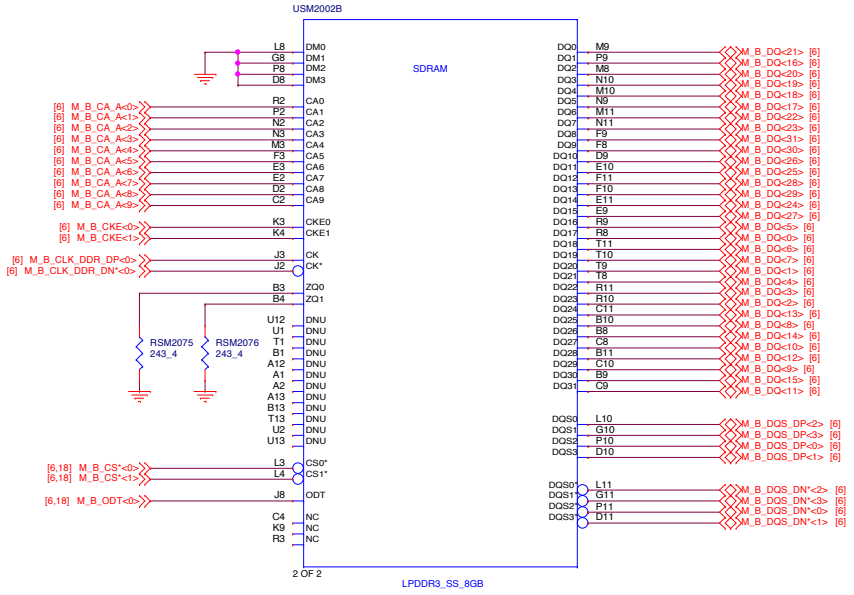
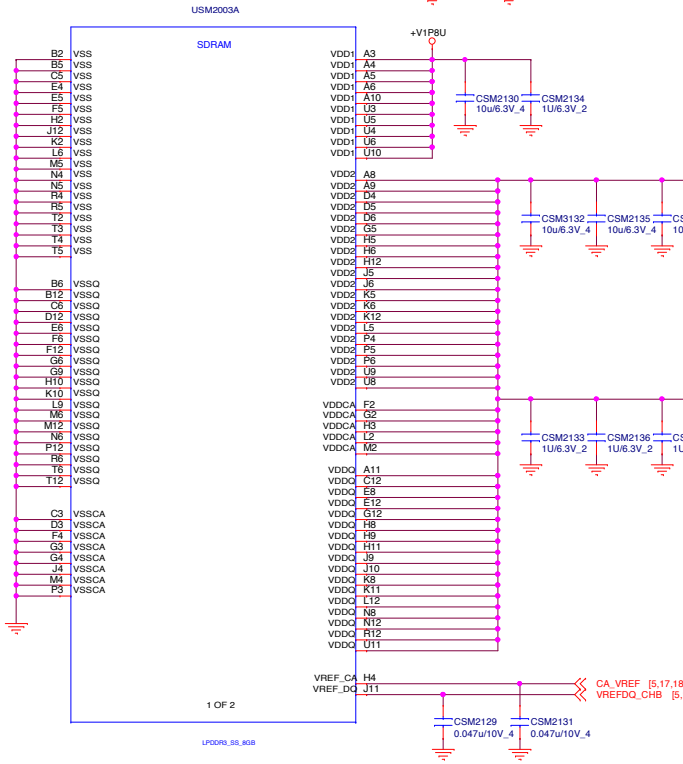
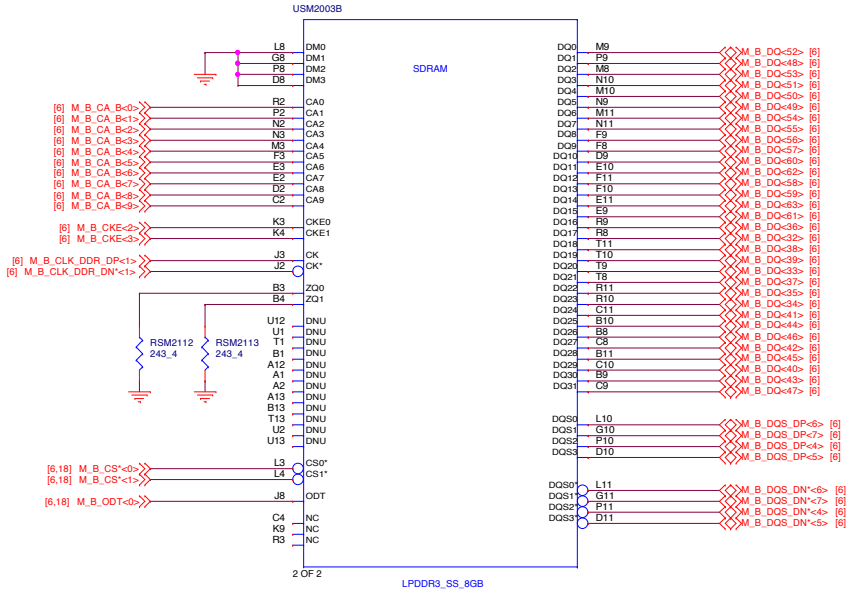
MEMORY - LPDDR3 CHANNEL B









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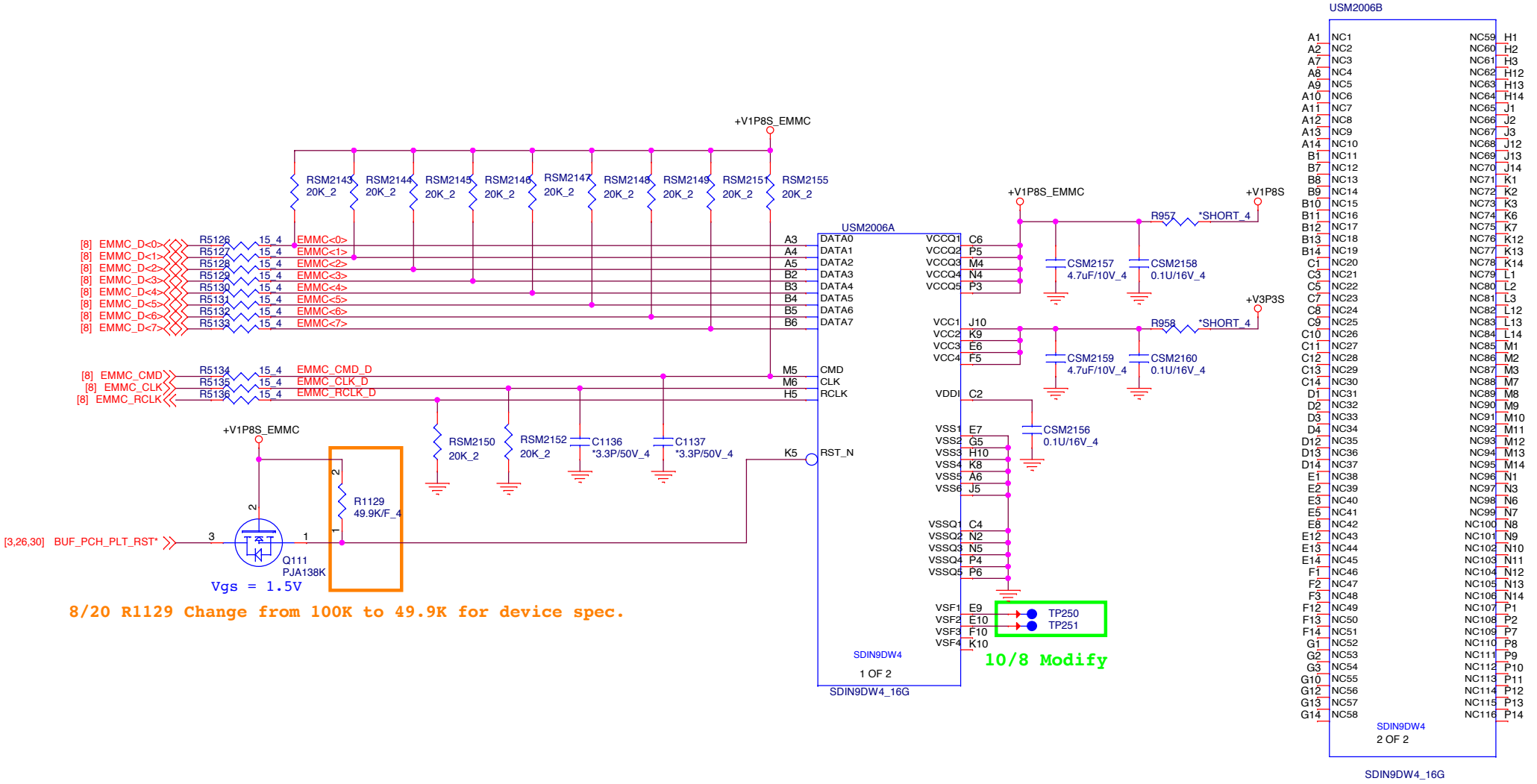
EMMC



Quanta Computer Inc.		
PROJECT : ZDA		
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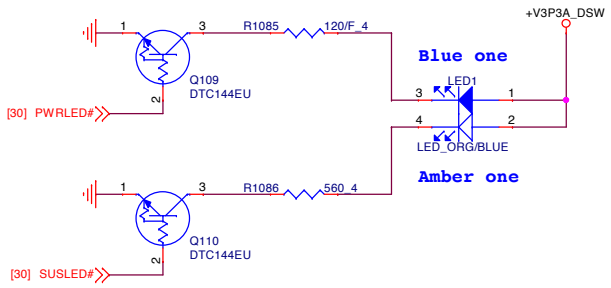
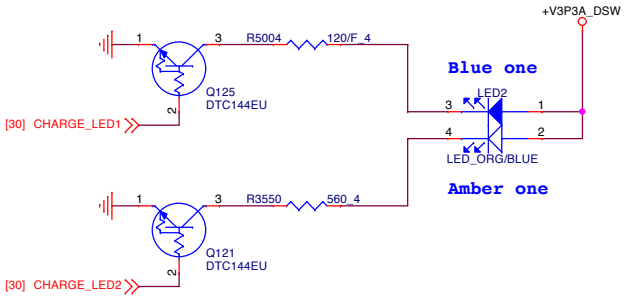
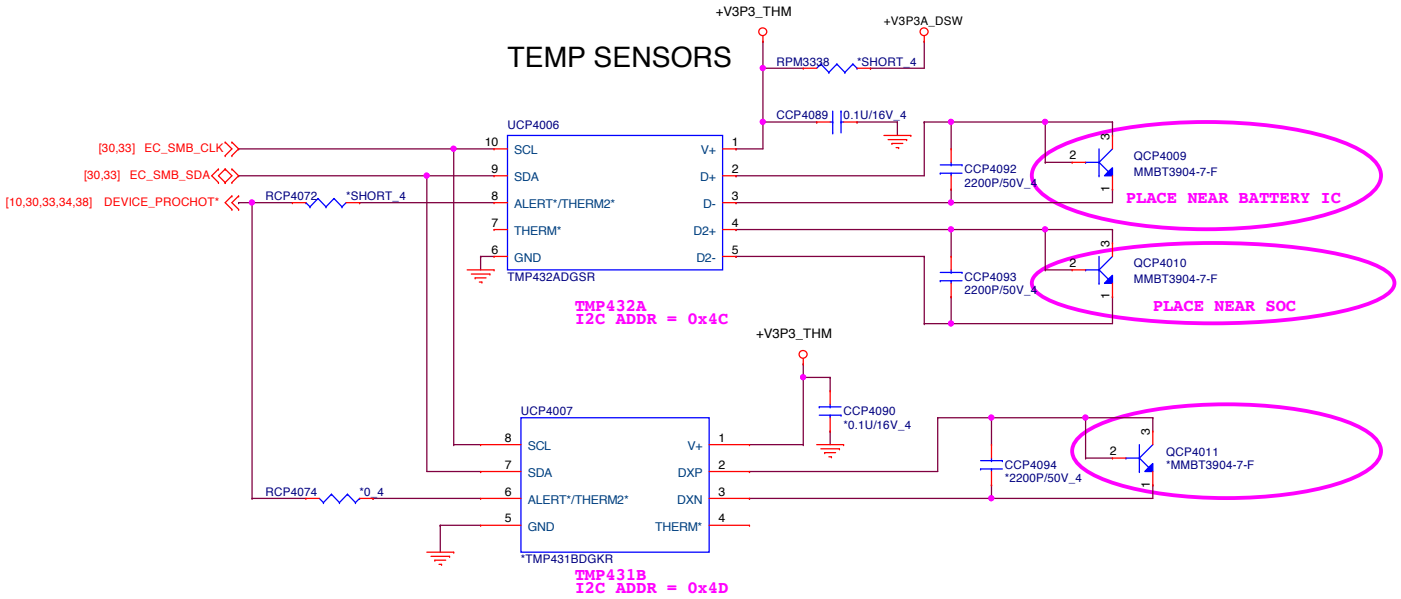
POWER LED STATUS



CHARGE LED STATUS



TEMP SENSORS



Quanta Computer Inc.

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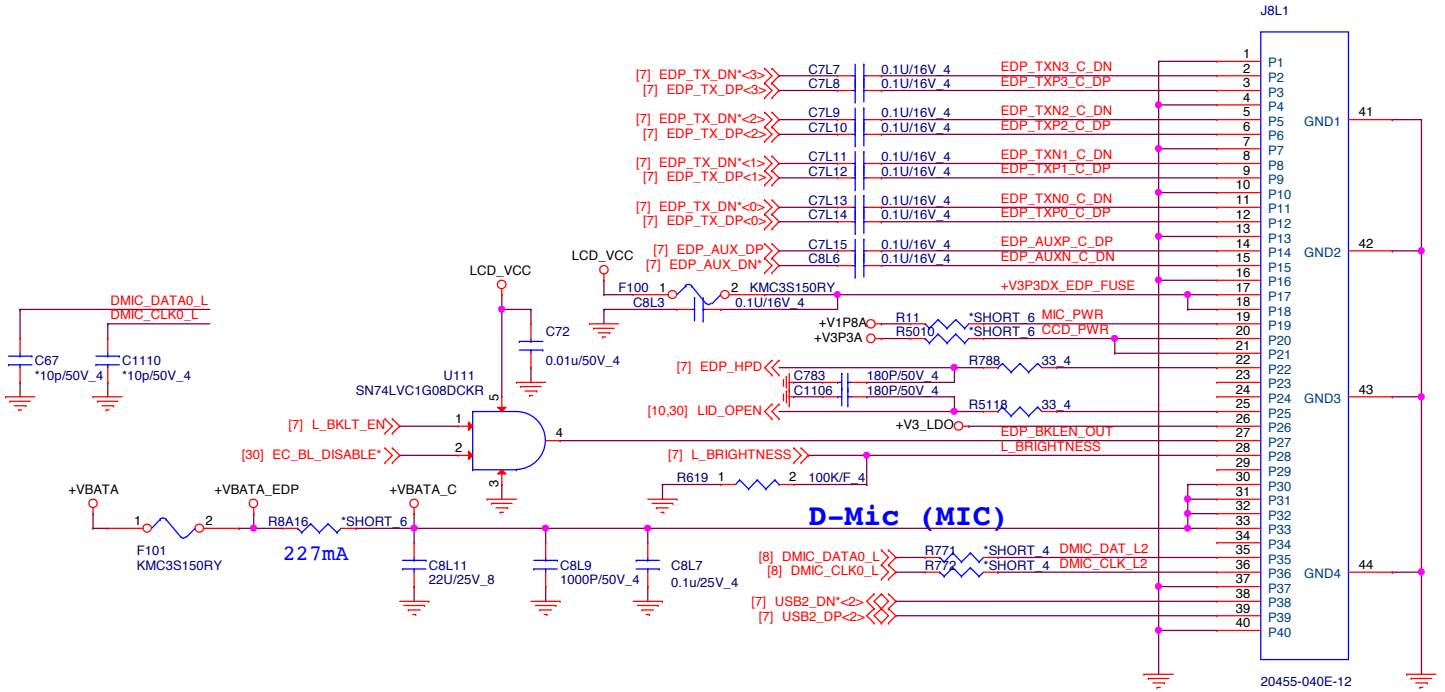
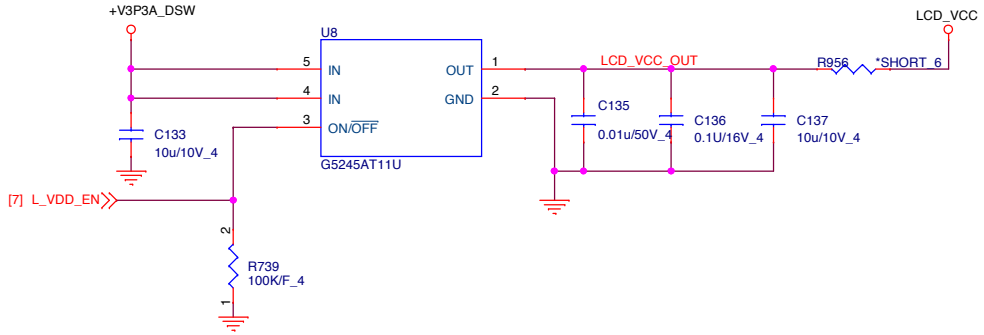
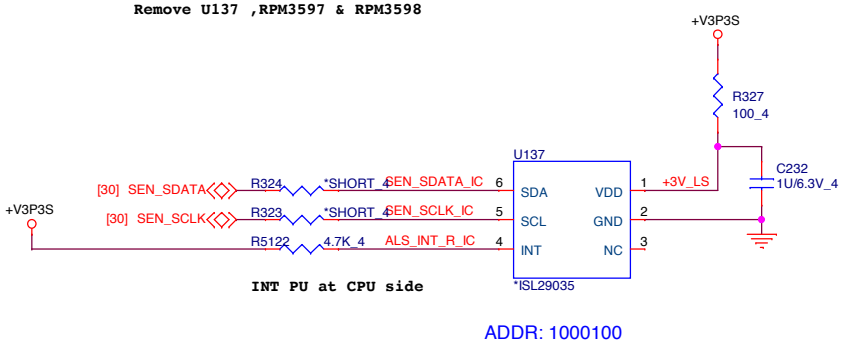
eDP DISPLAY PANEL



Light sensor (SER)

Remove U137 ,RPM3597 & RPM3598





INT PU at CPU side

ADDR: 1000100

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	EDP PANEL	8A

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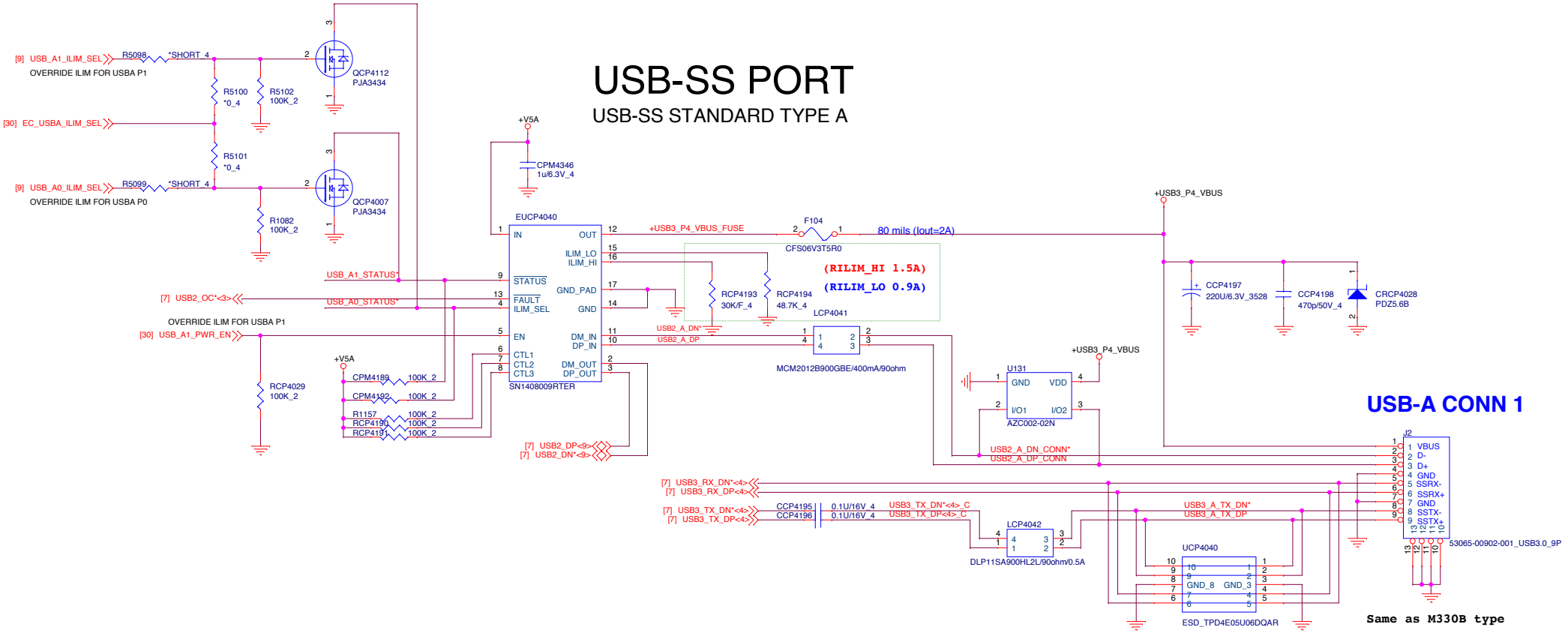
USB-SS PORT

USB-SS STANDARD TYPE A

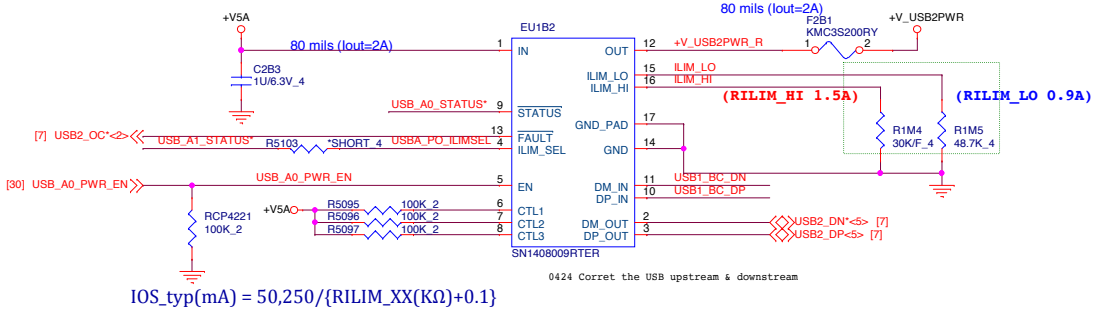


USB-A CONN 1

Same as M330B type

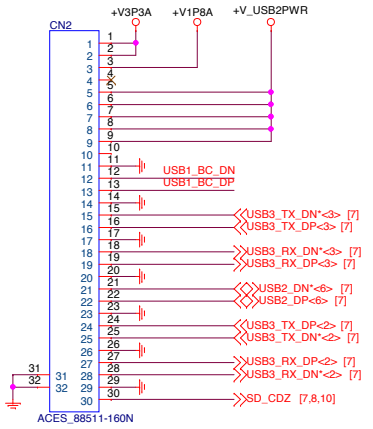
USB Charger

F2B1 is optional. Replace with short if not required.



$$IOS\_typ(mA) = 50{,}250/\{RILIM\_XX(K\Omega)+0.1\}$$

Condition	CTL1	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
SDP2	1	1	1	0



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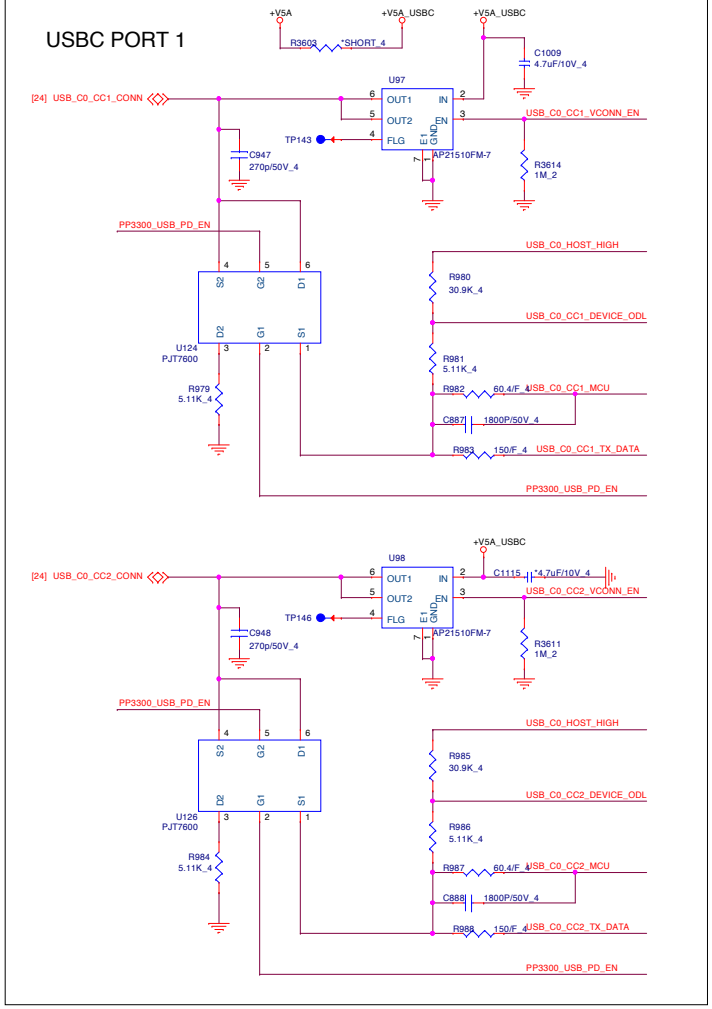
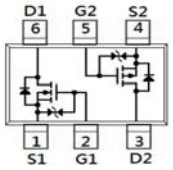
USBPD EC - CC LOGIC

USBC EC
CC NEGOTIATION

USBC PORT 1





4/13 LMLE : 750K->75K

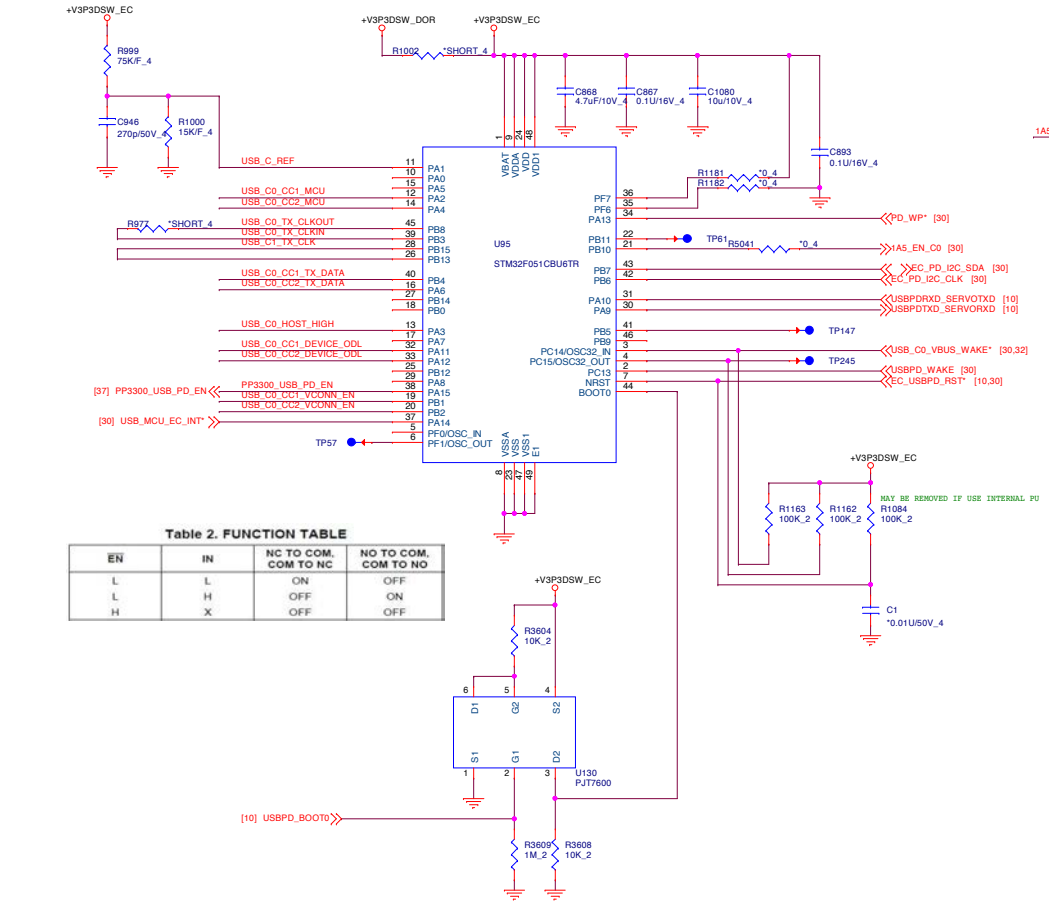
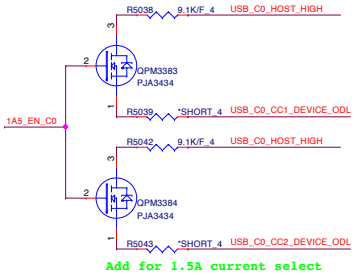
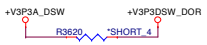


Table 2. FUNCTION TABLE

EN	IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	L	ON	OFF
L	H	OFF	ON
H	X	OFF	OFF



EC BACKUP POWER FOR DEAD BATTERY CORNER CASE



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	USBPD EC	8A
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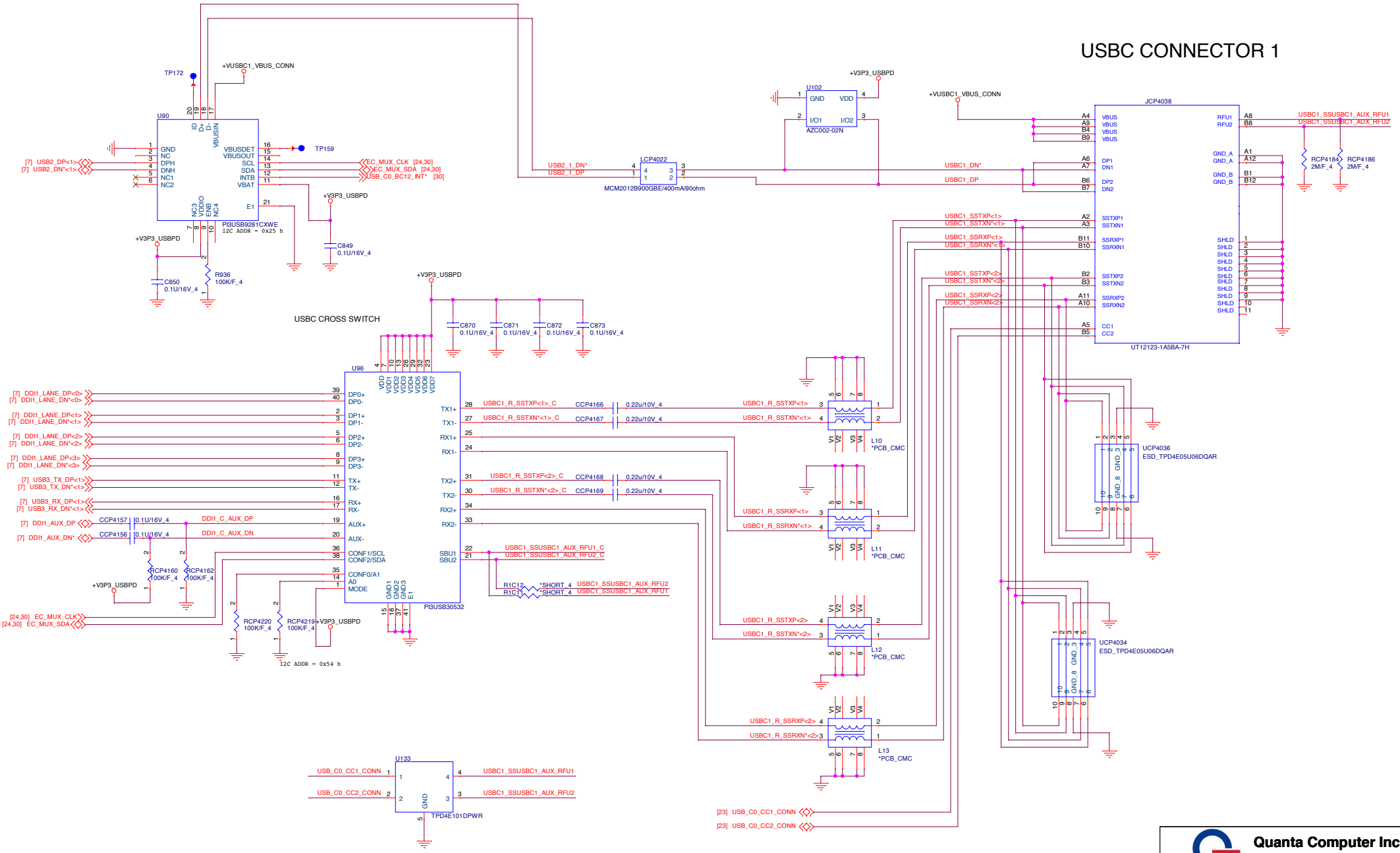
USBC PORT 1

USBC CONNECTOR 1



Quanta Computer Inc.		
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	USBC PORT	8A
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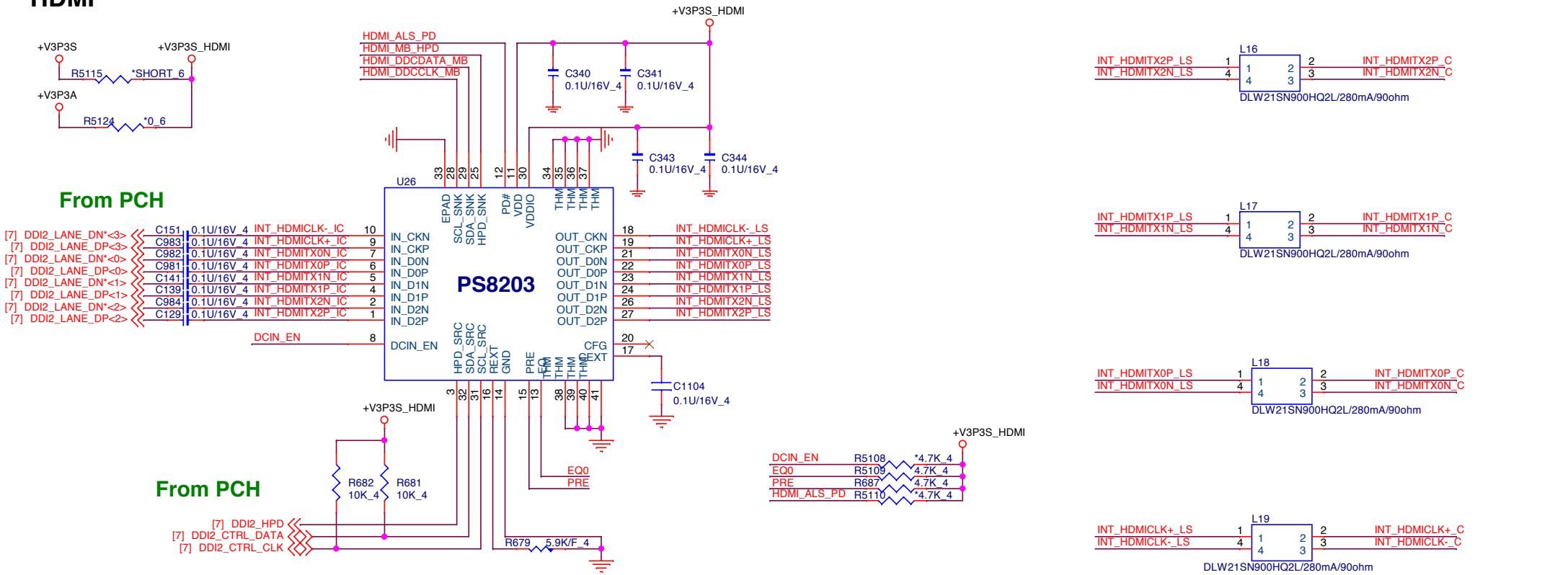
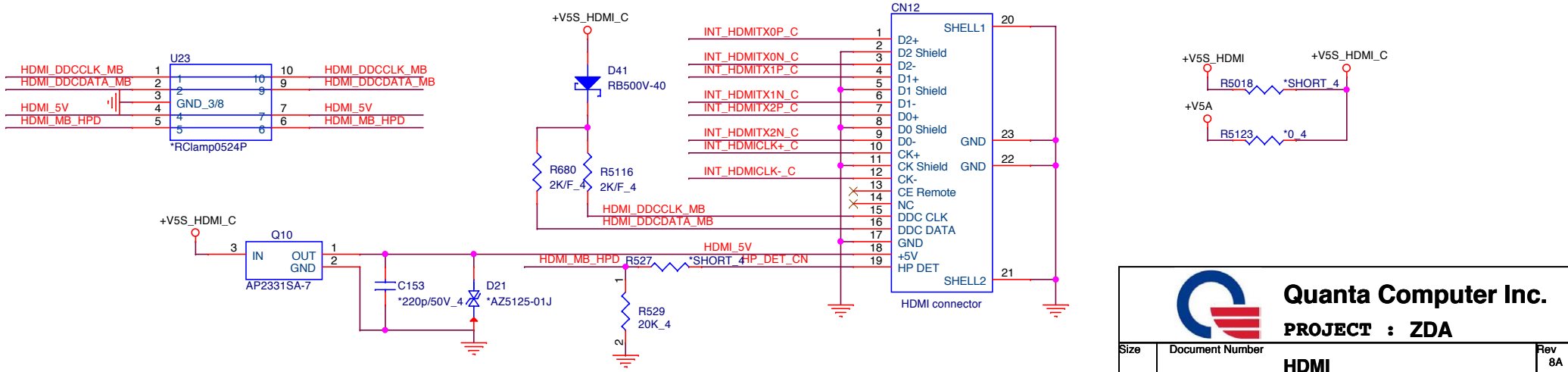
HDMI



HDMI connector



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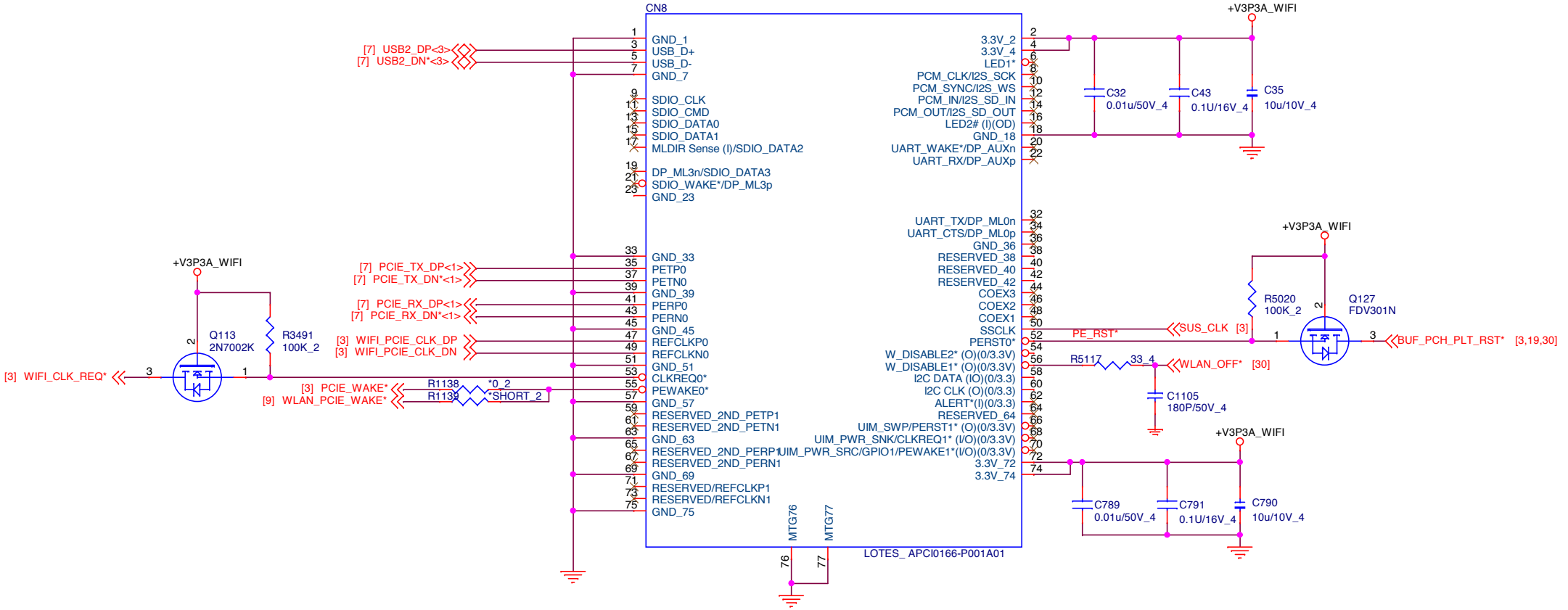
M.2 WIFI/BT

NGFF WIFI



For EMI

+V_BOOSTIN	+V_BOOSTIN	+VBATA	+VBATA	+VUSBC1_VBUS_CONN	+VUSBC1_VBUS_CONN	+VUSBC1_VBUS_CONN
C8L13 1000P/50V_4	C8L14 0.1u/25V_4	C8L15 1000P/50V_4	C8L16 0.1u/25V_4	C8L19 1000P/50V_4	C8L20 0.1u/25V_4	C1112 100p/50V_4

+VUSBC1_VBUS_CONN	+VUSBC1_VBUS_CONN	+VUSBC1_VBUS_CONN
C8L17 1000P/50V_4	C8L18 0.1u/25V_4	C1111 100p/50V_4

Quanta Computer Inc.

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	NGFF-WIFI/BT/DB	8A

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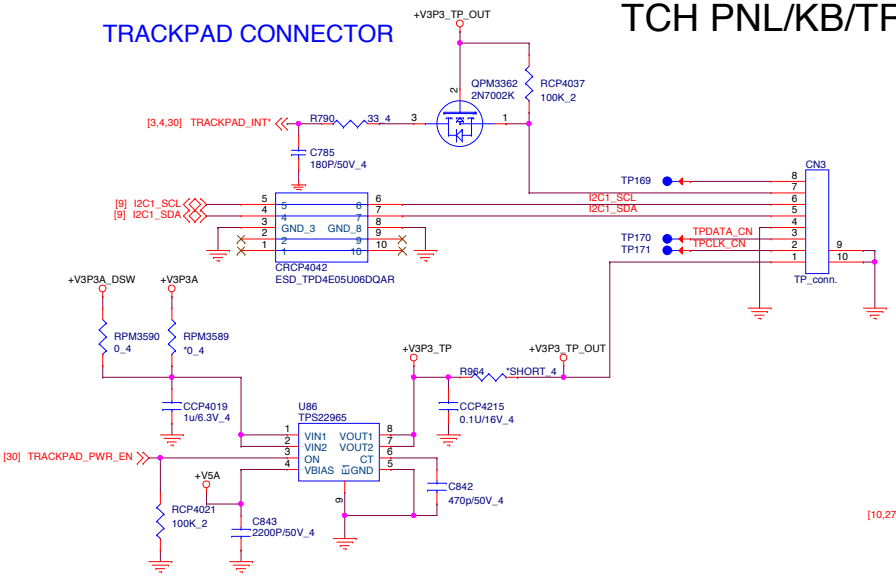
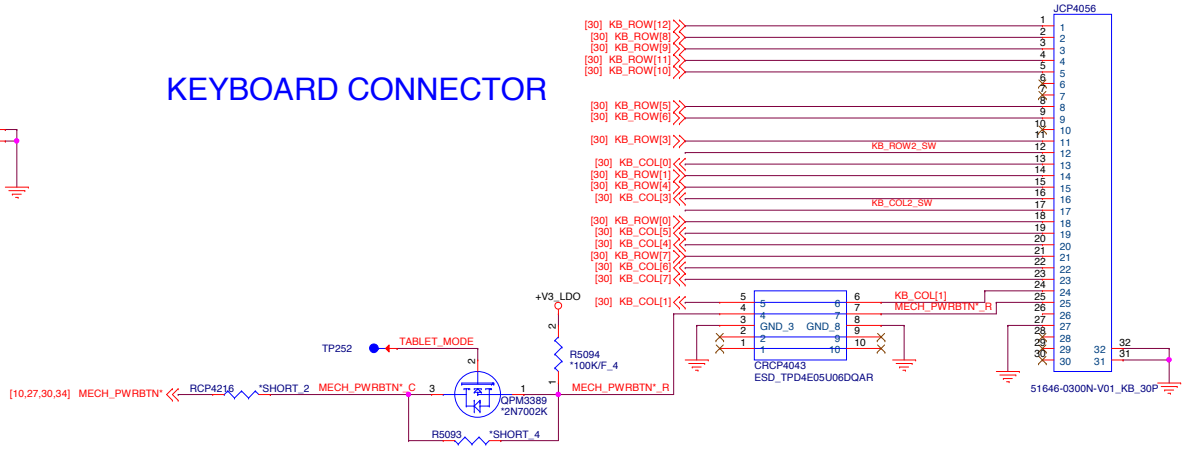
TCH PNL/KB/TRKPAD/FAN

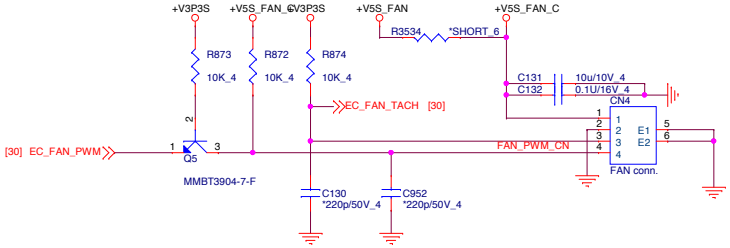
TRACKPAD CONNECTOR

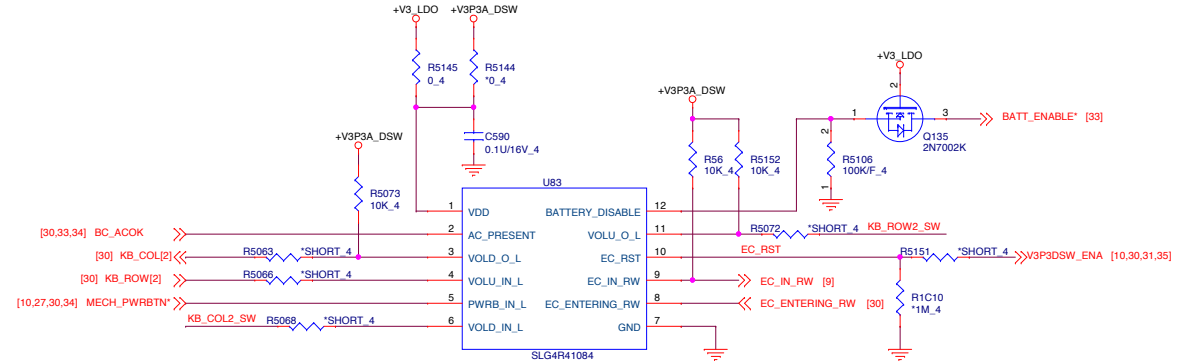


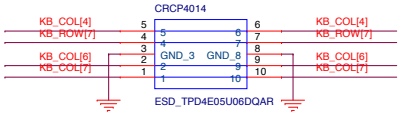
KEYBOARD CONNECTOR

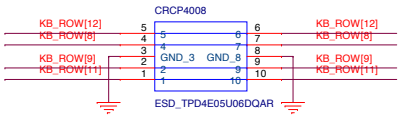


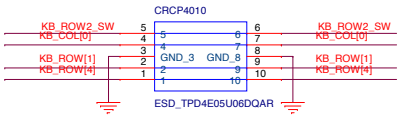
CPU FAN CONNECTOR

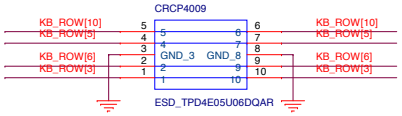


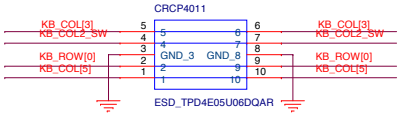




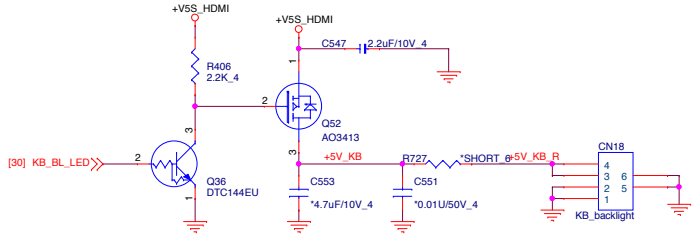




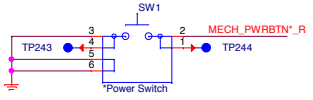




KB_BL LED (KBL)



For test only



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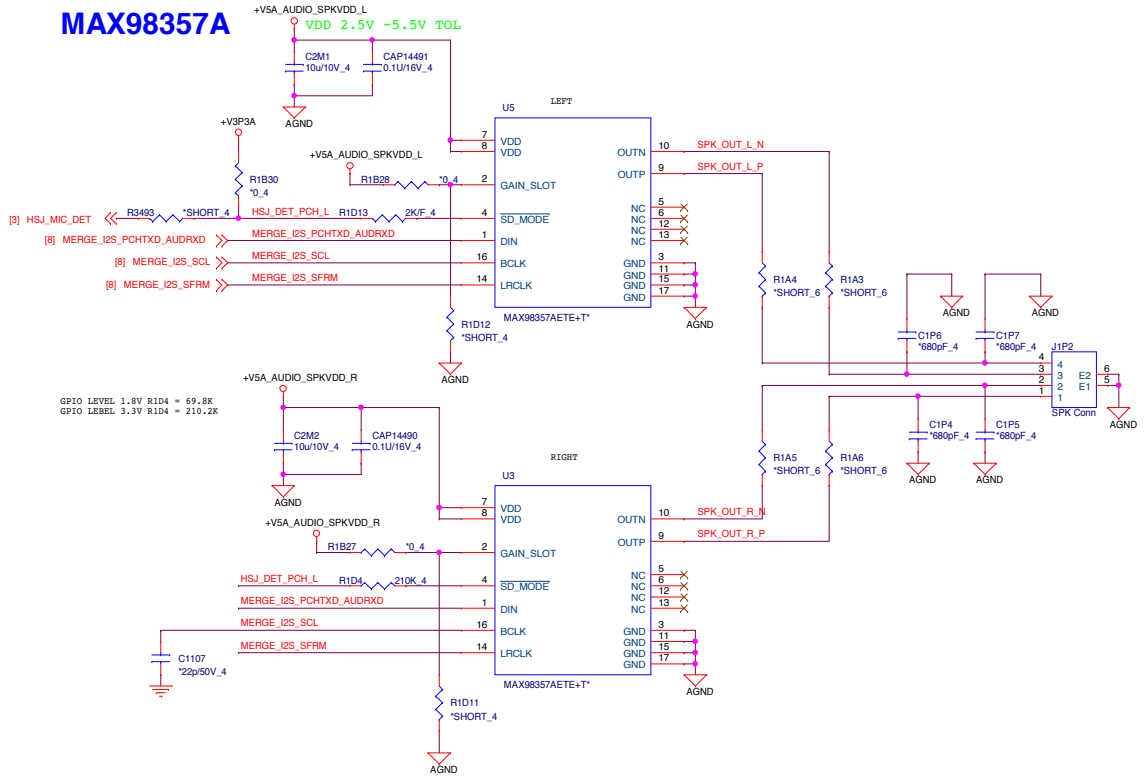
MAX98357A



LRCLK POLARITY

PART NUMBER	LRCLK POLARITY (LEFT CH)
MAX98357A	LOW
MAX98357B	HIGH

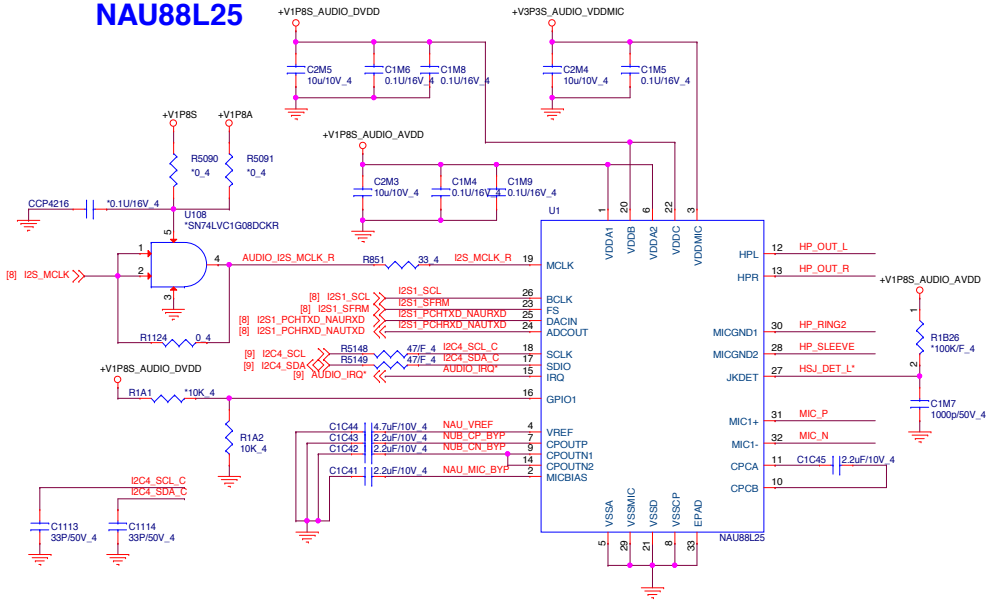
BCLK POLARITY

MODE	PART NUMBER	BCLK POLARITY
I2S	MAX98357A	Rising edge
Left Justified	MAX98357B	Rising edge
TDM	MAX98357A	Rising edge
	MAX98357B	Falling edge

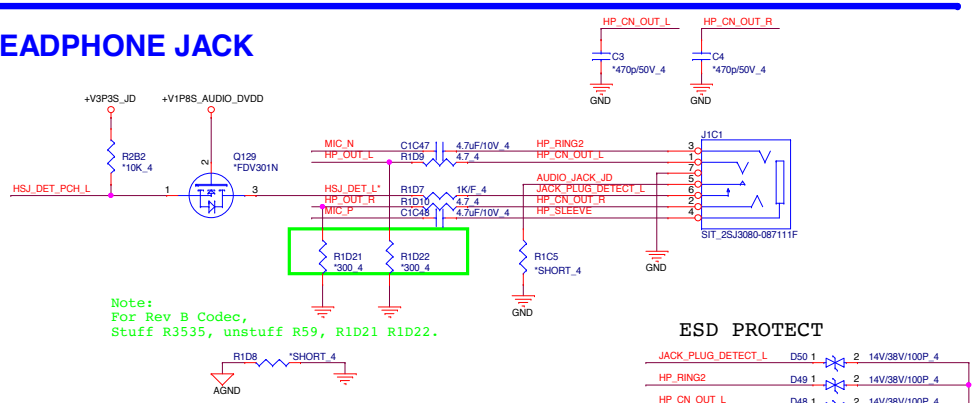
GAIN TABLE

GAIN_SLOT	GAIN(dB)
PL 100K TO GND	15
PL TO GND	12
FLOATING	9
PU TO VDD	6
PU 100K TO VDD	3

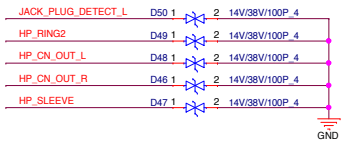
NAU88L25



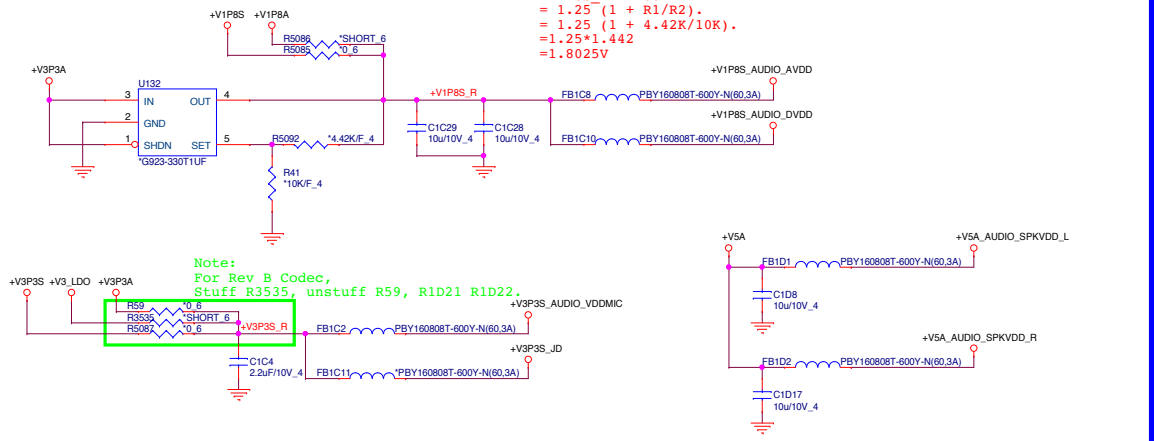
HEADPHONE JACK



ESD PROTECT

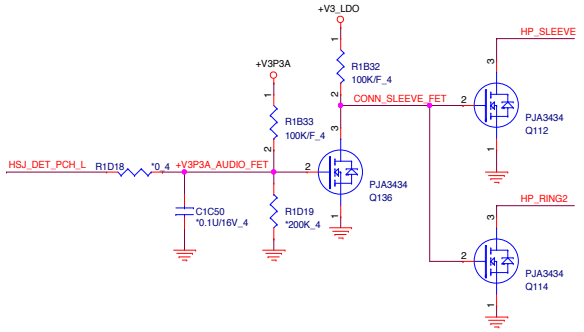


AUDIO_PD



Mic PULL DOWN

Note:
For Rev B Codec,
all components in Mic Pull Down circuit can be DNI.



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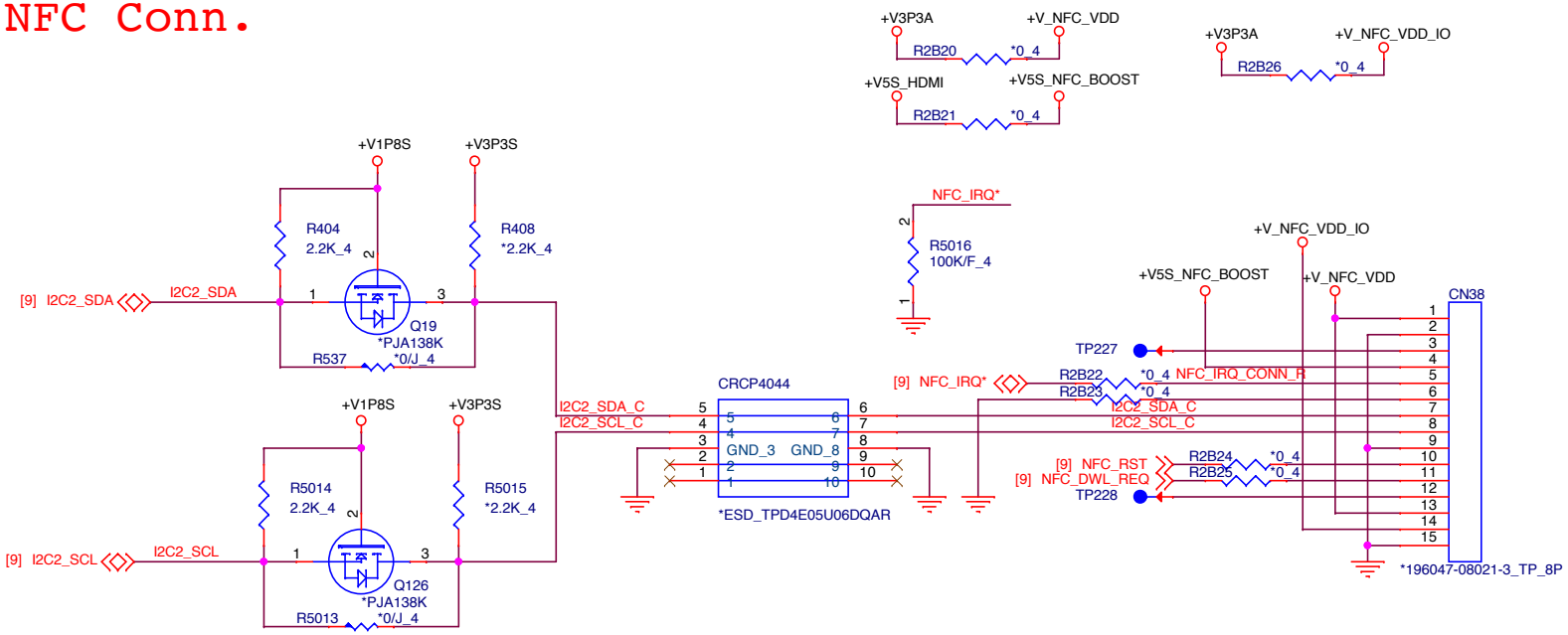
NFC Conn.

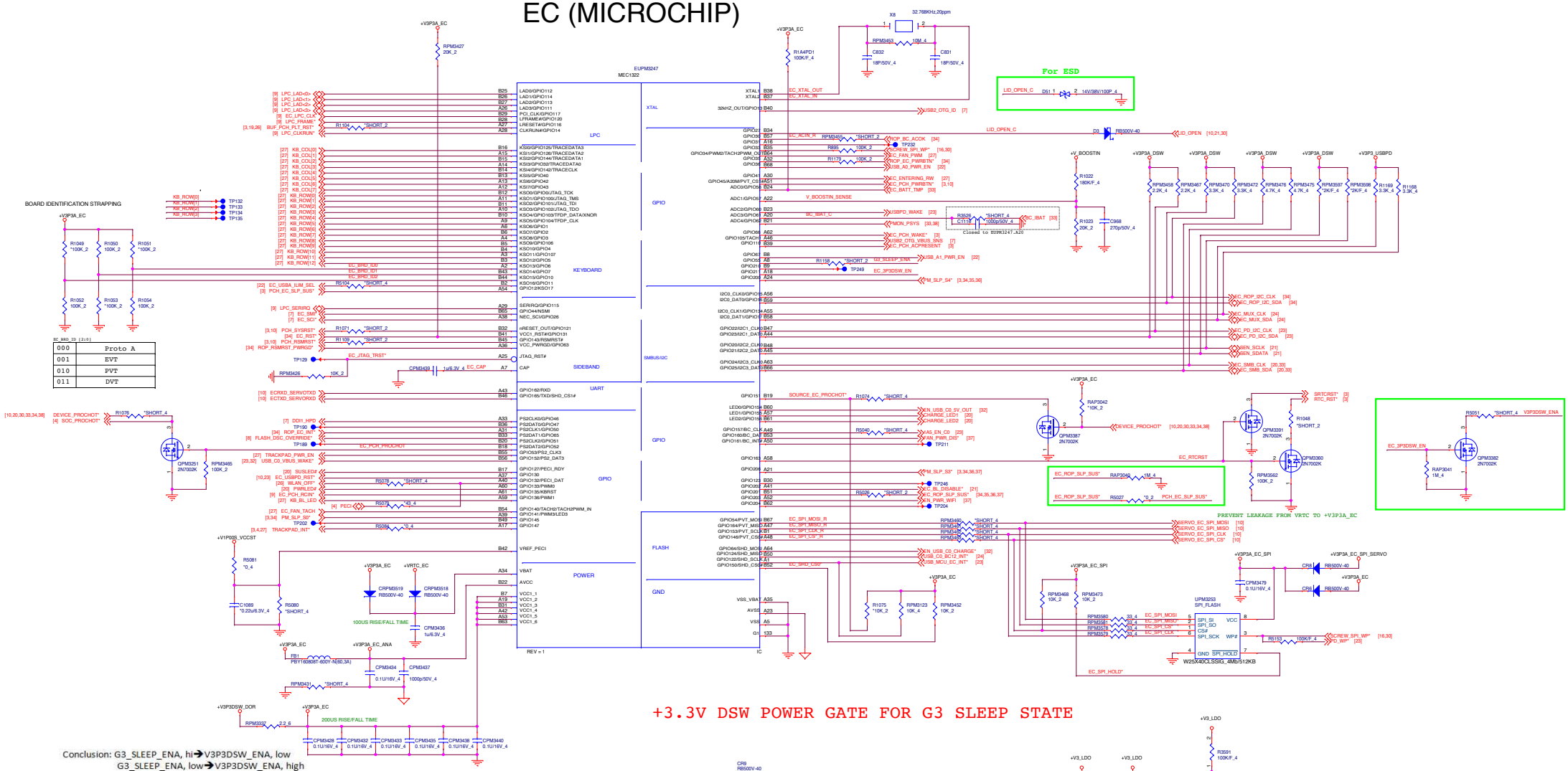


IV. Pin Definition

Host connector

	Pin number	Name	Configuration	Description
PWR	1	MOD_VDD	Power	3.3V power supply
GND	2	MOD_GND	Ground	Module ground
Test point	3	SWP	SWP data	SWP data line to UICC/SIM
PU	4	VCC_BOOST	Power supply	Power rail for Booster
GPIO/INT	5	IRQ	Output	Interrupt to host
PD	6	PMUVCC	Power supply	Power supply to UICC/SIM
SMBUS	7	I²C_SDA	Input/ Output	I²C data line
	8	I²C_SCL	Input	I²C clock
GND	9	MOD_GND	Ground	Module ground
GPIO/RST	10	Reset/Wakeup	Input	Wake up the module from standby mode or reset the module
GPIO/REQ	11	DWL_REQ	Input	Firmware download control
Test point	12	SIMVCC	Power	The power rail used to power UICC/SIM.
PWR	13	MOD_VDD	Power	3.3V power supply
PWR	14	VDD_IO	Power	3.3V for host IO reference voltage
GND	15	MOD_GND	Ground	Module ground

EC (MICROCHIP)



+3.3V DSW POWER GATE FOR G3 SLEEP STATE

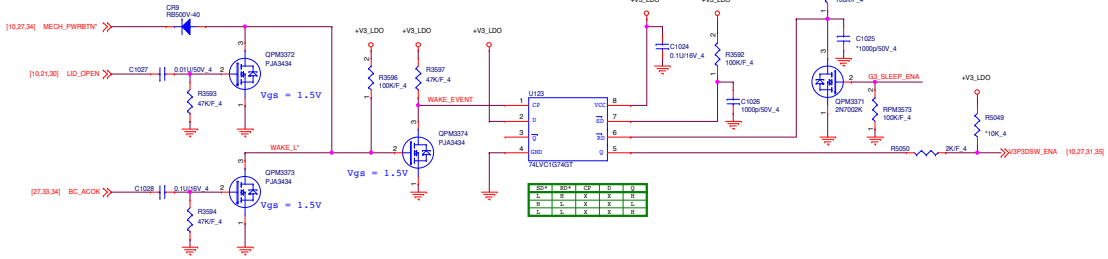


Table 4. Function table for asynchronous operation[1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Table 5. Function table for synchronous operation[1]

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

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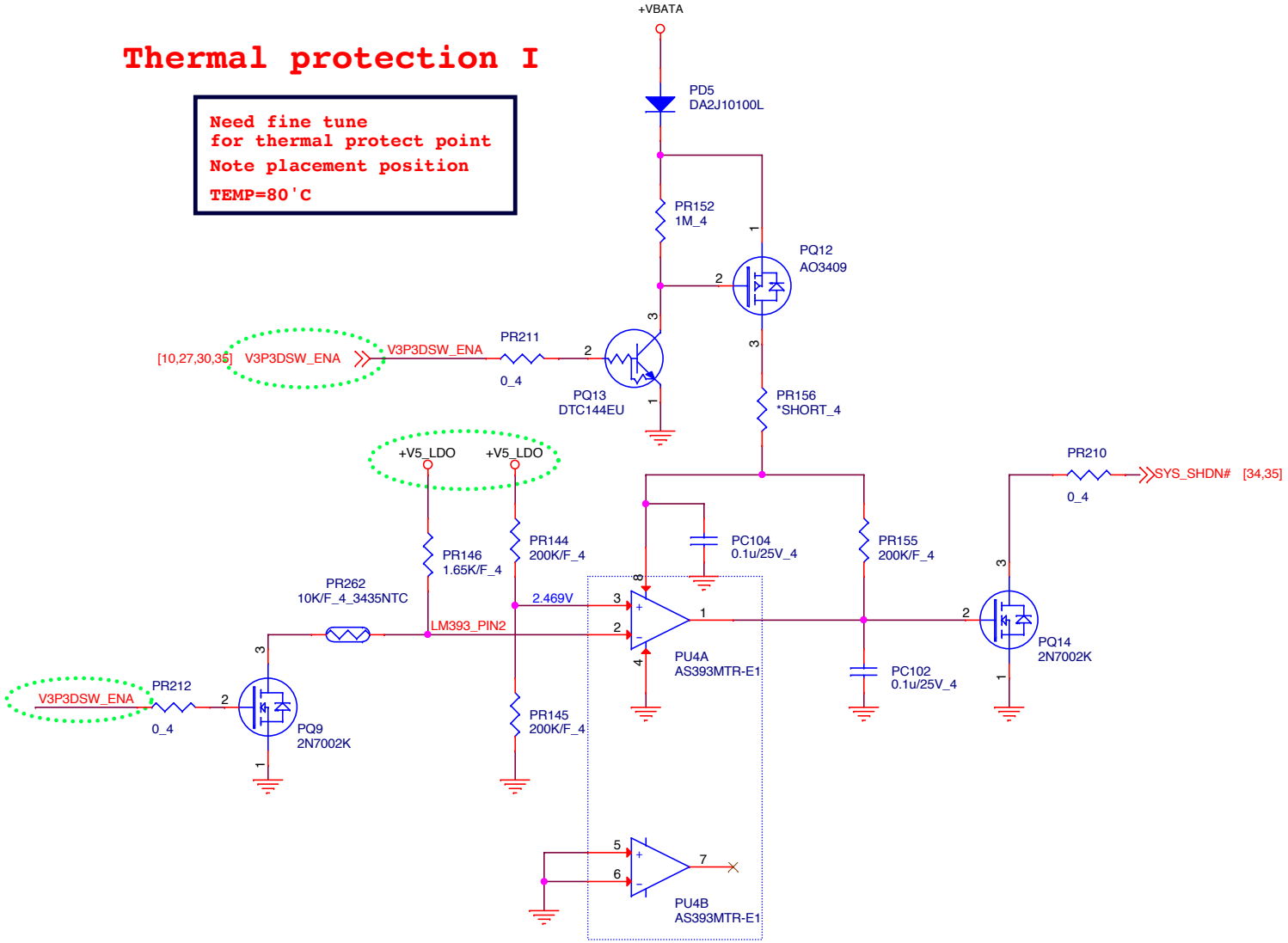
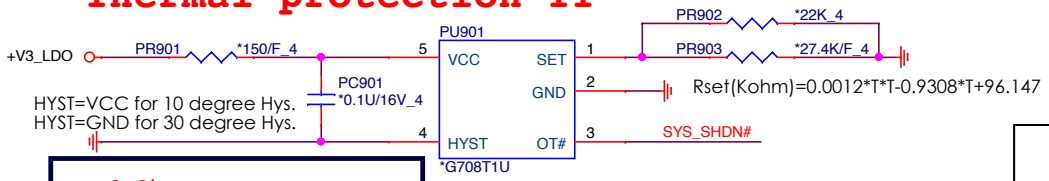
Thermal protection I

Need fine tune
for thermal protect point
Note placement position
TEMP=80'C



For EC control thermal protection (output 3.3V)

Thermal protection II



Need fine tune
for thermal protect point
Note placement position
TEMP=82.66'C [@27.4K/F_4]

Quanta Computer Inc.

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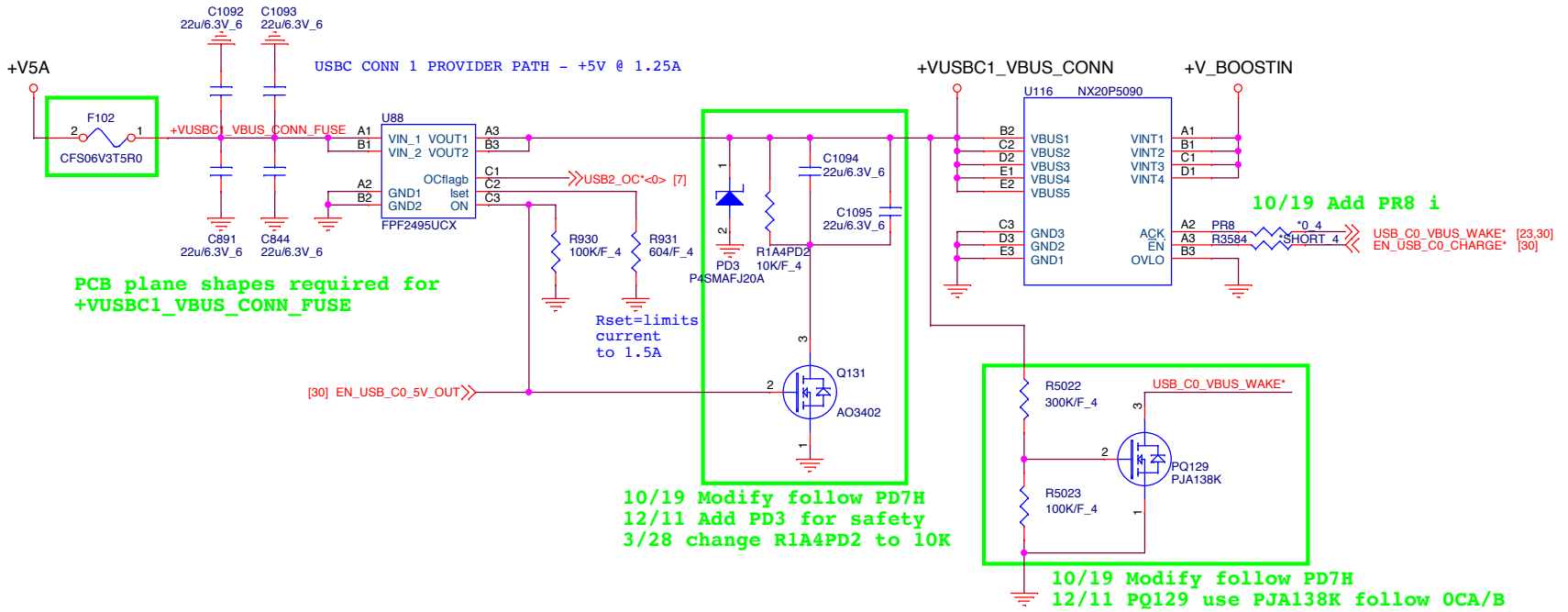
USBC-PD



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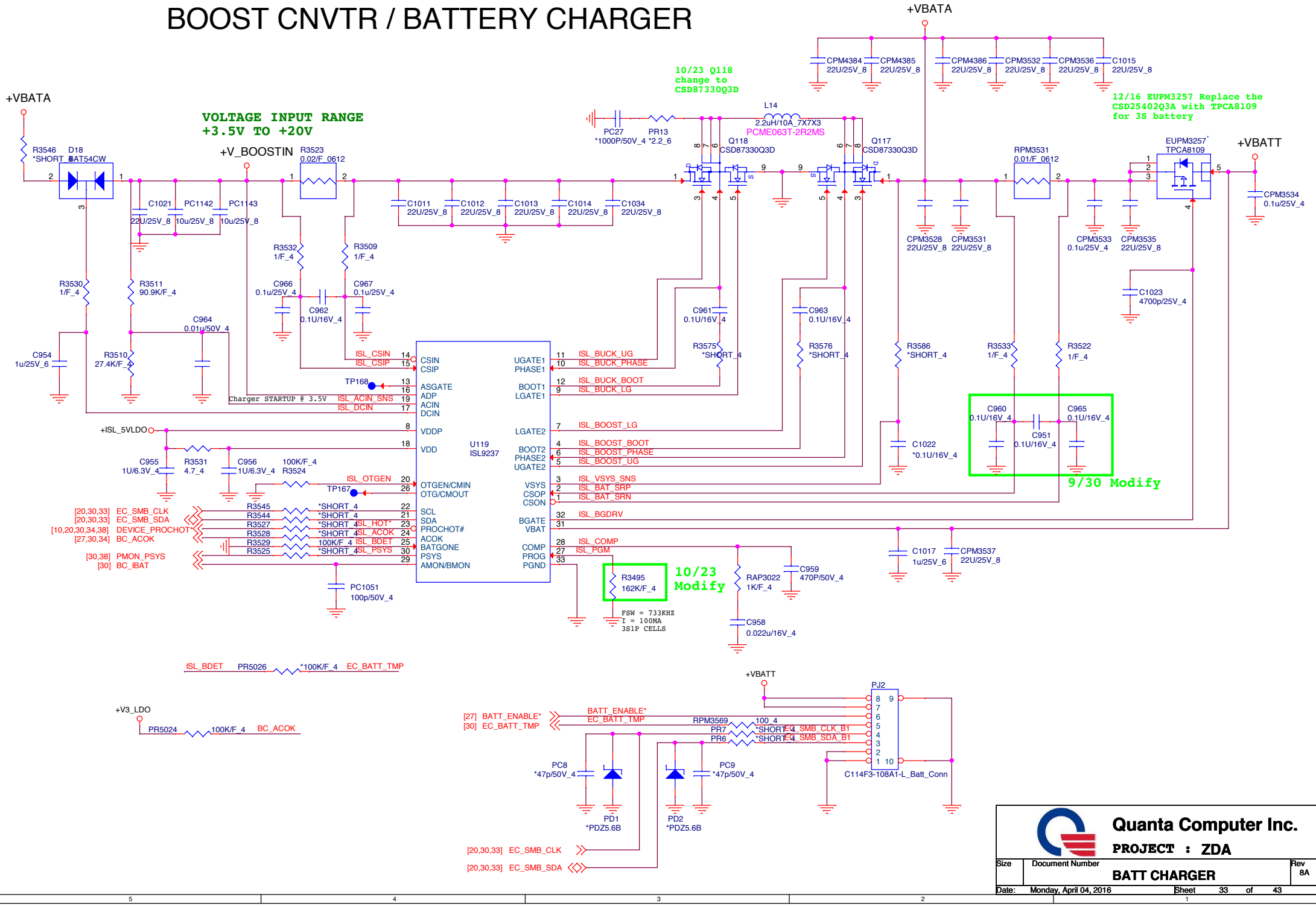
BOOST CNVTR / BATTERY CHARGER



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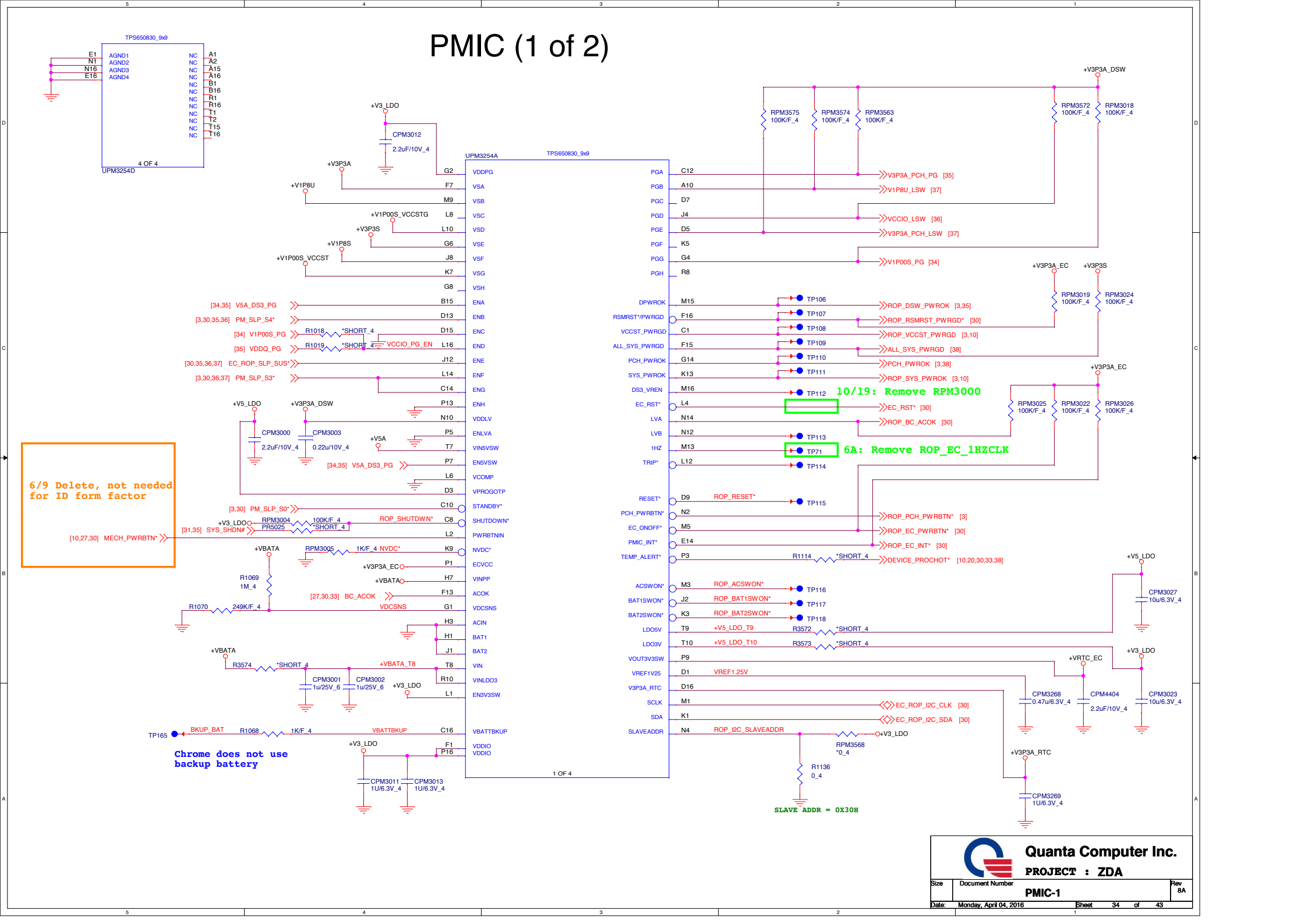
PMIC (1 of 2)


TPS650830_9x9
UPM3254D
4 OF 4
UPM3254A
TPS650830_9x9
1 OF 4
6/9 Delete, not needed for ID form factor
10/19: Remove RPM3000
6A: Remove ROP_EC_1HZCLK
Chrome does not use backup battery
SLAVE ADDR = 0X30H
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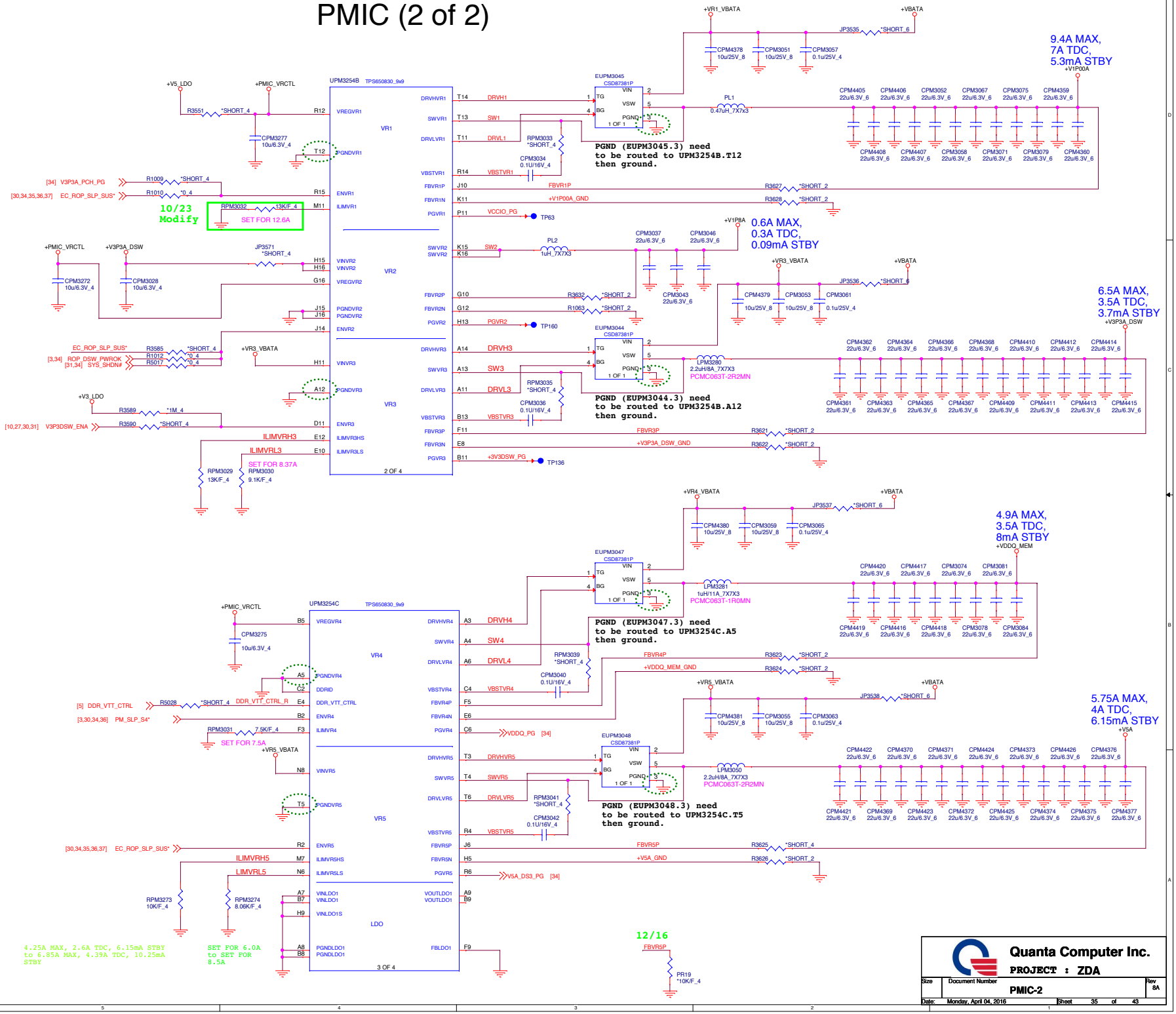
PMIC (2 of 2)



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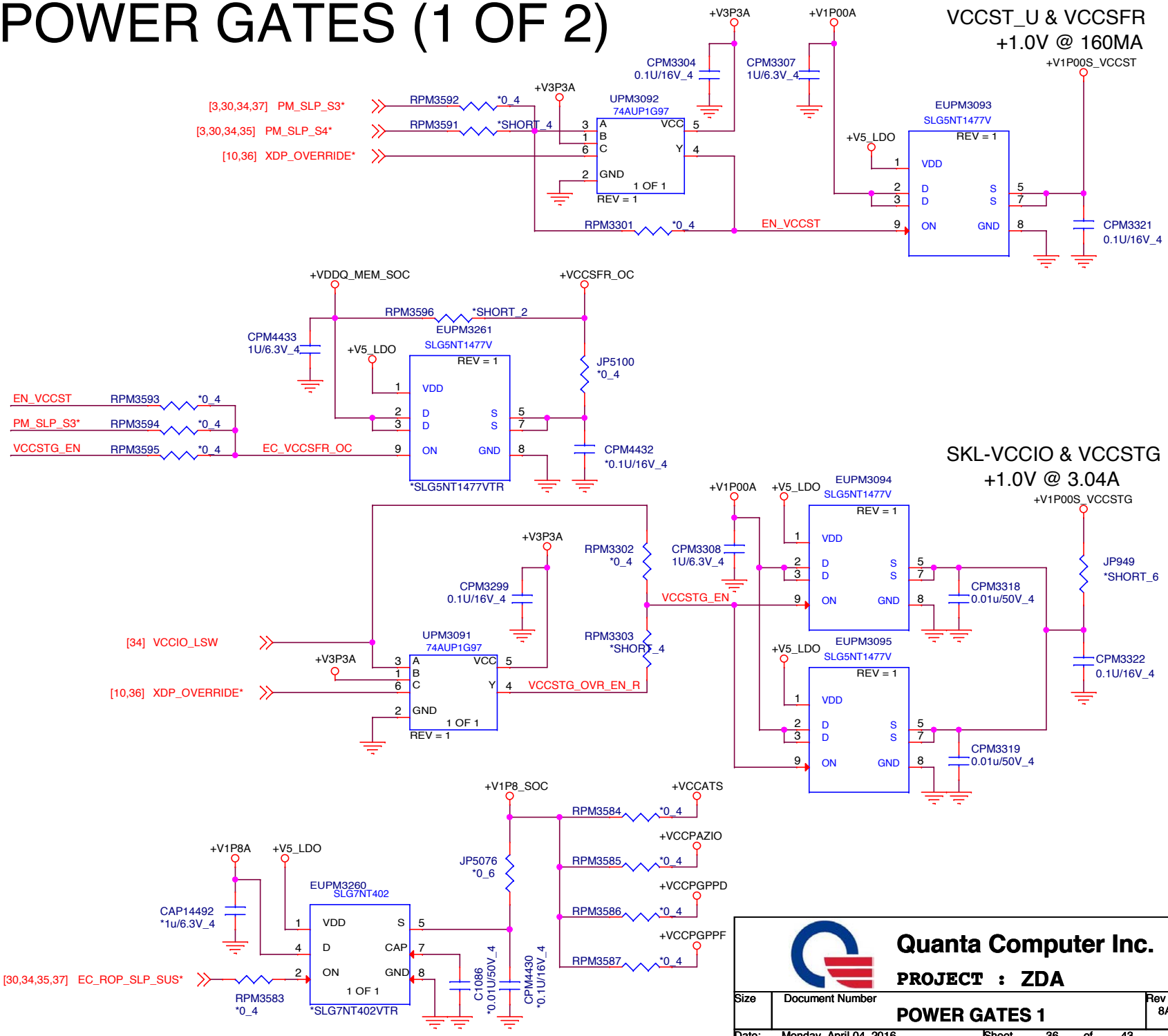
POWER GATES (1 OF 2)



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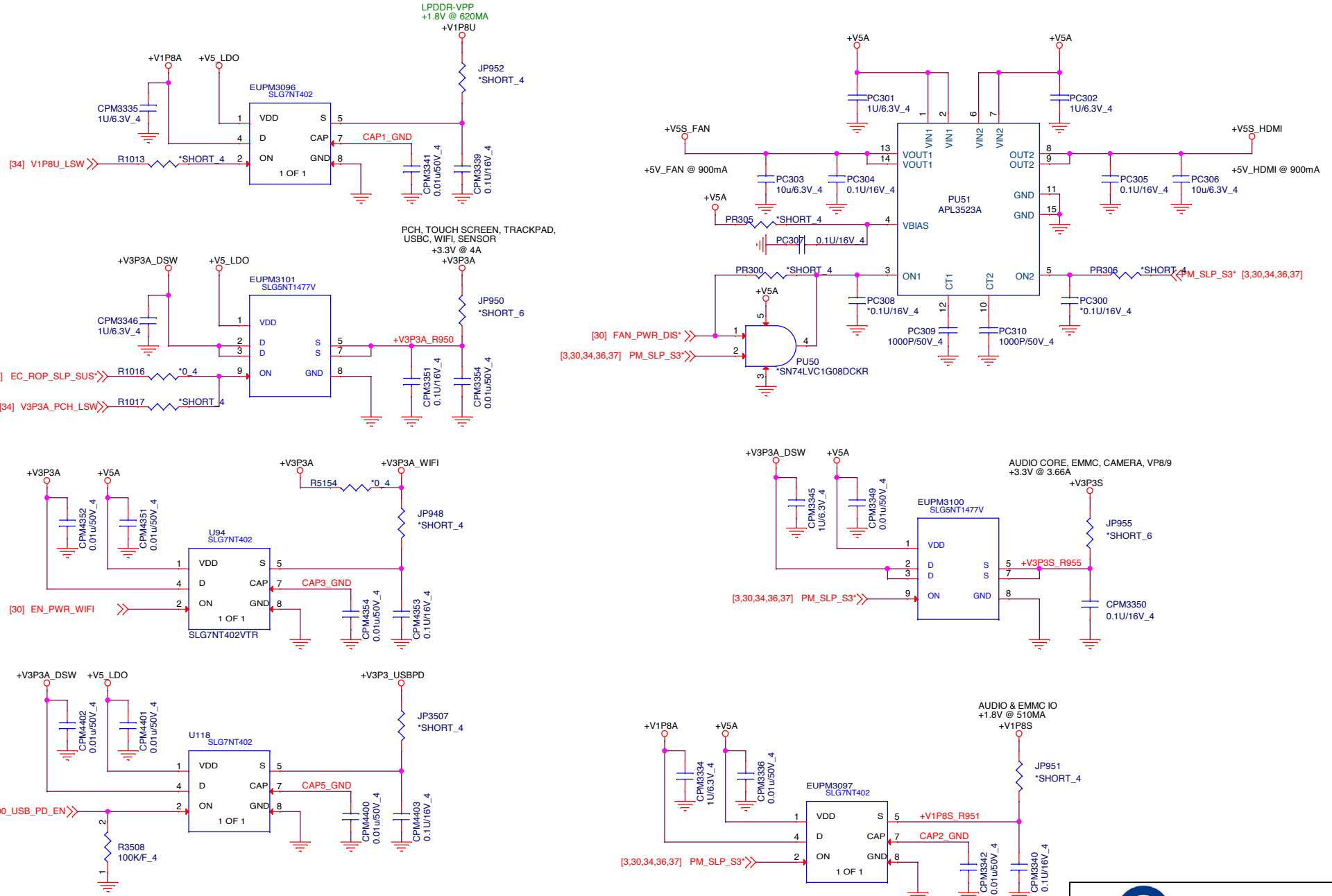
POWER GATES (2 OF 2)



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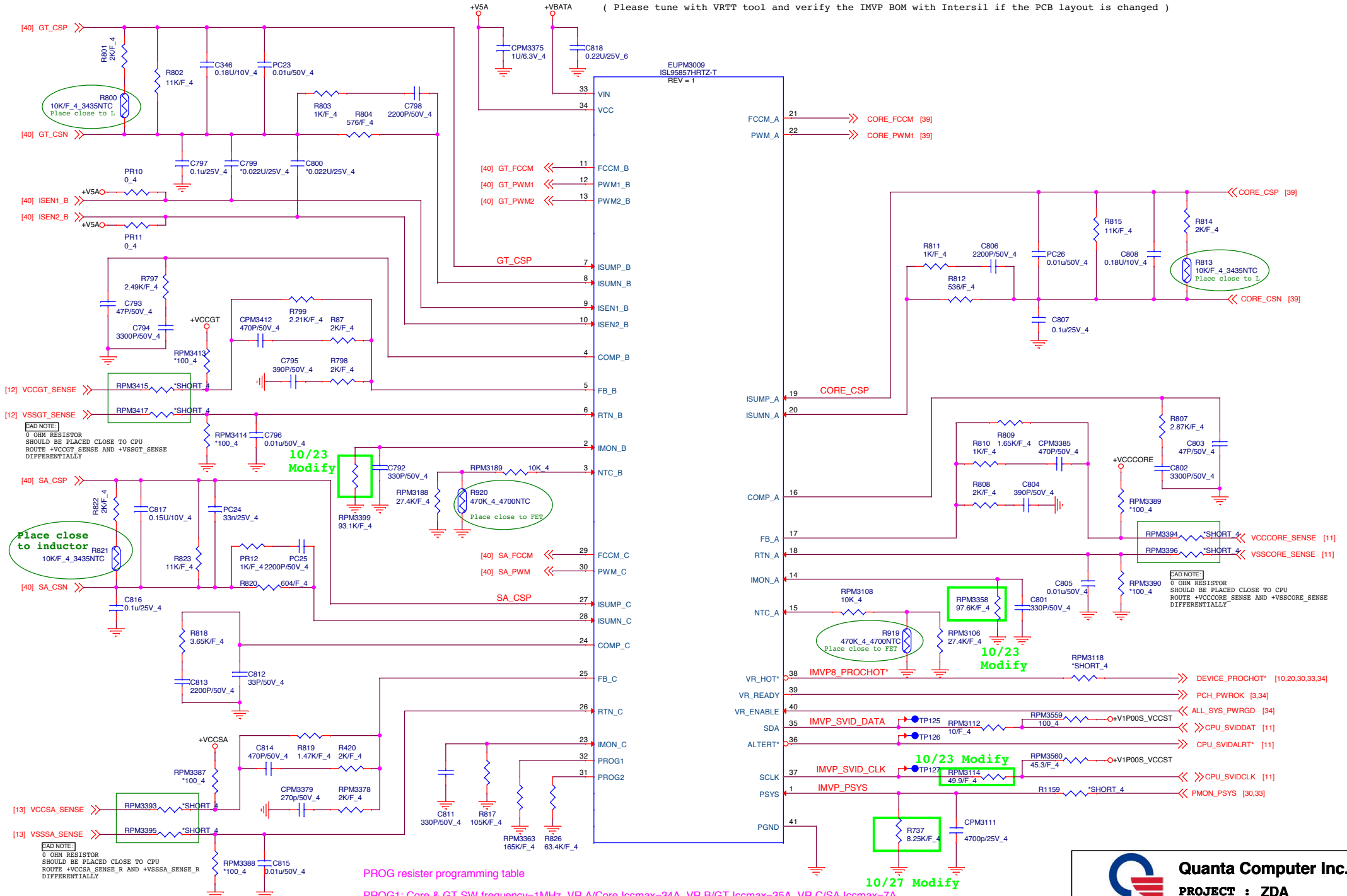
IMVP8 (1 of 3)

(Please tune with VRTT tool and verify the IMVP BOM with Intersil if the PCB layout is changed)



PROG resister programming table

PROG1: Core & GT SW frequency=1MHz, VR A/Core Iccmax=34A, VR B/GT Iccmax=35A, VR C/SA Iccmax=7A

PROG2: SA SW frequency=750KHz VR Address: ICore [00h] GT[01h] SA [02h]

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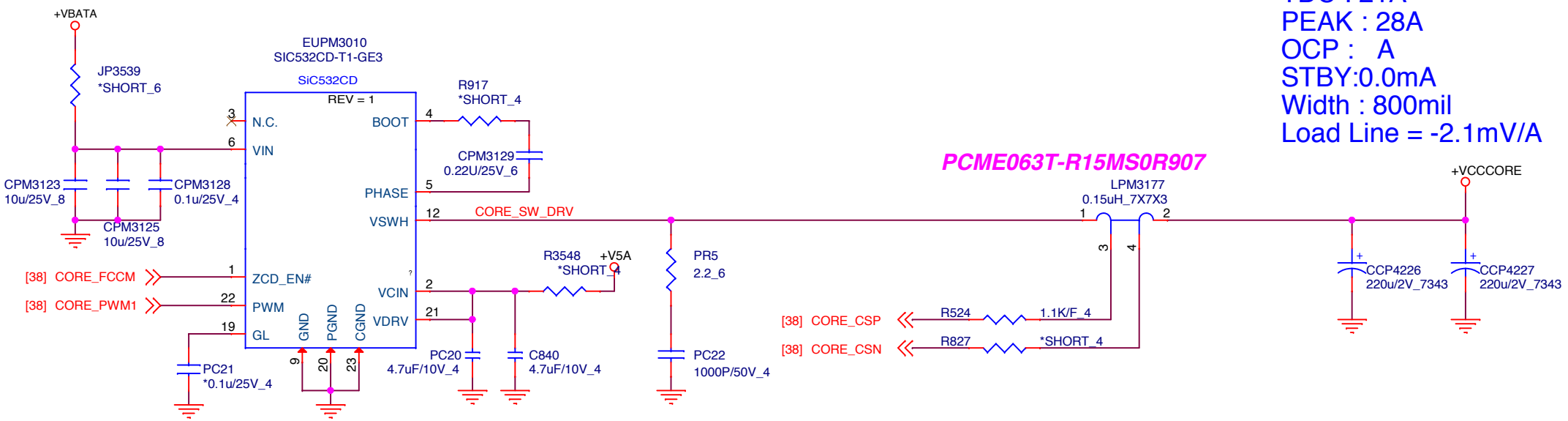
IMVP8 VCCORE

+VCCCORE
TDC : 21A
PEAK : 28A
OCP : A
STBY:0.0mA
Width : 800mil
Load Line = -2.1mV/A



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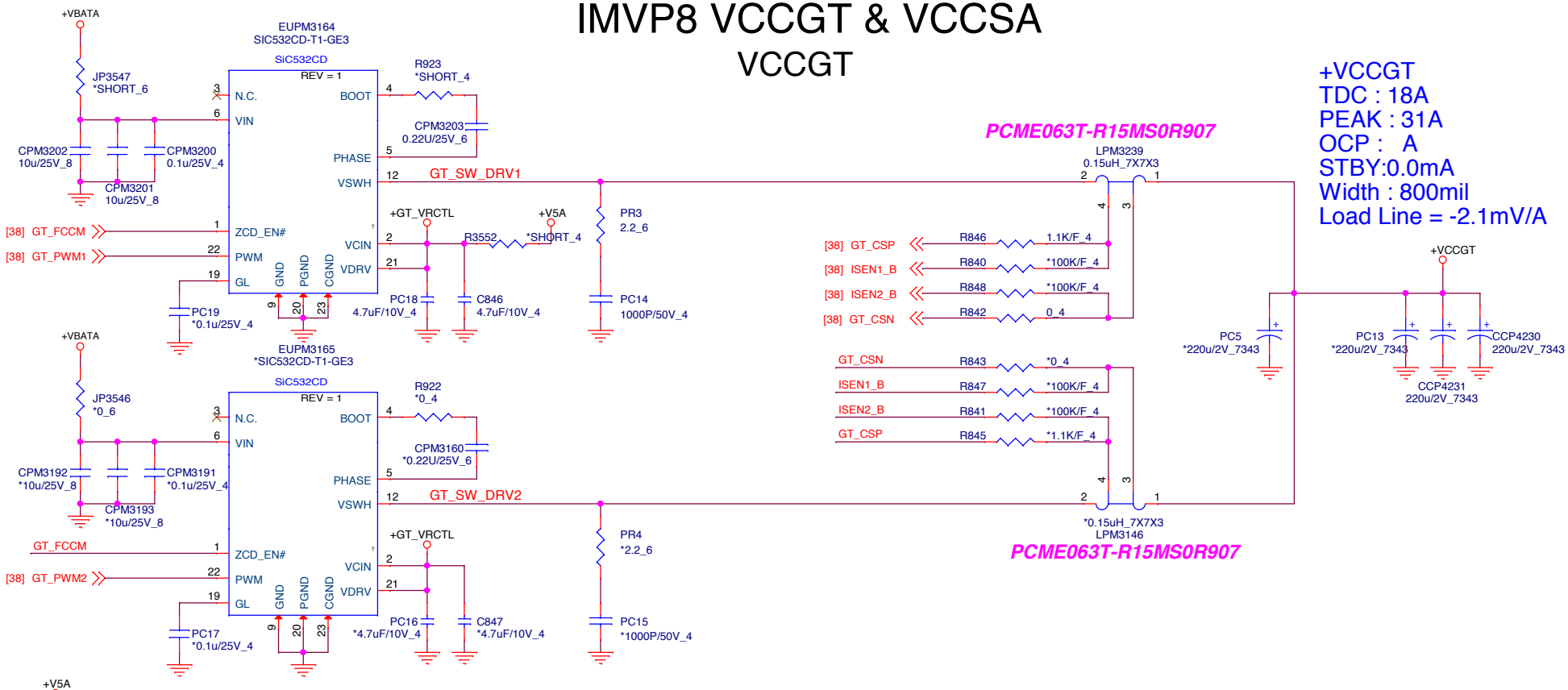
IMVP8 VCCGT & VCCSA

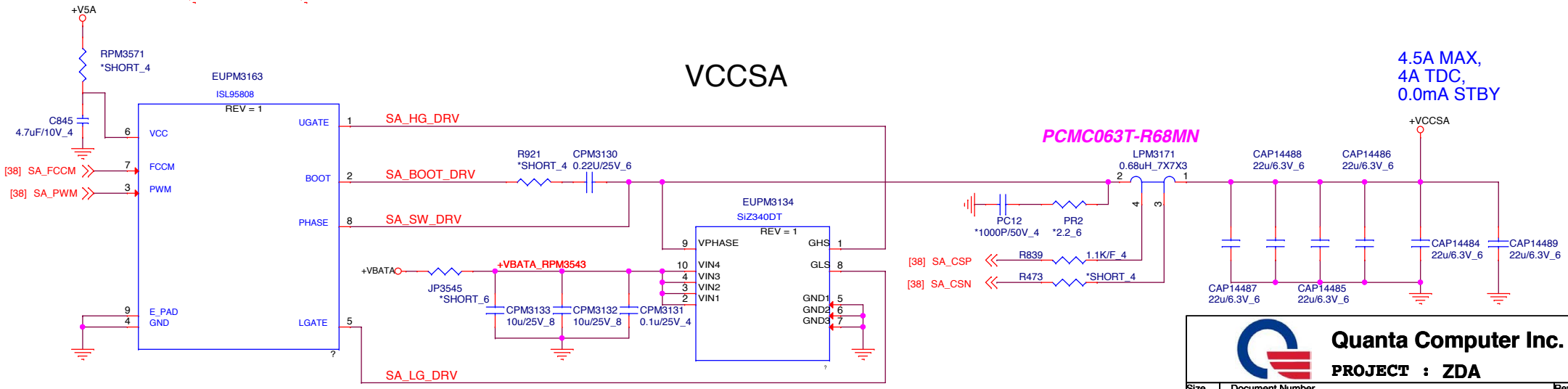
VCCGT

+VCCGT
TDC : 18A
PEAK : 31A
OCP : A
STBY:0.0mA
Width : 800mil
Load Line = -2.1mV/A



VCCSA

4.5A MAX,
4A TDC,
0.0mA STBY



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INA for +V3P3A_DSW

3/28 Delet PU21,RAP3024,
RAP3025,PC215,PC214.

INA for +VBATA

3/28 Delet PU23,RAP3028,
RAP3029,PC218,PC219.

INA for +V5A

3/28 Delet PU22,RAP3026,
RAP3027,PC216,PC217.

INA for +V1P00A

3/28 Delet PU26,RAP3036,
RAP3037,PC1049,PC1050.

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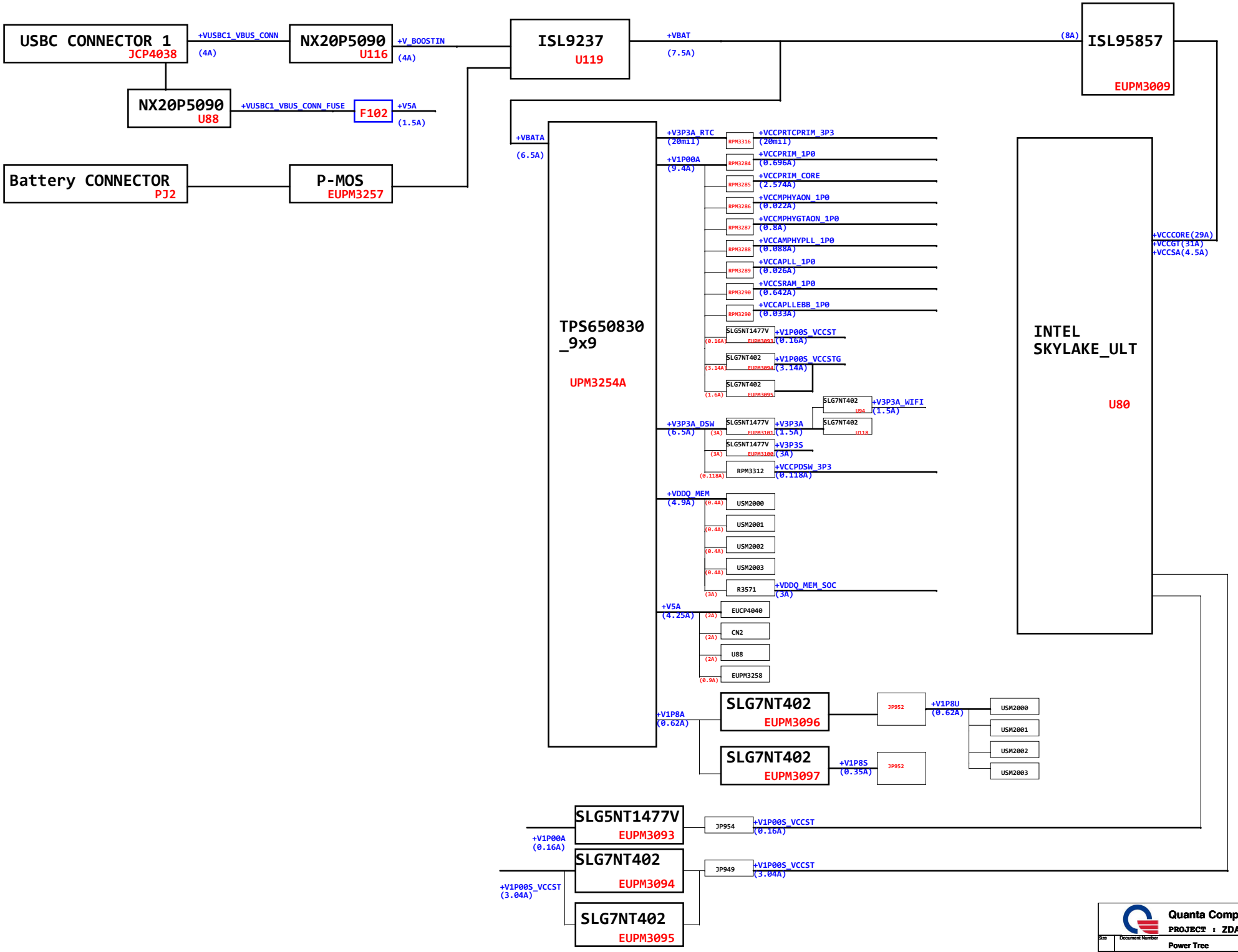
USBC CONNECTOR 1
JCP4038
+VUSBC1_VBUS_CONN
(4A)
NX20P5090
U116
+V_BOOSTIN
(4A)
ISL9237
U119
+VBAT
(7.5A)
(8A)
ISL95857
EUPM3009
NX20P5090
U88
+VUSBC1_VBUS_CONN_FUSE
F102
+V5A
(1.5A)
Battery CONNECTOR
PJ2
P-MOS
EUPM3257
+VBATA
(6.5A)
TPS650830_9x9
UPM3254A
+V3P3A_RTC
(20mil)
RPM3316
+VCCPRTCPRIM_3P3
(20mil)
+V1P00A
(9.4A)
RPM3284
+VCCPRIM_1P0
(0.696A)
RPM3285
+VCCPRIM_CORE
(2.574A)
RPM3286
+VCCMPHYAON_1P0
(0.022A)
RPM3287
+VCCMPHYGTAON_1P0
(0.8A)
RPM3288
+VCCAMPHYPLL_1P0
(0.088A)
RPM3289
+VCCAPLL_1P0
(0.026A)
RPM3290
+VCCSRAM_1P0
(0.642A)
RPM3290
+VCCAPLLEBB_1P0
(0.033A)
SLG5NT1477V
EUPM3093
(0.16A)
+V1P00S_VCCST
(0.16A)
SLG7NT402
EUPM3094
(3.14A)
+V1P00S_VCCSTG
(3.14A)
SLG7NT402
EUPM3095
(1.6A)
SLG7NT402
U94
+V3P3A_WIFI
(1.5A)
+V3P3A_DSW
(6.5A)
SLG5NT1477V
EUPM3101
(3A)
+V3P3A
(1.5A)
SLG7NT402
U118
SLG5NT1477V
EUPM3100
(3A)
+V3P3S
(3A)
RPM3312
(0.118A)
+VCCPDSW_3P3
(0.118A)
+VDDQ_MEM
(4.9A)
USM2000
(0.4A)
USM2001
(0.4A)
USM2002
(0.4A)
USM2003
(0.4A)
R3571
(3A)
+VDDQ_MEM_SOC
(3A)
+V5A
(4.25A)
EUCP4040
(2A)
CN2
(2A)
U88
(2A)
EUPM3258
(0.9A)
INTEL
SKYLAKE_ULT
U80
+VCCCORE(29A)
+VCCGT(31A)
+VCCSA(4.5A)
+V1P8A
(0.62A)
SLG7NT402
EUPM3096
JP952
+V1P8U
(0.62A)
USM2000
USM2001
USM2002
USM2003
SLG7NT402
EUPM3097
+V1P8S
(0.35A)
JP952
SLG5NT1477V
EUPM3093
+V1P00A
(0.16A)
JP954
+V1P00S_VCCST
(0.16A)
SLG7NT402
EUPM3094
+V1P00S_VCCST
(3.04A)
JP949
+V1P00S_VCCST
(3.04A)
SLG7NT402
EUPM3095
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Model	Version	CHANGE LIST
	1A	**1. Modify NFCsch.--page30** **2 : Change net name from +V3PS to +V3P3S--page XX** **3 .Reserve RAP3023 follow PD7H --page16** **4. X5(XTAL 24MHZ) Change to Load capacitance : 20PF for intel spec** **5. X6(32.768K) Change to +-30PPM,12.5PF for common part.** **6. Q111 ,QPM3372 ,QPM3373 ,QPM3374 & QCP4112 change to PJA138K VGS(th)=1.5V** **7. U90 Change packge to CSP.** **Sch. Rev: 0709_1100**
	2A	**1. Correct XDP pin define** **2 : Change pullup power for RPM3333 from +V3P3S to +V3P3A** **3 .Delete QCP4122 and R1061. Connect ILIM_SEL directly to PCH.** **4. Delete R3635, R3637, and CR14** **5. Delete R720** **6. CODEC_JD has 1.8V and 3.3V pullup. Delete R1C3.** **7. Remove USB_C1_VBUS_WAKE*** **8. Isolate PCH_PLT_RST* signal on wifi connector** **Sch. Rev: 0713_1800**
	3A	**1. C8L7 Change of voltage 16 to 25V** **2 : SWAP DDI2_LANE_DP<3> & DDI2_LANE_DN*<3> --Page 29**
	4A	**1. Change Battery conn.** **(1) Remove CN36 & CN41** **(2) Add. PJ2.** **2 : J2 Change footprint**
	5A	**1. Audio solution change from ALC5650 to NAU88L25+MAX98357**
	6A	**1. Add. sch. for battery / power LED indicator**
	11A	**1. Modify HDMI sch. ,Add HDMI Active level shift IC Page 25** **2. Add C1105 ,C785 ,C1106 ,C783 & R50 ,R5117 ,R5118 R788 ,R790 ,RPM3337 for ACER lessen learnt ESD request** **3. Add ALS sch. Page 21 , The int (U137.4) signal need EC GPIO pin assignment.** **4. Add Keyboard backlight sch. Page 27** **5. Add BUZZER sch. Page 8** **6. Add INA sch. Page 41**
	2B	**1. Change resistor values for RAP1405, RAP1406, RAP1409 and RAP1410 from 33 ohm to 0 ohm** **2. Change value of RPM3597 and RPM3598 to 2K** **3. Add R5144 & R5145** **4. Swap signal on R5066 (KB_ROW2_SW) with signal on R5072 (KB_ROW[2]) for SLG4R4935**
	3B	**5. Add PD3** **6. Add. D51** **7. Change value C289 & C291 to 15p** **8. Change value C186 & C187 to 33p** **9. Stuff PQ129** **10. Add R5140 ,R5141 ,R5142 & R5143** **11. Add C1109** **12. Add C67 & C1110** **13. Add C1111 ,C1112 ,C8L13 ,C8L14 ,C8L15 ,C8L16,C8L17 ,C8L18 ,C8L19 & C8L20** **14. Add U138 ,R5137 ,R5138 & R5139** **15. Unstuff SW1** **16. Unstuff C551 & C553** **17. Change F100 ,F101 ,F104 & F2B1 to RC0805 (0 ohm)** **18. Stuff R1051 & UNSTUFF R1054** **19. R406 change to 2.2K** **20. R5125 change to 33 ohm**
	4B	Power portion by M T Update. 21. Change CAP14485 to stuff 22. RPM3358 (100Kohm) changes to 97.6kohm 1% (97.6K/F_4) 23. RPM3399 (100Kohm) changes to 93.1kohm 1% (93.1K/F_4) 24. Replace JP5100 (0.01/F_4) with *0_4 (no stuff) 25. Add note "SET FOR 7.5A" close to ILIMVR4 & RPM3031 26. Replace RPM3032 with 13K (13K/F_4) 27. Add note "SET FOR 6.0A" close to ILIMVR5 & RPM3274 28. Add note "Replace the CSD25402Q3A with TPCA8109 for 3S battery" close to EUPM3257 29. Add PR5026 (*10K_4) between net BC_BATT_TMP and ISL_BDET 30. Add PC1051(*1000P/50V_4) on net BC_IBAT to GND 31. Replace R3495 with 158K (158K/F_4) 32. Replace PQ129 with PJA138K follow OCA/B case 33. Replace F102 with 0_6 becausse U88 can limit current under 1.5A 34. Add PR19 (*10K/F_4) on net F8VR5P to GND, and no stuff 35. Replace RPM3114 with 49.9 (49.9/F_4) 36. Replace R737 with 8.25K (8.25K/F_4) 37. Change EUPM3258 (SLG7NT402VTR) solution to PU51 (APL3523A) for separate 2 power sources on HDMI and FAN
		38. Add PC1051 & PR5026 **39. Add R5126 ~ R5136** **40. Unstuff R5139** **41. Unstuff R5140 & R5141 ,Stuff R5142 & R5143** **42. Add R5146 & R5147**
	5B	**43. Replace JP3535,JP3536,JP3537,JP3538,JP949,JP5076,JP955,JP950,JP3539,JP3545,JP3546,JP3547 (0.01/F_6) with 0_6** **43. Replace R3572,R3573,R3574,JP3544,JP3551,JP3571,JP954,JP948,JP951,JP952,JP3507,R3548,R3552,R3571 (0.01/F_4) with 0_4**
	1C	Power portion by M T Update. 1. Replace PC303,PC306 with 10u/6.3V_4 2. Replace CPM3027 with 10u/6.3V_4 3. Replace PC102,PC104,C966,C967,CPM3057,CPM3061,CPM3063,CPM3065 with 0.1u/25V_4 4. Replace RPM3112 with 10F_4 5. Replace C955,C956,CPM3375,PC301,PC302 with 1u/6.3V_4 6. Remove PR303,PR304 (0_8) 7. Replace JP949,JP950,JP955,JP3535,JP3536,JP3537,JP3538,JP3539,JP3545,JP3547 with shortpad (0603) 8. Replace RPM3596,R3621,R3623,R3627,R3632 with shortpad (0201) 9. Replace PC18,PC20,C840,C845,C846 with 4.7uF/10V_4 10. Replace PR12,R803,R810,R811,R1068,RPM3005 with 1K/F_4 11. Replace R3508,R3529,PR5024 with 100K/F_4 12. Replace R817 with 105K/F_4 for VCORE transient 13. Replace R804 with 576/F_4 for VCORE transient 14. Replace PC24 with 33n/25V_4 for VCORE transient 15. Replace C795,C804 with 390P/50V_4 for VCORE transient 16. Replace R3495 with 162K/F_4 for ISL9237 datasheet update **17. Change RAP1091 from 2.71K to 2.7K for standard part** **18. Stuff R1076 & UNSTUFF Rap30421054** **19. CN2.3 Chnage connect from +V3P3S to +V3P3A**
	2C	**20. On Page 28, Stuff R3535, unstuff R59, R1D21 R1D22 for Rev B Nau88L25** **21. Stuff R1050, unstuff R1053 for DVT** **22. Conn. of Internal Speaker (J1P2) change P/N** **23. R1085 & R5004 Change to 120 ohm for LED light guide.** **24. Add R5148 ,R5149 , Reserve C1113 & C1114** **25. CN2 PIN 1 ,2 & 3 Change connect from +V3P3S to +V3P3A** **26. Add R5150, unstuff RAP1081** **27. SWAP U133 PIN1 & PIN5** **28. U90 Change P/N** **29. Un-stuff RAP3042 and stuff R1076** **30. RPM3470 and RPM3472 Change to 3.3K.** **31. Stuff RAP3045 and unstuff RAP3046** **32. Add gating to the PCH_PLT_RST*** **33. Change R983 and R988 to 237 Ohm.** **34. Change RAP1047 , RAP1049 , RAP3043 & RAP3044 to 0402 size.** **35. Stuff capacitors C887, C888.** **36. Remove R5074, C8L12, Q133, CR17 and U132** **37. Reserve C1115** **38. Change the U83 part number from SLG4R4935 to SLG4R41084 & Remove Q124** **39. Add a NFET with the gate at EC_RTCRST, the source at ground, and the drain at SRTCRST*,**
	3C	**40. Change the R5073 value to 10K** **41. Remove R5061 and R5062** **42. Move R5193 to signal MERGE_I2S_PCHRXD_AUDTXD from I2S0_RXD, R5193 should be put close to Pin 12 of U136. net I2S0_RXD and I2S0_RXD_R be merged.** **43. Add C1116** **44. Unstuff CPM4432 ,EUPM3261 ,R1C10 & RPM3893 , Stuff PC1051** **45. RAP1047 & RAP1049 change to 4.7K**
	4C	**46. Add R5152** **47. Unstuff RAP1348** **48. connect C1106 between "BC_IBAT" and ground and stuff C1106. Place R3526 and C1106 close to EC GPIO61** **49. Change the gate of QPM3390 from +V1P8A to +V1P8S** **50. Change R56 pul up rail to +V3P3A_DSW** **51. Add a WP GPIO for STM**

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

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PROJECT : SDA
Change list

Model	Version	CHANGE LIST
	5C	**1. Add C1136 & C1137** **2. Add R5154** **3. Add R5153** **4. Replace RCP4193 and R1M4 with 30K ; RCP4194 and R1M5 with 48.7K to set USB A Min limit 0.9 and Max limit 1.5A (The 29.8K of value is not available in stock.)** **5. CN2,3 change connect to +V1P8A.**
	6C	**6. Change R5153 to 100K** **7. please add RC filter on I2C4_SCL/SDA**
	1D	Power portion by M T Update. 1.New add thermal protection circuit: PU901,PC901,PR901,PR902,PR903 in page.31 2.Change to no-stuff: PD5,PR152,PQ12,PQ13,PR211,PR156,PR210,PQ14,PR155,PC102,PC104,PU4,PR144,PR145,PR146,PR262,PQ9,PR212 in page.31. 3.Change to no-stuff: PC214,PC215,PC216,PC217,PC218,PC219,PC1049,PC1050,PU21,PU22,PU23,PU26,RAP3024,RAP3025,RAP3026,RAP3027,RAP3028,RAP3029 ,RAP3036,RAP3037 in page.41. 4.Change 0.001/F_3720 to *SHORT_3720: RPM3527,JP945,JP943,JP942. 5.Delet 0.001/F_3720: JP1,JP946,JP960,JP944. 6.Delet 0_4: JP3544,JP954,RPM3300. 7.Delet PC2,PC3,PC6,PC7. 8.Change 0_4 to *SHORT_4: R3584,PR6,PR7,R3525,R3527,R3528,R3544,R3545,R3546,R3575,R3576,R3586,PR5025,R1018,R1019,R1114,R3572,R3573,R3574, JP3571,R1009,R3551,R3585,R3590,R3625,R5028,RPM3033,RPM3035,RPM3039,RPM3041,RPM3591,RPM3303, JP948,JP951,JP952,JP3507,PR300,PR305,PR306,R1013,R1017, R1159,RPM3118,RPM3393,RPM3394,RPM3395,RPM3396,RPM3415,RPM3417,R827,R917,R3548,R473,R921,R923,R3552,RPM3571,
		9. Remove R210 ,R213 ,R688 ,R689 ,R690 ,R691 ,R692 & R693 **10. Unstuff CN17** **11. Change to short pad :** **(1) Footprint : 0201 to SHORT0201** **Location : R1048 ,R1071 ,R1104 ,R1109 ,R1115 ,R1116 ,R1118 ,R1119 ,RR1139 ,R1158 ,R3501, R3502 ,R3504 ,R5026 ,R5107 ,RAP1325 ,RAP1326 ,RAP1360 ,RAP1364 ,RAP1405 ,RAP1406 ,RAP1409 ,RAP1410 ,RAP1422 ,RAP1428 ,RAP1429 ,RAP1457 ,RAP1459 ,RCP4216 & RPM3455** **(2) Footprint : 0402 to SHORT0402** **Location : R1002 ,R1074 ,R1076 ,R1105 ,R1C11 ,R1C12 ,R1C5 ,R1D10 ,R1D11 ,R1D12 ,R1D8 ,R1D9 ,R3493 ,R3526 ,R3603 ,R3620 ,R5018 ,R5039 ,R5040 ,R5043 ,R5051 ,R5063 ,R5066 ,R5068,RR5072 ,R5078 ,R5080 ,R5093 ,R5098 ,R5099 ,R5103 ,R5104 ,R5151 ,R771 ,R772 ,R957 ,R958 ,R960 ,R964 ,R777 ,RAP1345 ,RAP1346 ,RAP1349 ,RAP1351 ,RAP1352 ,RAP1356 ,RAP1367 ,RAP1374 ,RAP1375 ,RAP1376 ,RAP1377 ,RAP1381 ,RAP1382 ,RAP1383 ,RAP1384 ,RAP1385 ,RAP1386 ,RCP4072 ,RPM3285 ,RPM3287 ,RPM3288 ,RPM3290 ,RPM3291 ,RPM3292 ,RPM3293 ,RPM3294 3295 ,RPM3296 ,RPM3297 ,RPM3298 ,RPM3305 ,RPM3309 ,RPM3310 ,RPM3312 ,RPM3314 ,RPM3315 ,RPM3316 ,RPM3317 ,RPM3323 ,RPM3324 ,RPM3326 ,RPM3327 ,RPM3328 ,RPM3329 ,RPM3331 ,RPM3333 ,RPM3338 ,RPM3431 ,RPM3460 ,RPM3461 ,RPM3462 ,RPM3463** **(3) Footprint : 0603 to SHORT0603** **Location : R11, R1A3 , R1A4 , R1A5 , R1A6 , R3534 , R3535 , R5010 , R5086 , R5115 , R8A16 , R956 , RPM3282 , RPM3284** **(4) Footprint : 0603 to SHORT0603** **Location : R3571, RPM3283 ,RPM3286 RPM3289** **12. Unstuff : CN17** **13. Unstuff : R1051 & Stuff R1054 for PVT** **14. Remove NFC function : Unstuff R2B20 ,R2B21 ,R2B22 ,R2B23 ,R2B24 ,R2B25 ,R2B26 ,R408 ,CRCP4044 ,Q19 ,Q126 & R5015**
	2D	Power portion by M T Update. 1.Chage back the thermal protection solution in page.31: Stuff PD5,PR152,PQ12,PQ13,PR211,PR210,PQ14,PR155,PC102,PC104,PU4,PR144,PR145,PR146,PR262,PQ9,PR212. Unstuff PU901,PC901,PR901,PR902,PR903. 2.Change 680_4 to 604/F_4 with R931 in page.32 3.Change 0_4 to *SHORT_4: PR156 in page.31 4.Delet INA: PU21,PU22,PU23,PU26 in page.41 5.Delet JP942,JP943,JP945 in page.35 6.Delet RPM3527 in page.33 7.Change 1.2K to 1.65K with PR146 for thermal protection setting in page.31 8.Change 100K to 10K with R1A4PD2 in page.32
		9. Add C2 ,C3 & C4 **10. Change R982, R987 to 60.4 ohm. 0.5%** **Change R983, R988 to 145 ohm. 0.5%** **Change C887, C888 to 1800 pF.**

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:		DATE:	Quanta Computer Inc. PROJECT : ZDA
	PART NUMBER:		DRAWING BY:		REVISON:	Change list